Name: Ayesha Ahmad EE-272L Digital Systems Design

Reg. No. : 2021-EE-052 Marks Obtained: _____

Lab Manual 5

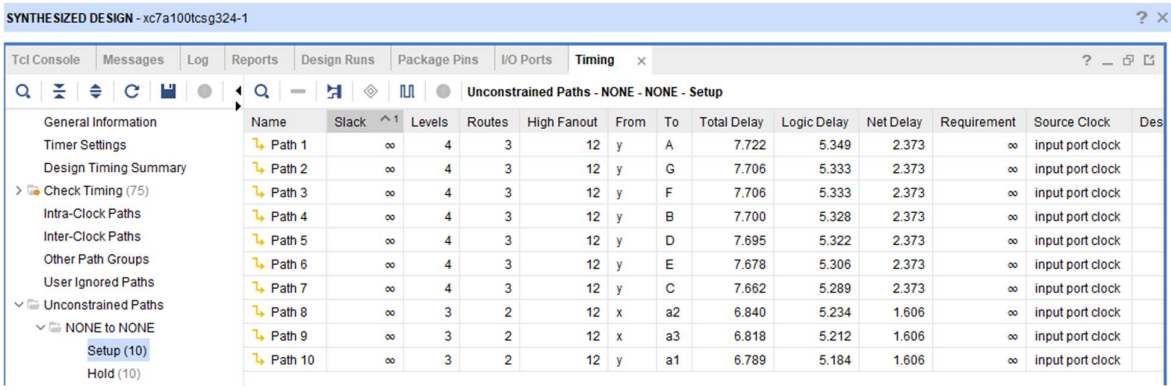
Combinational Circuit: Seven Segments

Display using Latches

Question 1

Part C

The maximum delay in Synthesis is from y to A of 7.722ns.

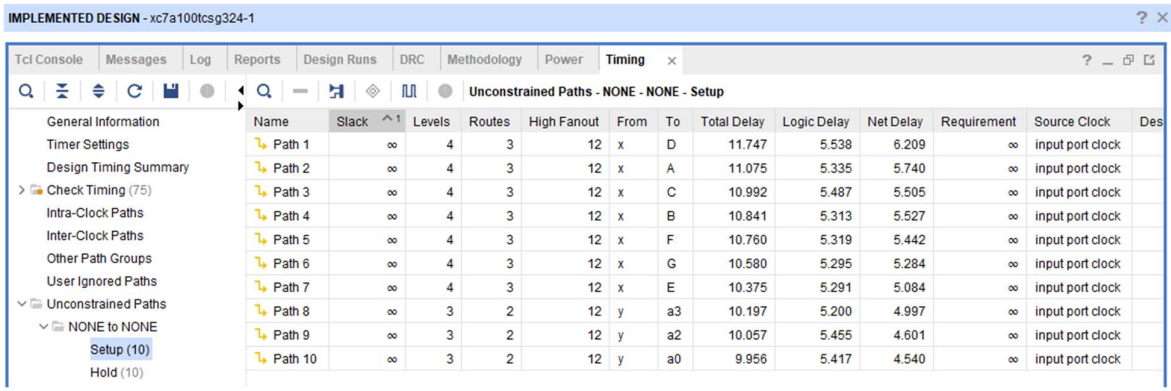


Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	4	3	12	y	A	7.722	5.349	2.373	∞	input port clock
Path 2	∞	4	3	12	y	G	7.706	5.333	2.373	∞	input port clock
Path 3	∞	4	3	12	y	F	7.706	5.333	2.373	∞	input port clock
Path 4	∞	4	3	12	y	B	7.700	5.328	2.373	∞	input port clock
Path 5	∞	4	3	12	y	D	7.695	5.322	2.373	∞	input port clock
Path 6	∞	4	3	12	y	E	7.678	5.306	2.373	∞	input port clock
Path 7	∞	4	3	12	y	C	7.662	5.289	2.373	∞	input port clock
Path 8	∞	3	2	12	x	a2	6.840	5.234	1.606	∞	input port clock
Path 9	∞	3	2	12	x	a3	6.818	5.212	1.606	∞	input port clock
Path 10	∞	3	2	12	y	a1	6.789	5.184	1.606	∞	input port clock

Part D

The maximum delay in Implementation is from x to D of 11.747 ns.

The path is not the same as in the synthesis report and neither is the max delay.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	4	3	12	x	D	11.747	5.538	6.209	∞	input port clock
Path 2	∞	4	3	12	x	A	11.075	5.335	5.740	∞	input port clock
Path 3	∞	4	3	12	x	C	10.992	5.487	5.505	∞	input port clock
Path 4	∞	4	3	12	x	B	10.841	5.313	5.527	∞	input port clock
Path 5	∞	4	3	12	x	F	10.760	5.319	5.442	∞	input port clock
Path 6	∞	4	3	12	x	G	10.580	5.295	5.284	∞	input port clock
Path 7	∞	4	3	12	x	E	10.375	5.291	5.084	∞	input port clock
Path 8	∞	3	2	12	y	a3	10.197	5.200	4.997	∞	input port clock
Path 9	∞	3	2	12	y	a2	10.057	5.455	4.601	∞	input port clock
Path 10	∞	3	2	12	y	a0	9.956	5.417	4.540	∞	input port clock

Part E

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	15	0	63400	0.02
LUT as Logic	15	0	63400	0.02
LUT as Memory	0	0	19000	0.00
Slice Registers	16	0	126800	0.01
Register as Flip Flop	0	0	126800	0.00
Register as Latch	16	0	126800	0.01
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

Name	Dir...	Ne...	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination
All ports (19)												
Scalar ports (19)												
a	IN		J15	✓	15	LVCMOS33	3.300				NONE	NONE
b	IN		L16	✓	14	LVCMOS33	3.300				NONE	NONE
c	IN		M13	✓	14	LVCMOS33	3.300				NONE	NONE
d	IN		R15	✓	14	LVCMOS33	3.300				NONE	NONE
en	IN		U12	✓	14	LVCMOS33	3.300				NONE	NONE
x	IN		U11	✓	14	LVCMOS33	3.300				NONE	NONE
y	IN		V10	✓	14	LVCMOS33	3.300				NONE	NONE
A	OUT		T10	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
a0	OUT		J17	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
a1	OUT		J18	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
a2	OUT		T9	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
a3	OUT		J14	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
B	OUT		R10	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
C	OUT		K16	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
D	OUT		K13	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
DP	OUT		H15	✓	15	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
E	OUT		P15	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
F	OUT		T11	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50
G	OUT		L18	✓	14	LVCMOS33	3.300		12	SLOW	NONE	FP_VTT_50