Experiment 7

Sequential Circuit Design: News Ticker

In this lab, we are going to design a sequential circuit which is going to act as a news ticker.

Tasks

A sample output can be seen in https://www.youtube.com/watch?v=X8szESJvHAw. You are supposed to scroll your EE registration No. on the display. The direction button scrolls the text from left to right and right to left. Fig. 7.1 shows the modular diagram for this task.

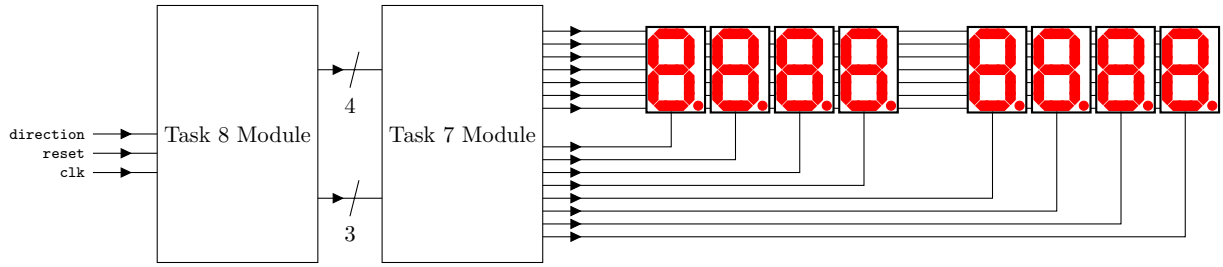

Fig. 7.1: Lab task modular circuit.

The diagram above shows that you can use the 7-segment display driver circuit that you built in the previous lab. The reuse of the 7-segment display driver shows how easily you can build complex designs by breaking them into smaller designs. You don't need to verify 7-segment display driver if you did that in the previous lab and need to test the design portion that you are developing in this lab only. Therefore, it is always better if you break your designs into multiple smaller modules and then test each module independently.

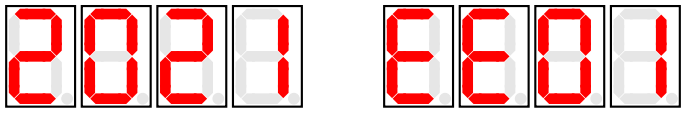

Fig. 7.2: Sample output for the Lab Task with `direction=1'b0` at `t=0`.

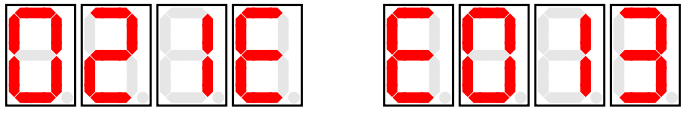

Fig. 7.3: Sample output for the Lab Task with `direction=1'b0` at `t=1`.

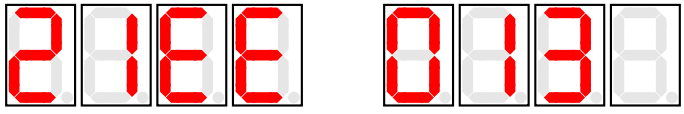

Fig. 7.4: Sample output for the Lab Task with `direction=1'b0` at `t=2`.

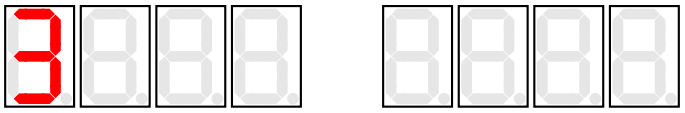

Fig. 7.5: Sample output for the Lab Task with `direction=1'b0` at `t=9`.

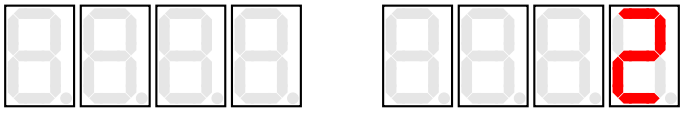

Fig. 7.6: Sample output for the Lab Task with `direction=1'b0` at `t=11`.

Note:
Use of latches are not allowed in the design of synchronous circuits for the lab. Synchronous circuits must be designed with flip-flops.

Deliverables

1. A report containing the following items:
   (a) The designed circuit for task module in the diagram above with hand-sketched design partition of the system. The design partition should include multiplexers, encoders, decoders and flip-flops, and should avoid gates as much as possible. The design should also show the labels of wires , along with the label for the width of the line for multi-bit wires.
   (b) Synthesis maximum combinational delay: Read the synthesis report of your circuit and describe which path has the maximum combinational delay?
   (c) Implementation maximum combinational delay: Read the post implementation static timing report and identify the path with the maximum combinational delay? Is the path same as the one in the synthesis report?
   (d) Resource Utilization Report: Read the synthesis report and identify how many resources in the FPGA such as lookup tables (LUTs), input/output (IOs), etc., has been utilized.
2. Simulation of your designed module on QuestaSim. Show the simulation to the instructor.
3. FPGA Implementation: Synthesize the circuit for Nexys A7 FPGA available in the lab. Tie inputs to the switches and outputs to the seven-segment displays available on the board.

The collaboration between students is encouraged, but blind code sharing/copying is not allowed. If you are unable to explain anything in your code, it will be assumed you have copied it. So make sure you know every thing you have written in your code. We are least concerned about how you have learnt something as long as you have learnt it well.

Acknowledgments

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