Name: Ayesha Ahmad & Rohiya Shafiq EE-272L Digital Systems Design

Reg. No. : 2021-EE-052 & 2021-EE-055 Marks Obtained: _____

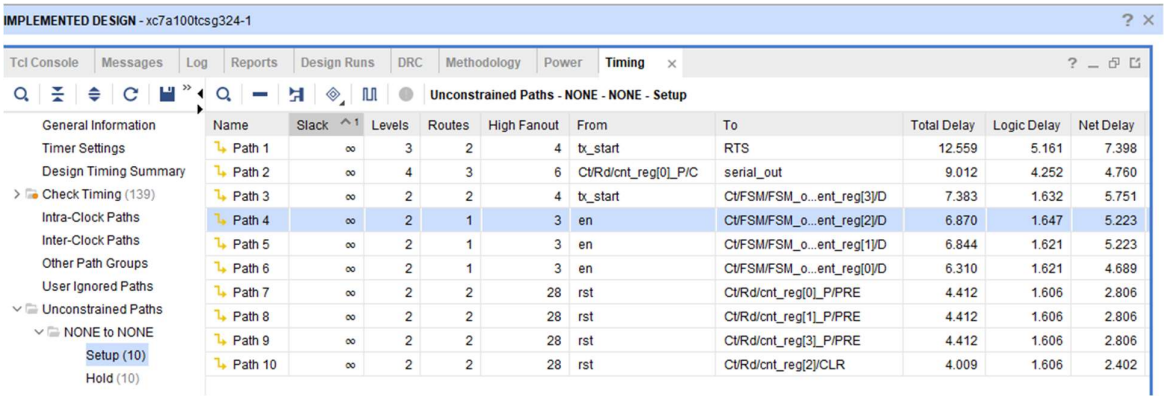
Complex Engineering Problem

UART Transmitter: Datapath and Controller

Question 1

Part D

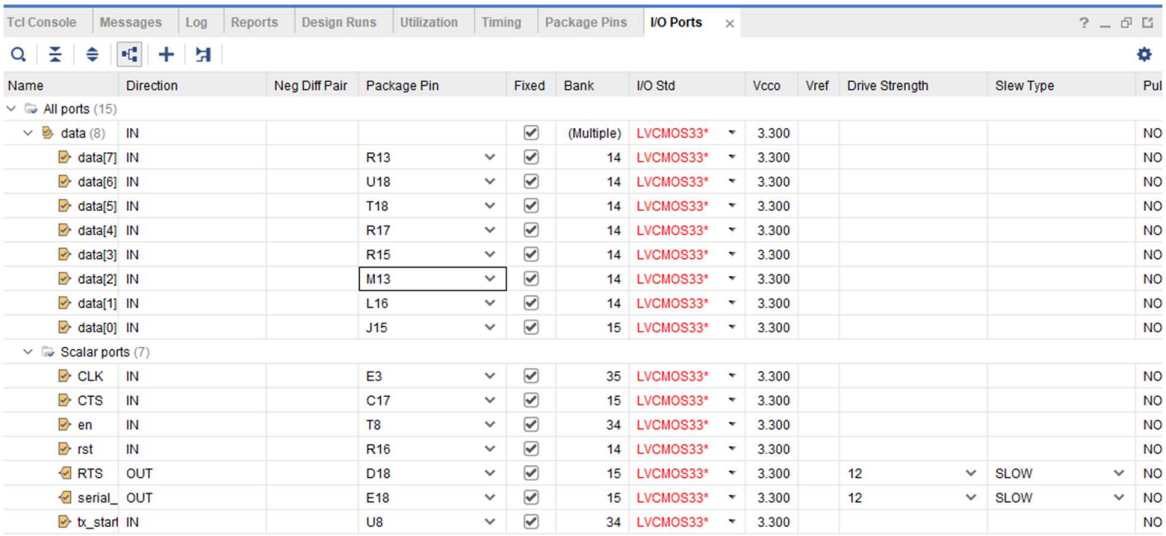
The maximum delay in Implementation is from tx_start of 12.559 ns.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	3	2	4	tx_start	RTS	12.559	5.161	7.398
Path 2	∞	4	3	6	Ct/Rd/cnt_reg[0]_P/C	serial_out	9.012	4.252	4.760
Path 3	∞	2	2	4	tx_start	Ct/FSM/FSM_o...ent_reg[3]/D	7.383	1.632	5.751
Path 4	∞	2	1	3	en	Ct/FSM/FSM_o...ent_reg[2]/D	6.870	1.647	5.223
Path 5	∞	2	1	3	en	Ct/FSM/FSM_o...ent_reg[1]/D	6.844	1.621	5.223
Path 6	∞	2	1	3	en	Ct/FSM/FSM_o...ent_reg[0]/D	6.310	1.621	4.689
Path 7	∞	2	2	28	rst	Ct/Rd/cnt_reg[0]_P/PRE	4.412	1.606	2.806
Path 8	∞	2	2	28	rst	Ct/Rd/cnt_reg[1]_P/PRE	4.412	1.606	2.806
Path 9	∞	2	2	28	rst	Ct/Rd/cnt_reg[3]_P/PRE	4.412	1.606	2.806
Path 10	∞	2	2	28	rst	Ct/Rd/cnt_reg[2]/CLR	4.009	1.606	2.402

Part E

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	28	0	63400	0.04
LUT as Logic	28	0	63400	0.04
LUT as Memory	0	0	19000	0.00
Slice Registers	30	0	126800	0.02
Register as Flip Flop	29	0	126800	0.02
Register as Latch	1	0	126800	<0.01
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pul
All ports (15)											
data (8)	IN			☑	(Multiple)	LVCMOS33*	3.300				NO
data[7]	IN		R13	☑	14	LVCMOS33*	3.300				NO
data[6]	IN		U18	☑	14	LVCMOS33*	3.300				NO
data[5]	IN		T18	☑	14	LVCMOS33*	3.300				NO
data[4]	IN		R17	☑	14	LVCMOS33*	3.300				NO
data[3]	IN		R15	☑	14	LVCMOS33*	3.300				NO
data[2]	IN		M13	☑	14	LVCMOS33*	3.300				NO
data[1]	IN		L16	☑	14	LVCMOS33*	3.300				NO
data[0]	IN		J15	☑	15	LVCMOS33*	3.300				NO
Scalar ports (7)											
CLK	IN		E3	☑	35	LVCMOS33*	3.300				NO
CTS	IN		C17	☑	15	LVCMOS33*	3.300				NO
en	IN		T8	☑	34	LVCMOS33*	3.300				NO
rst	IN		R16	☑	14	LVCMOS33*	3.300				NO
RTS	OUT		D18	☑	15	LVCMOS33*	3.300		12	SLOW	NO
serial_	OUT		E18	☑	15	LVCMOS33*	3.300		12	SLOW	NO
tx_start	IN		U8	☑	34	LVCMOS33*	3.300				NO

Part F

Roll Number	Name	Task
2021-EE-52	Ayesha Ahmad	Designed and Coded Controller
2021-EE-55	Rohiya Shafiq	Designed and Coded Datapath