# Experiment 5

# Combinational Circuit: Seven Segments Display using Latches

In this lab, we are going to display different characters on seven segment using latches and enable.

## Tasks

You are required to build a circuit to display different characters (0 to F) on four of the eight seven-segment display. Fig. 5.1 shows the modular diagram for this task.

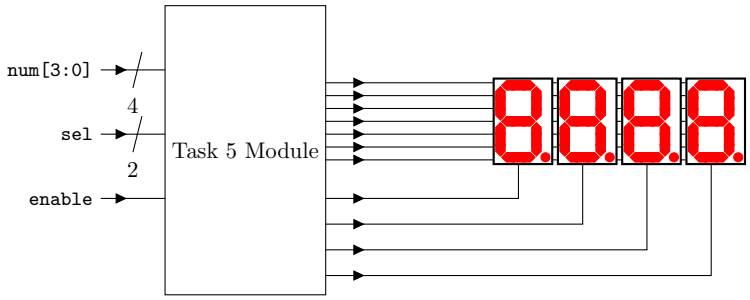


Fig. 5.1: Lab task modular circuit.

The user enters a four bit number to be displayed on the first seven-segment display by choosing `sel=2'b00` and `num = desired number`. Then the user enters another four bit number and stores the number to be displayed on the second seven-segment display by choosing `sel = 2'b01`, `num = desired number`, and turning the `enable` switch ON and then OFF. Again the user enters another four bit number and stores the number to be displayed on the third seven-segment display by choosing `sel = 2'b10`, `num = desired number`, and turning the `enable` switch ON and then OFF. In other words, enable and select pins combined store and display data for second third and fourth segments. Table 1 explains the operations of the circuit in more detail.

| *Number* | *Select* | *Enable* | *Output* |
|---|---|---|---|
| desired number | 0 | X | Entered value displayed on first seven segment. Fig. 5.2 |
| desired number | 1 | 1 | Value stored for second seven segment, nothing displayed. |
| X | 1 | 0 | Stored value displayed on second seven segment. Fig. 5.3 |
| desired number | 2 | 1 | Value stored for third seven segment, nothing displayed. |
| X | 2 | 0 | Stored value displayed on third seven segment. |
| desired number | 3 | 1 | Value stored for fourth seven segment, nothing displayed. |
| X | 3 | 0 | Stored value displayed on fourth seven segment. |

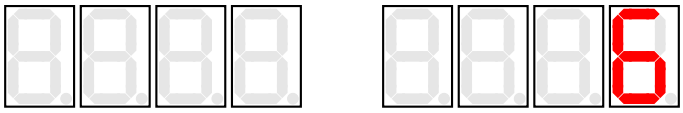

Fig. 5.2: Sample output for the Lab Task with `sel=2'b00` and `num=4'b0110`.

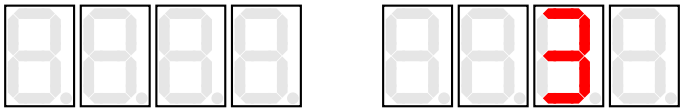

Fig. 5.3: Sample output for the Lab Task with `sel=2'b01` when stored number is `num=4'b0011`.

## Deliverables

1. A report containing the following items:
   (a) The designed circuit for task module in the diagram above with hand-sketched design partition of the system. The design partition should include latches, muxes and decoders,etc. (Decoder is just the circuit you implement to convert the input to the required output.) The design should also show the labels of wires, along with the label for the width of the line for multi-bit wires.
   (b) A hand-sketched gate-level diagram for each component you have drawn (which you haven't already provided in the previous manual). You can use behavioral modeling for only the components you have studied in the class. Use K-Maps to generate rest of the component circuits.
   (c) Synthesis maximum combinational delay: Read the synthesis report of your circuit and describe which path has the maximum combinational delay?
   (d) Implementation maximum combinational delay: Read the post implementation static timing report and identify the path with the maximum combinational delay? Is the path same as the one in the synthesis report?
   (e) Resource Utilization Report: Read the synthesis report and identify how many resources in the FPGA such as lookup tables (LUTs), input/output (IOs), etc., has been utilized.
2. Simulation of your designed module on QuestaSim. Show the simulation to the instructor.
3. FPGA Implementation: Synthesize the circuit for Nexys A7 FPGA available in the lab. The inputs to the switches and outputs to the seven-segment displays available on the board.

The collaboration between students is encouraged, but blind code sharing/copying is not allowed. If you are unable to explain anything in your code, it will be assumed you have copied it. So make sure you know every thing you have written in your code. We are least concerned about how you have learnt something as long as you have learnt it well.

## Acknowledgments

The manual has been written by Dr. Ubaid Ullah Fayyaz and Ms. Shehzeen Malik.