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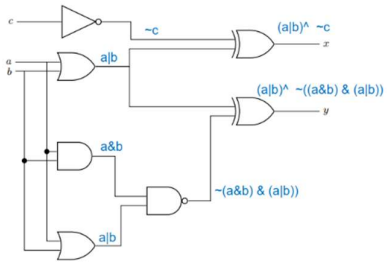
Reg. No. : 2021-EE-052 Marks Obtained: _____

Lab Manual 3

Combinational Circuit Design using Vivado



Question 1

Part A

A	*B*	*C*	$O=\overline{C}$	$R=P=A+B$	$Q=AB$	$S=\overline{Q}\overline{R}$	$X=O\oplus P$	$Y=P\oplus S$
0	*0*	*0*	1	0	0	1	1	1
0	*0*	*1*	0	0	0	1	0	1
0	*1*	*0*	1	1	0	1	0	0
0	*1*	*1*	0	1	0	1	1	0
1	*0*	*0*	1	1	0	1	0	0
1	*0*	*1*	0	1	0	1	1	0
1	*1*	*0*	1	1	1	0	0	1
1	*1*	*1*	0	1	1	0	1	1

Part B

The maximum combinational delay is from b to y with a time delay of 6.771ns.

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	2	b	y	6.771	5.165	1.606	∞	input port clock
Path 2	∞	3	2	1	c	x	6.735	5.130	1.606	∞	input port clock

Part C

It used 2 LUTs and 5 IOs; 3 of which are for inputs and 2 for outputs.

Ref Name	Used	Functional Category
IBUF	3	IO
OBUF	2	IO
LUT3	1	LUT
LUT2	1	LUT

Question 2

```
`timescale 1ns / 1ps
module task1(output logic x,y,
input logic a,b,c
);

assign x = (a | b) ^ ~ c;
assign y = (a | b) ^ ( (a & b) ~& (a | b) );

endmodule
```