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Reg. No. : 2021-EE-052 Marks Obtained: _____

Lab Manual 4b

Combinational Circuit Design using K-Maps

Question 1

Part A

Select which number to display:

a	b	c	d	**Character**	Seg.A	Seg.B	Seg.C	Seg. D	Seg.E	Seg.F	Seg.G	DP
0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	1	0	0	1	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0	1
0	0	1	1	3	0	0	0	0	1	1	0	1
0	1	0	0	4	1	0	0	1	1	0	0	1
0	1	0	1	5	0	1	0	0	1	0	0	1
0	1	1	0	6	0	1	0	0	0	0	0	1
0	1	1	1	7	0	0	0	1	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0	1
1	0	0	1	9	0	0	0	0	1	0	0	1
1	0	1	0	A	0	0	0	1	0	0	0	1
1	0	1	1	B	1	1	0	0	0	0	0	1
1	1	0	0	C	0	1	1	0	0	0	1	1
1	1	0	1	D	1	0	0	0	0	1	0	1
1	1	1	0	E	0	1	1	0	0	0	0	1
1	1	1	1	F	0	1	1	1	0	0	0	1

Select which 7-segment to display on:

x	y	z	AN0	AN1	AN2	AN3	AN4	AN5	AN6	AN7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Part B

A = $\bar{a}\bar{b}\bar{c}d + \bar{a}bc\bar{d} + ab\bar{c}d + a\bar{b}cd$

a b \ c d	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	0	1	0	0
10	0	0	1	0

B = $\bar{a}b\bar{c}d + ab\bar{d} + acd + bc\bar{d}$

a b \ c d	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	0	1	1
10	0	0	1	0

C = $ab\bar{d} + abc + \bar{a}\bar{b}c\bar{d}$

a b \ c d	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	0	1	1
10	0	0	0	0

D = $\bar{a}b\bar{c}\bar{d} + \bar{a}\bar{b}cd + a\bar{b}c\bar{d} + bcd$

a b \ c d	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	1	0
10	0	0	0	1

E = $\bar{a}b\bar{c} + \bar{b}c\bar{d} + \bar{a}d$

a b \ c d	00	01	11	10
00	0	1	1	0
01	1	1	1	0
11	0	0	0	0
10	0	1	0	0

F = $ab\bar{c}d + \bar{a}\bar{b}d + \bar{a}\bar{b}c + \bar{a}cd$

a b \ c d	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	0	1	0	0
10	0	0	0	0

G = $\bar{a}\bar{b}\bar{c} + \bar{a}bcd + ab\bar{c}\bar{d}$

a b \ c d	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	0	0	0
10	0	0	0	0

AN0 = $\bar{x}\,\bar{y}\,\bar{z}$

x y \ z	0	1
00	1	0
01	0	0
11	0	0
10	0	0

AN1 = $\bar{x}\,\bar{y}\,z$

x y \ z	0	1
00	0	1
01	0	0
11	0	0
10	0	0

AN2 = $\bar{x}\,y\,\bar{z}$

x y \ z	0	1
00	0	0
01	1	0
11	0	0
10	0	0

AN3 = $\bar{x}\,y\,z$

x y \ z	0	1
00	0	0
01	0	1
11	0	0
10	0	0

AN4 = $x\,\bar{y}\,\bar{z}$

x y \ z	0	1
00	0	0
01	0	0
11	0	0
10	1	0

AN5 = $x\,\bar{y}\,z$

x y \ z	0	1
00	0	0
01	0	0
11	0	0
10	0	1

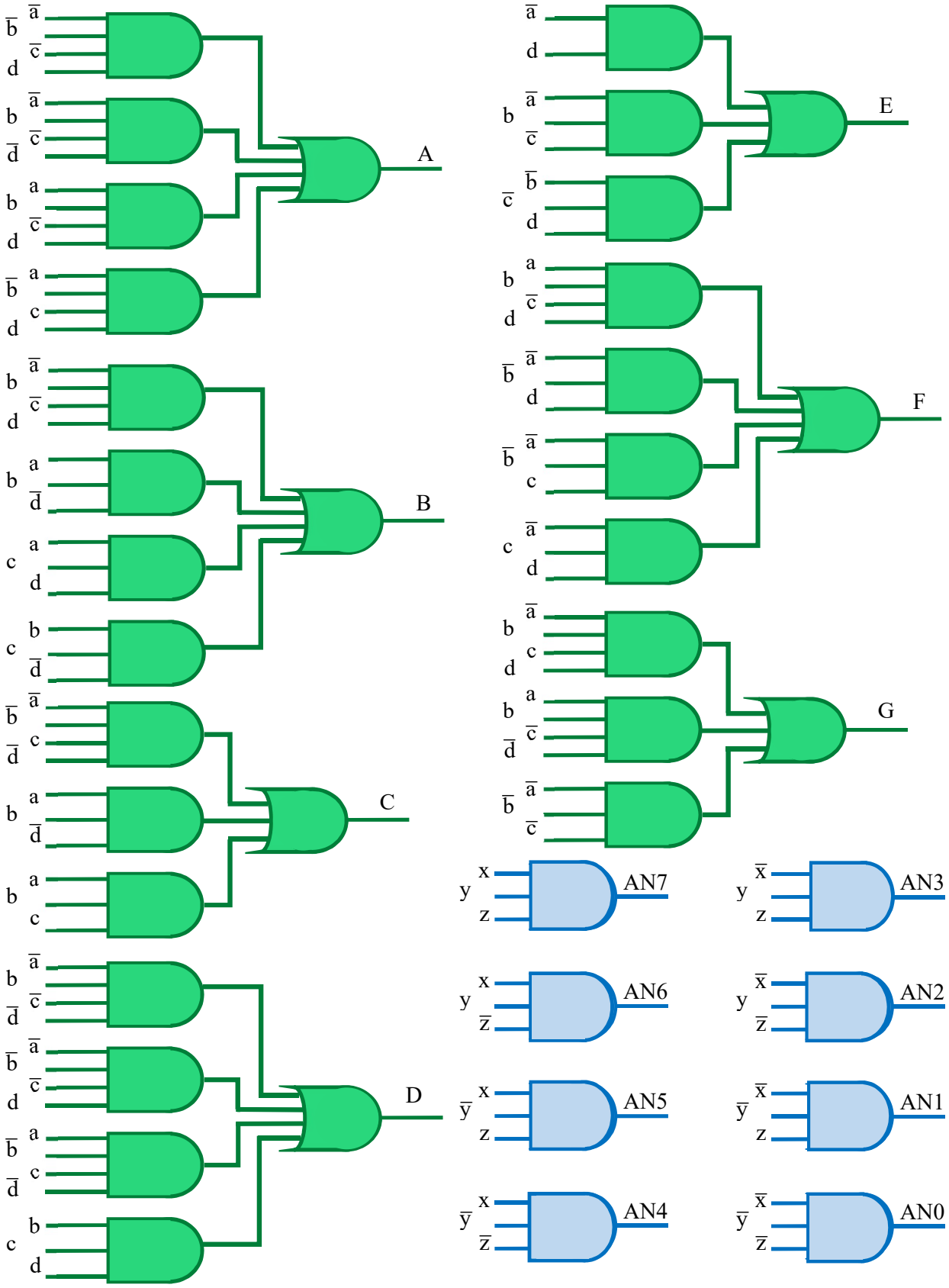
AN6 = $x\,y\,\bar{z}$

x y \ z	0	1
00	0	0
01	0	0
11	1	0
10	0	0

AN7 = $x\,y\,z$

x y \ z	0	1
00	0	0
01	0	0
11	0	1
10	0	0

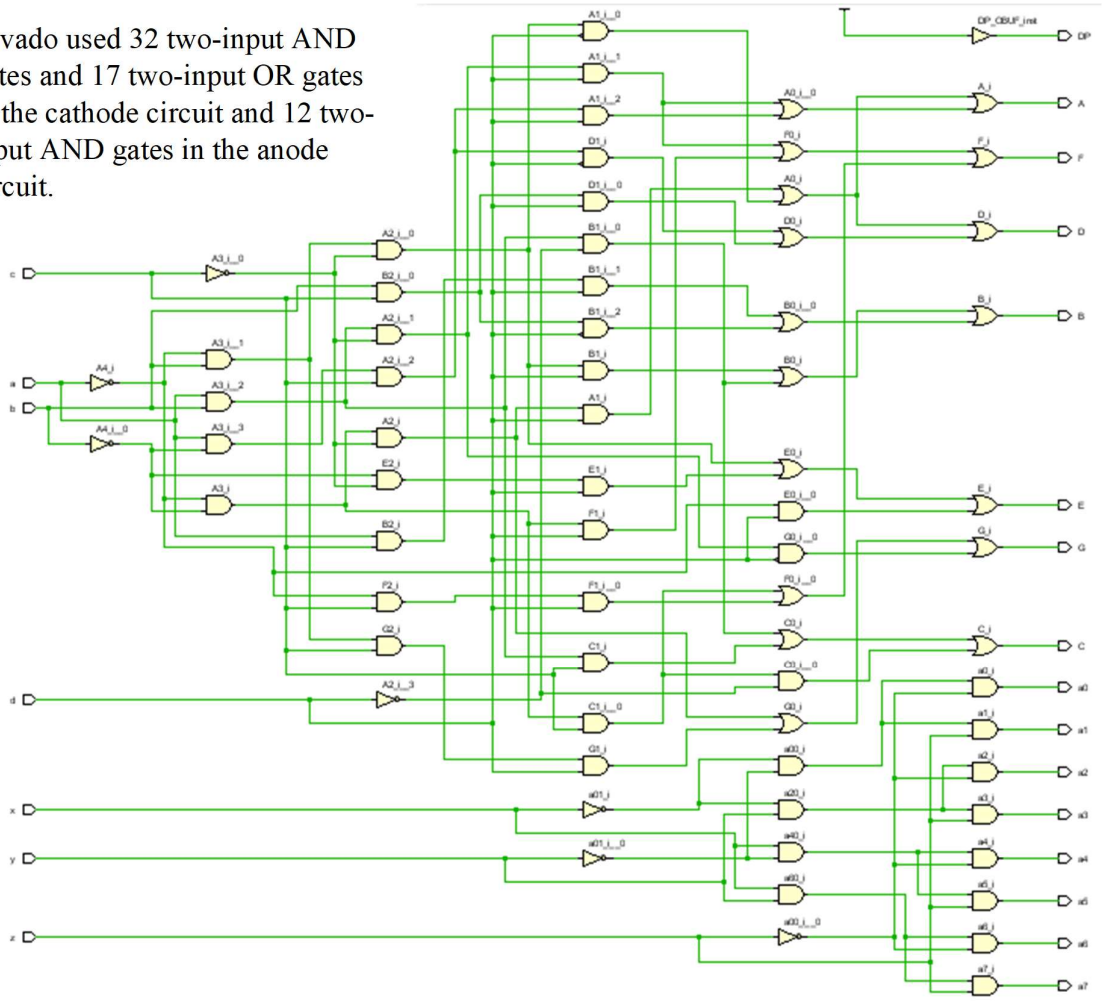
Part C



Part D

Vivado only used two-input gates: 44 AND and 17 OR gate. Mine has 33 AND and 7 OR gates with varying number of inputs.

Vivado used 32 two-input AND gates and 17 two-input OR gates in the cathode circuit and 12 two-input AND gates in the anode circuit.



My circuit has the following list of AND gates: 2 two-input, 12 three-input and 12 four-input, and OR gates: 3 three-input and 4 four-input, in the cathode circuit. And 8 three-input AND gates in the anode circuit.

Part E

The maximum delay in Synthesis is from x to a2 of 6.851ns.

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	8	x	a2	6.851	5.246	1.606	∞	input port clock
Path 2	∞	3	2	8	x	a7	6.832	5.227	1.606	∞	input port clock
Path 3	∞	3	2	8	x	a3	6.829	5.223	1.606	∞	input port clock
Path 4	∞	3	2	8	z	a5	6.805	5.200	1.606	∞	input port clock
Path 5	∞	3	2	8	z	a4	6.804	5.198	1.606	∞	input port clock
Path 6	∞	3	2	7	c	F	6.800	5.194	1.606	∞	input port clock
Path 7	∞	3	2	8	x	a6	6.797	5.191	1.606	∞	input port clock
Path 8	∞	3	2	7	c	B	6.794	5.189	1.606	∞	input port clock
Path 9	∞	3	2	7	c	A	6.792	5.186	1.606	∞	input port clock
Path 10	∞	3	2	8	z	a1	6.789	5.184	1.606	∞	input port clock

Part F

The maximum delay in Implementation is from z to a6 of 12.565 ns.

The path is not the same as in the synthesis report and neither is the max delay.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	8	z	a6	12.565	5.400	7.166	∞	input port clock
Path 2	∞	3	2	7	a	A	10.419	5.409	5.010	∞	input port clock
Path 3	∞	3	2	8	z	a3	10.310	5.433	4.877	∞	input port clock
Path 4	∞	3	2	8	z	a0	10.223	5.414	4.810	∞	input port clock
Path 5	∞	3	2	7	a	B	10.115	5.157	4.958	∞	input port clock
Path 6	∞	3	2	7	a	F	10.100	5.398	4.702	∞	input port clock
Path 7	∞	3	2	8	z	a1	10.093	5.184	4.910	∞	input port clock
Path 8	∞	3	2	7	a	D	9.621	5.382	4.240	∞	input port clock
Path 9	∞	3	2	8	z	a2	9.477	5.222	4.255	∞	input port clock
Path 10	∞	3	2	8	z	a4	9.444	5.198	4.246	∞	input port clock

Part G

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	8	0	63400	0.01
LUT as Logic	8	0	63400	0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
All ports (23)										
Scalar ports (23)										
a	IN		J15	☑	15	LVCMOS33*	3.300			
b	IN		L16	☑	14	LVCMOS33*	3.300			
c	IN		M13	☑	14	LVCMOS33*	3.300			
d	IN		R15	☑	14	LVCMOS33*	3.300			
x	IN		U12	☑	14	LVCMOS33*	3.300			
y	IN		U11	☑	14	LVCMOS33*	3.300			
z	IN		V10	☑	14	LVCMOS33*	3.300			
A	OUT		T10	☑	14	LVCMOS33*	3.300		12	SLOW
a0	OUT		J17	☑	15	LVCMOS33*	3.300		12	SLOW
a1	OUT		J18	☑	15	LVCMOS33*	3.300		12	SLOW
a2	OUT		T9	☑	14	LVCMOS33*	3.300		12	SLOW
a3	OUT		J14	☑	15	LVCMOS33*	3.300		12	SLOW
a4	OUT		P14	☑	14	LVCMOS33*	3.300		12	SLOW
a5	OUT		T14	☑	14	LVCMOS33*	3.300		12	SLOW
a6	OUT		K2	☑	35	LVCMOS33*	3.300		12	SLOW
a7	OUT		U13	☑	14	LVCMOS33*	3.300		12	SLOW
B	OUT		R10	☑	14	LVCMOS33*	3.300		12	SLOW
C	OUT		K16	☑	15	LVCMOS33*	3.300		12	SLOW
D	OUT		K13	☑	15	LVCMOS33*	3.300		12	SLOW
DP	OUT		H15	☑	15	LVCMOS33*	3.300		12	SLOW
E	OUT		P15	☑	14	LVCMOS33*	3.300		12	SLOW
F	OUT		T11	☑	14	LVCMOS33*	3.300		12	SLOW
G	OUT		L18	☑	14	LVCMOS33*	3.300		12	SLOW