Name: Ayesha Ahmad EE-272L Digital Systems Design

Reg. No. : 2021-EE-052 Marks Obtained: _____

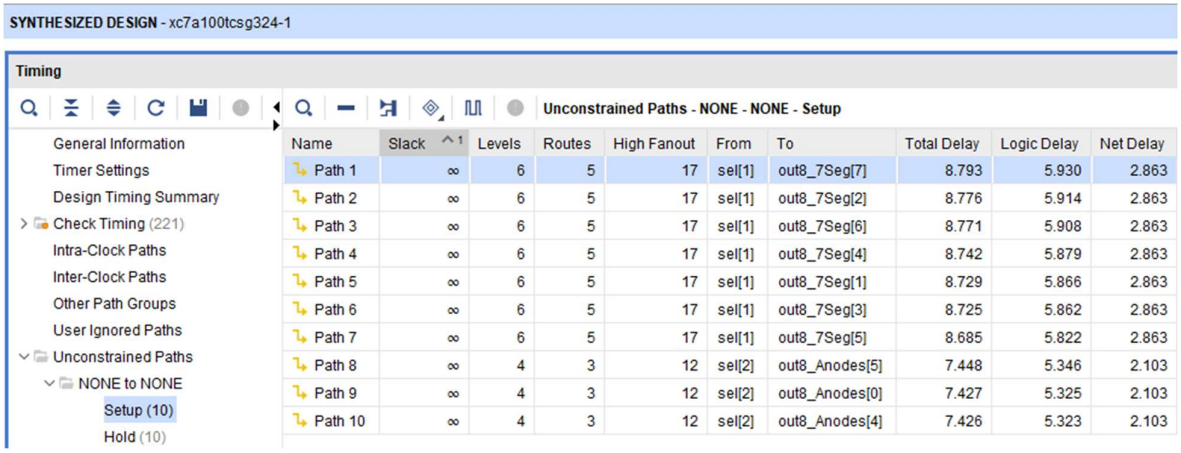
Lab Manual 6

Sequential Circuit Design

Question 1

Part C

The maximum delay in Synthesis is from sel[1] to out8_7Seg[7] of 8.793ns.



SYNTHESIZED DESIGN - xc7a100tcsg324-1

Timing

Unconstrained Paths - NONE - NONE - Setup

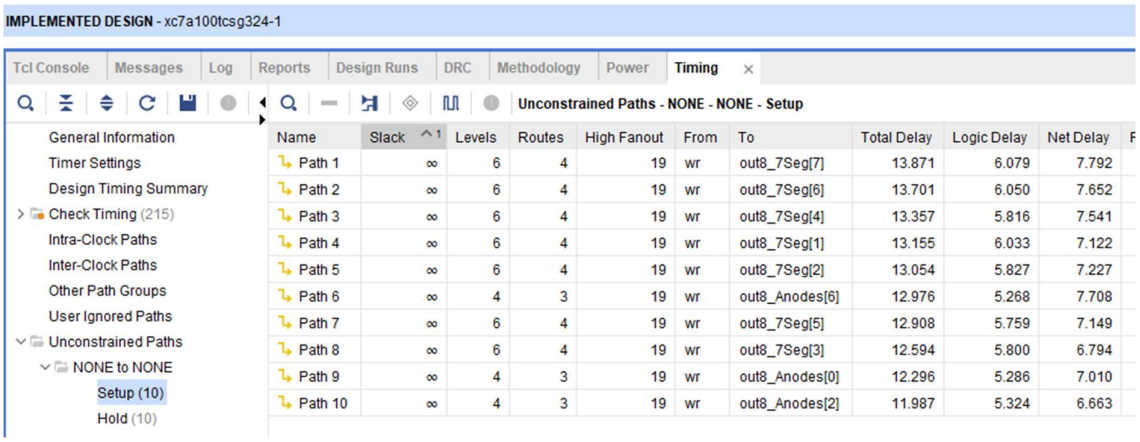
- General Information
- Timer Settings
- Design Timing Summary
- Check Timing (221)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths
  - NONE to NONE
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	6	5	17	sel[1]	out8_7Seg[7]	8.793	5.930	2.863
Path 2	∞	6	5	17	sel[1]	out8_7Seg[2]	8.776	5.914	2.863
Path 3	∞	6	5	17	sel[1]	out8_7Seg[6]	8.771	5.908	2.863
Path 4	∞	6	5	17	sel[1]	out8_7Seg[4]	8.742	5.879	2.863
Path 5	∞	6	5	17	sel[1]	out8_7Seg[1]	8.729	5.866	2.863
Path 6	∞	6	5	17	sel[1]	out8_7Seg[3]	8.725	5.862	2.863
Path 7	∞	6	5	17	sel[1]	out8_7Seg[5]	8.685	5.822	2.863
Path 8	∞	4	3	12	sel[2]	out8_Anodes[5]	7.448	5.346	2.103
Path 9	∞	4	3	12	sel[2]	out8_Anodes[0]	7.427	5.325	2.103
Path 10	∞	4	3	12	sel[2]	out8_Anodes[4]	7.426	5.323	2.103

Part D

The maximum delay in Implementation is from wr to out8_7Seg[7] of 13.871 ns.

The path is not the same as in the synthesis report and neither is the max delay.



IMPLEMENTED DESIGN - xc7a100tcsg324-1

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing

Unconstrained Paths - NONE - NONE - Setup

- General Information
- Timer Settings
- Design Timing Summary
- Check Timing (215)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths
  - NONE to NONE
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	6	4	19	wr	out8_7Seg[7]	13.871	6.079	7.792
Path 2	∞	6	4	19	wr	out8_7Seg[6]	13.701	6.050	7.652
Path 3	∞	6	4	19	wr	out8_7Seg[4]	13.357	5.816	7.541
Path 4	∞	6	4	19	wr	out8_7Seg[1]	13.155	6.033	7.122
Path 5	∞	6	4	19	wr	out8_7Seg[2]	13.054	5.827	7.227
Path 6	∞	4	3	19	wr	out8_Anodes[6]	12.976	5.268	7.708
Path 7	∞	6	4	19	wr	out8_7Seg[5]	12.908	5.759	7.149
Path 8	∞	6	4	19	wr	out8_7Seg[3]	12.594	5.800	6.794
Path 9	∞	4	3	19	wr	out8_Anodes[0]	12.296	5.286	7.010
Path 10	∞	4	3	19	wr	out8_Anodes[2]	11.987	5.324	6.663

Part E

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	50	0	63400	0.08
LUT as Logic	50	0	63400	0.08
LUT as Memory	0	0	19000	0.00
Slice Registers	53	0	126800	0.04
Register as Flip Flop	53	0	126800	0.04
Register as Latch	0	0	126800	0.00
F7 Muxes	4	0	31700	0.01
F8 Muxes	0	0	15850	0.00

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength
All ports (26)									
Scalar ports (3)									
CLK	IN		E3	☑	35	LVCMOS33*	3.300		
rst	IN		H6	☑	35	LVCMOS33*	3.300		
wr	IN		T13	☑	14	LVCMOS33*	3.300		
num (4)	IN			☑	(Multiple)	LVCMOS33*	3.300		
num[3]	IN		R15	☑	14	LVCMOS33*	3.300		
num[2]	IN		M13	☑	14	LVCMOS33*	3.300		
num[1]	IN		L16	☑	14	LVCMOS33*	3.300		
num[0]	IN		J15	☑	15	LVCMOS33*	3.300		
sel (3)	IN			☑	14	LVCMOS33*	3.300		
sel[2]	IN		V10	☑	14	LVCMOS33*	3.300		
sel[1]	IN		U11	☑	14	LVCMOS33*	3.300		
sel[0]	IN		U12	☑	14	LVCMOS33*	3.300		
out8_7Seg (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300		12
out8_7Seg[7]	OUT		T10	☑	14	LVCMOS33*	3.300		12
out8_7Seg[6]	OUT		R10	☑	14	LVCMOS33*	3.300		12
out8_7Seg[5]	OUT		K16	☑	15	LVCMOS33*	3.300		12
out8_7Seg[4]	OUT		K13	☑	15	LVCMOS33*	3.300		12
out8_7Seg[3]	OUT		P15	☑	14	LVCMOS33*	3.300		12
out8_7Seg[2]	OUT		T11	☑	14	LVCMOS33*	3.300		12
out8_7Seg[1]	OUT		L18	☑	14	LVCMOS33*	3.300		12
out8_7Seg[0]	OUT		H15	☑	15	LVCMOS33*	3.300		12
out8_Anodes (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300		12
out8_Anodes[7]	OUT		U13	☑	14	LVCMOS33*	3.300		12
out8_Anodes[6]	OUT		K2	☑	35	LVCMOS33*	3.300		12
out8_Anodes[5]	OUT		T14	☑	14	LVCMOS33*	3.300		12
out8_Anodes[4]	OUT		P14	☑	14	LVCMOS33*	3.300		12
out8_Anodes[3]	OUT		J14	☑	15	LVCMOS33*	3.300		12
out8_Anodes[2]	OUT		T9	☑	14	LVCMOS33*	3.300		12
out8_Anodes[1]	OUT		J18	☑	15	LVCMOS33*	3.300		12
out8_Anodes[0]	OUT		J17	☑	15	LVCMOS33*	3.300		12