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Reg. No. : 2021-EE-052 Marks Obtained: _____

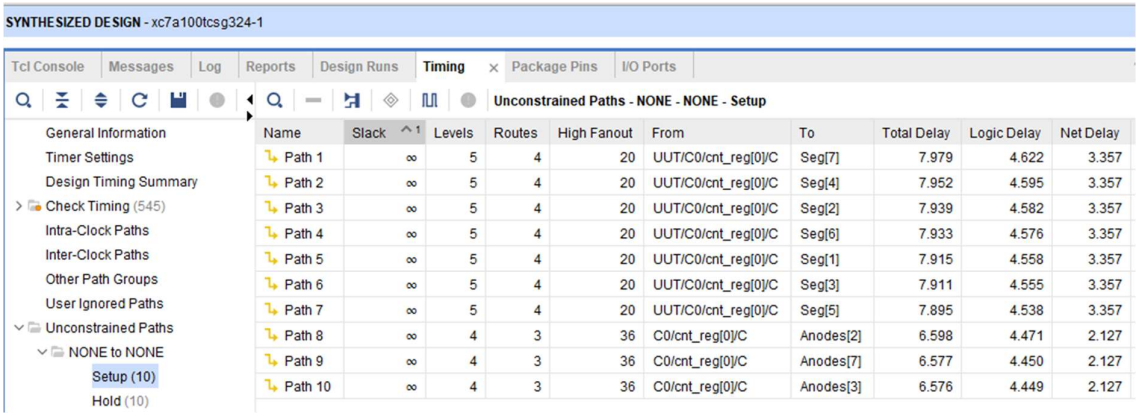
Lab Manual 7

Sequential Circuit Design: News Ticker

Question 1

Part B

The maximum delay in Synthesis is from cnt_reg[0]/C to Seg[7] of 7.979 ns.

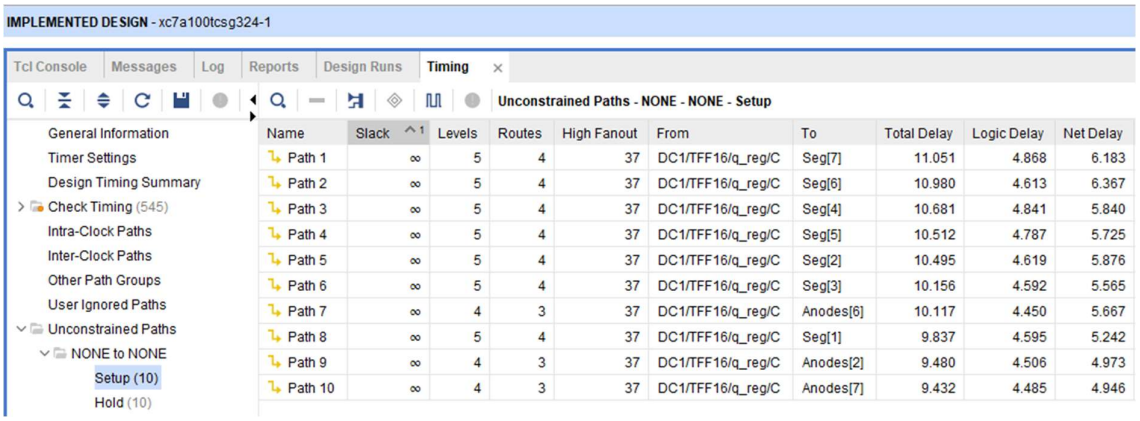


Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[7]	7.979	4.622	3.357
Path 2	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[4]	7.952	4.595	3.357
Path 3	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[2]	7.939	4.582	3.357
Path 4	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[6]	7.933	4.576	3.357
Path 5	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[1]	7.915	4.558	3.357
Path 6	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[3]	7.911	4.555	3.357
Path 7	∞	5	4	20	UUT/C0/cnt_reg[0]/C	Seg[5]	7.895	4.538	3.357
Path 8	∞	4	3	36	C0/cnt_reg[0]/C	Anodes[2]	6.598	4.471	2.127
Path 9	∞	4	3	36	C0/cnt_reg[0]/C	Anodes[7]	6.577	4.450	2.127
Path 10	∞	4	3	36	C0/cnt_reg[0]/C	Anodes[3]	6.576	4.449	2.127

Part C

The maximum delay in Implementation is from q_reg/C to Seg[7] of 11.051 ns.

The path is not the same as in the synthesis report and neither is the max delay.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[7]	11.051	4.868	6.183
Path 2	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[6]	10.980	4.613	6.367
Path 3	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[4]	10.681	4.841	5.840
Path 4	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[5]	10.512	4.787	5.725
Path 5	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[2]	10.495	4.619	5.876
Path 6	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[3]	10.156	4.592	5.565
Path 7	∞	4	3	37	DC1/TFF16/q_reg/C	Anodes[6]	10.117	4.450	5.667
Path 8	∞	5	4	37	DC1/TFF16/q_reg/C	Seg[1]	9.837	4.595	5.242
Path 9	∞	4	3	37	DC1/TFF16/q_reg/C	Anodes[2]	9.480	4.506	4.973
Path 10	∞	4	3	37	DC1/TFF16/q_reg/C	Anodes[7]	9.432	4.485	4.946

Part D

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	152	0	63400	0.24
LUT as Logic	152	0	63400	0.24
LUT as Memory	0	0	19000	0.00
Slice Registers	144	0	126800	0.11
Register as Flip Flop	144	0	126800	0.11
Register as Latch	0	0	126800	0.00
F7 Muxes	4	0	31700	0.01
F8 Muxes	0	0	15850	0.00

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref
All ports (19)								
Anodes (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300	
Anodes[7]	OUT		U13	☑	14	LVCMOS33*	3.300	
Anodes[6]	OUT		K2	☑	35	LVCMOS33*	3.300	
Anodes[5]	OUT		T14	☑	14	LVCMOS33*	3.300	
Anodes[4]	OUT		P14	☑	14	LVCMOS33*	3.300	
Anodes[3]	OUT		J14	☑	15	LVCMOS33*	3.300	
Anodes[2]	OUT		T9	☑	14	LVCMOS33*	3.300	
Anodes[1]	OUT		J18	☑	15	LVCMOS33*	3.300	
Anodes[0]	OUT		J17	☑	15	LVCMOS33*	3.300	
Seg (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300	
Seg[7]	OUT		T10	☑	14	LVCMOS33*	3.300	
Seg[6]	OUT		R10	☑	14	LVCMOS33*	3.300	
Seg[5]	OUT		K16	☑	15	LVCMOS33*	3.300	
Seg[4]	OUT		K13	☑	15	LVCMOS33*	3.300	
Seg[3]	OUT		P15	☑	14	LVCMOS33*	3.300	
Seg[2]	OUT		T11	☑	14	LVCMOS33*	3.300	
Seg[1]	OUT		L18	☑	14	LVCMOS33*	3.300	
Seg[0]	OUT		H15	☑	15	LVCMOS33*	3.300	
Scalar ports (3)								
CLK	IN		E3	☑	35	LVCMOS33*	3.300	
dir	IN		H6	☑	35	LVCMOS33*	3.300	
rst	IN		T13	☑	14	LVCMOS33*	3.300	