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Reg. No. : 2021-EE-052 Marks Obtained: _____

Lab Manual 3

Combinational Circuit Design using KMaps

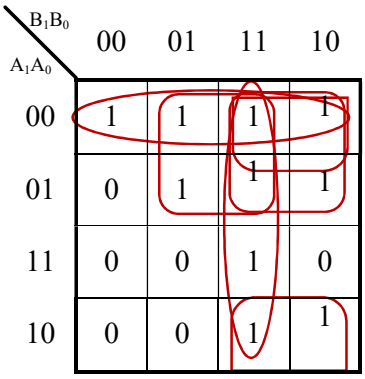
Question 1

Part A

A_1	A_0	B_1	B_0	Relation	R	G	B	Colors
0	0	0	0	a = b	1	0	1	Purple
0	0	0	1	a < b	1	1	0	Yellow
0	0	1	0	a < b	1	1	0	Yellow
0	0	1	1	a < b	1	1	0	Yellow
0	1	0	0	a > b	0	1	1	Cyan
0	1	0	1	a = b	1	0	1	Purple
0	1	1	0	a < b	1	1	0	Yellow
0	1	1	1	a < b	1	1	0	Yellow
1	0	0	0	a > b	0	1	1	Cyan
1	0	0	1	a > b	0	1	1	Cyan
1	0	1	0	a = b	1	0	1	Purple
1	0	1	1	a < b	1	1	0	Yellow
1	1	0	0	a > b	0	1	1	Cyan
1	1	0	1	a > b	0	1	1	Cyan
1	1	1	0	a > b	0	1	1	Cyan
1	1	1	1	a = b	1	0	1	Purple

Part B

Red



Prime Implicants

$\bar{A}_1\bar{A}_0$
B_1B_0
$\bar{A}_1B_0$
$\bar{A}_1B_1$
$\bar{A}_0B_1$

Essential Implicants

$\bar{A}_1\bar{A}_0$
B_1B_0
$\bar{A}_1B_0$
$\bar{A}_1B_1$
$\bar{A}_0B_1$

Green

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	1	0	1	1
11	1	1	0	1
10	1	1	1	0

Prime Implicants

$A_0\bar{B}_0$
$A_1\bar{B}_1$
$\bar{A}_0B_0$
$\bar{A}_1B_1$

Essential Implicants

$A_0\bar{B}_0$
$A_1\bar{B}_1$
$\bar{A}_0B_0$
$\bar{A}_1B_1$

Blue

A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	1	1	0	0
11	1	1	1	1
10	1	1	0	1

Prime Implicants

A_1A_0
$\bar{B}_1\bar{B}_0$
$A_0\bar{B}_1$
$A_1\bar{B}_1$
$A_1\bar{B}_0$

Essential Implicants

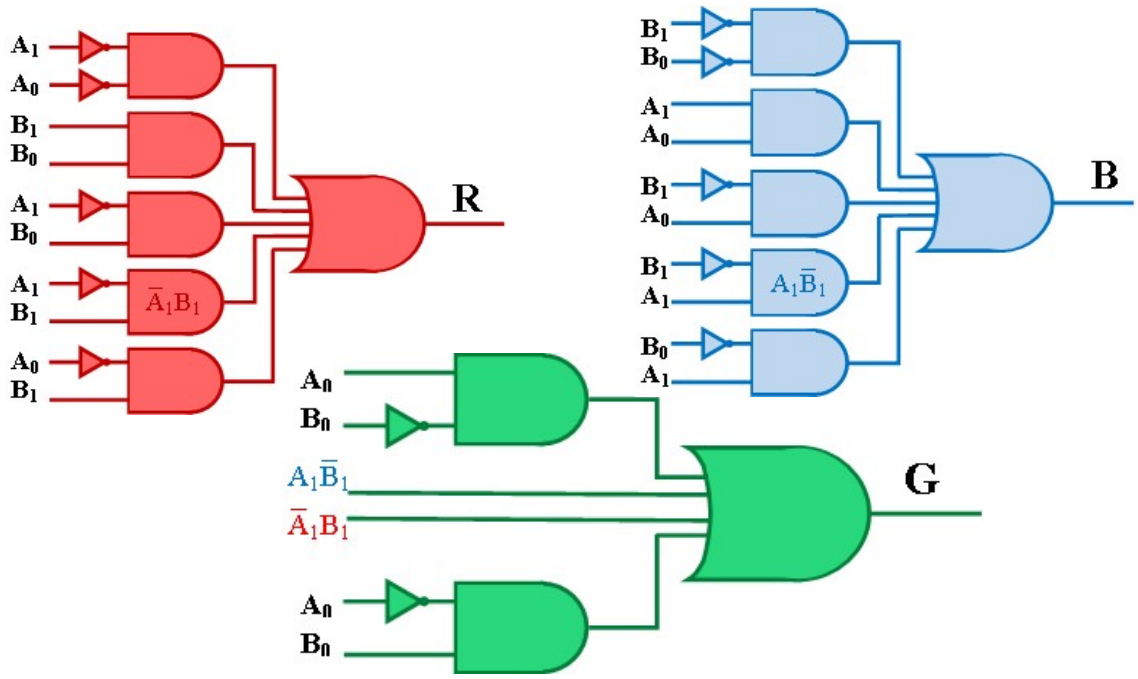
A_1A_0
$\bar{B}_1\bar{B}_0$
$A_0\bar{B}_1$
$A_1\bar{B}_1$
$A_1\bar{B}_0$

$R = \bar{A}_1\bar{A}_0 + B_1B_0 + \bar{A}_1B_0 + \bar{A}_1B_1 + \bar{A}_0B_1$

$G = A_0\bar{B}_0 + A_1\bar{B}_1 + \bar{A}_0B_0 + \bar{A}_1B_1$

$B = A_1A_0 + \bar{B}_1\bar{B}_0 + A_0\bar{B}_1 + A_1\bar{B}_1 + A_1\bar{B}_0$

Part C

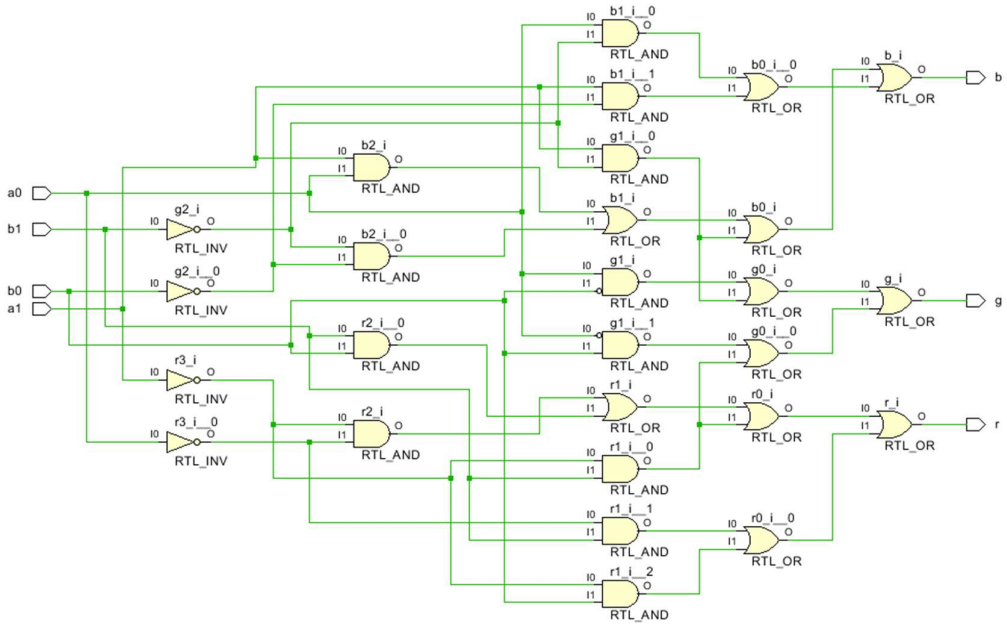


Part D

They are similar except that Vivado only used two-input gates.

Vivado used 12 two-input AND gates and 11 two-input OR gates.

My circuit has 12 two-input AND gates, 2 five-input OR gates and 1 four-input OR gate.



Part E

The maximum combinational delay is from b1 to b with a time delay of 6.782ns.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	3	b1	b	6.782	5.177	1.606	∞	input port clock
Path 2	∞	3	2	3	b1	r	6.754	5.149	1.606	∞	input port clock
Path 3	∞	3	2	3	b1	g	6.736	5.130	1.606	∞	input port clock

Part F

Tcl Console | Messages | Log | Reports | Design Runs | Package Pins | I/O Ports

Name	Direction	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
Scalar ports (7)												
a0	IN	L16	✓	14	LVCMOS33*	3.300				NONE	NONE	
a1	IN	J15	✓	15	LVCMOS33*	3.300				NONE	NONE	
b	OUT	R12	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
b0	IN	R15	✓	14	LVCMOS33*	3.300				NONE	NONE	
						3.300				NONE	NONE	
						3.300		12	SLOW	NONE	FP_VTT_50	
						3.300		12	SLOW	NONE	FP_VTT_50	

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	7	0	210	3.33
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2	0	63400	<0.01
LUT as Logic	2	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00