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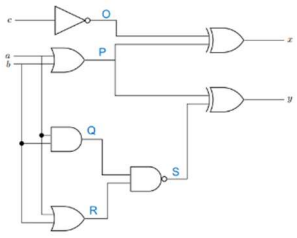
Reg. No.: 2021-EE-052 Marks Obtained: _____

Lab Manual 2

Combinational Circuit Simulation



Question 1

Part A

A	B	C	O = $\bar{C}$	R=P=A+B	Q=AB	S=$\bar{Q}\bar{R}$	X=O⊕P	Y=P⊕S
0	**0**	**0**	1	0	0	1	1	1
0	**0**	**1**	0	0	0	1	0	1
0	**1**	**0**	1	1	0	1	0	0
0	**1**	**1**	0	1	0	1	1	0
1	**0**	**0**	1	1	0	1	0	0
1	**0**	**1**	0	1	0	1	1	0
1	**1**	**0**	1	1	1	0	0	1
1	**1**	**1**	0	1	1	0	1	1

Part B

The errors found in Listing 4 include:

1. Line 4: A ‘;’ (semicolon) was used but a ‘,’ (comma) should have been used.
2. Line 9: A ‘;’ (semicolon) was missing at the end of the line.
3. Line 10: The ‘&’ (AND symbol) was missing between ‘c’ and ‘(a ^ b)’.

The errors found in Listing 5 include:

1. Line 8: Missing instance name in initiation of module.
2. Line 19: Logic a, b, and c are not defined here so it is incorrect. Instead use a1, b1 and c1.
3. Line 21: c is used here instead of c1.
4. Line 25: b is used here instead of b1.
5. Line 31: a is used here instead of a1.
6. Line 36: Missing ‘end’

Part C

Corrected code of Listing 4 is:

```
module full_adder(
input logic a,
input logic b,
input logic c,
output logic sum,
output logic carry
);

assign sum = (a ^ b) ^ c;
assign carry = (a & b) | (c & (a ^ b));

endmodule
```

Corrected code of Listing 5 is:

```
module full_adder_tb();
logic a1;
logic b1;
logic c1;
logic sum1;
logic carry1;

full_adder UUT(
.a(a1),
.b(b1),
.c(c1),
.sum(sum1),
.carry(carry1)
);

initial
begin
// Provide different combinations of the
inputs to check validity of code
a1 = 0; b1 = 0; c1 = 0;
#10;
a1 = 0; b1 = 0; c1 = 1;
#10;
a1 = 0; b1 = 1; c1 = 0;
#10;
a1 = 0; b1 = 1; c1 = 1;
#10;
a1 = 1; b1 = 0; c1 = 0;
#10;
a1 = 1; b1 = 0; c1 = 1;
#10;
a1 = 1; b1 = 1; c1 = 0;
#10
a1 = 1; b1 = 1; c1 = 1;
#10;
$stop;
end
endmodule
```

Question 2

System Verilog code of given circuit is:

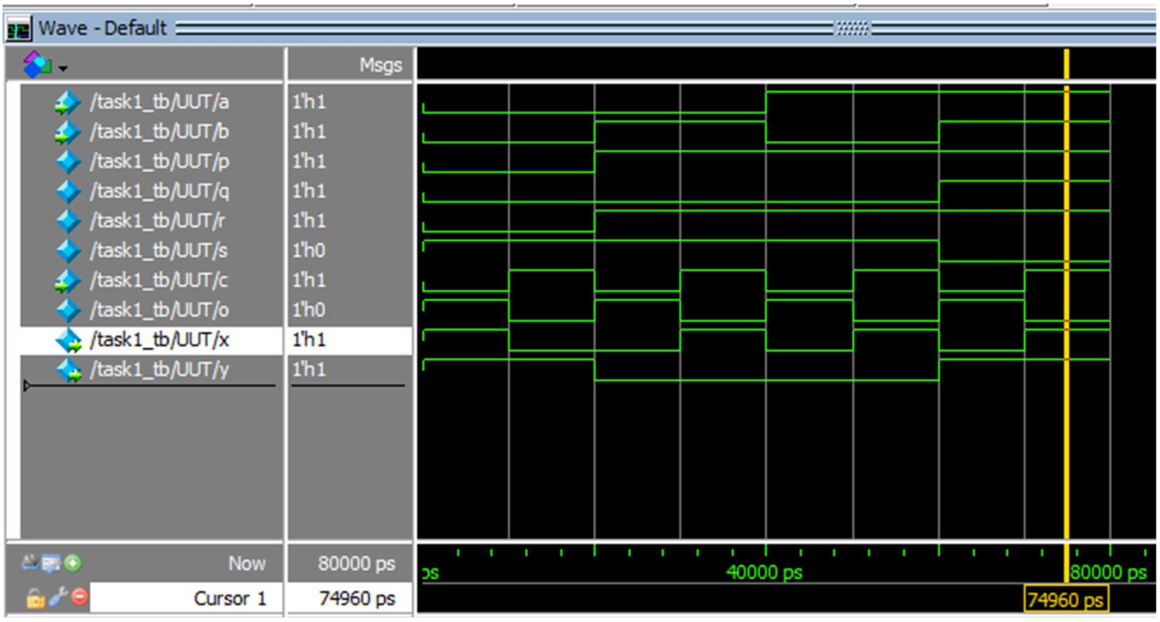
```
`timescale 1ns/10ps

module task1(output logic x,y,
input logic a,b,c
);
wire o,p,q,r,s;

not n1(o,c);
or o1(p,a,b);
or o2(r,a,b);
and a1(q,a,b);
nand na1(s,q,r);
xor xo1(x,o,p);
xor xo2(y,p,s);

endmodule
```

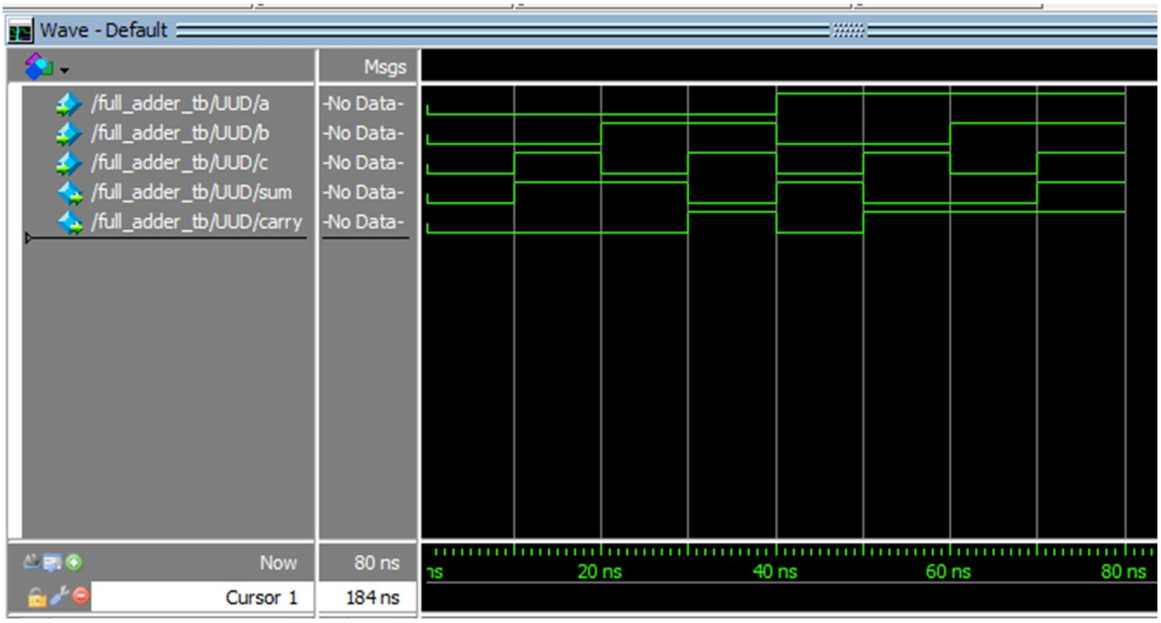
Question 3

Test Bench code of given circuit is:

```
`timescale 1ns/10ps

module task1_tb;
logic a1;
logic b1;
logic c1;
logic x1;
logic y1;

localparam period = 10;
task1 UUT(
.a(a1),
.b(b1),
.c(c1),
.x(x1),
.y(y1)
);

initial //initial block executes only once
begin
// Provide different combinations of the
inputs to check validity of code
a1 = 0; b1 = 0; c1 = 0;
#period;
a1 = 0; b1 = 0; c1 = 1;
#period;
a1 = 0; b1 = 1; c1 = 0;
#period;
a1 = 0; b1 = 1; c1 = 1;
#period;
a1 = 1; b1 = 0; c1 = 0;
#period;
a1 = 1; b1 = 0; c1 = 1;
#period;
a1 = 1; b1 = 1; c1 = 0;
#period;
a1 = 1; b1 = 1; c1 = 1;
#period;
$stop;
end

initial
begin
/*the following system task will print
out the signal values
every time they change on the Transcript
Window */
$monitor("y=%b, x=%b, a=%b, b=%b,
c=%b", y1,x1,a1,b1,c1);
end

endmodule
```

Question 4


Wave - Default
Msgs
/task1_tb/UUT/a
/task1_tb/UUT/b
/task1_tb/UUT/p
/task1_tb/UUT/q
/task1_tb/UUT/r
/task1_tb/UUT/s
/task1_tb/UUT/c
/task1_tb/UUT/o
/task1_tb/UUT/x
/task1_tb/UUT/y
1'h1
1'h1
1'h1
1'h1
1'h1
1'h0
1'h1
1'h0
1'h1
1'h1
Now
80000 ps
Cursor 1
74960 ps
40000 ps
80000 ps
74960 ps


Wave - Default
Msgs
/full_adder_tb/UUD/a
/full_adder_tb/UUD/b
/full_adder_tb/UUD/c
/full_adder_tb/UUD/sum
/full_adder_tb/UUD/carry
-No Data-
-No Data-
-No Data-
-No Data-
-No Data-
Now
80 ns
Cursor 1
184 ns
20 ns
40 ns
60 ns
80 ns