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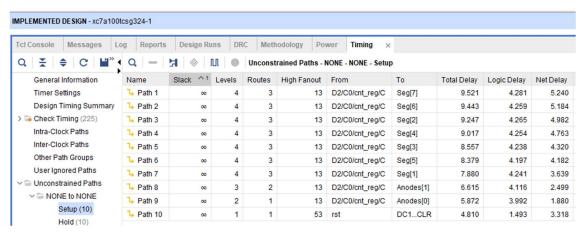Reg. No. : 2021-EE-052   Marks Obtained: _____

Lab Manual 8

State Machines: A Read-Modify-Write Circuit

Question 1

Part C

The maximum delay in Implementation is from cnt_reg/C to Seg[7] of 9.521 ns.

IMPLEMENTED DESIGN - xc7a100tcsg324-1

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	4	3	13	D2/C0/cnt_reg/C	Seg[7]	9.521	4.281	5.240
Path 2	∞	4	3	13	D2/C0/cnt_reg/C	Seg[6]	9.443	4.259	5.184
Path 3	∞	4	3	13	D2/C0/cnt_reg/C	Seg[2]	9.247	4.265	4.982
Path 4	∞	4	3	13	D2/C0/cnt_reg/C	Seg[4]	9.017	4.254	4.763
Path 5	∞	4	3	13	D2/C0/cnt_reg/C	Seg[3]	8.557	4.238	4.320
Path 6	∞	4	3	13	D2/C0/cnt_reg/C	Seg[5]	8.379	4.197	4.182
Path 7	∞	4	3	13	D2/C0/cnt_reg/C	Seg[1]	7.880	4.241	3.639
Path 8	∞	3	2	13	D2/C0/cnt_reg/C	Anodes[1]	6.615	4.116	2.499
Path 9	∞	2	1	13	D2/C0/cnt_reg/C	Anodes[0]	5.872	3.992	1.880
Path 10	∞	1	1	53	rst	DC1...CLR	4.810	1.493	3.318

Part D

```
+--------------------------+------+-------+-----------+-------+
|        Site Type         | Used | Fixed | Available | Util% |
+--------------------------+------+-------+-----------+-------+
| Slice LUTs*              |  44  |   0   |   63400   | 0.07  |
|   LUT as Logic           |  44  |   0   |   63400   | 0.07  |
|   LUT as Memory          |   0  |   0   |   19000   | 0.00  |
| Slice Registers          |  62  |   0   |  126800   | 0.05  |
|   Register as Flip Flop  |  61  |   0   |  126800   | 0.05  |
|   Register as Latch      |   1  |   0   |  126800   | <0.01 |
| F7 Muxes                 |   0  |   0   |   31700   | 0.00  |
| F8 Muxes                 |   0  |   0   |   15850   | 0.00  |
+--------------------------+------+-------+-----------+-------+
```

I/O Ports

Name	Direction ^1	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
∨ 🗁 All ports (23)							
∨ 🗁 Scalar ports (4)							
📝 bit_value	IN		T18 ∨	☑	14	LVCMOS33* ▾	3.300
📝 CLK	IN		E3 ∨	☑	35	LVCMOS33* ▾	3.300
📝 rst	IN		R17 ∨	☑	14	LVCMOS33* ▾	3.300
📝 valid_in	IN		R15 ∨	☑	14	LVCMOS33* ▾	3.300
∨ 📝 bit_index (3)	IN			☑	(Multiple)	LVCMOS33*	3.300
📝 bit_index[2]	IN		M13 ∨	☑	14	LVCMOS33* ▾	3.300
📝 bit_index[1]	IN		L16 ∨	☑	14	LVCMOS33* ▾	3.300
📝 bit_index[0]	IN		J15 ∨	☑	15	LVCMOS33* ▾	3.300
∨ 📝 Anodes (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300
📝 Anodes[7]	OUT		U13 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Anodes[6]	OUT		K2 ∨	☑	35	LVCMOS33* ▾	3.300
📝 Anodes[5]	OUT		T14 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Anodes[4]	OUT		P14 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Anodes[3]	OUT		J14 ∨	☑	15	LVCMOS33* ▾	3.300
📝 Anodes[2]	OUT		T9 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Anodes[1]	OUT		J18 ∨	☑	15	LVCMOS33* ▾	3.300
📝 Anodes[0]	OUT		J17 ∨	☑	15	LVCMOS33* ▾	3.300
∨ 📝 Seg (8)	OUT			☑	(Multiple)	LVCMOS33*	3.300
📝 Seg[7]	OUT		T10 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Seg[6]	OUT		R10 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Seg[5]	OUT		K16 ∨	☑	15	LVCMOS33* ▾	3.300
📝 Seg[4]	OUT		K13 ∨	☑	15	LVCMOS33* ▾	3.300
📝 Seg[3]	OUT		P15 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Seg[2]	OUT		T11 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Seg[1]	OUT		L18 ∨	☑	14	LVCMOS33* ▾	3.300
📝 Seg[0]	OUT		H15 ∨	☑	15	LVCMOS33* ▾	3.300