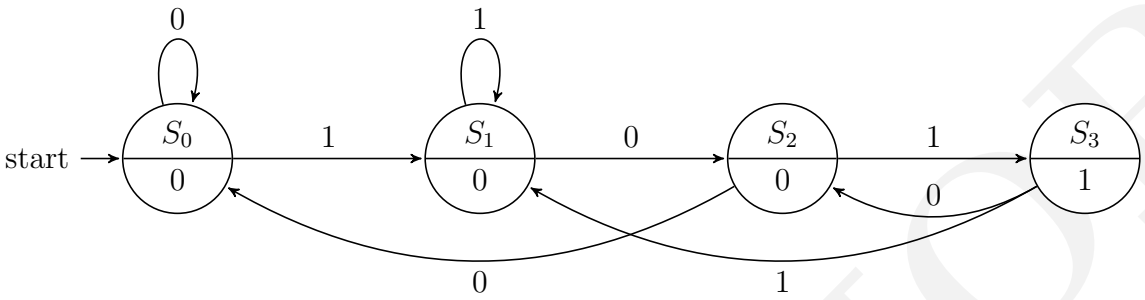
Finite State Machines

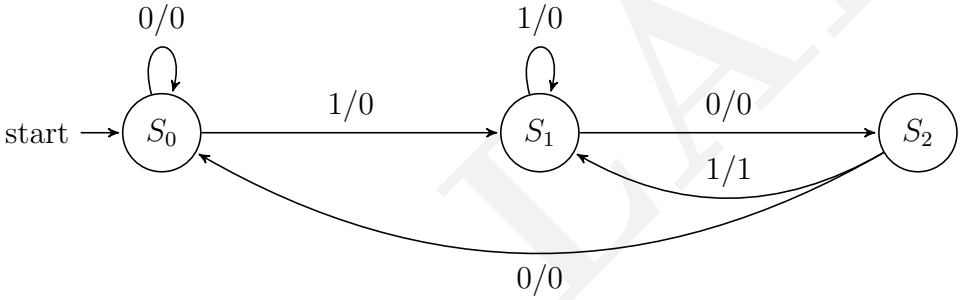
We are going to design Moore and Mealy state machines for detection of *overlapping* sequence *101*.

Moore State Machine



It can be coded as shown in Listing 1.

Mealy State Machine



It can be coded as shown in Listing 2.

UET, LAHORE

```
module stg101(
   input logic clk,
   input logic reset,
   input logic in,
   output logic out );

logic [1:0] c_state, n_state;
parameter S0=2'b00, S1=2'b01, S2=2'b10, S3=2'b11;

//state register
always_ff @ (posedge clk or negedge reset)
begin
//reset is active low
if (!reset)
   c_state <= S0;
else
   c_state <= n_state;
end

//next_state always block
always_comb
begin
case (c_state)
S0: begin if (in) n_state = S1;
          else    n_state = S0; end

S1: begin if (in) n_state = S1;
          else    n_state = S2; end

S2: begin if (in) n_state = S3;
          else    n_state = S0; end

S3: begin if (in) n_state = S1;
          else    n_state = S2; end

default:          n_state = S0;
endcase
end

//output always block
always_comb
begin
case (c_state)
     S0: out = 1'b0;
     S1: out = 1'b0;
     S2: out = 1'b0;
     S3: out = 1'b1;
default: out = 1'b0;
endcase
end
endmodule
```

Listing 1: System Verilog Code for Moore STG

UET, LAHORE

```
module stg101(
input logic clk,
input logic reset,
input logic in,
output logic out );

logic [1:0] c_state, n_state;
parameter S0=2'b00, S1=2'b01, S2=2'b10;

//state register
always_ff @ (posedge clk or negedge reset)
begin
//reset is active low
if (!reset)
c_state <= S0;
else
c_state <= n_state;
end

//next_state always block
always_comb
begin
case (c_state)
S0: begin if (in) n_state = S1;
else    n_state = S0; end

S1: begin if (in) n_state = S1;
else    n_state = S2; end

S2: begin if (in) n_state = S1;
else    n_state = S0; end

default:          n_state = S0;
endcase
end

//output always block
always_comb
begin
case (c_state)
S0: begin if (in) out = 1'b0;
else    out = 1'b0; end

S1: begin if (in) out = 1'b0;
else    out = 1'b0; end

S2: begin if (in) out = 1'b1;
else    out = 1'b0; end

default:          out = S0;
endcase
end
endmodule
```

Listing 2: System Verilog Code for Mealy STG

UET, LAHORE