Example

1. Assume it takes 1 extra cycle if the instruction misses in the cache is found in the Pre-fetch buffer. Suppose that the pre-fetch hit rate is 30%, instruction cache miss rate 2%, hit time takes 2 cycles, and miss penalty takes 50 cycles. What is the effective miss rate using instruction prefetching?

- 2. Assume it takes 2 extra cycles to find the entry in the alternative cache using pseudo-associative scheme. Hit time takes 2 cycles, and miss penalty takes 50 cycles. Suppose that miss rate of a 16K direct map cache is 2%, miss rate of a 16K 2-way set associative cache is 1.2%, Compute the average memory access time of a 16K pseudo set associative cache.

Answer 1

- AMAT_prefetch
  = HitTime + MissRate * PrefetchHitRate*1 + MissRate*(1-PrefetchHitRate)*MissPenalty
  = 2 + 2%*70%*1 + 2%*30%*50 = 2+0.014+0.3=2.314

AMAT = HitTime + EffectiveMissRate*MissPenalty

2.314 = 2 + EffectiveMissRate*50

EffectiveMissRate = 0.628%

Answer 2

- AMAT_pseudo

  = HitTime_pseudo

  + MissRate_pseudo * MissPenatly_pseudo

= HitTime + AltHitRate*2

  + MissRate_2way * MissPenalty

= 2 + (MissRate_1way – MissRate_2way)*2

  + 1.2% *50

= 2 + (2%-1.2%)*2 + 1.2%*50 = 2+0.016+0.6=2.616

Ex

- The impact of second-level cache associativity on the miss penalty

- Assume
  - Two-way set associativity increases hit time by 10% of a CPU clock cycle
  - Hit time(L2) for direct mapped cache = 10 clock cycles
  - Local miss rate(L2) for direct mapped = 25%
  - Local miss rate(L2) for two-way set associative = 20%
  - Miss penalty(L2) =50 cycles

- What is the First level cache miss penalty for
  - Direct mapped L2 cache
  - 2-way associative L2 Cache

AMAT = Hit TimeL1 + Miss RateL1 x Miss PenaltyL1
Miss PenaltyL1 = Hit TimeL2 + Miss RateL2 x Miss PenaltyL2

AMAT = Hit TimeL1 + Miss RateL1 x (Hit TimeL2 + Miss RateL2 x Miss PenaltyL2)

Ans

- For a direct-mapped
  - First level cache Miss penalty(1 way, L2) = 10+25%x50 = 22.5 clock cycles
- For a two-way set associative
  - First level cache Miss Penalty(2 way, L2) = 10.1 + 20%x50 = 20.1 clock cycles
- If we restrict the hit time to be an integer number of clock cycles
  - Miss Penalty(2 way, L2) = 11 + 20%x50 = 21 clock cycles