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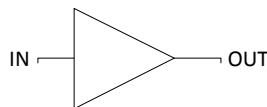
ECE 198 JL Worksheet 8: Storage elements

Before you come to discussion, please read about the tri-state buffer below and Lecture Notes on *Random Access Memory*.

In this discussion section, you will analyze the work of a static RAM cell. You will also implement the logic necessary to control the RAM cell in order to enable it to store data at a location specified by an address. And finally you will learn how to build memory systems by using smaller memory chips.

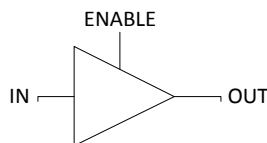
Tri-state buffer

- A *buffer* is a device that passes an input to its output



IN	OUT
0	0
1	1

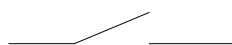
- A *tri-state buffer* is a device with 3 output states: 0, 1, and 'Z' (high impedance)



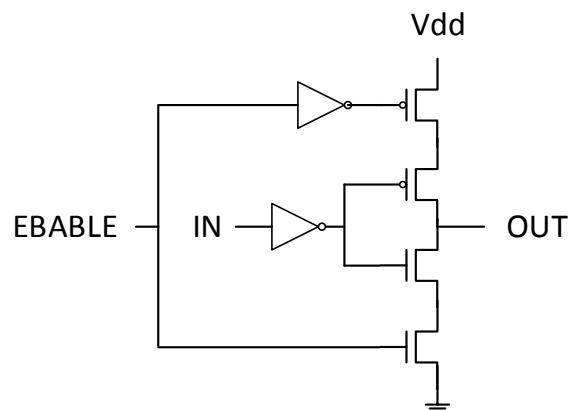
IN	ENABLE	OUT
0	1	0
1	1	1
X	0	Z

- Z, or Hi-Z output means "Disconnected" - no output appears at all, similar to what a mechanical switch would do

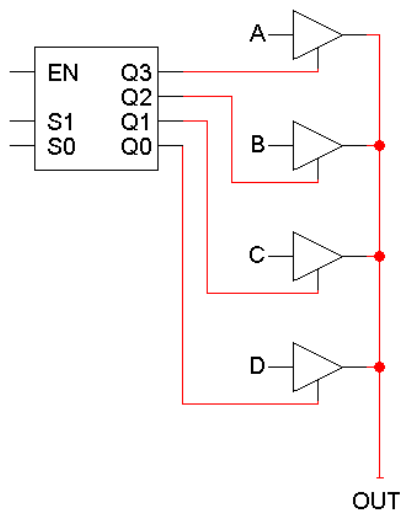
ENABLE



- We can build a tri-state buffer using just a few MOS FETs



- We will use tri-state buffer to connect multiple outputs together



Decoder disabled

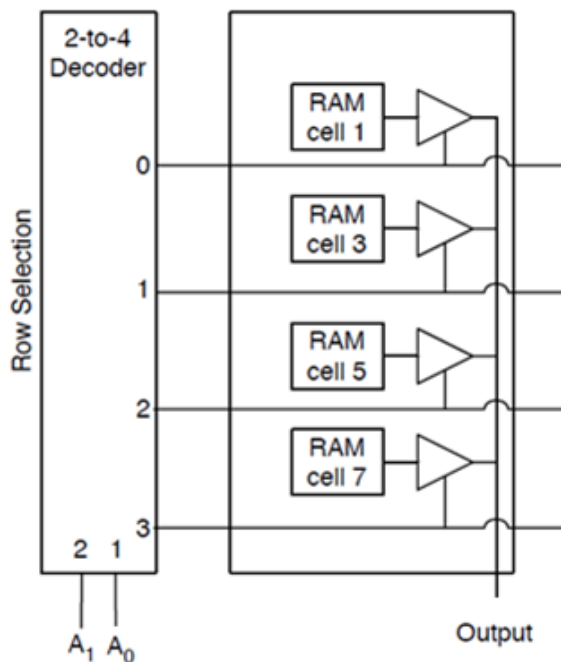
- all the three-state buffers will appear to be disconnected, and OUT will also appear disconnected

Decoder enabled

- exactly one of its outputs will be true, so only one of the tri-state buffers will be connected and produce an output

- RAM using tri-state buffers

- Let's say we have a large array of RAM. It's not economical to multiplex every bit. Consider the case of a 1KB (1K x 8-bit) RAM. If we were to use multiplexers to access individual bytes at a time, we would need have a 1024-to-1 8-bit multiplexer. The logic involved to create such a MUX would be huge as well as the necessary wires to connect everything.
- The selection logic to output a particular bit can be greatly reduced by using tri-state buffers. In this setup each RAM cell will have its own tri-state buffer on the output as illustrated below for a 4x1-bit RAM



RAM chips gated with a tri-state buffer are drawn with a triangle sign next to the output port.

