Sltiu Instruction

Datapath:

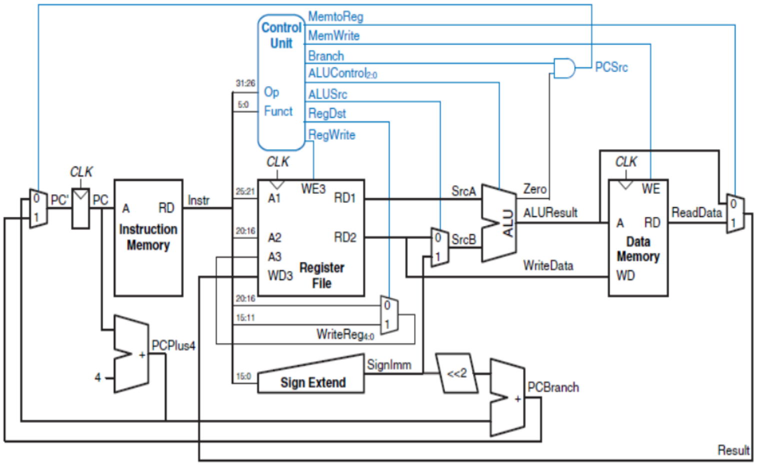
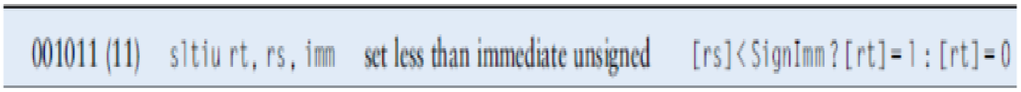


Figure 7.11 Complete single-cycle MIPS processor



001011 (11)	sltiu rt, rs, imm	set less than immediate unsigned	[rs]<SignImm ? [rt]=1 : [rt]=0

This instruction works as following, first there is a comparison between the rs register and the unsigned immediate. If the rs is less than the immediate, then rt is set to 1, else, rt is set to zero.
First, the rs is fetched into the register file, it's then decoded and sent to the ALU to operate on. What we changed is that the mux at SrcB chooses between the RD2 from register file, the SignImm and the ZeroExtend and we want the

zeroextend for the instruction to operate correctly. Again, there is no need for the data memory so the ALUResult is sent directly to the register file, whether rt is zero or one.

- ***Control Unit:***

RegWrite	***RegDst***	***MemWrite***	***MemToReg***	***Branch***	***AluControl***	***AluSrc***
11	***0***	***0***	***0***	***0***	***1100***	***01***

✓ *Hardware*

For the hardware implementation, to add Sltiu instruction we went with Three main steps:

- ***1st Step***

We added the op code and controls of this instruction to the MainDecoder (maindec) and you can see the controls of this instruction in the table above.

- ***2nd Step***

After that, we went to the AluDecoder (aludec) to add the aluop of this instruction, given that it's an I-Type instruction so there will be no access to func.

- ***3rd Step***

Finally, now we added the sltiu instruction operation code to the Alu.