Andrew Nguyen

PERSONAL INFO

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TECHNICAL SKILLS

</> C++, Python, Verilog, Golang

Arduino, Circuit Studio, Soldering

INTERESTS

- **Compiler design and optimization**
  Modern computing architectures are ever-improving, and compilers must evolve to match. This includes the creation of compilers for domain specific accelerators and languages.
- **High performance computing and heterogeneous systems**
  Improvements in computing performance rely less and less on Moore's Law. Modern computing paradigms and programming systems must be designed for a post-Moore world.

EDUCATION

Northeastern University, Boston, MA *May 2024*
Candidate for Bachelor of Science in Electrical and Computer Engineering GPA 3.785
Honors: Dean's List
Coursework: Computer Architecture and Organization, Simulation and Performance Evaluation, Digital Design and Computer Organization, Algorithms, Electromagnetics, Electronics
Activities: IEEE, Student Cluster Competition at SC22

EXPERIENCE

Advanced Micro Devices Inc. *June 2023 - December 2023*
Shader Compiler Engineer

- Diagnosed and repaired defects in the shader compiler such as undefined instruction operands being produced during IR code generation, and shaders failing to execute properly during runtime.
- Built, tested, and debugged GPU drivers through running benchmarks for real-world applications in order to validate the changes made to said drivers via modifications to the shader compiler.
- Investigated the efficacy of implementing features used in ray tracing shader compilation for the compilation of general compute shaders in order to improve memory allocation and prevent register spilling.
- Modified the compiler to examine the memory usage of compute shaders by calculating the per-region register pressure for Vector General Purpose Registers (VGPRs) within the shader's IR code flow graph.

Notch Inc. *July 2022 - December 2022*
Electrical and Computer Engineering Co-op

- Programmed embedded control code for the Raspberry Pi Pico and the ATTiny85 microprocessors for interfacing with components such as multiplexers and analog to digital converters via the I2C communication protocol.
- Redesigned a modular antenna control system consisting of interconnected circuit boards with SMT components (0402, 0603) connected to an embedded microcontroller capable of outputting 30 to 2160 unique load lines.
- Created a test board for connecting to the modular system and testing the functionality of all components and system configurations, along with testing software allowing the system to detect and self diagnose bugs.
- Debugged the modular system, diagnosing issues such as overloaded power rails and faulty board-to-board connectors and reworked the circuit boards to incorporate improvements such as more robust FFC connectors to link boards.

RESEARCH

Northeastern University Computer Architecture Research Lab *January 2022 - Present*
Luthier: A Binary Instrumentator for AMD GPUs
Advisor: Dr. David Kaeli

- A dynamic binary instrumentation framework targeting AMD's CDNA Instinct GPUs, inspired by tools such as Nvidia's NVBit and Intel's Pin Tool.
- Instrumenting code by capturing binary code objects during runtime intialization and inserting calls to instrumentation functions at the binary level.
- Integrating LLVM libraries to facilitate JIT compilation for dynamic code generation and validation in order to edit already compiled binaries.

NaviSim
Advisor: Dr. Yifan Sun

- An event driven GPU simulator designed to accurately and efficiently model the behavior of GPUs built off of AMD's RDNA and CDNA architectures
- Validated the GPU behavior for computational workloads by running various benchmarks, and recording data using Jupyter notebook to inform the tuning and optimization of the simulator code.

POSTERS

Sibir: A Binary Instrumentation Framework for AMD GPUs *April 2023*
Presented as poster at the RISE 2023 research expo. *Northeastern University*

PROJECTS

5 Staged Pipeline ARM Microprocessor *June 2022*

- Converted the 5 stage MIPS pipeline to the LEGv8 instruction set in Vivado, resulting in a working 32-bit CPU that implements optimized designs for digital circuits such as a look and carry ALU, capable of loading and storing 64-bit words as well as handling branching instructions.
- Programmed a test script for the microprocessor in ARM assembly consisting of over 200 instructions spread across 12 basic blocks that tested branching, arithmetic, logical operations, and memory access.

Sudoku Solving Program *December 2021*

- Programmed a recursive, back-tracking algorithm to solve Sudoku puzzles using an object-oriented approach in C++, optimized the algorithm to be able to solve difficult puzzles within 138,000 recursions.
- Collaborated in a team with two other students in order to efficiently delegate work and to quickly implement different methods for optimizations.

Video Game Project for Embedded Design *June 2021*

- Created a game using C++ to control the Altera DE1-SoC FPGA board's embedded hardware, which included video output onto an external VGA display, audio output from an external speaker, and input using push-buttons.
- Optimized algorithms for drawing moving shapes of different lengths and colors to run efficiently while playing sounds.