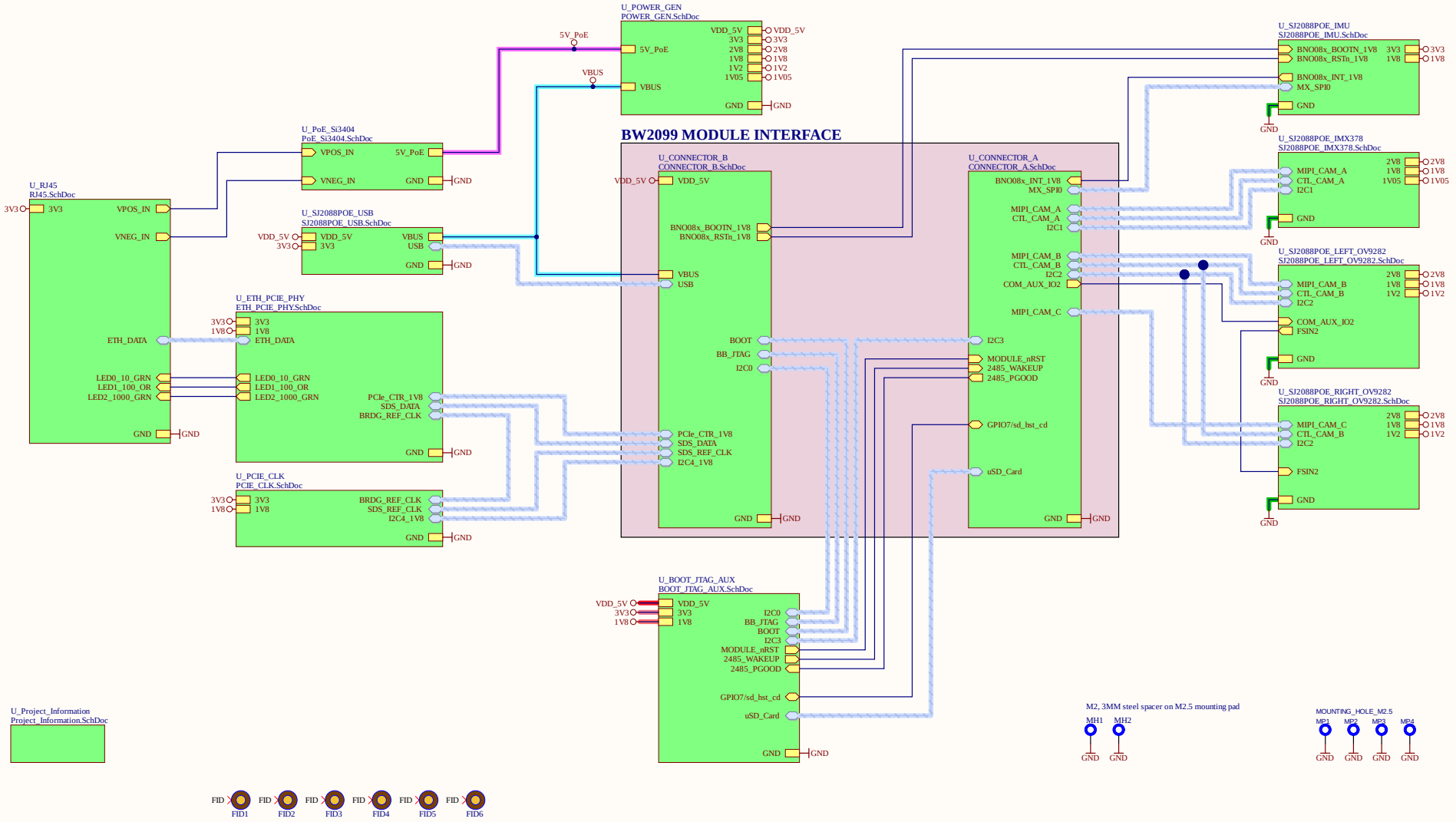
Project: ***SJ2088POE***
Current Revision: ***R0M0E0***

SJ2088POE Revision History:

Date	Revision	Reason for Change	Changes Implemented
5/12/2020	Iniital Release -> R0M0E0		
...	...	..	...
...	...	...	...

Title	***SJ2088POE***		*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number: D2098000	Revision: R0M0E0		
Date: 5/01/2021	Time: 10:26:16 PM	Sheet 1 of 12		
Drawn by: ***Brian Weinstein / Sandesh Joshi***				



Title	SJ2088POE		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:16 PM	Sheet 2 of 12	
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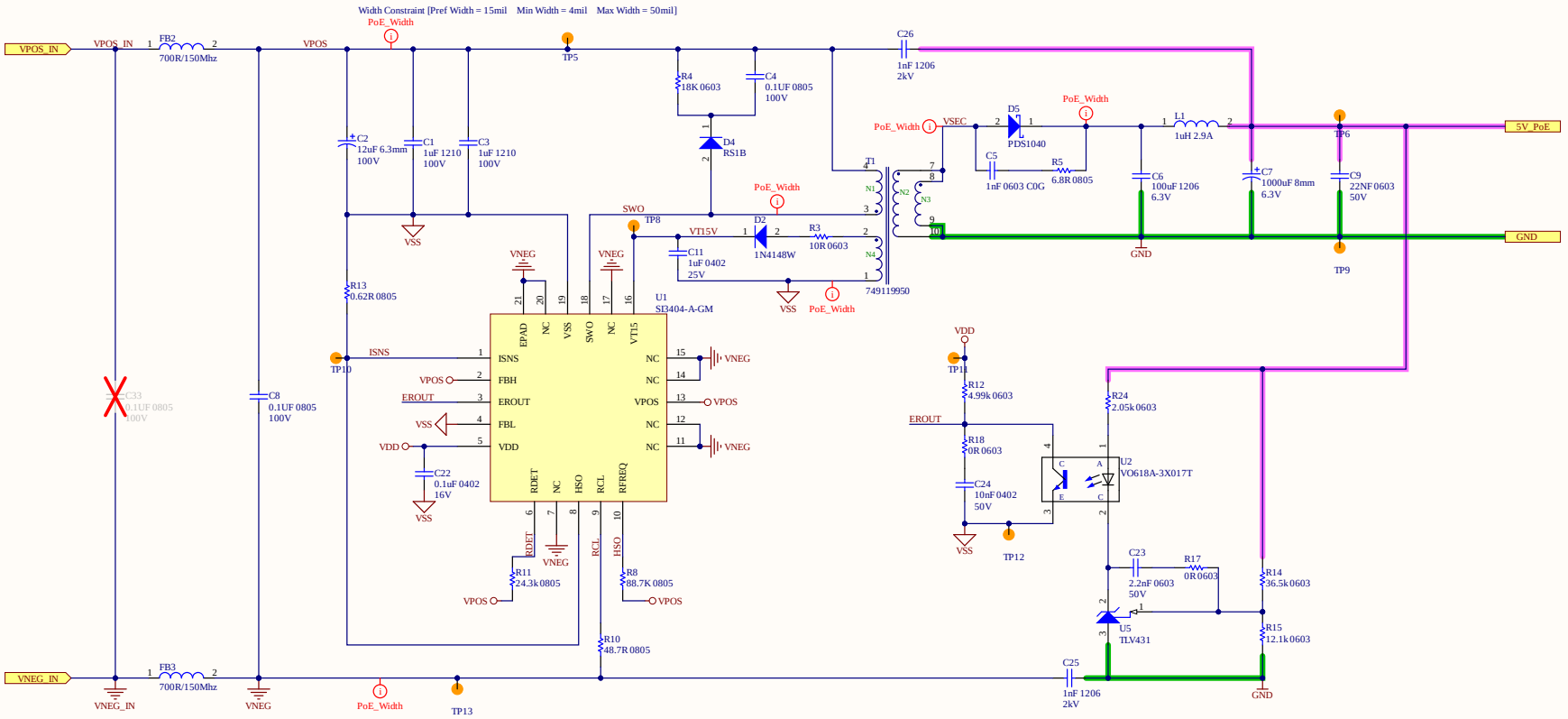
Width Constraint [Pref Width = 15mil Min Width = 4mil Max Width = 50mil]
VPOS_IN
VPOS_IN
FB2
700R/150Mhz
VPOS
PoE_Width
TP5
C26
1nF 1206
2kV
R4
18K 0603
C4
0.1UF 0805
100V
C2
12uF 6.3mm
100V
C1
1uF 1210
100V
C3
1uF 1210
100V
D4
RS1B
VSS
PoE_Width
VSEC
D5
PDS1040
L1
1uH 2.9A
5V_PoE
TP6
C5
1nF 0603 C0G
R5
6.8R 0805
C6
100uF 1206
6.3V
C7
1000uF 8mm
6.3V
C9
22NF 0603
50V
GND
TP9
T1
749119950
SWO
TP8
VT15V
D2
1N4148W
R3
10R 0603
C11
1uF 0402
25V
VNEG
R13
0.62R 0805
U1
SI3404-A-GM
EPAD
NC
VSS
SWO
NC
VT15
ISNS
FBH
EROUT
FBL
VDD
RDET
NC
HSO
RCL
RFREQ
NC
VPOS
TP10
C33
0.1UF 0805
100V
C8
0.1UF 0805
100V
C22
0.1uF 0402
16V
R11
24.3k 0805
R8
88.7K 0805
R10
48.7R 0805
VDD
TP11
R12
4.99k 0603
R18
0R 0603
C24
10nF 0402
50V
TP12
U2
VO618A-3X017T
R24
2.05k 0603
C23
2.2nF 0603
50V
R17
0R 0603
R14
36.5k 0603
U5
TLV431
R15
12.1k 0603
C25
1nF 1206
2kV
VNEG_IN
FB3
700R/150Mhz
VNEG
TP13
VNEG is a thermal plane as well as ESD and EMI. Use thermal vias to at least 1 inch square plane on backside.
Schematic based on the reference design for the SI3404 PoE.
Title SJ2088POE
Size: Tabloid
Number: D2098000
Revision: R0M0E0
Date: 5/01/2021
Time: 10:26:16 PM
Sheet 3 of 12
Drawn by: Brian Weinstein / Sandesh Joshi
Luxonis Holding
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United States
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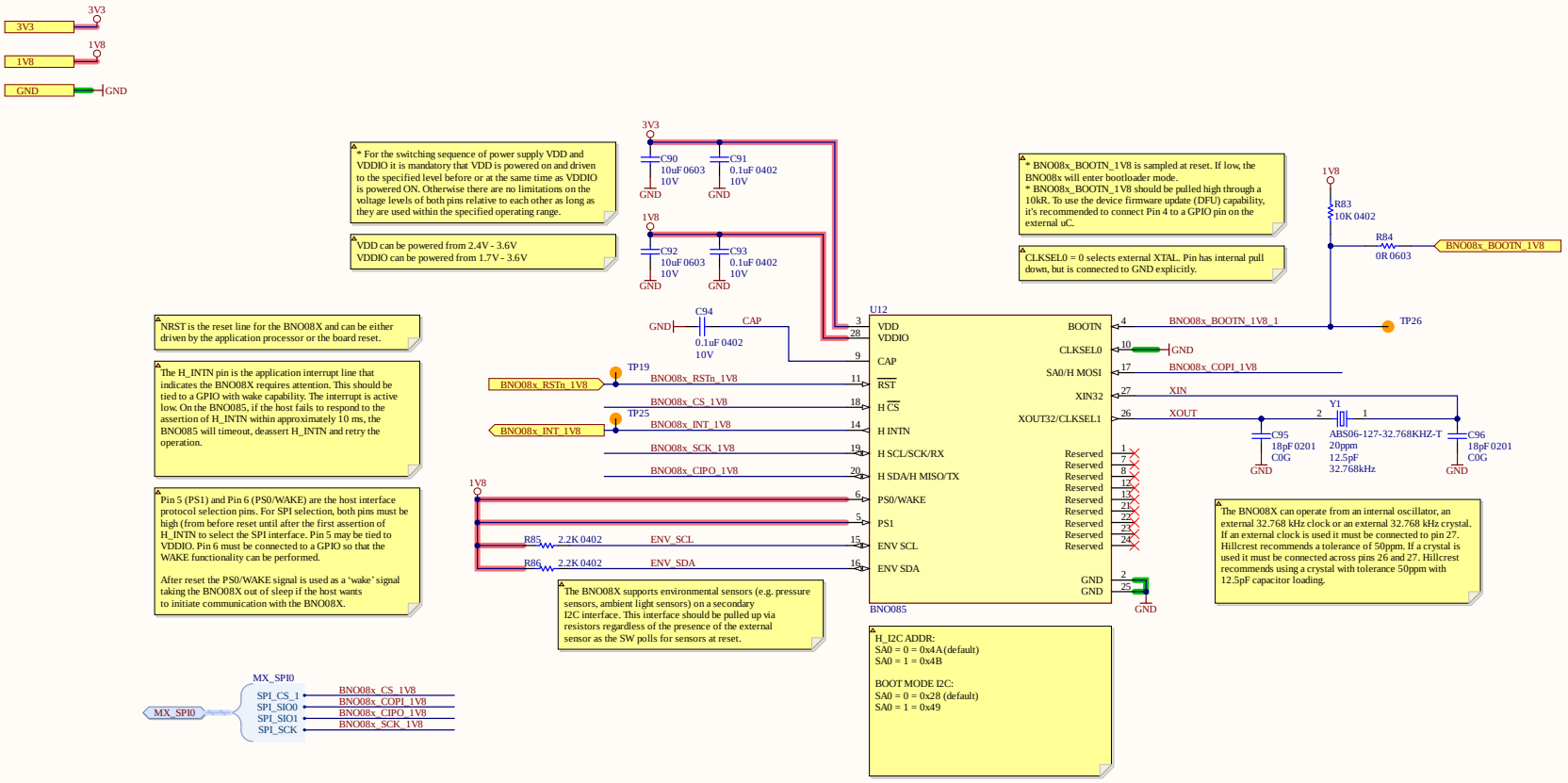

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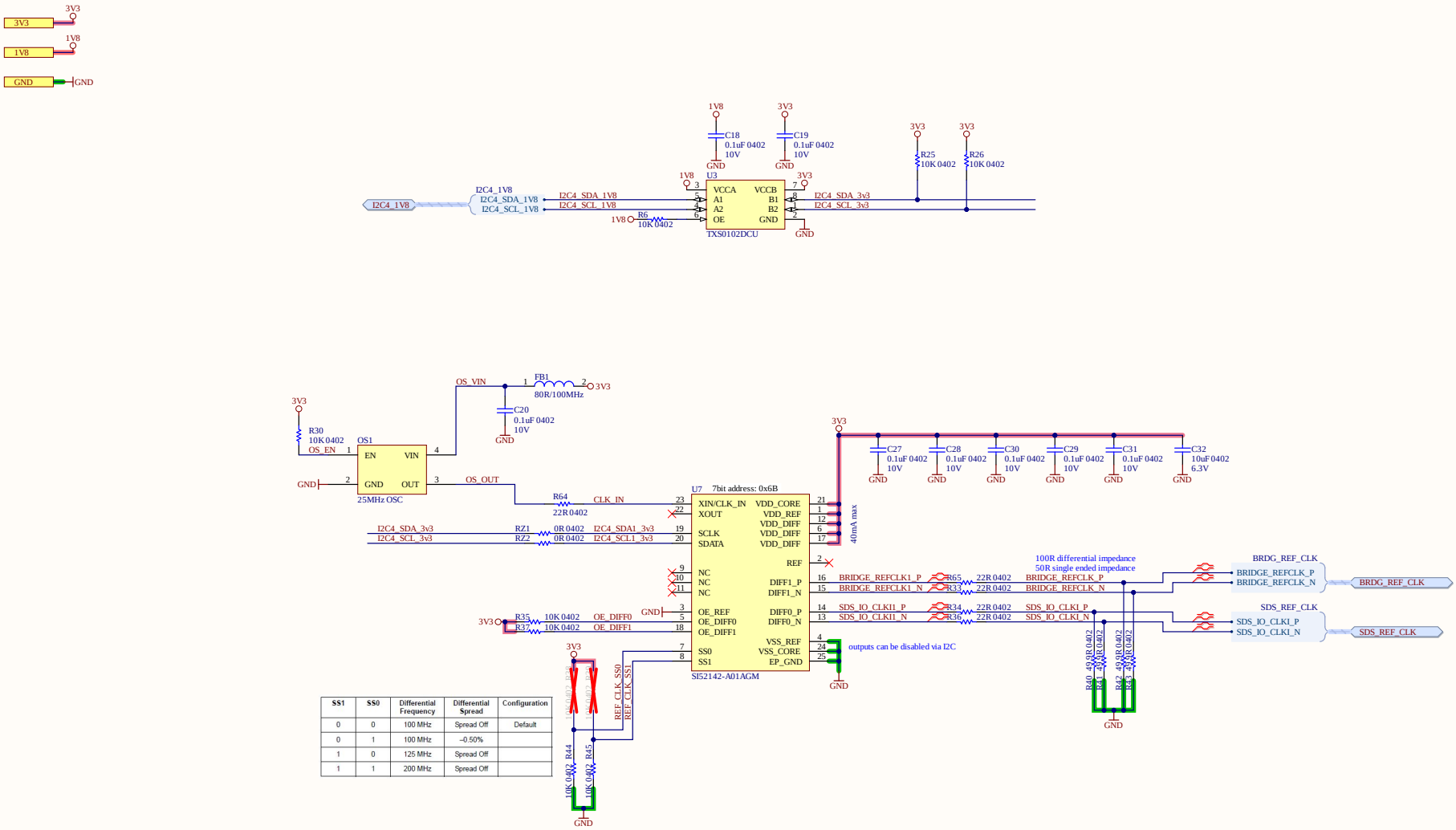
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:16 PM	Sheet 4 of 11	
Drawn by: Brian Weinstein / Sandesh Joshi			



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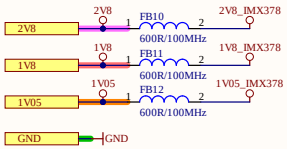
Date: 5/01/2021	Time: 10:26:16 PM	Sheet 4 of 12			
Drawn by: Brian Weinstein / Sandesh Joshi					

Place FBs and caps close to their associated camera connector.



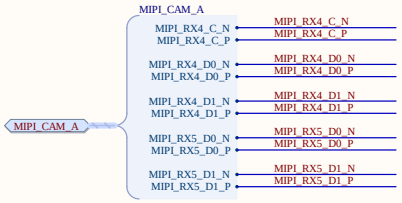
Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

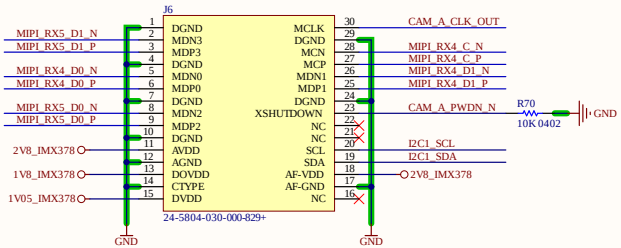
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

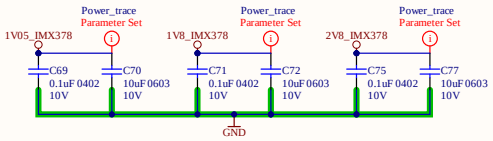
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

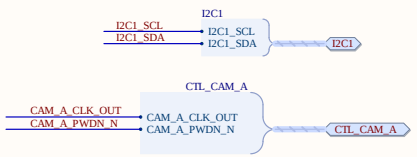


IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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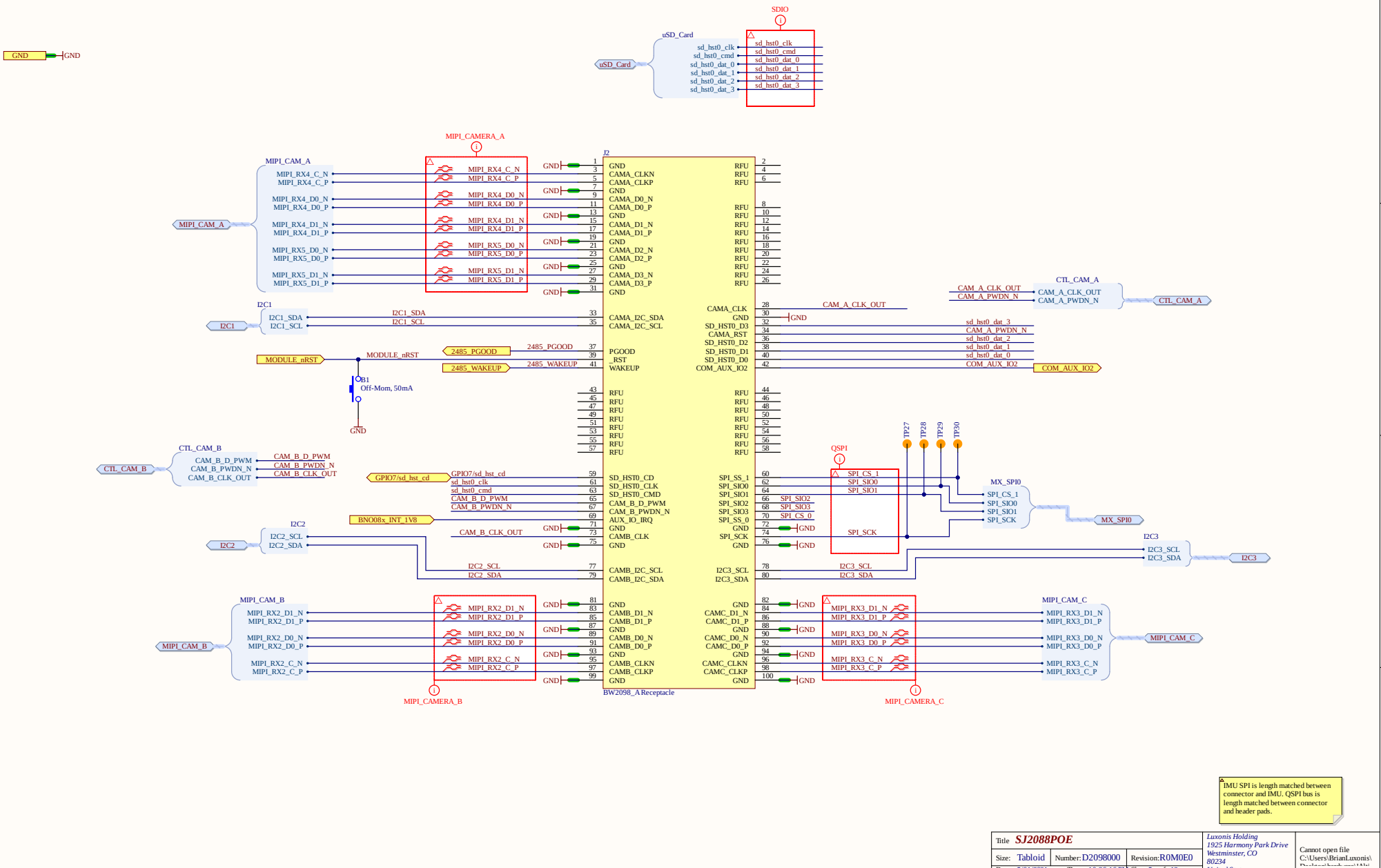
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:16 PM	Sheet 5 of 11	
Drawn by: Brian Weinstein / Sandesh Joshi			


GND
SDIO
uSD_Card
sd_hst0_clk
sd_hst0_cmd
sd_hst0_dat_0
sd_hst0_dat_1
sd_hst0_dat_2
sd_hst0_dat_3
MIPI_CAMERA_A
J2
MIPI_CAM_A
MIPI_RX4_C_N
MIPI_RX4_C_P
MIPI_RX4_D0_N
MIPI_RX4_D0_P
MIPI_RX4_D1_N
MIPI_RX4_D1_P
MIPI_RX5_D0_N
MIPI_RX5_D0_P
MIPI_RX5_D1_N
MIPI_RX5_D1_P
I2C1
I2C1_SDA
I2C1_SCL
MODULE_nRST
2485_PGOOD
2485_WAKEUP
B1
Off-Mom, 50mA
CTL_CAM_A
CAM_A_CLK_OUT
CAM_A_PWDN_N
COM_AUX_IO2
CTL_CAM_B
CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
GPIO7/sd_hst_cd
BNO08x_INT_1V8
I2C2
I2C2_SCL
I2C2_SDA
QSPI
SPI_CS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3
SPI_CS_0
SPI_SCK
MX_SPI0
I2C3
I2C3_SCL
I2C3_SDA
TP27
TP28
TP29
TP30
MIPI_CAM_B
MIPI_RX2_D1_N
MIPI_RX2_D1_P
MIPI_RX2_D0_N
MIPI_RX2_D0_P
MIPI_RX2_C_N
MIPI_RX2_C_P
MIPI_CAMERA_B
MIPI_CAM_C
MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P
MIPI_CAMERA_C
BW2098_A Receptacle
IMU SPI is length matched between connector and IMU. QSPI bus is length matched between connector and header pads.
Title SJ2088POE
Size: Tabloid
Number: D2098000
Revision: R0M0E0
Date: 5/01/2021
Time: 10:26:16 PM
Sheet 5 of 12
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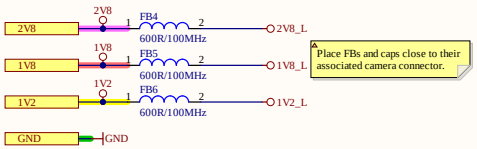
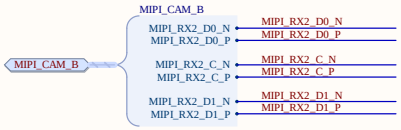
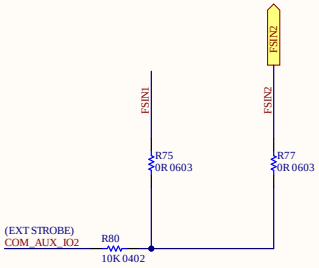


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	0V09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

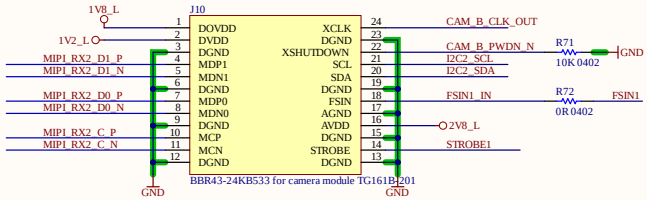
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

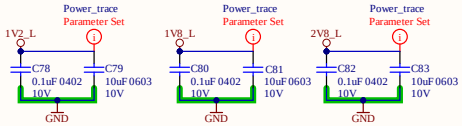


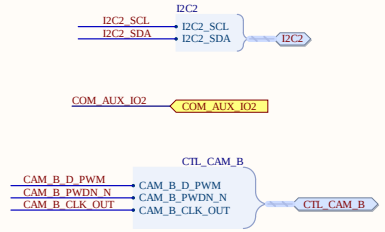


Camera timing Sync Option

Mark "LEFT" on PCB
Place so that is the module's left camera.







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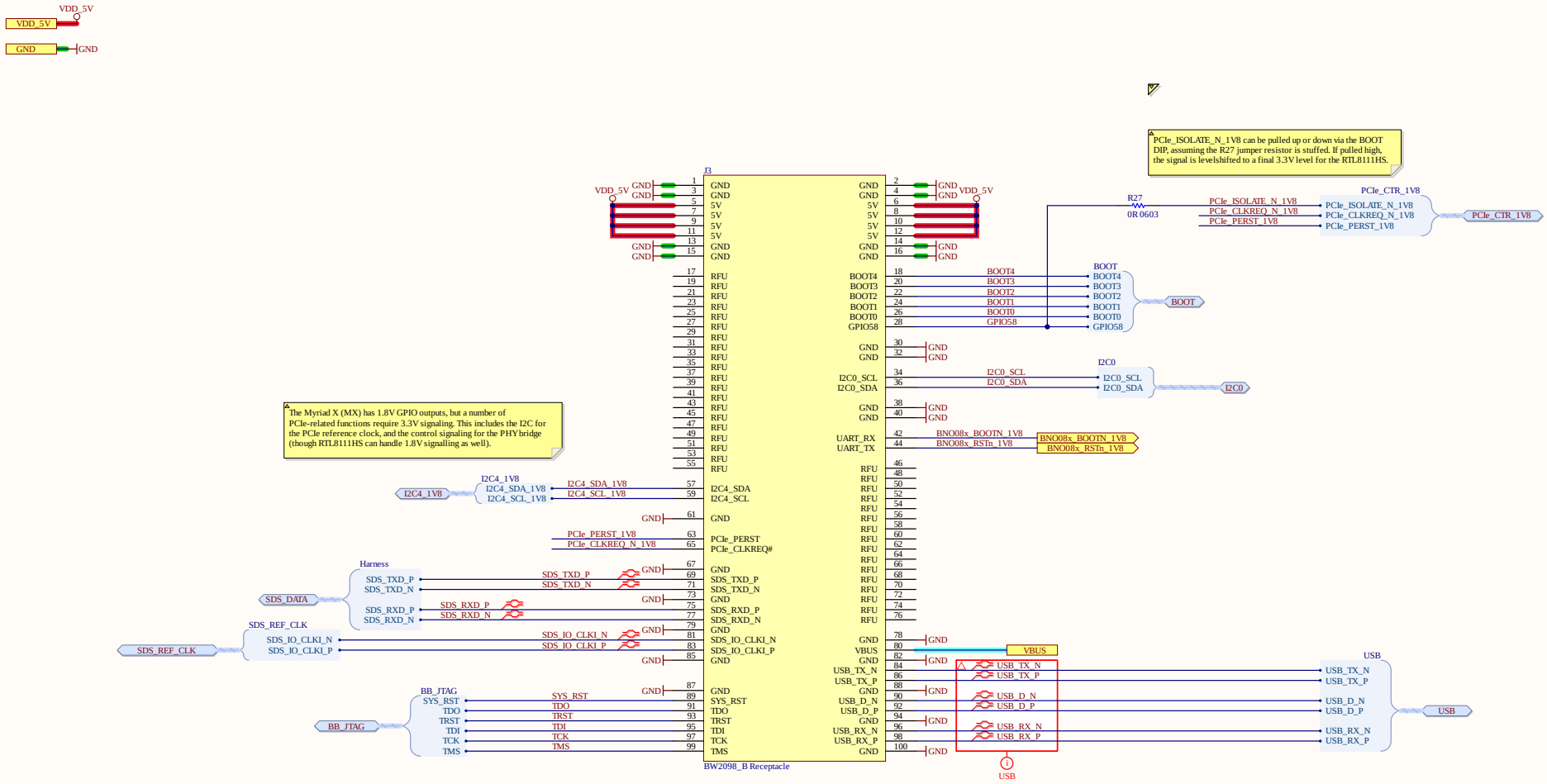

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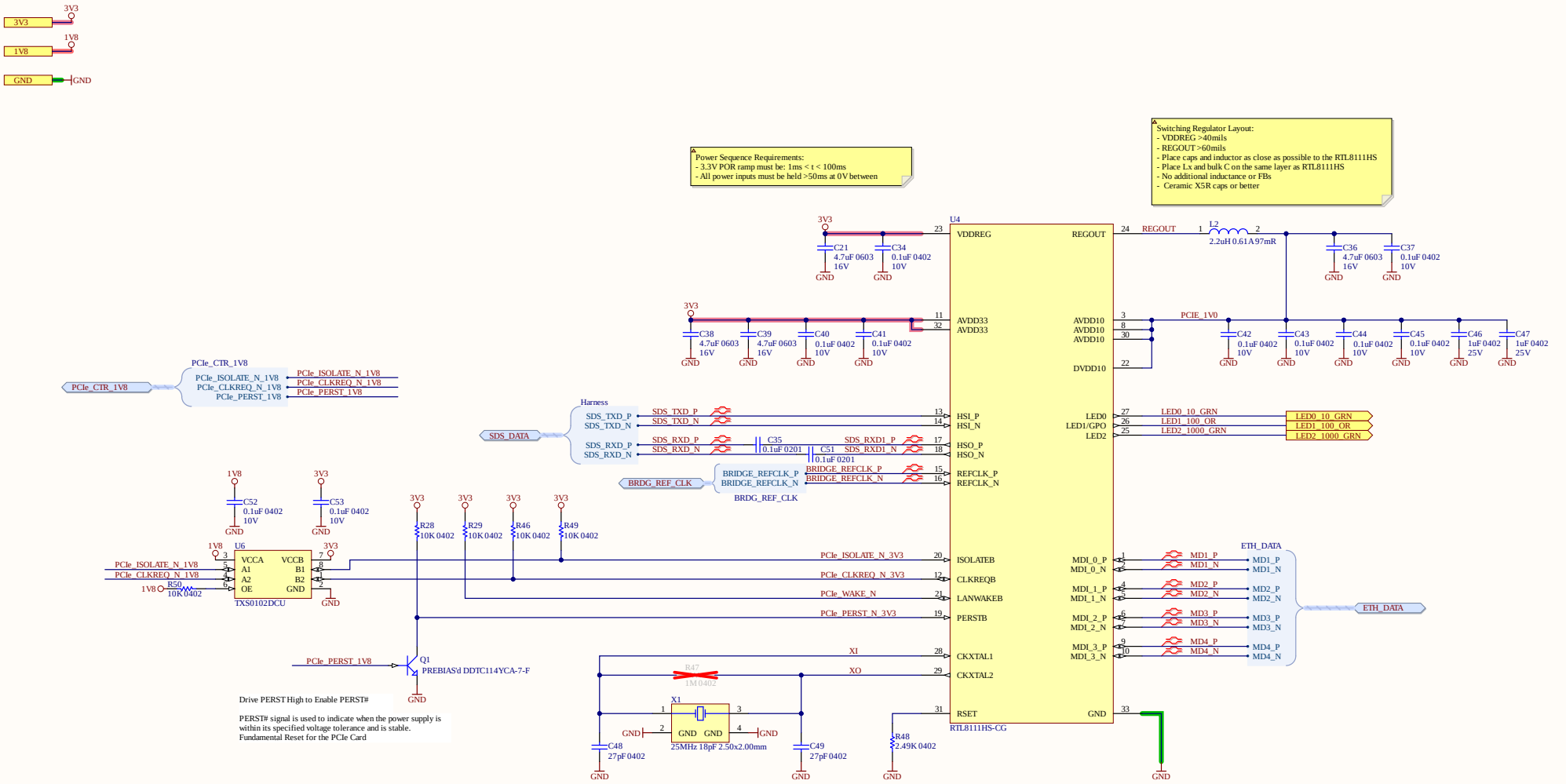
3V3
1V8
GND
Power Sequence Requirements:
- 3.3V POR ramp must be: 1ms < t < 100ms
- All power inputs must be held >50ms at 0V between
Switching Regulator Layout:
- VDDREG >40mils
- REGOUT >60mils
- Place caps and inductor as close as possible to the RTL8111HS
- Place Lx and bulk C on the same layer as RTL8111HS
- No additional inductance or FBs
- Ceramic X5R caps or better
U4
RTL8111HS-CG
VDDREG
REGOUT
AVDD33
AVDD10
DVDD10
HSI_P
HSI_N
HSO_P
HSO_N
REFCLK_P
REFCLK_N
LED0
LED1/GPO
LED2
ISOLATEB
CLKREQB
LANWAKEB
PERSTB
CKXTAL1
CKXTAL2
RSET
MDI_0_P
MDI_0_N
MDI_1_P
MDI_1_N
MDI_2_P
MDI_2_N
MDI_3_P
MDI_3_N
L2
2.2uH 0.61A 97mR
PCIE_1V0
Harness
SDS_DATA
SDS_TXD_P
SDS_TXD_N
SDS_RXD_P
SDS_RXD_N
C35
0.1uF 0201
C51
0.1uF 0201
BRDG_REF_CLK
BRIDGE_REFCLK_P
BRIDGE_REFCLK_N
LED0_10_GRN
LED1_100_OR
LED2_1000_GRN
ETH_DATA
PCIe_CTR_1V8
PCIe_ISOLATE_N_1V8
PCIe_CLKREQ_N_1V8
PCIe_PERST_1V8
PCIe_ISOLATE_N_3V3
PCIe_CLKREQ_N_3V3
PCIe_WAKE_N
PCIe_PERST_N_3V3
U6
TXS0102DCU
VCCA
VCCB
A1
B1
A2
B2
OE
GND
R50
10K 0402
R28
10K 0402
R29
10K 0402
R46
10K 0402
R49
10K 0402
C52
0.1uF 0402
10V
C53
0.1uF 0402
10V
Q1
PREBIAS'd DDTC114YCA-7-F
Drive PERST High to Enable PERST#
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
Fundamental Reset for the PCIe Card
R47
1M 0402
X1
25MHz 18pF 2.50x2.00mm
C48
27pF 0402
C49
27pF 0402
R48
2.49K 0402
C21
4.7uF 0603
16V
C34
0.1uF 0402
10V
C36
4.7uF 0603
16V
C37
0.1uF 0402
10V
C38
4.7uF 0603
16V
C39
4.7uF 0603
16V
C40
0.1uF 0402
10V
C41
0.1uF 0402
10V
C42
0.1uF 0402
10V
C43
0.1uF 0402
10V
C44
0.1uF 0402
10V
C45
0.1uF 0402
10V
C46
1uF 0402
25V
C47
1uF 0402
25V
Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.
Title SJ2088POE
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Number: D2098000
Revision: R0M0E0
Date: 5/01/2021
Time: 10:26:17 PM
Sheet 7 of 12
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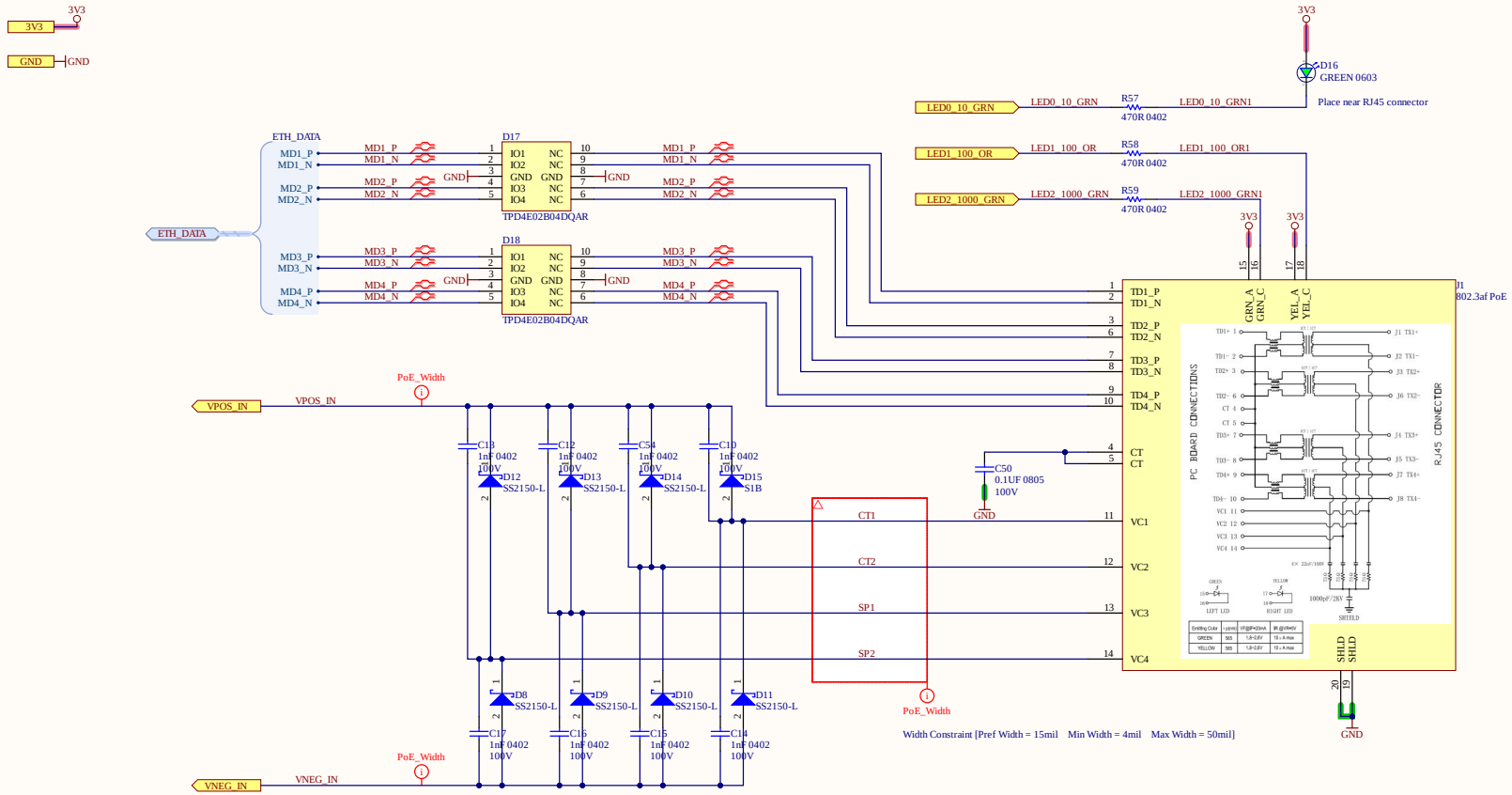

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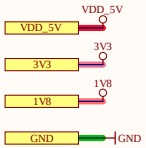
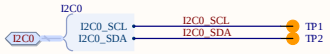
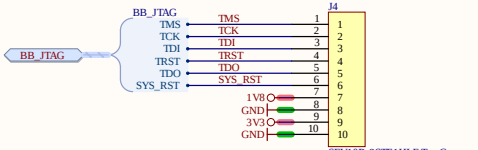
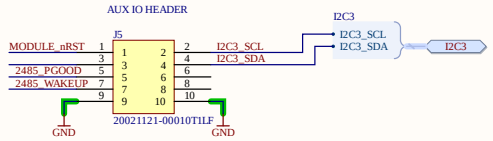




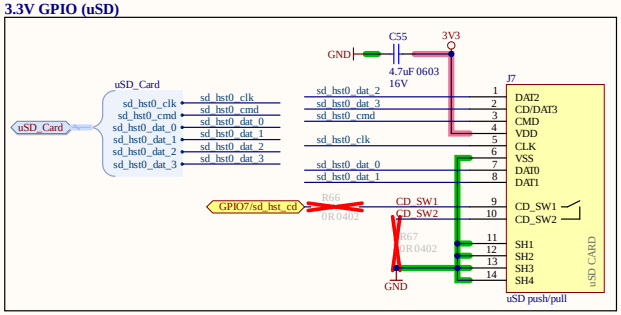
LED INDICATORS



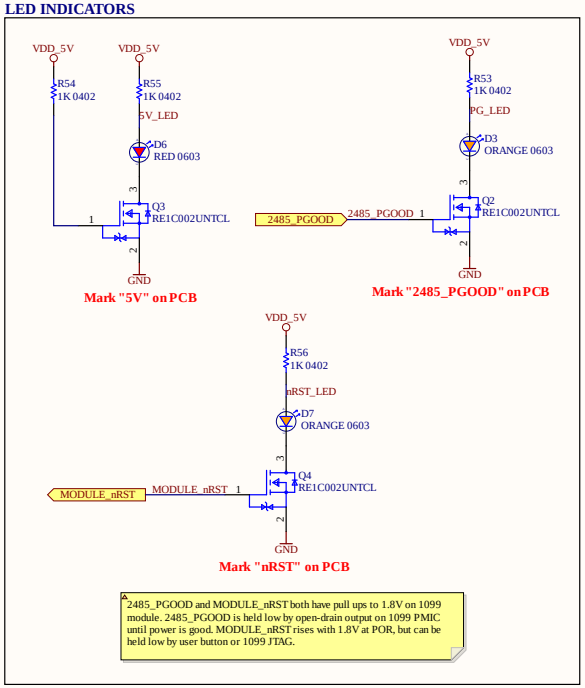
AUX IO HEADER



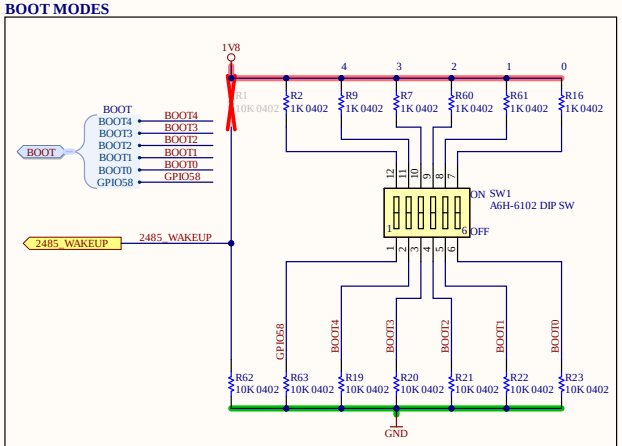
3.3V GPIO (uSD)



LED INDICATORS



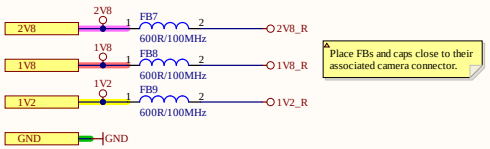
BOOT MODES



QUAD SPI

SPI HEADER --> Not used

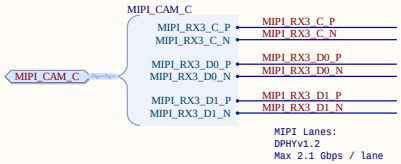
Title: SJ2088POE			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:17 PM	Sheet 9 of 12	
Drawn by: Brian Weinstein / Sandesh Joshi			



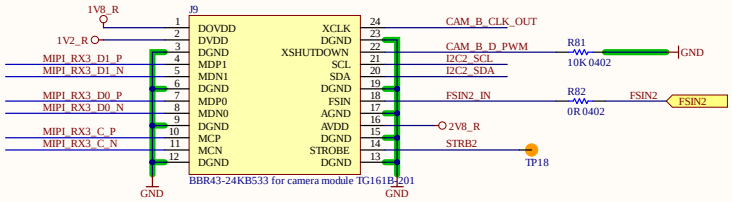
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

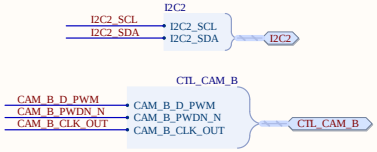
Supply Information

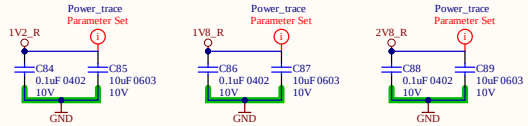
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



Mark "RIGHT" on PCB
Place so that this is the module's right camera.







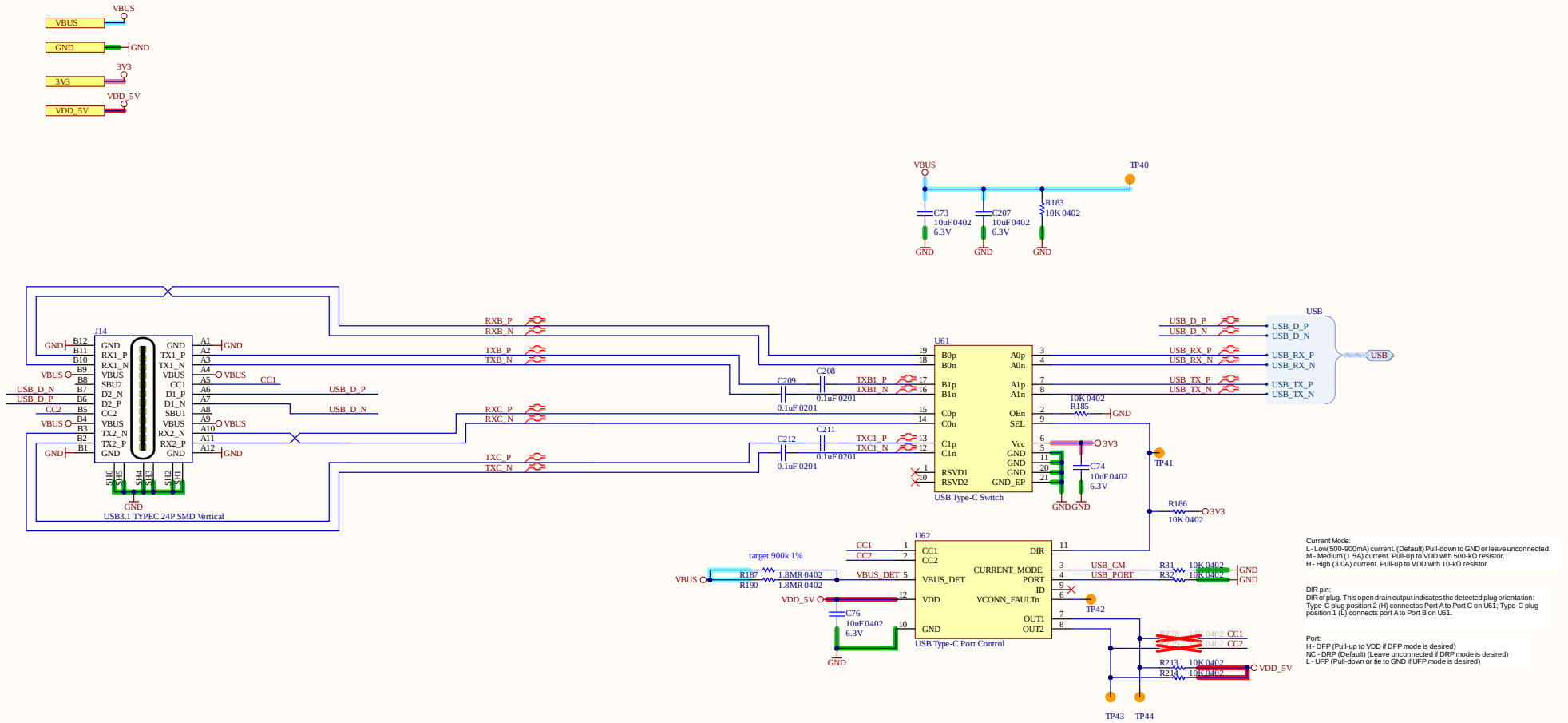
Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

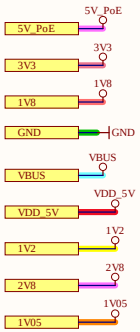
CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

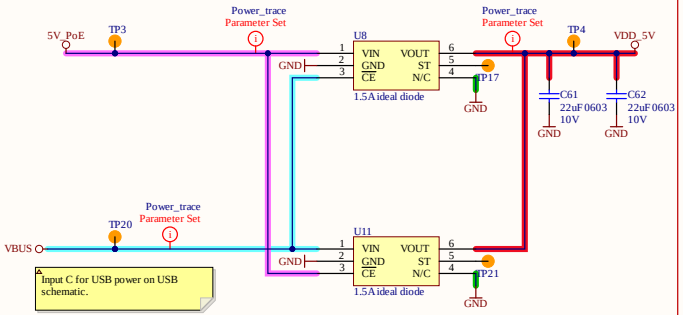
Title	SJ2088POE		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:17 PM	Sheet 10 of 11	
Drawn by: Brian Weinstein / Sandesh Joshi			



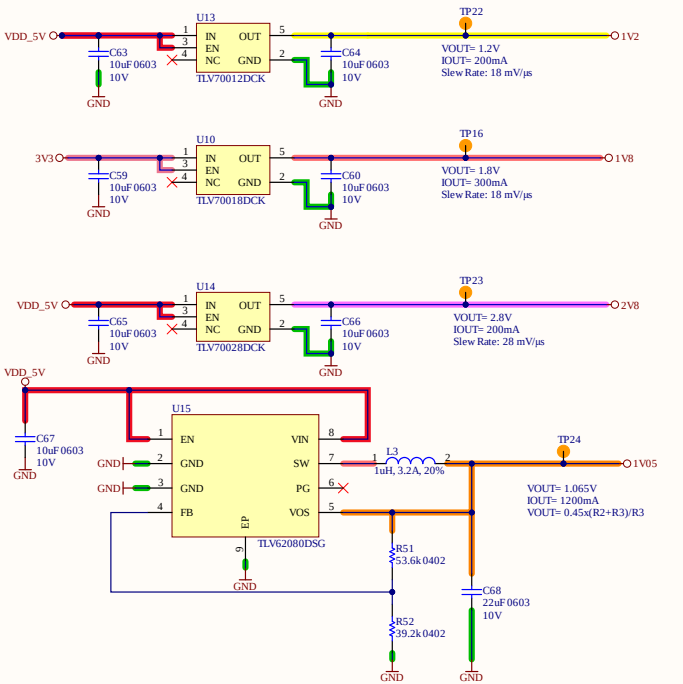
Title	SJ2088POE		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2098000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 5/01/2021	Time: 10:26:18 PM	Sheet 11 of 12	
Drawn by: Brian Weinstein / Sandesh Joshi			



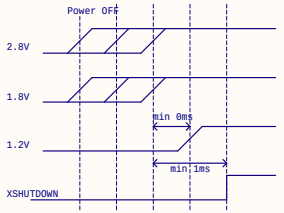
POWER INPUT



POWER SUPPLIES FOR CAMERA MODULES



OV9282 POWER REQUIREMENTS

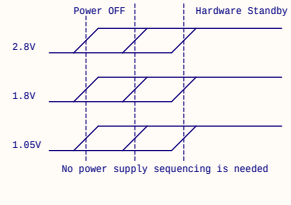


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

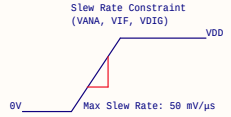
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

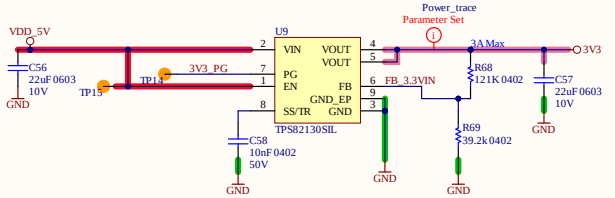
Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA



POWER SEQUENCING REQUIREMENTS:

The BW2099 module handles it's own power sequencing on-board. (TBC)

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.



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Date: 5/01/2021	Time: 10:26:18 PM	Sheet 12 of 12	
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