

A

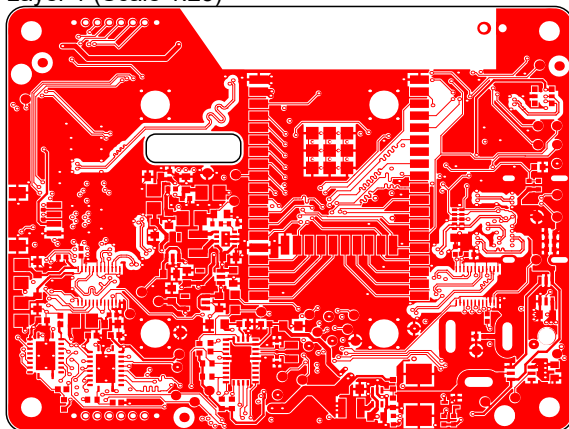
B

C

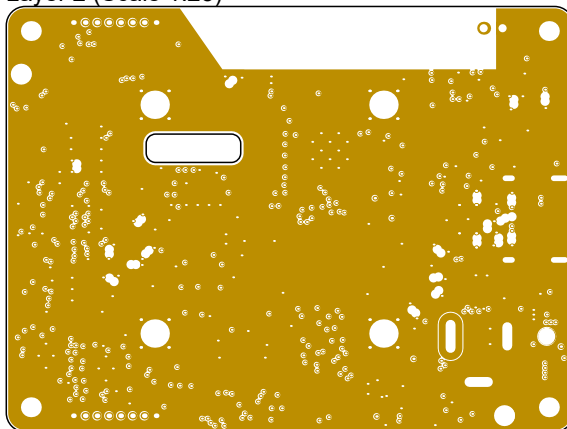
D

E

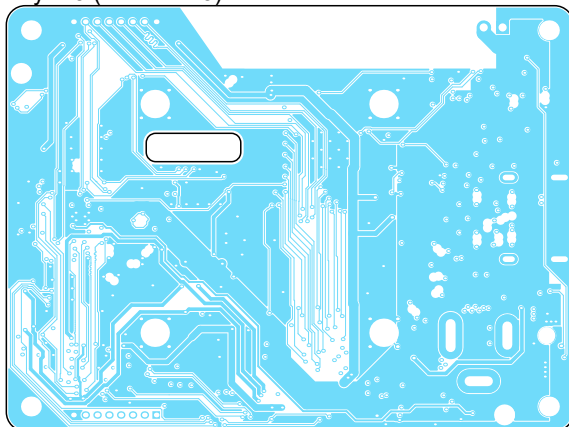
Layer 1 (Scale 1.25)



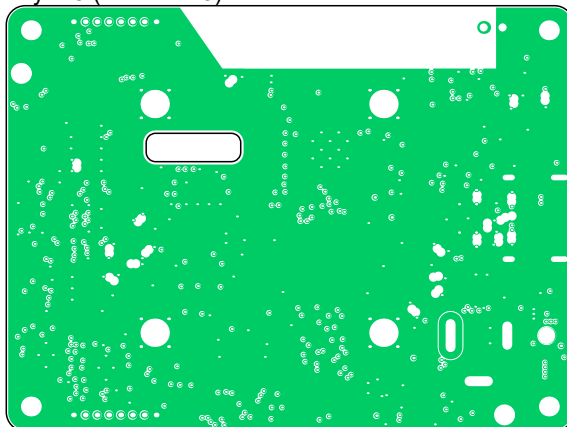
Layer 2 (Scale 1.25)



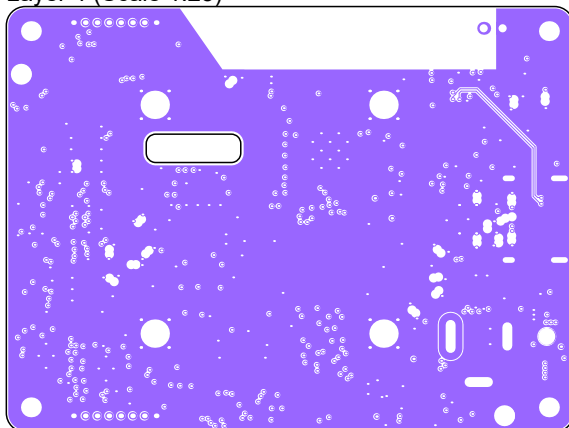
Layer 3 (Scale 1.25)



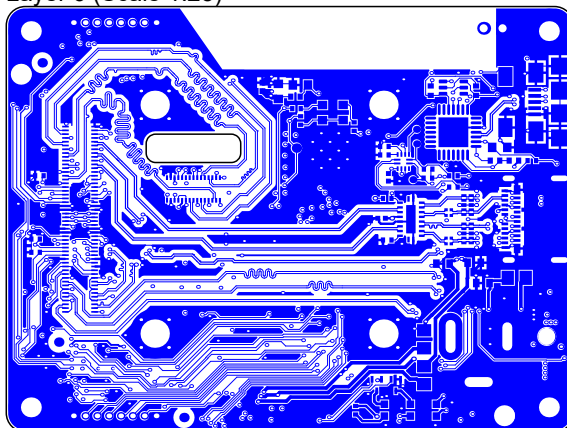
Layer 5 (Scale 1.25)



Layer 4 (Scale 1.25)



Layer 6 (Scale 1.25)

**FABRICATION NOTES:**

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

- * PCB has 6 copper layers
- * Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- * PCB thickness: please refer to the Layer Stack Legend
- * Min. trace width/clearance: 4/4mil
- * Min. hole drill/ring: 8mil/16mil
- * Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- * Silkscreen, non-conductive epoxy ink, color: white
- * Solder mask color: green
- * Remove silkscreen as needed to prevent ink on any exposed copper
- * Surface finish: ENIG
- * Hole dimensions are finished size, +/-3mil
- * Linear board dimension tolerance: +/-10mil
- * Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- * PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- * PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- * All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.
- * GM1 shall be used as PCB outline GKO can be ignored.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: **DM1092**

Number: DXXXX

Revision: R2M2
E2

Date: 02/08/2021

Sheet: 1 of 3

Drawn by: David Malovrh

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Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	479	8.00mil(0.203mm)	Plated	
▽	21	10.00mil(0.254mm)	Plated	
☆	16	19.69mil(0.500mm)	Plated	
⊗	4	23.62mil(0.600mm)	Plated	
⊕	2	33.86mil(0.860mm)	Plated	
✱	3	41.34mil(1.050mm)	Plated	
☆	1	70.87mil(1.800mm)	Non-Plated	
⊗	2	78.74mil(2.000mm)	Non-Plated	
○	4	82.68mil(2.100mm)	Plated	
◇	4	118.11mil(3.000mm)	Plated	
	536 Total			

Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.59mil(0.015mm)	Solder Mask	GTS		3,8
Layer 1	1.38mil(0.035mm)	Signal	GTL		
	3.94mil(0.100mm)	Dielectric			4,05
Layer 2	0.71mil(0.018mm)	Signal	G1		
	22.24mil(0.565mm)	Dielectric			4,5
Layer 3	0.71mil(0.018mm)	Signal	G2		
	5.00mil(0.127mm)	Dielectric			4,25
Layer 4	0.71mil(0.018mm)	Signal	G3		
	22.24mil(0.565mm)	Dielectric			4,5
Layer 5	0.71mil(0.018mm)	Signal	G4		
	3.94mil(0.100mm)	Dielectric			4,05
Layer 6	1.38mil(0.035mm)	Signal	GBL		
Bottom Mask	0.59mil(0.015mm)	Solder Mask	GBS		3,8
Bottom Overlay		Legend	GBO		
Total thickness: 64.14mil(1.629mm)					

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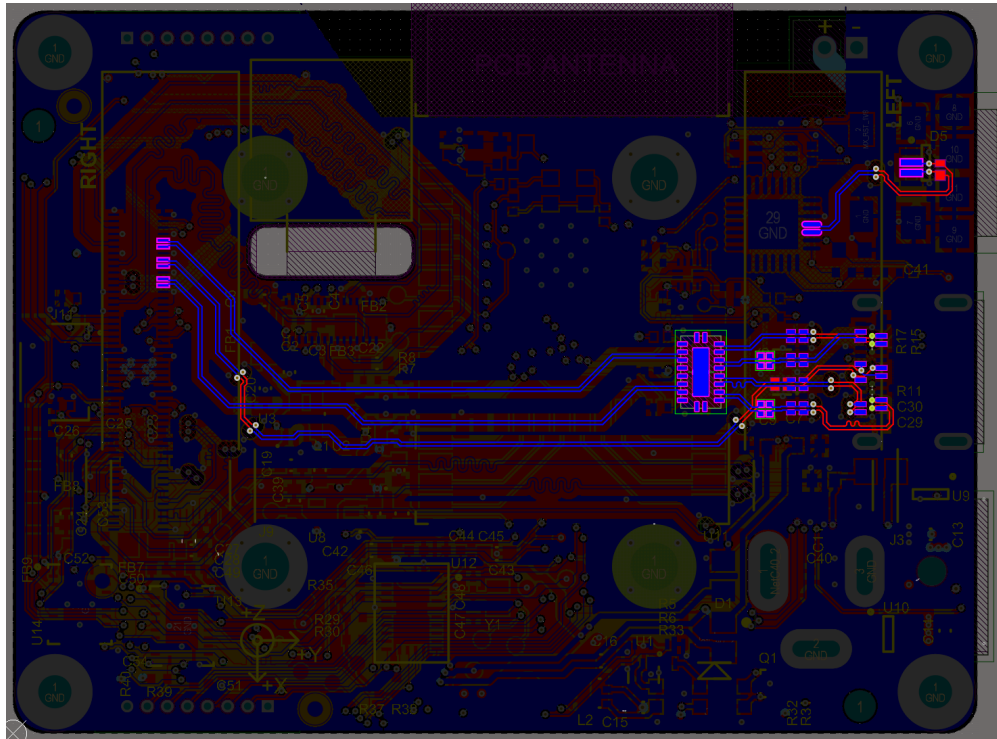
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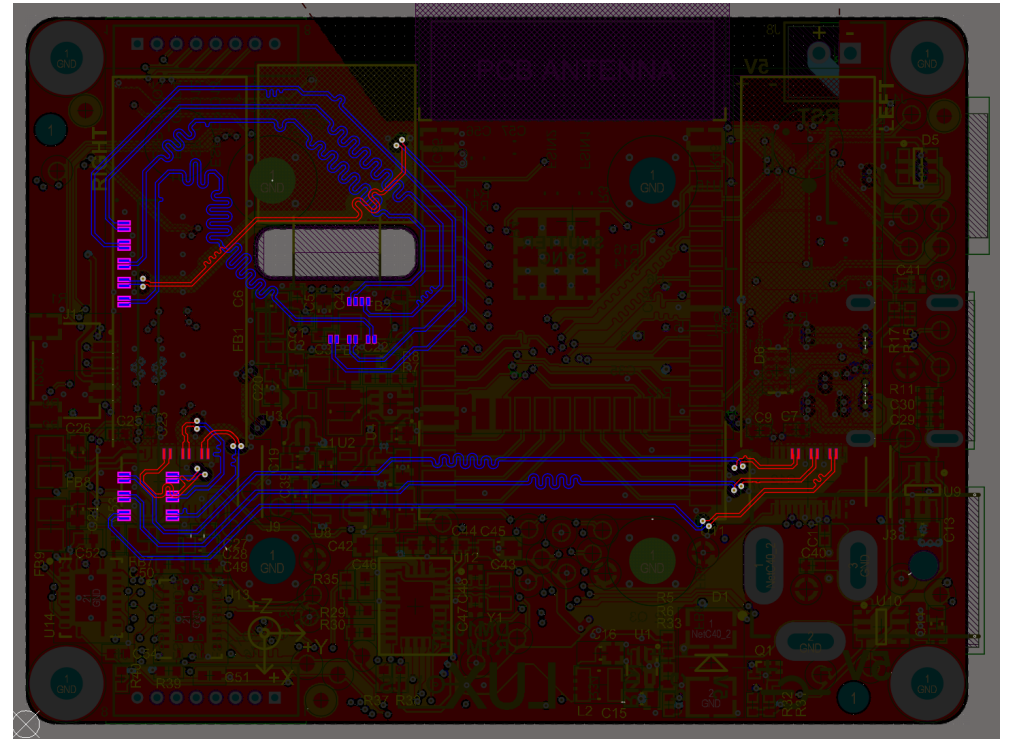
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90 OHM (+/-10%) DIFF PAIRS



100 OHM (+/-10%) DIFF PAIRS

Transmission Line Structure Table

Impedance Id	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
1	90	90.89	Layer 1	5.0mil(0.127mm)	4.4mil(0.113mm)	4.0mil(0.102mm)	Layer 2
2	100	101.50	Layer 1	4.0mil(0.102mm)	3.4mil(0.088mm)	4.5mil(0.114mm)	Layer 2
5	90	90.89	Layer 6	5.0mil(0.127mm)	4.4mil(0.113mm)	4.0mil(0.102mm)	Layer 5
6	100	101.50	Layer 6	4.0mil(0.102mm)	3.4mil(0.088mm)	4.5mil(0.114mm)	Layer 5

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