Project: ***BW1098FFC***
Current Revision: ***R1M1E1***

BW1098FFC Revision History:

Date	Revision	Reason for Change	Changes Implemented
11/29/2019	R0M0E0 -> R1M1E1	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Standardize FFC connector alignment with edge of board when connector is closed. 3) Existing design was not standardized on LuxonisMaster library format	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names, Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Moved each of the FFC connectors toward the board edge so that they are flush with edge when closed. 3) Updated schematic and component information to align with LuxonisMaster library system

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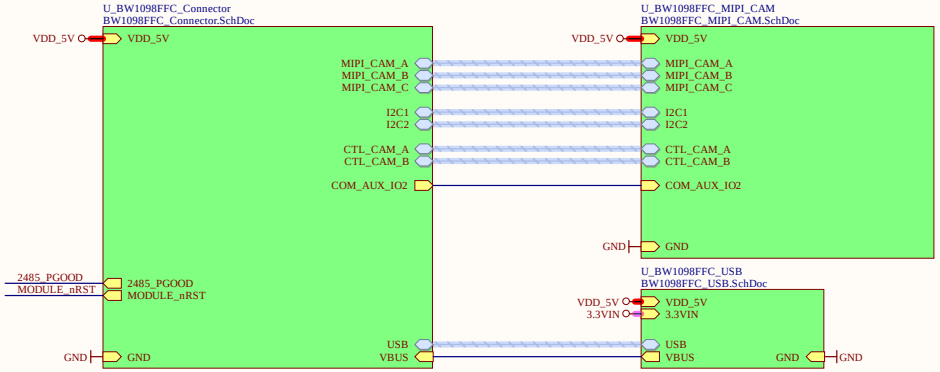
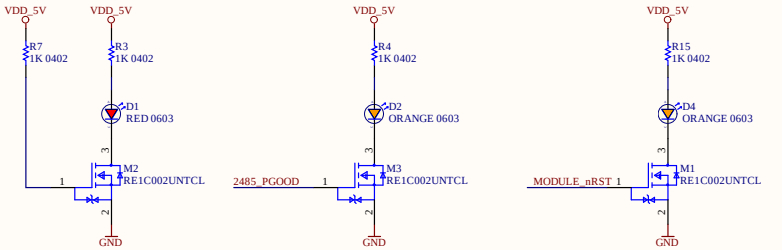
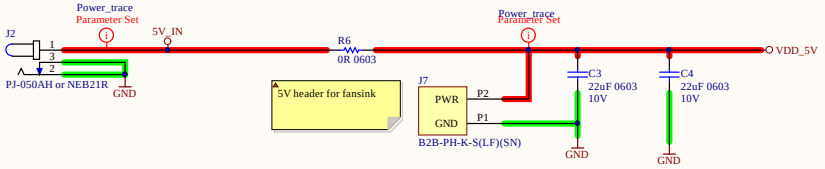
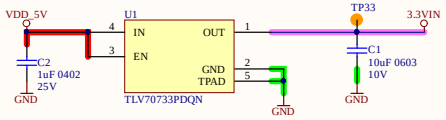
Drawn by: ***Brian Weinstein***			

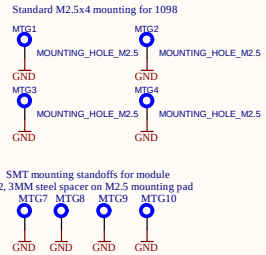




2485_PGOOD and MODULE_nRST both have pull ups to 1.8V on 1099 module. 2485_PGOOD is held low by open-drain output on 1099 PMIC until power is good. MODULE_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.







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VDD_5V

VBUS

GND

VDD_5V drawn by BW1099 can be up to 1A

VBUS on BW1099 is only sense input

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

Z1

BW1099 Placement Guide

Layout guide for BW1099

Code executed when PMS150C comes out of RST (PRST#), toggling RST_1 as required.

PMS150C powered by 5V so that it is the first in the power sequence to turn on.

Slow ramp on PRST# from RC during POR.

MODULE_nRST

D3 BAS16XV2T1G

RST_1

GND

U2 PMS150C-U06

nMR

R5 10K 0603

R1 10K 0603

C5 4.7uF 0603 16V

Parameter Set

MIPI_CAM_A

J1

MIPI_RX4_C_N
MIPI_RX4_C_P
MIPI_RX4_D0_N
MIPI_RX4_D0_P
MIPI_RX4_D1_N
MIPI_RX4_D1_P
MIPI_RX5_D0_N
MIPI_RX5_D0_P
MIPI_RX5_D1_N
MIPI_RX5_D1_P

GND
CAMA_CLKN
CAMA_CLKP
CAMA_D0_N
CAMA_D0_P
CAMA_D1_N
CAMA_D1_P
CAMA_D2_N
CAMA_D2_P
CAMA_D3_N
CAMA_D3_P

UART_RX
UART_TX

2485_UART_RX
2485_UART_TX

USB_RX_P
USB_RX_N
USB_D_P
USB_D_N
USB_TX_P
USB_TX_N

USBD2_P
USBD2_N

USB

I2C1

I2C1_SDA
I2C1_SCL

CAMA_I2C_SDA
CAMA_I2C_SCL

CAMA_CLK
CAM_A_CLK_OUT
CAM_A_PWDN_N
SD_HST0_D3
SD_HST0_D2
SD_HST0_D1
SD_HST0_D0
COM_AUX_IO2

CTL_CAM_A

2485_PGOOD
MODULE_nRST
2485_WAKEUP

PGOOD
_RST
WAKEUP

TP2

1099 only accepts 1.8V input on GPIOs.

B1
Off-Mom, 50mA

VDD_5V

VBUS

TP6

SPI
Parameter Set

SDIO
Parameter Set

SD_HST0_CD
SD_HST0_CLK
SD_HST0_CMD

SPI_SS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3
SPI_SS_0
SPI_SCK

CTL_CAM_B

CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
AUX_IO_IRQ

I2C2

I2C2_SCL
I2C2_SDA

I2C3_SCL
I2C3_SDA

MIPI_RX2_D1_N
MIPI_RX2_D1_P
MIPI_RX2_D0_N
MIPI_RX2_D0_P
MIPI_RX2_C_N
MIPI_RX2_C_P

CAMB_D1_N
CAMB_D1_P
CAMB_D0_N
CAMB_D0_P
CAMB_CLKN
CAMB_CLKP
CAMB_I2C_SCL
CAMB_I2C_SDA

MIPI_CAM_B

Parameter Set
MIPI_CAM_B

MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P

CAMC_D1_N
CAMC_D1_P
CAMC_D0_N
CAMC_D0_P
CAMC_CLKN
CAMC_CLKP

MIPI_CAM_C

Parameter Set
MIPI_CAM_C

DF40HC(3.0)-100DS-0.4V_BW1099G2 Receptacle
3mm

AUX IO HEADER

J4

MODULE_nRST
AUX_IO_IRQ
2485_PGOOD
2485_WAKEUP
I2C3_SCL
I2C3_SDA
2485_UART_RX
2485_UART_TX

20021121-00010T1LF

SPI HEADER

J5

SPI_SCK
SPI_SS_0
SPI_SS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3

20021121-00010T1LF

3.3V SD HEADER

J3

SD_HST0_CLK
SD_HST0_CMD
SD_HST0_CD
SD_HST0_D0
SD_HST0_D1
SD_HST0_D2
SD_HST0_D3

20021121-00010T1LF

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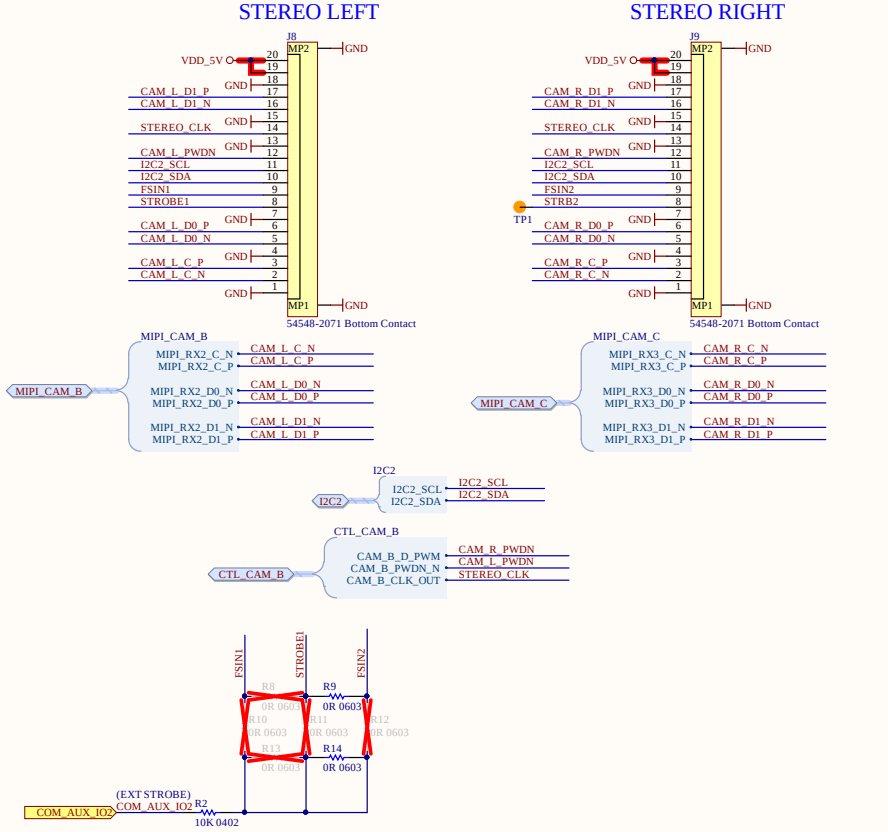
LUXonis

STEREO CAMERA PAIR



Jumper configuration for FSIN and STROBE pins

PCB NOTE: Add below diagram to the PCB

Supported Modes of Operation

- NO SYNC
- NORMAL
- TIMING MASTER
- TIMING SLAVE

This header is used for configuring the STROBE signal direction between the camera boards by using jumpers. A strobe signal may drive FSIN signal for waking up a sensor from its low power mode. See the "Supported Modes of Operation" note for supported jumper settings.

- "NO SYNC" is the mode in which none of the camera modules is excited by any strobe signal.

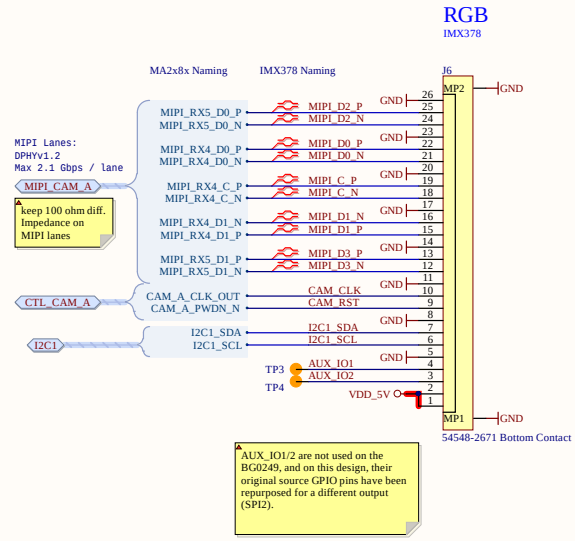
- "NORMAL" mode means STROBE mechanism works only among the stereo cameras themselves. In this mode, CAM1 strobe is connected to the CAM2 FSIN input.

- "TIMING MASTER" mode means CAM1 STROBE signal drives the EXT_STROBE signal as well as the CAM2 FSIN input. EXT_STROBE signal circulates among the other camera ports so that one camera module can manage the timing of all cameras within the system.

- "TIMING SLAVE" mode uses external strobe signal which is driven externally by another camera. In this mode, CAM1 and CAM2 are excited by the EXT_STROBE signal.

Note that, at most only one camera can be in the "TIMING MASTER" mode at a time. STROBE generation and FSIN reception should be configured via software.

RGB CAMERA



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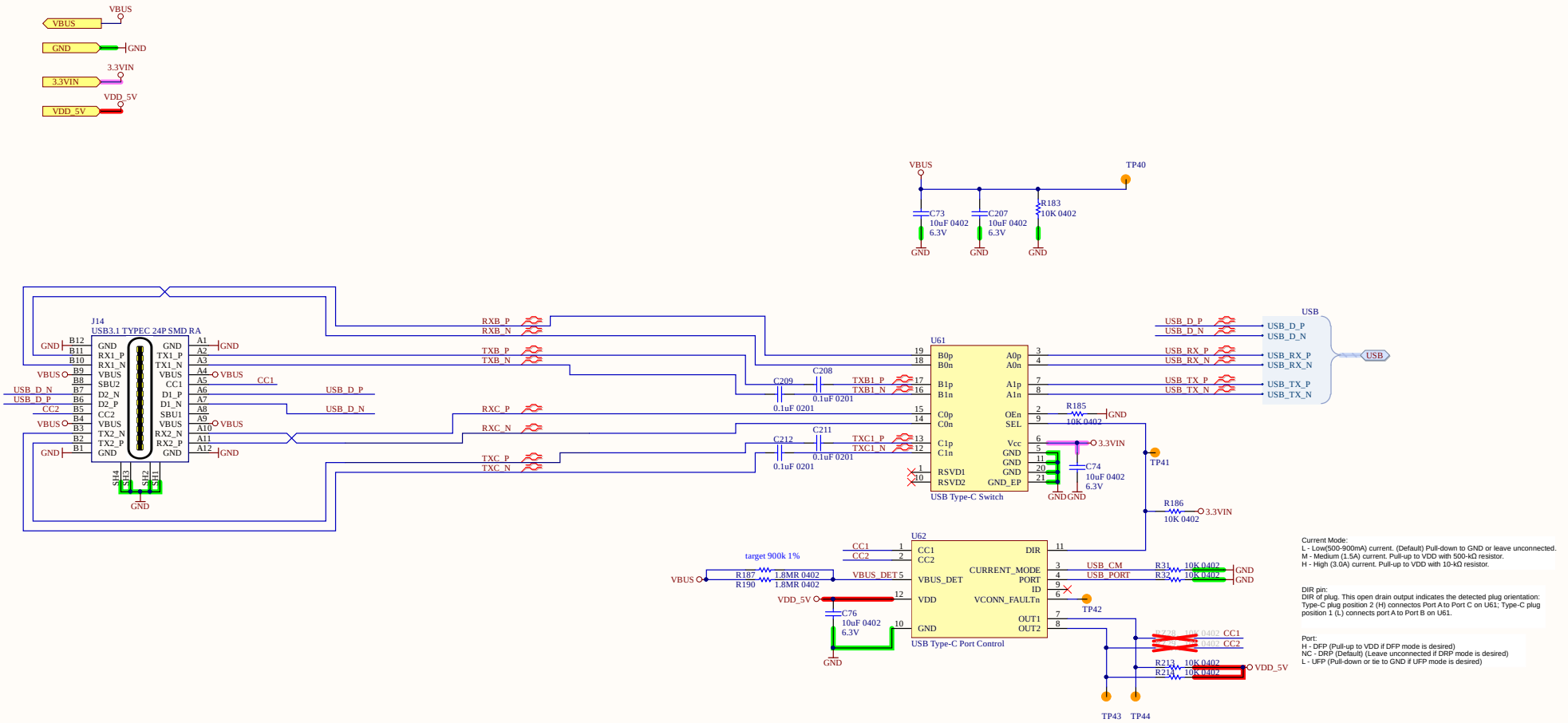

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