Project: ***DM1097***
Current Revision: ***R0M0E0***

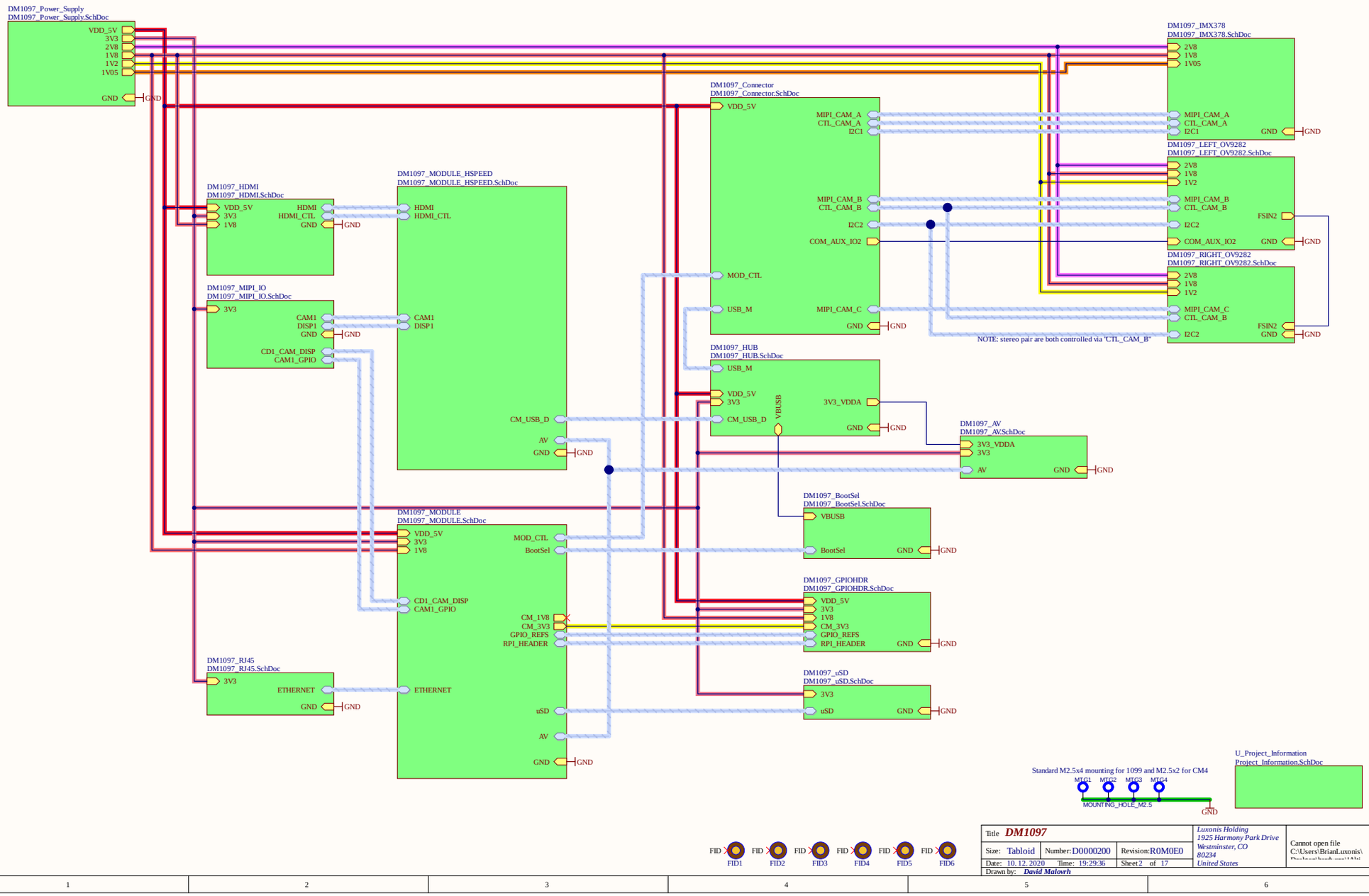
BW1097 Revision History:

Date	Revision	Reason for Change	Changes Implemented
11/29/2019	R1M1E2 -> R2M2E3	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Header jumpers are unnecesary and expensive, and can be repalced with a simpler solution 3) Existing design was not standardized on LuxonisMaster library format 4) Series input power resistor is a sense resistor, but should be 0 ohm 5) The OV9282 LDOs have unncessary components compared to the most recent baseboards 6) Depopped R26 had no set component value. 7) HDMI connector footprint was found to be slightly crooked 8) PGOOD LED driver did not match other boards 9) DMG1012 FETs were automotive qualified, changed to non-automotive for entry into LuxonisMaster 10) Passive component equivalent part substitions as library was built up	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names, Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Removed header jumpers and exchanged with resistor jumper networks 3) Updated schematic and component information to align with LuxonisMaster library system. 4) Changed input series resistor to 0603 0ohm to match 1098OBC, 1098FFC, and 1094. 5) Removed RC circuit on OV9282 LDOs to match 1098OBC 6) Added 47K as default, but R26 remains depopulated 7) Corrected HDMI footprint to match recommended PCB layout from Wurth 685119134923 8) Changed transistor on PGOOD LED to be RE1C002UNTCL, to match other boards (Q5) 9) Changed from DMG1012TG-7 to DMG1012T7 (Q1, Q2, Q3, Q4, Q6) 10) Many passive components did not exist in LuxonisMaster, so in some cases, equivalent from a different manufacturer are used. For 332R and 100K resistors, all were standardized to 0402, rather than a mix of sizes.

DM1097 Revision History:

	R0M0E0 -> R0M0E1	.	
	R0M0E1 -> R1M1E2		
	R1M1E2 -> R2M2E3		

Title ***DM1097***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 10. 12. 2020 Time: 19:29:35	Sheet 1 of 17		
Drawn by: ***David Malovrh***			


DM1097_Power_Supply
DM1097_Power_Supply.SchDoc
VDD_5V
3V3
2V8
1V8
1V2
1V05
GND
DM1097_IMX378
DM1097_IMX378.SchDoc
2V8
1V8
1V05
MIPI_CAM_A
CTL_CAM_A
I2C1
GND
DM1097_Connector
DM1097_Connector.SchDoc
VDD_5V
MIPI_CAM_A
CTL_CAM_A
I2C1
DM1097_LEFT_OV9282
DM1097_LEFT_OV9282.SchDoc
2V8
1V8
1V2
MIPI_CAM_B
CTL_CAM_B
FSIN2
I2C2
COM_AUX_IO2
DM1097_RIGHT_OV9282
DM1097_RIGHT_OV9282.SchDoc
MOD_CTL
USB_M
MIPI_CAM_C
NOTE: stereo pair are both controlled via "CTL_CAM_B"
DM1097_HDMI
DM1097_HDMI.SchDoc
HDMI
HDMI_CTL
DM1097_MODULE_HSPEED
DM1097_MODULE_HSPEED.SchDoc
DM1097_MIPI_IO
DM1097_MIPI_IO.SchDoc
CAM1
DISP1
CD1_CAM_DISP
CAM1_GPIO
DM1097_HUB
DM1097_HUB.SchDoc
VBUSB
3V3_VDDA
CM_USB_D
AV
DM1097_AV
DM1097_AV.SchDoc
DM1097_BootSel
DM1097_BootSel.SchDoc
BootSel
DM1097_MODULE
DM1097_MODULE.SchDoc
DM1097_GPIOHDR
DM1097_GPIOHDR.SchDoc
CM_1V8
CM_3V3
GPIO_REFS
RPI_HEADER
DM1097_RJ45
DM1097_RJ45.SchDoc
ETHERNET
DM1097_uSD
DM1097_uSD.SchDoc
uSD
Standard M2.5x4 mounting for 1099 and M2.5x2 for CM4
MTG1
MTG2
MTG3
MTG4
MOUNTING_HOLE_M2.5
U_Project_Information
Project_Information.SchDoc
FID1
FID2
FID3
FID4
FID5
FID6
Title DM1097
Size: Tabloid
Number: D0000200
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Date: 10.12.2020
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Drawn by: David Malowrh
Luxonis Holding
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80234
United States
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SMT mounting standoffs for module and for CM4

MTG7 MTG8 MTG9 MTG10 MTG5 MTG6

M2, 3MM steel spacer on M2.5 mounting pad

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

Code executed when PMS150C comes out of RST (PRST#), toggling RST_1 as required.

PMS150C powered by 5V so that it is the first in the power sequence to turn on.

Slow ramp on PRST# from RC during POR.

1099 only accepts 1.8V input on GPIOs. Must protect these lines for the 3.3V CM3 GPIO case.

MODULE_nRST is pulled to 1.8V on BW1099.

Note on silk that this button only resets the BW1099.

GPIO33/MRST toggled high will put the 1099 module into RST.

Default GPIO33 is low (internal PD).

J1 — DF40HC(3.0)-100DS-0.4V_BW1099G2 Receptacle 3mm

1	GND	GND	2
3	CAMA_CLKN	UART_RX	4
5	CAMA_CLKP	UART_TX	6
7	GND		
9	CAMA_D0_N		
11	CAMA_D0_P	GND	8
13	GND	USB_RX_P	10
15	CAMA_D1_N	USB_RX_N	12
17	CAMA_D1_P	GND	14
19	GND	USB_D_P	16
21	CAMA_D2_N	USB_D_N	18
23	CAMA_D2_P	GND	20
25	GND	USB_TX_P	22
27	CAMA_D3_N	USB_TX_N	24
29	CAMA_D3_P	GND	26
31	GND		
33	CAMA_I2C_SDA	CAMA_CLK	28
35	CAMA_I2C_SCL	GND	30
37	PGOOD	SD_HST0_D3	32
39	_RST	CAMA_RST	34
41	WAKEUP	SD_HST0_D2	36
43	GND	SD_HST0_D1	38
45	GND	SD_HST0_D0	40
47	5V	COM_AUX_IO2	42
49	5V	GND	44
51	5V	GND	46
53	5V	5V	48
55	GND	5V	50
57	GND	5V	52
59	SD_HST0_CD	5V	54
61	SD_HST0_CLK	GND	56
63	SD_HST0_CMD	GND	58
65	CAM_B_D_PWM	SD_HST0_CD	60
67	CAM_B_PWDN_N	SPI_SS_1	62
69	AUX_IO_IRQ	SPI_SIO0	64
71	GND	SPI_SIO1	66
73	CAMB_CLK	SPI_SIO2	68
75	GND	SPI_SIO3	70
77	CAMB_I2C_SCL	SPI_SS_0	72
79	CAMB_I2C_SDA	SPI_SCK	74
81	GND	GND	76
83	CAMB_D1_N	I2C3_SCL	78
85	CAMB_D1_P	I2C3_SDA	80
87	GND	GND	82
89	CAMB_D0_N	CAMC_D1_N	84
91	CAMB_D0_P	CAMC_D1_P	86
93	GND	GND	88
95	CAMB_CLKN	CAMC_D0_N	90
97	CAMB_CLKP	CAMC_D0_P	92
99	GND	GND	94
		CAMC_CLKN	96
		CAMC_CLKP	98
		GND	100

AUX IO HEADER — J5 — 20021121-00010T1LF

MODULE_nRST	1	2	I2C3_SCL
AUX_IO_IRQ	3	4	I2C3_SDA
2485_PGOOD	5	6	UART_RX
2485_WAKEUP	7	8	UART_TX
GND	9	10	GND

SPI HEADER — J7 — 20021121-00010T1LF

SPI_SCK	1	2	SPI_SIO0
SPI_SS_0	3	4	SPI_SIO1
SPI_SS_1	5	6	SPI_SIO2
GND	7	8	SPI_SIO3
GND	9	10	GND

3.3V SD HEADER — J8 — 20021121-00010T1LF

SD_HST0_CLK	1	2	SD_HST0_D0
SD_HST0_CMD	3	4	SD_HST0_D1
SD_HST0_CD	5	6	SD_HST0_D2
GND	7	8	SD_HST0_D3
GND	9	10	GND

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Size: Tabloid	Number: D0000200	Revision: R0M0E0	
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Drawn by: David Malovrh			

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United States

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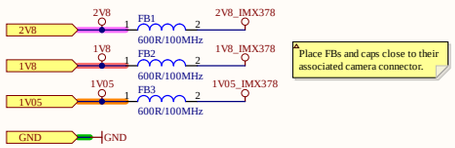


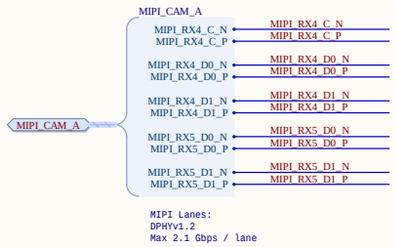
Place FBs and caps close to their associated camera connector.

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

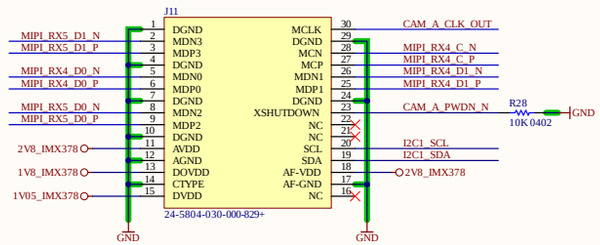
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

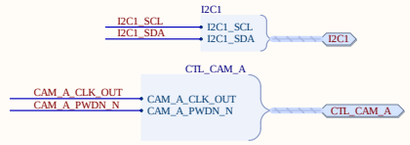
IMX378 MODULE CONNECTOR

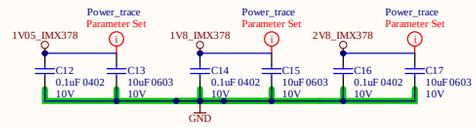
MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz



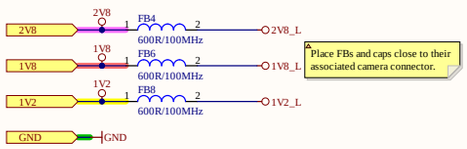
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane







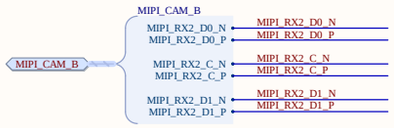
Title	***DM1097***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D0000200	Revision: R0M0E0		Cannot open file C:\Users\BrianLuxonis\
Date: 10. 12. 2020	Time: 19:29:36	Sheet 4 of 17		
Drawn by: ***David Malovrh***				

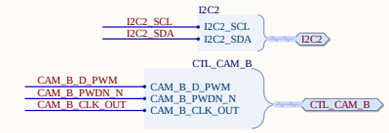


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

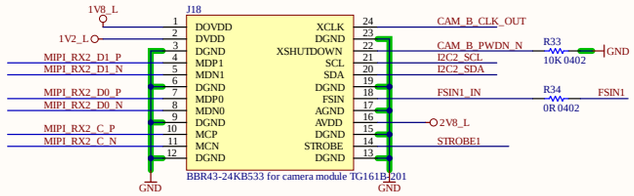
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

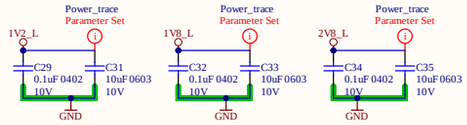


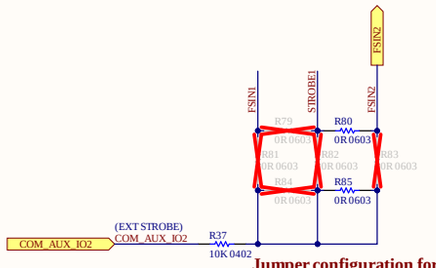


Mark "LEFT" on PCB

Place so that is the module's left camera.



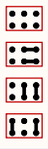




Jumper configuration for FSIN and STROBE pins

PCB NOTE: Add below diagram to the PCB

Supported Modes of Operation



NO SYNC

NORMAL

TIMING MASTER

TIMING SLAVE

This header is used for configuring the STROBE signal direction between the camera boards by using jumpers. A strobe signal may drive FSIN signal for waking up a sensor from its low power mode. See the "Supported Modes of Operation" note for supported jumper settings.

- "NO SYNC" is the mode in which none of the camera modules is excited by any strobe signal.

- "NORMAL" mode means STROBE mechanism works only among the stereo cameras themselves. In this mode, CAM1 strobe is connected to the CAM2 FSIN input.

- "TIMING MASTER" mode means CAM1 STROBE signal drives the EXT_STROBE signal as well as the CAM2 FSIN input. EXT_STROBE signal circulates among the other camera ports so that one camera module can manage the timing of all cameras within the system.

- "TIMING SLAVE" mode uses external strobe signal which is driven externally by another camera. In this mode, CAM1 and CAM2 are excited by the EXT_STROBE signal.

Note that, at most only one camera can be in the "TIMING MASTER" mode at a time. STROBE generation and FSIN reception should be configured via software.

Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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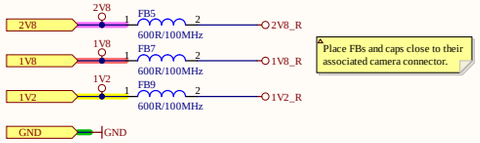
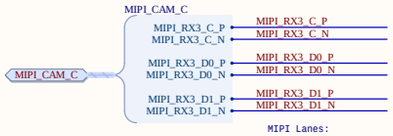


Place FBs and caps close to their associated camera connector.

MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

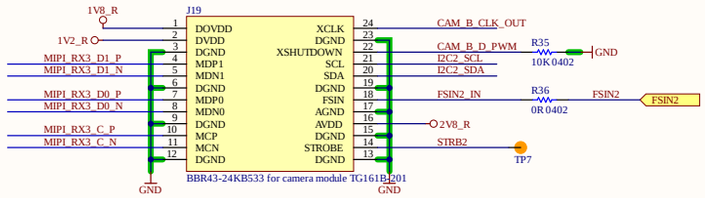
Supply Information

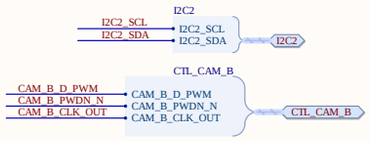
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

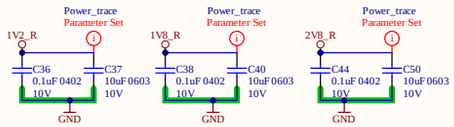


MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

Mark "RIGHT" on PCB
Place so that is the module's right camera.







Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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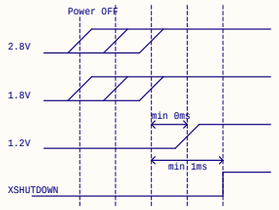
OV9282 POWER REQUIREMENTS

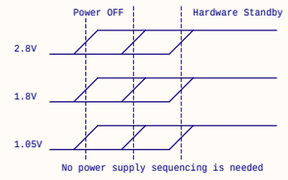


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

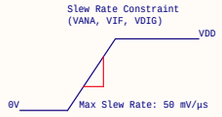
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA



POWER SEQUENCING REQUIREMENTS:

The CM3 reqeuests a power sequence such that, "supplies should be staggered so that the highest voltage comes up first, then the remaining voltages in descending order. this is to avoid forward biasing internal (on-chip) diodes between supplies, and causing latch-up. Alternatively supplies can be synchronised to come up at exactly the same time as long as at no point a lower voltages supply rail exceeeds a higher voltage supply rail."

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

5V header for fansink

Loading:
OV9282 - 52mA max, each.

Loading:
OV9282 - 24mA max, each
IMX378 - 55mA max
CM_VDAC - 25mA, if active for A/V output

Placed RC timing circuit for EN pins in order to obtain the appropriate power supply sequencing if ncessary

Mark "PWR" on PCB

1ms slew meets the 50mV/us max slew requirement for the IMX378. This also provides ratiometric start-up, which meets the CM3 power on sequence requirement to avoid latch up.

SET POINT EQN FOR ALL REG OUTPUTS:

R2 = R1 x (0.6V / (Vout - 0.6V))

Compensation adjusted to set Fc 1/10th Fsw (200kHz) for all three outputs. The compensation circuitry has not been fully tuned.

Effective capacitance targets for each rail, taking into account DC bias and other effects:
3.3V C_eff = 24uF
1.8V C_eff = 26uF
1.05V C_eff = 70uF

Voltage ripple and allowed voltage tolerance on all rails is +/-5%

Load step design assumptions, based on worst case rail loading:
3.3V - 2.5A step
1.8V - 1A step
1.05 - 0.5A step

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Date: 10. 12. 2020	Time: 19:29:37	Sheet 7 of 17	
Drawn by: David Malovrh			

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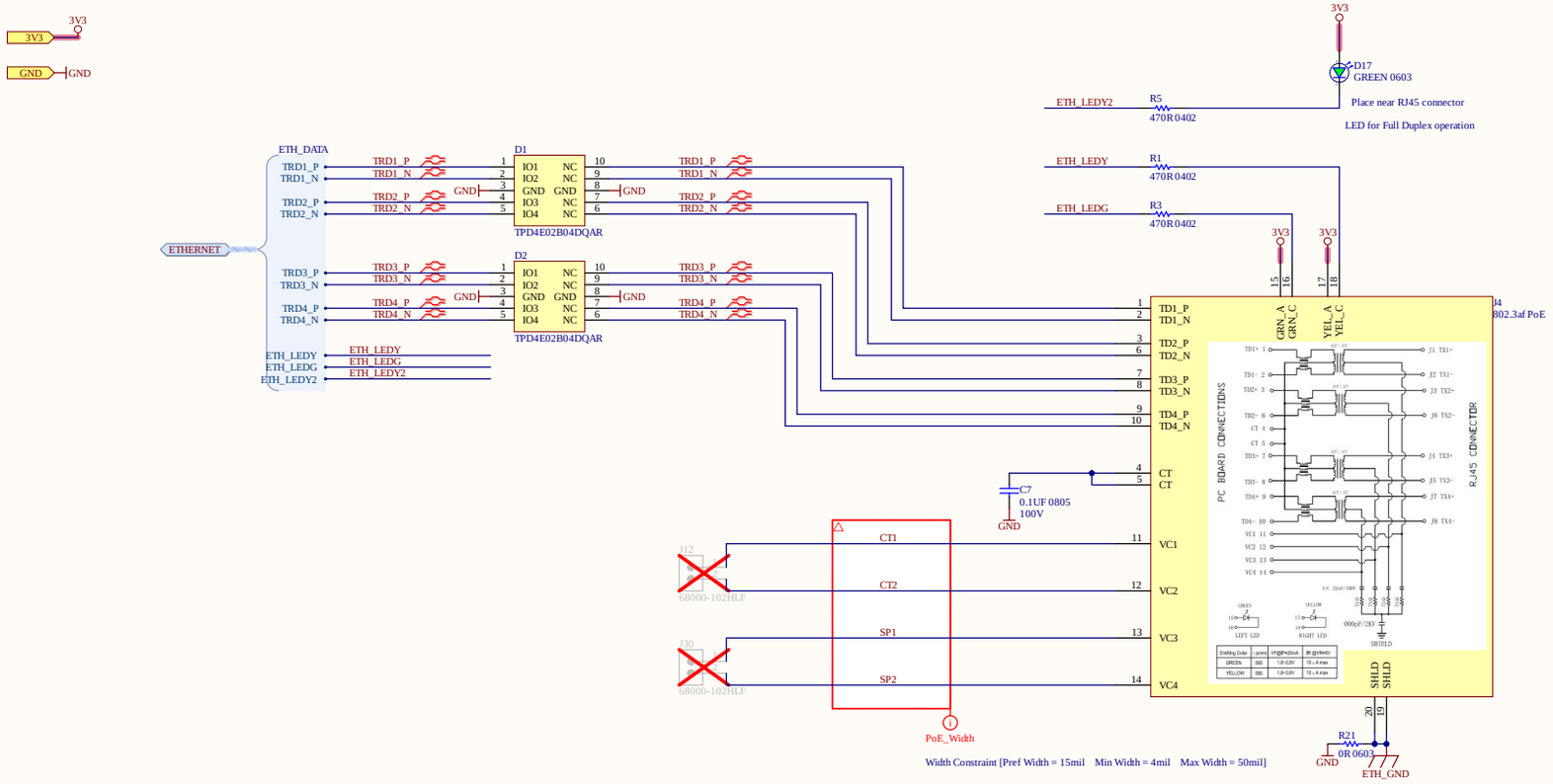

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Date: 10. 12. 2020	Time: 19:29:37	Sheet 8 of 12	
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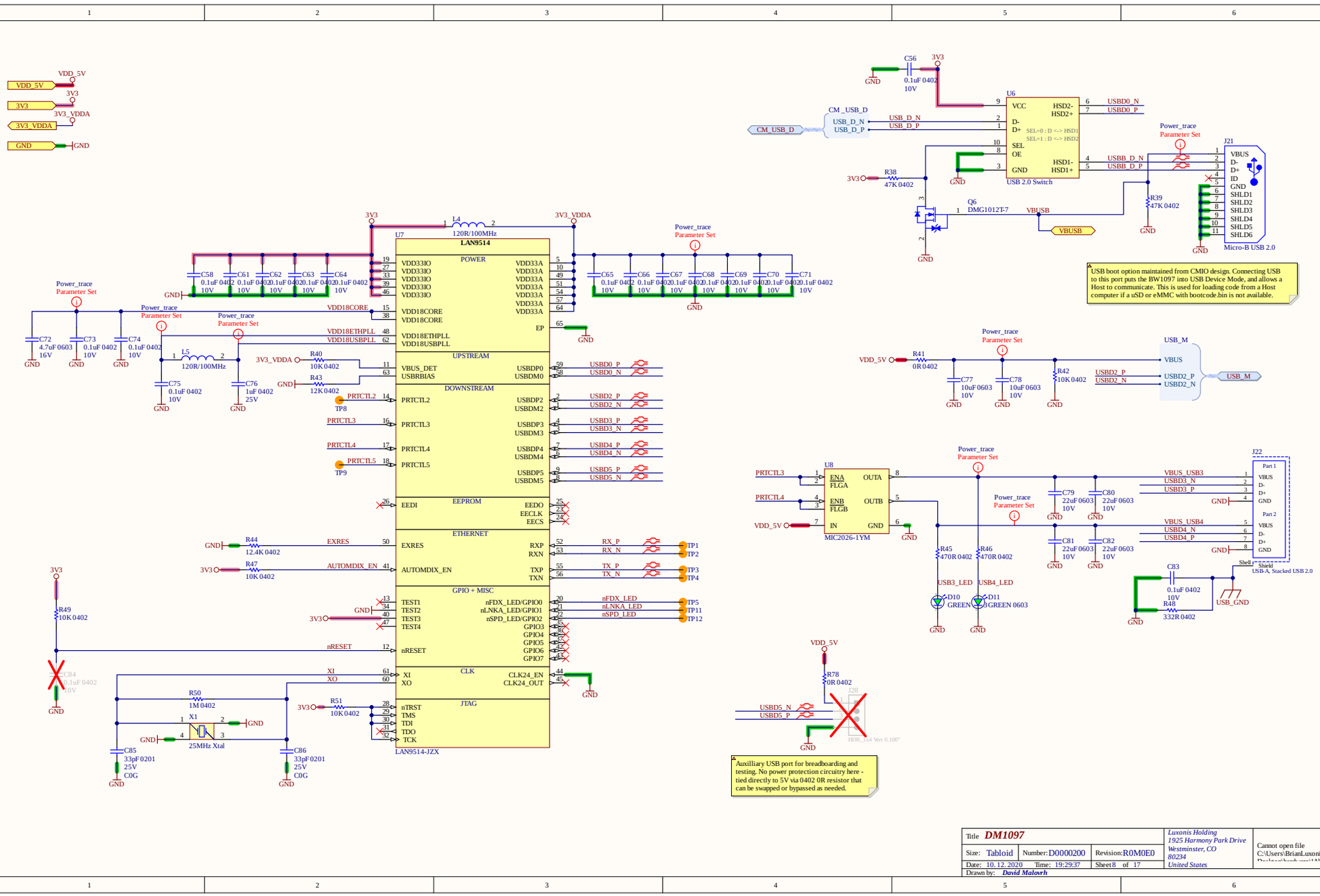
VDD_5V
3V3
3V3_VDDA
GND
U7
LAN9514
POWER
UPSTREAM
DOWNSTREAM
EEPROM
ETHERNET
GPIO + MISC
CLK
JTAG
LAN9514-JZX
L4 120R/100MHz
L5 120R/100MHz
U6
USB 2.0 Switch
CM_USB_D
Q6 DMG1012T-7
VBUSB
J21
Micro-B USB 2.0
USB boot option maintained from CMIO design. Connecting USB to this port puts the BW1097 into USB Device Mode, and allows a Host to communicate. This is used for loading code from a Host computer if a uSD or eMMC with bootcode.bin is not available.
USB_M
U8
MIC2026-1YM
J22
Shield
USB-A, Stacked USB 2.0
USB_GND
Auxilliary USB port for breadboarding and testing. No power protection circuitry here - tied directly to 5V via 0402 0R resistor that can be swapped or bypassed as needed.
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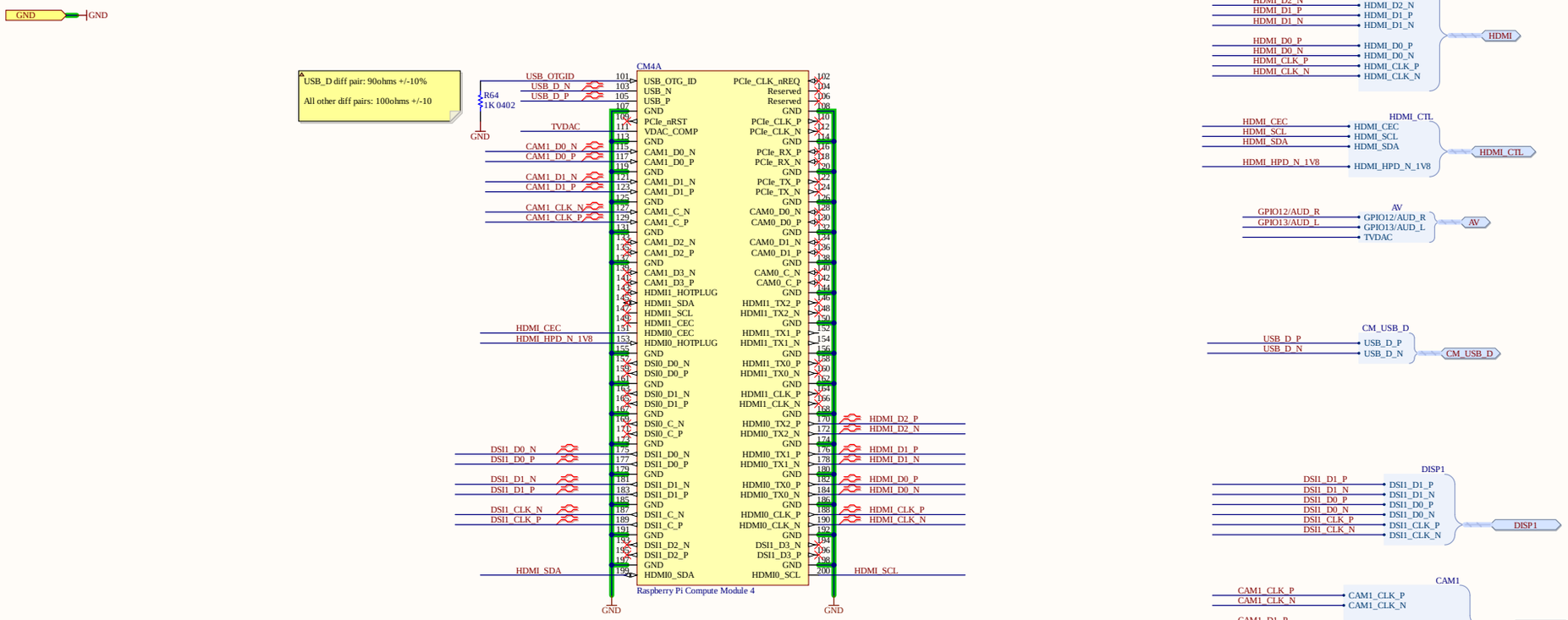

Title	DM1097
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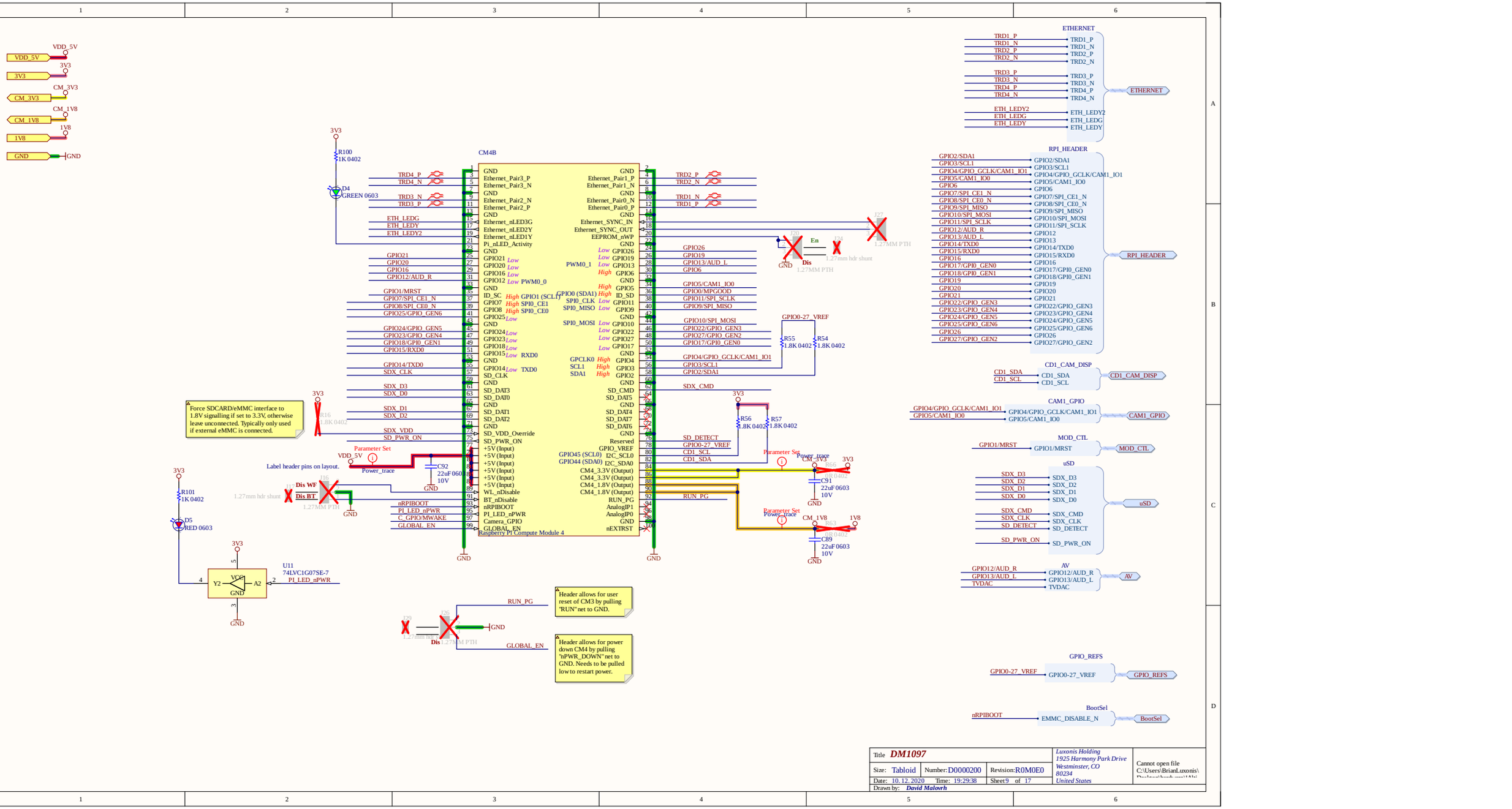
VDD_5V
3V3
CM_3V3
CM_1V8
1V8
GND
CM4B
Raspberry Pi Compute Module 4
Force SDCARD/eMMC interface to 1.8V signalling if set to 3.3V, otherwise leave unconnected. Typically only used if external eMMC is connected.
Label header pins on layout.
Header allows for user reset of CM3 by pulling "RUN" net to GND.
Header allows for power down CM4 by pulling "nPWR_DOWN" net to GND. Needs to be pulled low to restart power.
U11
74LVC1G07SE-7
ETHERNET
RPI_HEADER
CD1_CAM_DISP
CAM1_GPIO
MOD_CTL
uSD
AV
GPIO_REFS
BootSel
Title DM1097
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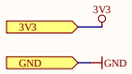
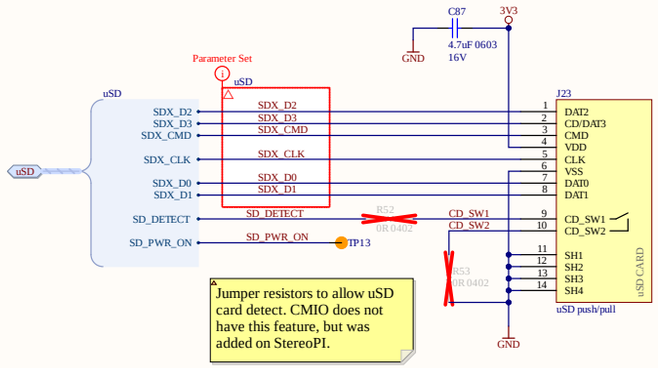


CMIO Note:

uSD is only used for modules with no on-board Flash (eMMC)



Jumper resistors to allow uSD card detect. CMIO does not have this feature, but was added on StereoPI.

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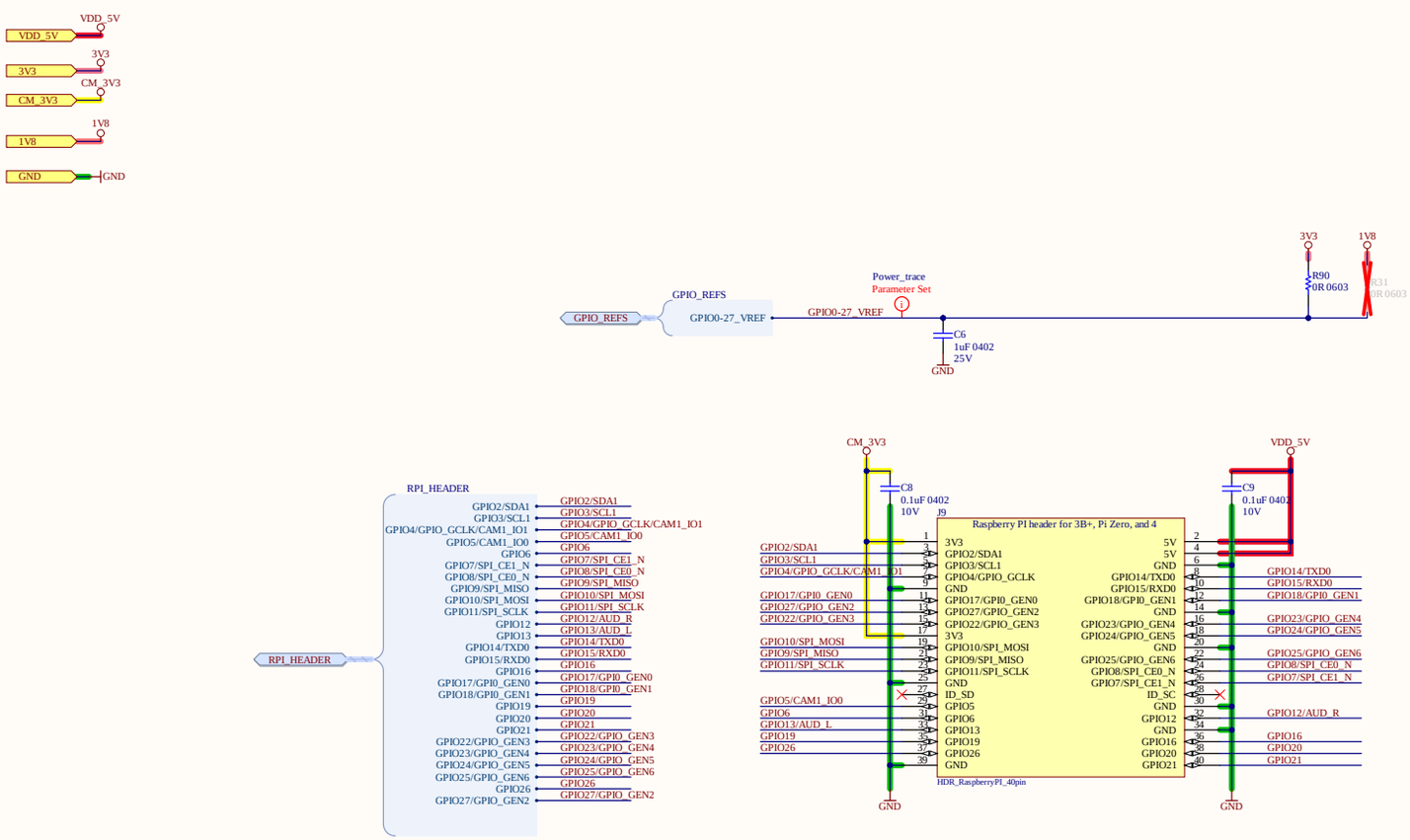
Drawn by: *David Malovrh*				



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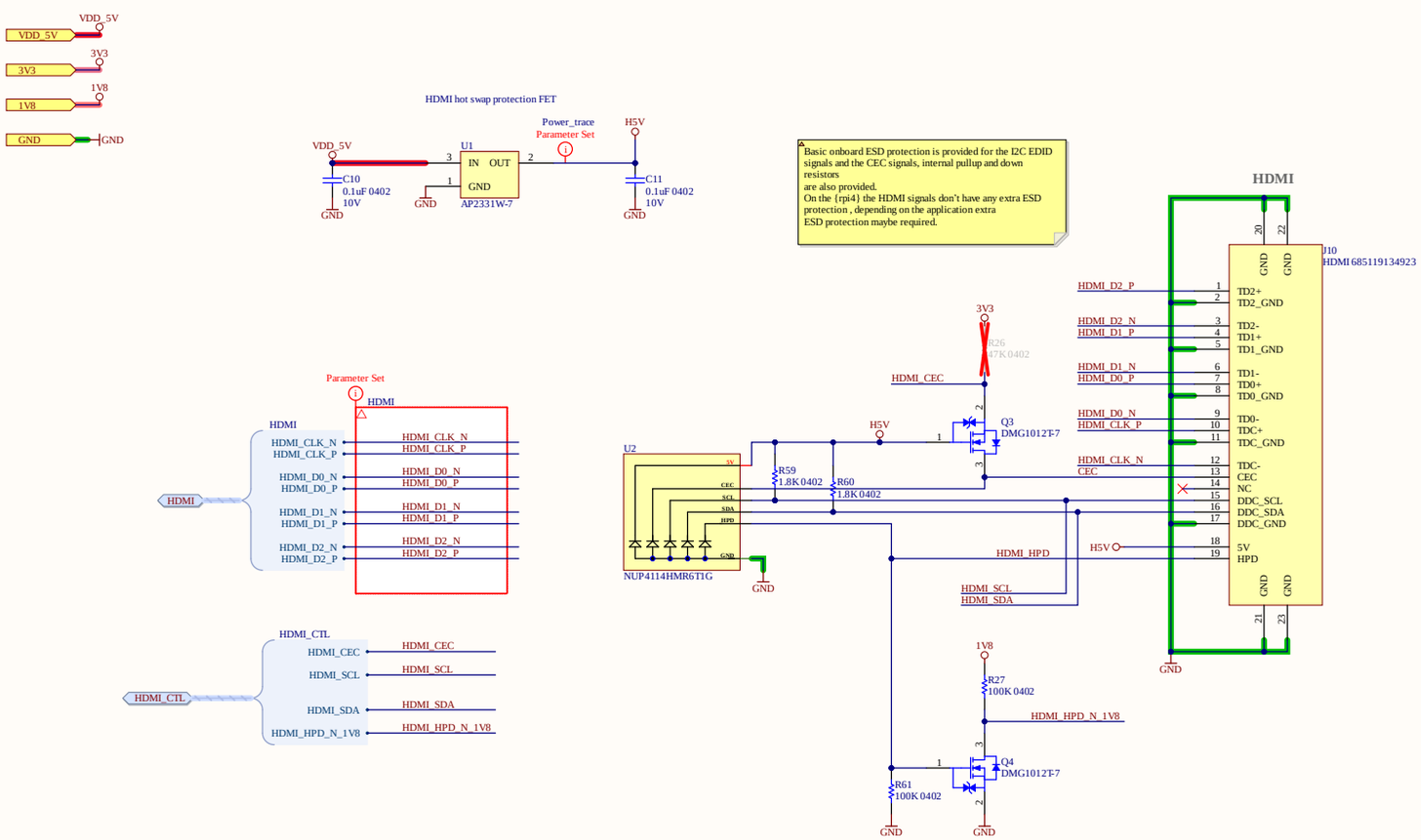

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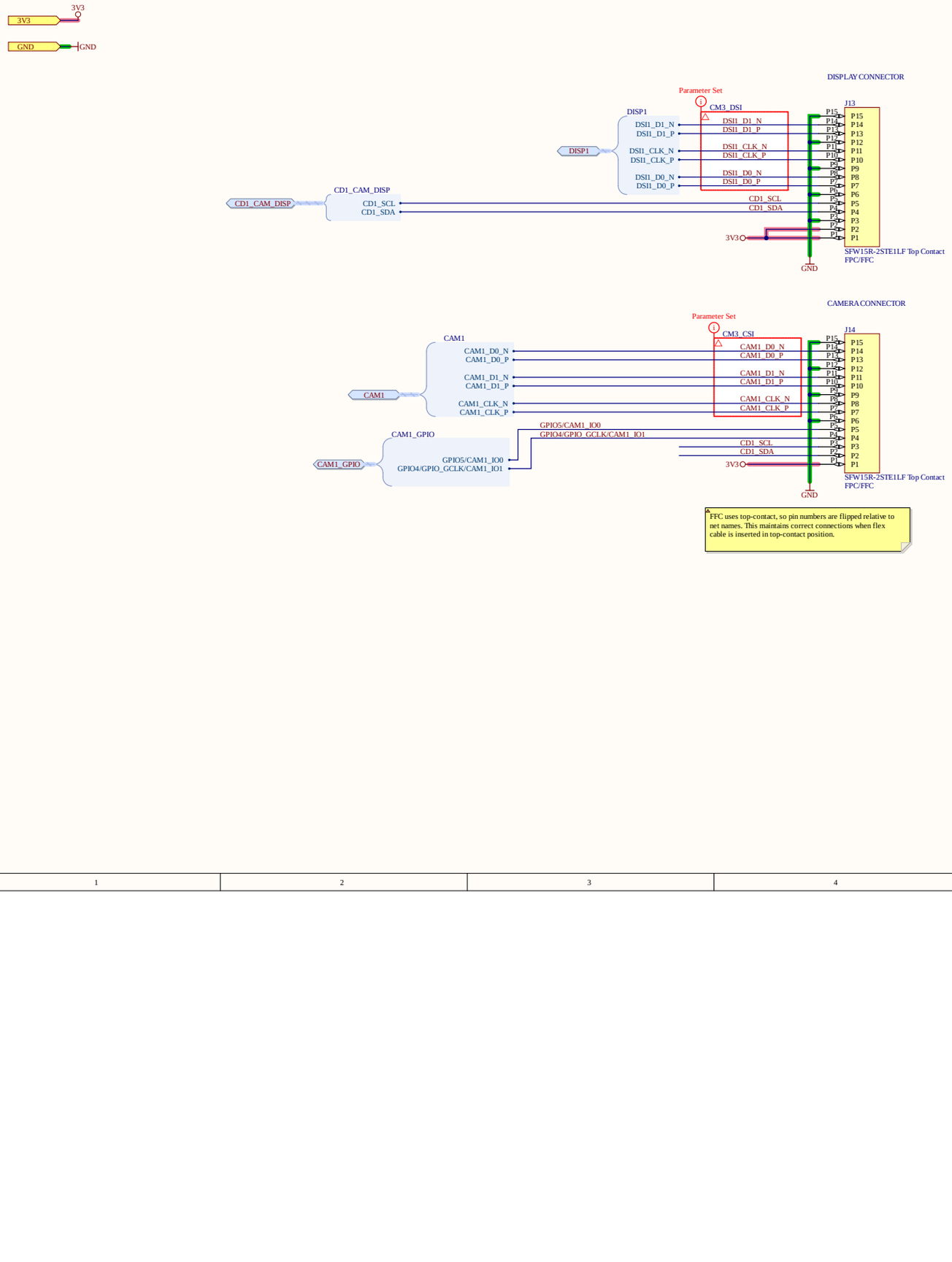

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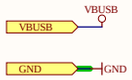
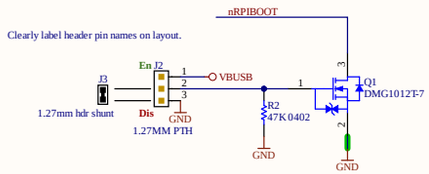
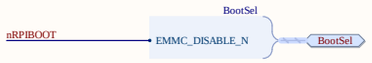


MODULE BOOT OPTIONS:

Short the nRPIBOOT pin to ground to force USB boot mode. The CM4IO board has a jumper for nRPIBOOT This can be used to enable different boot modes (e.g. network) and enable UART logging.





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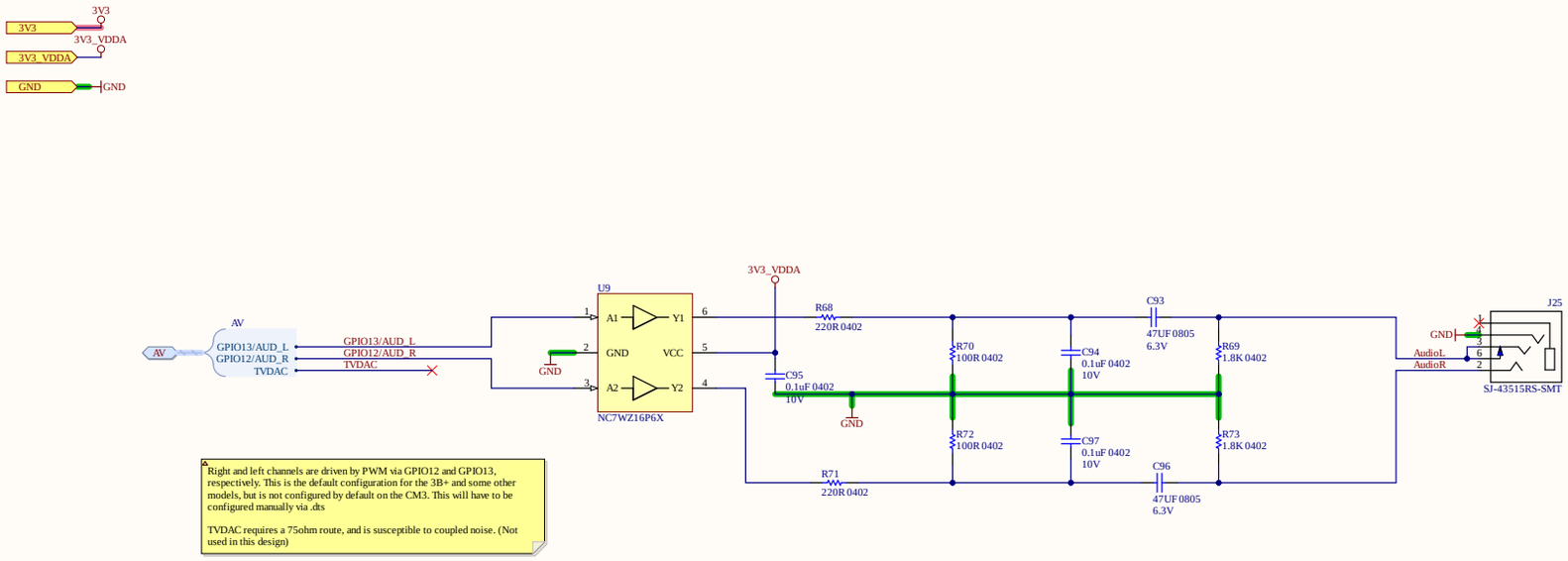

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