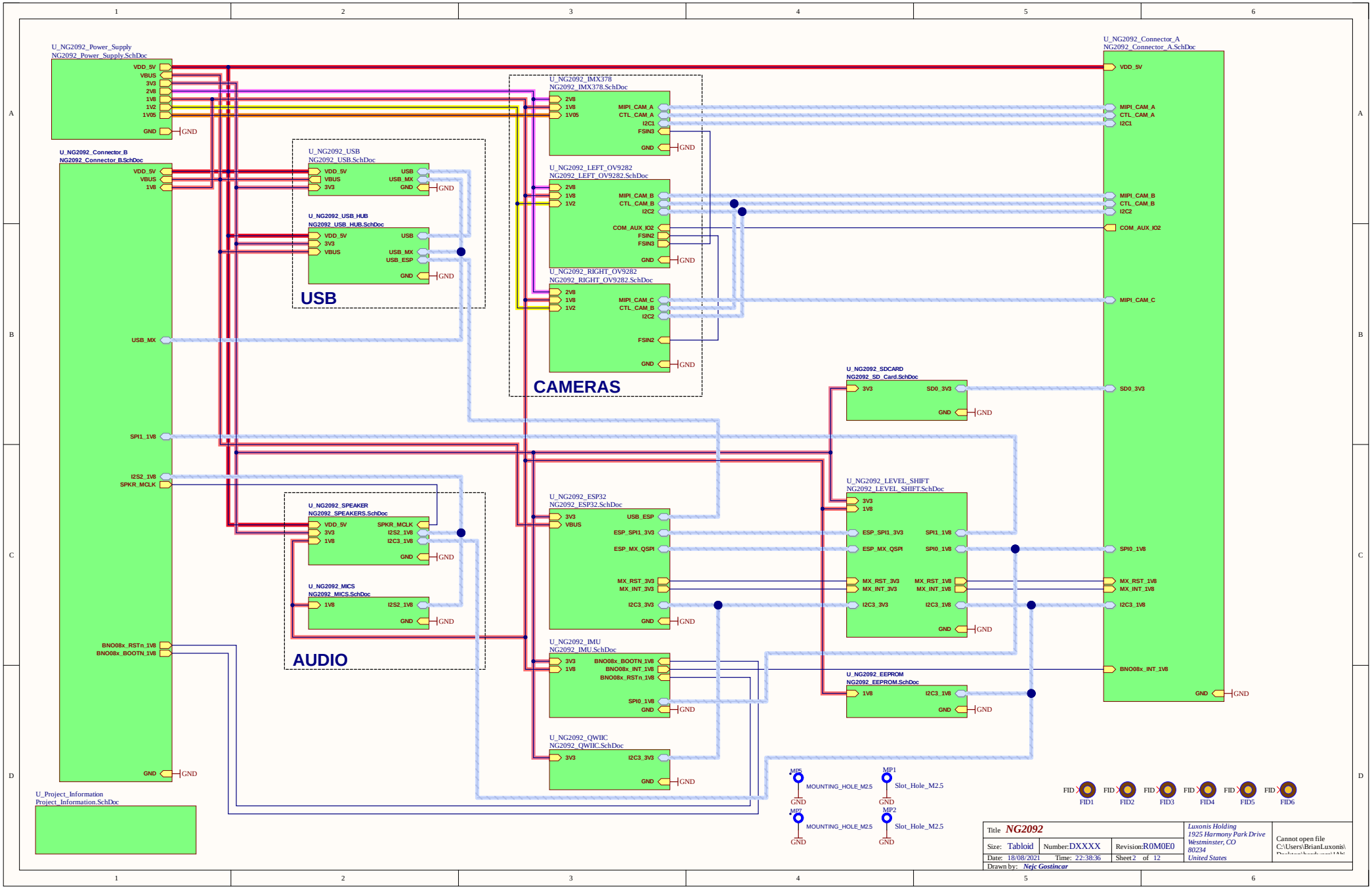
Project: ***NG2092***
Current Revision: ***R0M0E0***

NG2092 *Revision History:*

Date	Revision	Reason for Change	Changes Implemented
June 24th, 2021	Initial release		

Title: *NG2092*			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number: DXXXX	Revision: R0M0E0		
Date: 18/08/2021 Time: 22:38:35		Sheet 1 of 12		
Drawn by: ***Nejc Gostincar***				


U_NG2092_Power_Supply
NG2092_Power_Supply.SchDoc
VDD_5V
VBUS
3V3
2V8
1V8
1V2
1V05
GND
U_NG2092_Connector_B
NG2092_Connector_B.SchDoc
USB_MX
SPI1_1V8
I2S2_1V8
SPKR_MCLK
BNO08x_RSTn_1V8
BNO08x_BOOTN_1V8
U_NG2092_USB
NG2092_USB.SchDoc
USB
USB_ESP
U_NG2092_USB_HUB
NG2092_USB_HUB.SchDoc
USB
U_NG2092_SPEAKER
NG2092_SPEAKERS.SchDoc
U_NG2092_MICS
NG2092_MICS.SchDoc
AUDIO
U_NG2092_IMX378
NG2092_IMX378.SchDoc
MIPI_CAM_A
CTL_CAM_A
I2C1
FSIN3
U_NG2092_LEFT_OV9282
NG2092_LEFT_OV9282.SchDoc
MIPI_CAM_B
CTL_CAM_B
I2C2
COM_AUX_IO2
FSIN2
U_NG2092_RIGHT_OV9282
NG2092_RIGHT_OV9282.SchDoc
MIPI_CAM_C
CAMERAS
U_NG2092_ESP32
NG2092_ESP32.SchDoc
ESP_SPI1_3V3
ESP_MX_QSPI
MX_RST_3V3
MX_INT_3V3
I2C3_3V3
U_NG2092_IMU
NG2092_IMU.SchDoc
BNO08x_INT_1V8
U_NG2092_QWIIC
NG2092_QWIIC.SchDoc
U_NG2092_SDCARD
NG2092_SD_Card.SchDoc
SD0_3V3
U_NG2092_LEVEL_SHIFT
NG2092_LEVEL_SHIFT.SchDoc
SPI1_1V8
SPI0_1V8
MX_RST_1V8
MX_INT_1V8
I2C3_1V8
U_NG2092_EEPROM
NG2092_EEPROM.SchDoc
U_NG2092_Connector_A
NG2092_Connector_A.SchDoc
U_Project_Information
Project_Information.SchDoc
MP5
MOUNTING_HOLE_M2.5
MP1
Slot_Hole_M2.5
MP7
MP2
FID1
FID2
FID3
FID4
FID5
FID6
Title NG2092
Size: Tabloid
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Revision:R0M0E0
Date: 18/08/2021
Time: 22:38:36
Sheet 2 of 12
Drawn by: Nejc Gostincar
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
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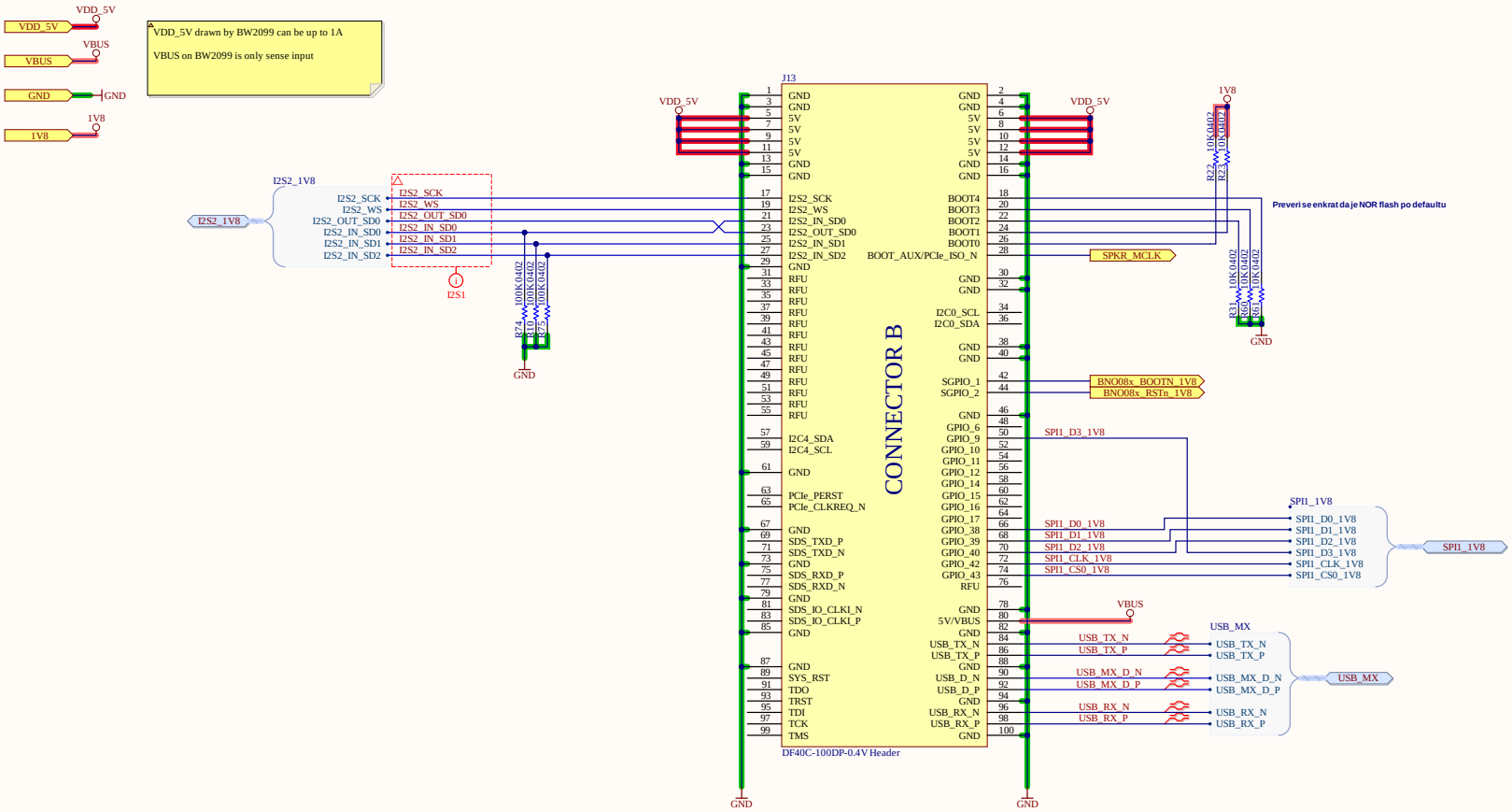

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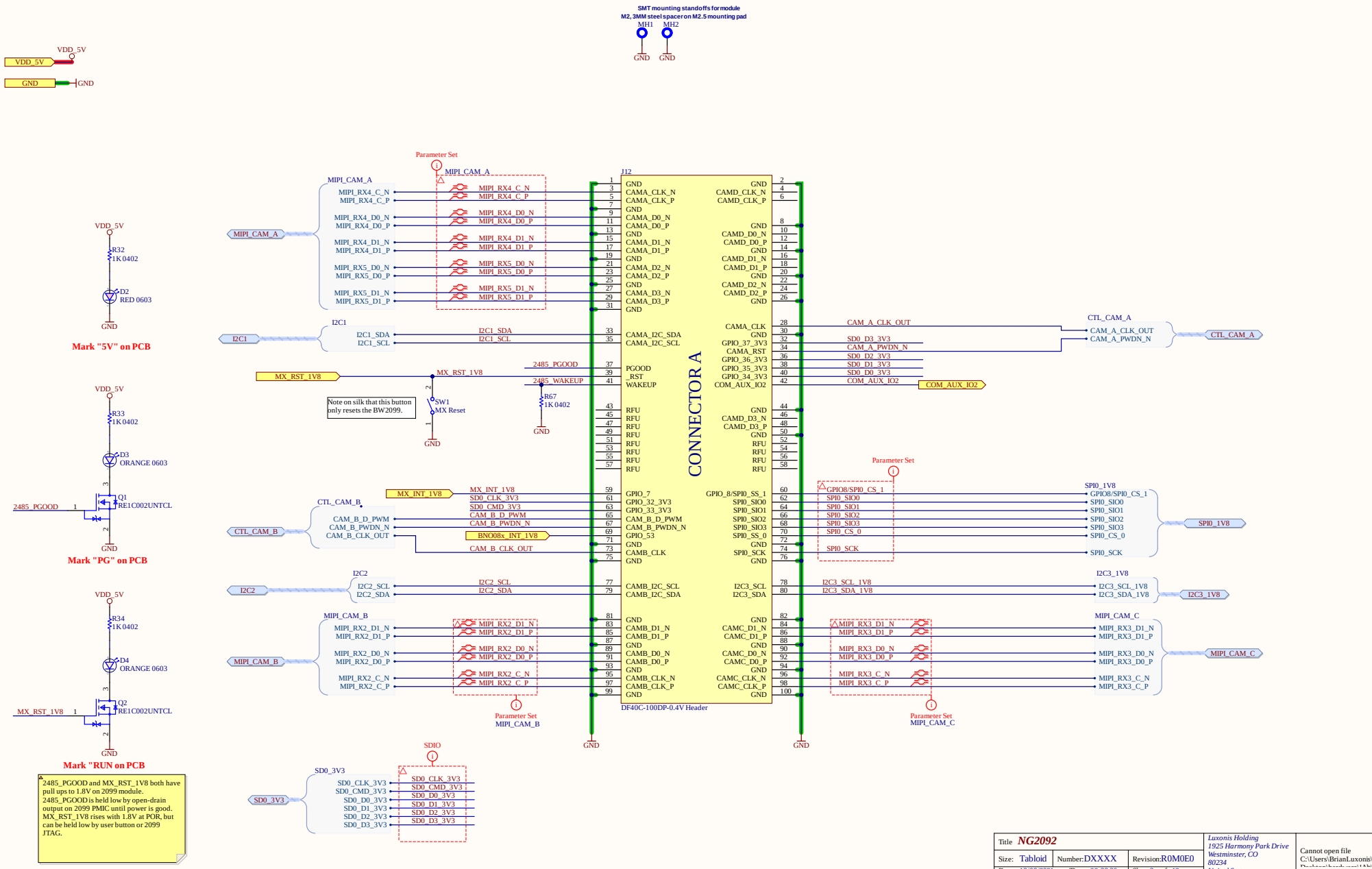
SMT mounting standoffs for module
M2, 3MM steel spacer on M2.5 mounting pad
MH1
MH2
GND
VDD_5V
R32
1K 0402
D2
RED 0603
Mark "5V" on PCB
R33
1K 0402
D3
ORANGE 0603
Q1
RE1C002UNTCL
2485_PGOOD
Mark "PG" on PCB
R34
1K 0402
D4
ORANGE 0603
Q2
RE1C002UNTCL
MX_RST_1V8
Mark "RUN on PCB
2485_PGOOD and MX_RST_1V8 both have pull ups to 1.8V on 2099 module.
2485_PGOOD is held low by open-drain output on 2099 PMIC until power is good.
MX_RST_1V8 rises with 1.8V at POR, but can be held low by user button or 2099 JTAG.
Parameter Set
MIPI_CAM_A
MIPI_RX4_C_N
MIPI_RX4_C_P
MIPI_RX4_D0_N
MIPI_RX4_D0_P
MIPI_RX4_D1_N
MIPI_RX4_D1_P
MIPI_RX5_D0_N
MIPI_RX5_D0_P
MIPI_RX5_D1_N
MIPI_RX5_D1_P
I2C1
I2C1_SDA
I2C1_SCL
2485_PGOOD
MX_RST_1V8
2485_WAKEUP
R67
1K 0402
SW1
MX Reset
Note on silk that this button only resets the BW2099.
J12
CONNECTOR A
DF40C-100DP-0.4V Header
CAMA_CLK_N
CAMA_CLK_P
CAMA_D0_N
CAMA_D0_P
CAMA_D1_N
CAMA_D1_P
CAMA_D2_N
CAMA_D2_P
CAMA_D3_N
CAMA_D3_P
CAMA_I2C_SDA
CAMA_I2C_SCL
PGOOD
_RST
WAKEUP
CAMD_CLK_N
CAMD_CLK_P
CAMD_D0_N
CAMD_D0_P
CAMD_D1_N
CAMD_D1_P
CAMD_D2_N
CAMD_D2_P
CAMD_D3_N
CAMD_D3_P
CAMA_CLK
CAMA_RST
GPIO_37_3V3
GPIO_36_3V3
GPIO_35_3V3
GPIO_34_3V3
COM_AUX_IO2
CAM_A_CLK_OUT
SD0_D3_3V3
CAM_A_PWDN_N
SD0_D2_3V3
SD0_D1_3V3
SD0_D0_3V3
CTL_CAM_A
CAM_A_CLK_OUT
CAM_A_PWDN_N
MX_INT_1V8
SD0_CLK_3V3
SD0_CMD_3V3
CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
BNO08x_INT_1V8
CTL_CAM_B
GPIO_7
GPIO_32_3V3
GPIO_33_3V3
GPIO_53
CAMB_CLK
GPIO_8/SPI0_SS_1
SPI0_SIO0
SPI0_SIO1
SPI0_SIO2
SPI0_SIO3
SPI0_SS_0
SPI0_SCK
SPI0_1V8
GPIO8/SPI0_CS_1
SPI0_CS_0
I2C2
I2C2_SCL
I2C2_SDA
CAMB_I2C_SCL
CAMB_I2C_SDA
I2C3_SCL
I2C3_SDA
I2C3_SCL_1V8
I2C3_SDA_1V8
I2C3_1V8
MIPI_CAM_B
MIPI_RX2_D1_N
MIPI_RX2_D1_P
MIPI_RX2_D0_N
MIPI_RX2_D0_P
MIPI_RX2_C_N
MIPI_RX2_C_P
CAMB_D1_N
CAMB_D1_P
CAMB_D0_N
CAMB_D0_P
CAMB_CLK_N
CAMB_CLK_P
CAMC_D1_N
CAMC_D1_P
CAMC_D0_N
CAMC_D0_P
CAMC_CLK_N
CAMC_CLK_P
MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P
MIPI_CAM_C
SDIO
SD0_3V3
SD0_CLK_3V3
SD0_CMD_3V3
SD0_D0_3V3
SD0_D1_3V3
SD0_D2_3V3
SD0_D3_3V3
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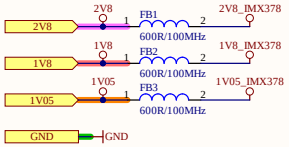
Place FBs and caps close to their associated camera connector.



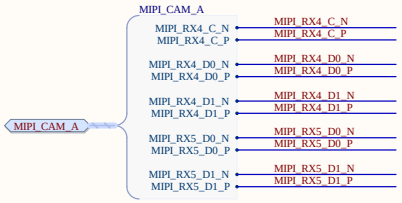
Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

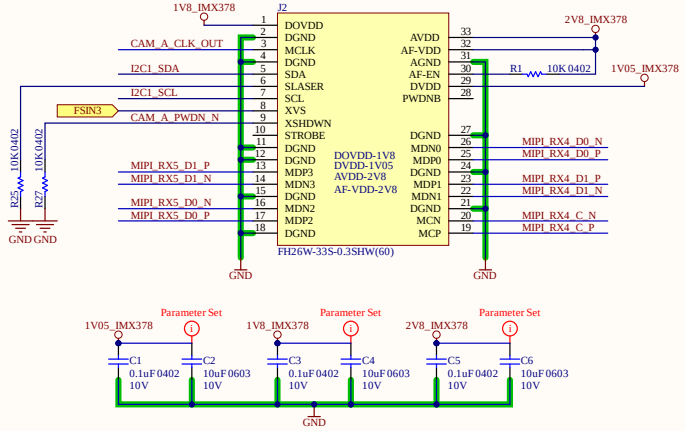
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

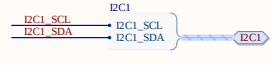
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

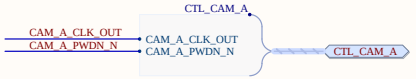


IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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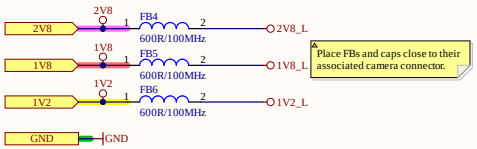
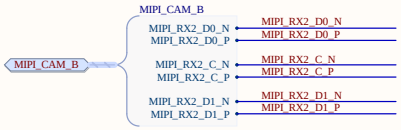


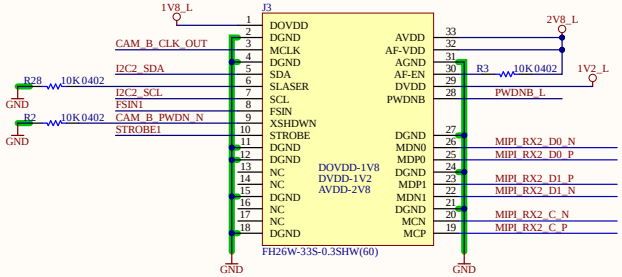
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

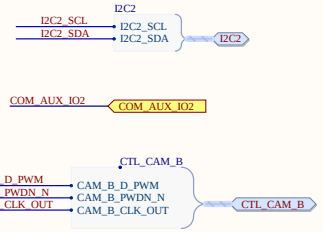
Supply Information

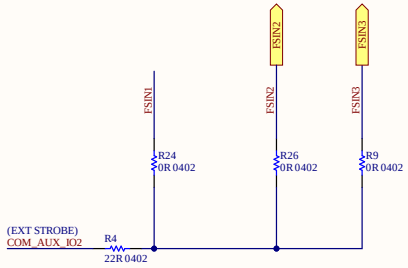
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



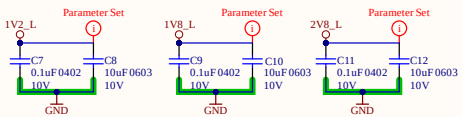
Mark "LEFT" on PCB
Place so that is the module's left camera.







Camera timing Sync Option



Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to tl sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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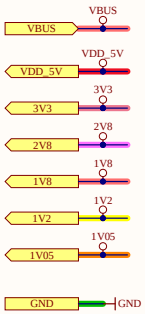
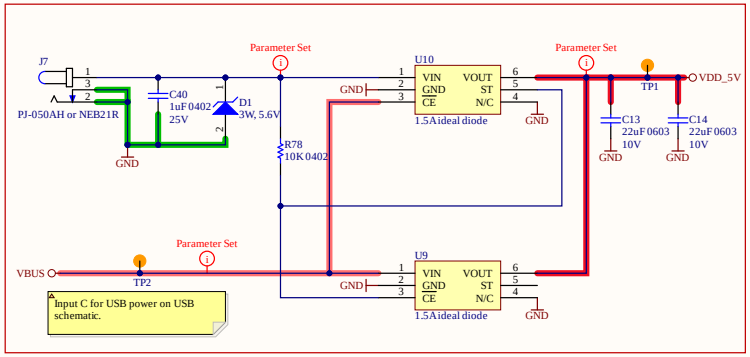
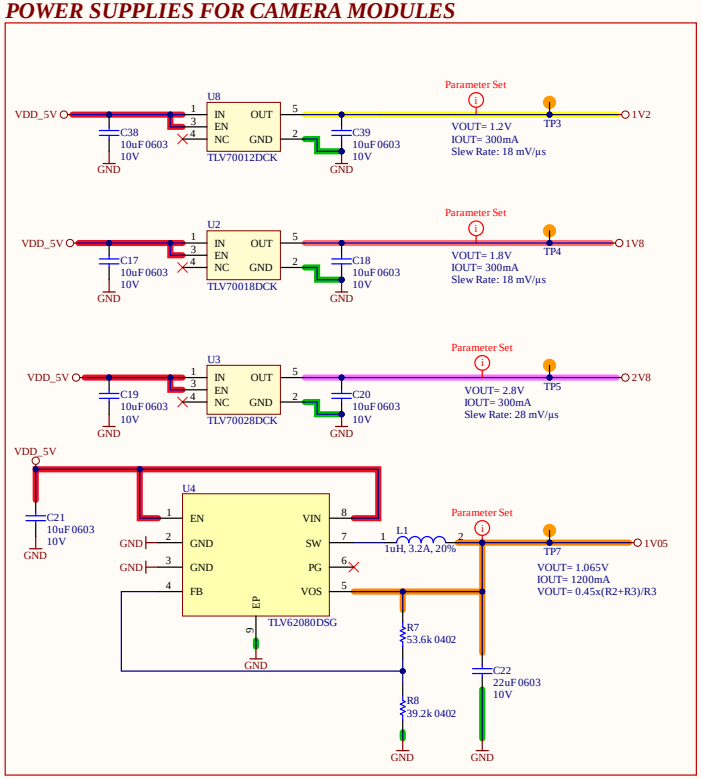
Drawn by: Nejc Gostincar			



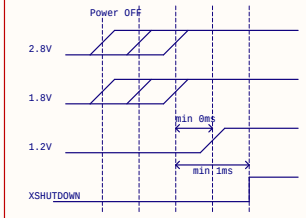
POWER INPUT



POWER SUPPLIES FOR CAMERA MODULES



OV9282 POWER REQUIREMENTS

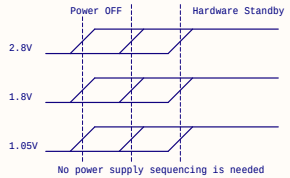


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

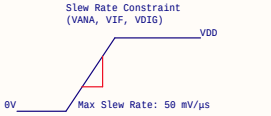
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

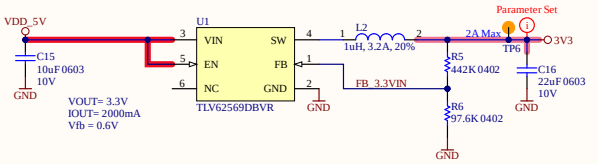


POWER SEQUENCING REQUIREMENTS:

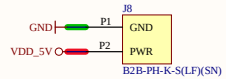
The BW2099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

3.3V POWER



FAN CONTROLLER



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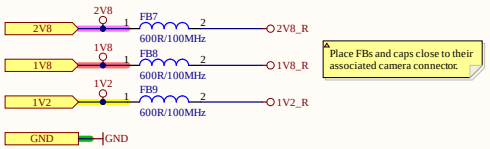
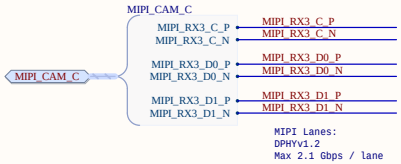


Place FBs and caps close to their associated camera connector.

MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

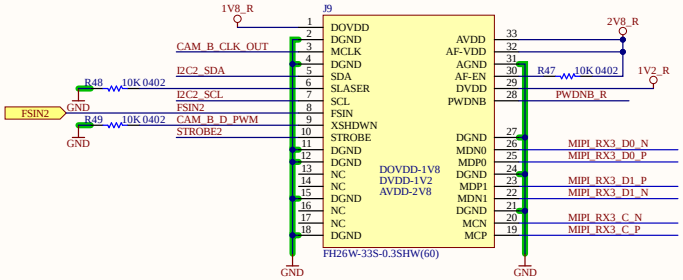
Supply Information

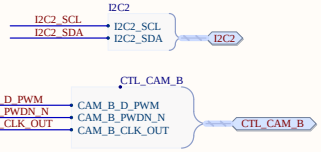
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

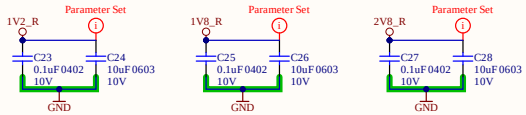


MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

Mark "RIGHT" on PCB
Place so that this is the module's right camera.







Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if t stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to t sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title	NG2092		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number:DXXXX	Revision:R0M0E0	
Date: 18/08/2021 Time: 22:38:36	Sheet 7 of 12		
Drawn by: Nejc Gostincar			

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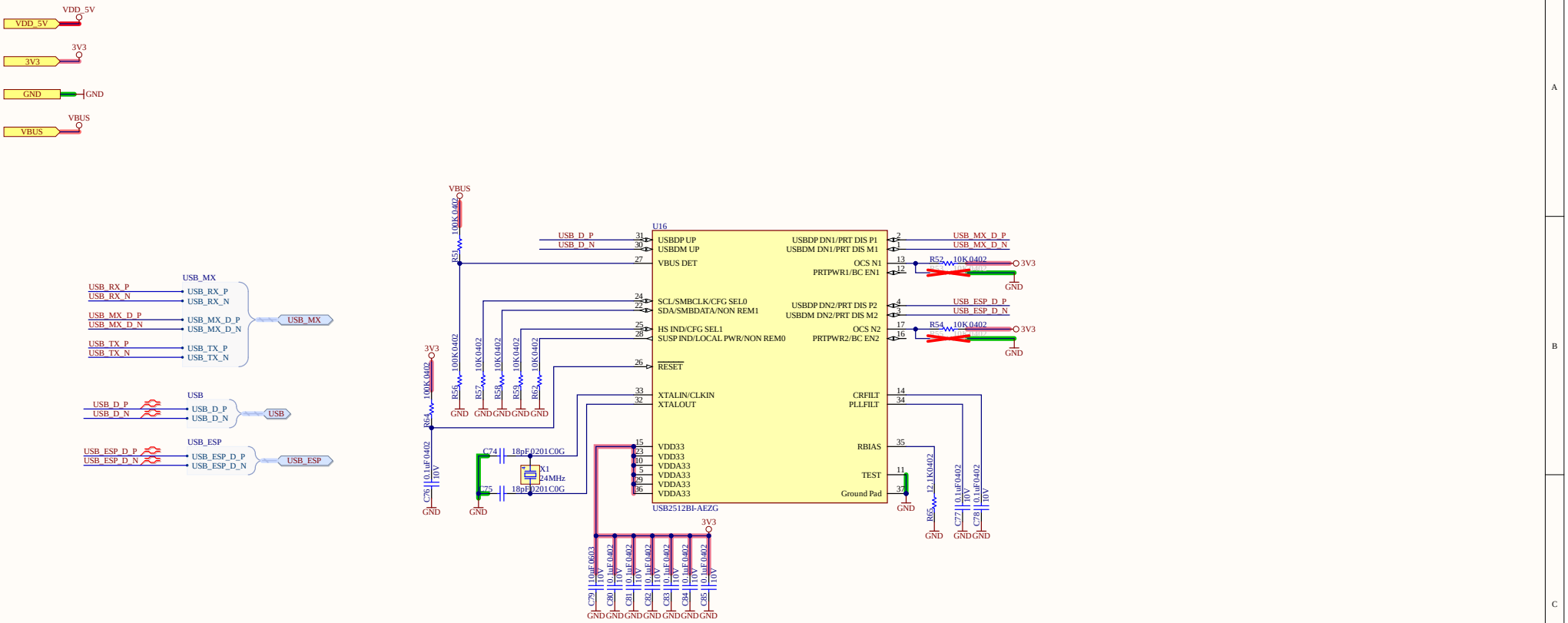

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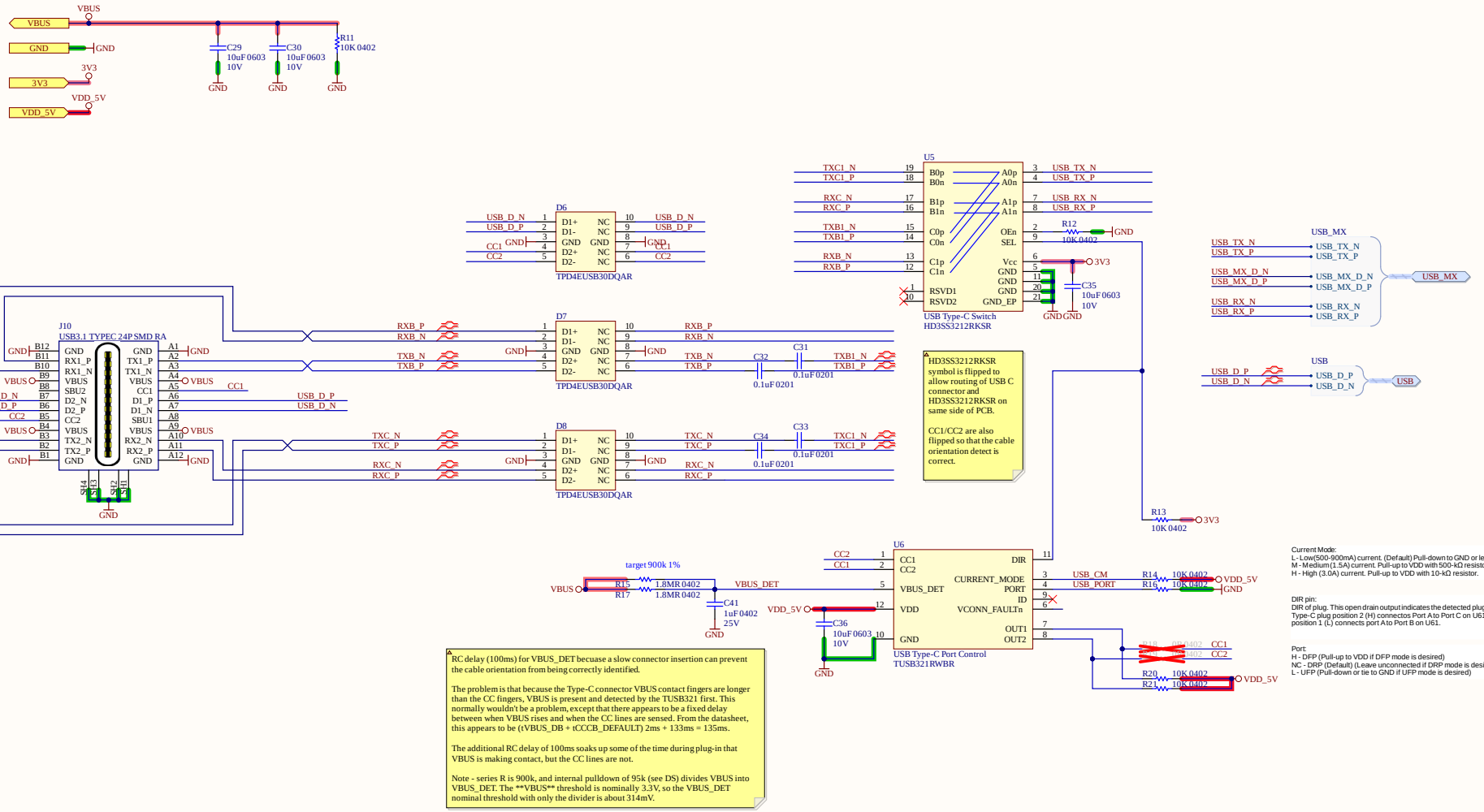

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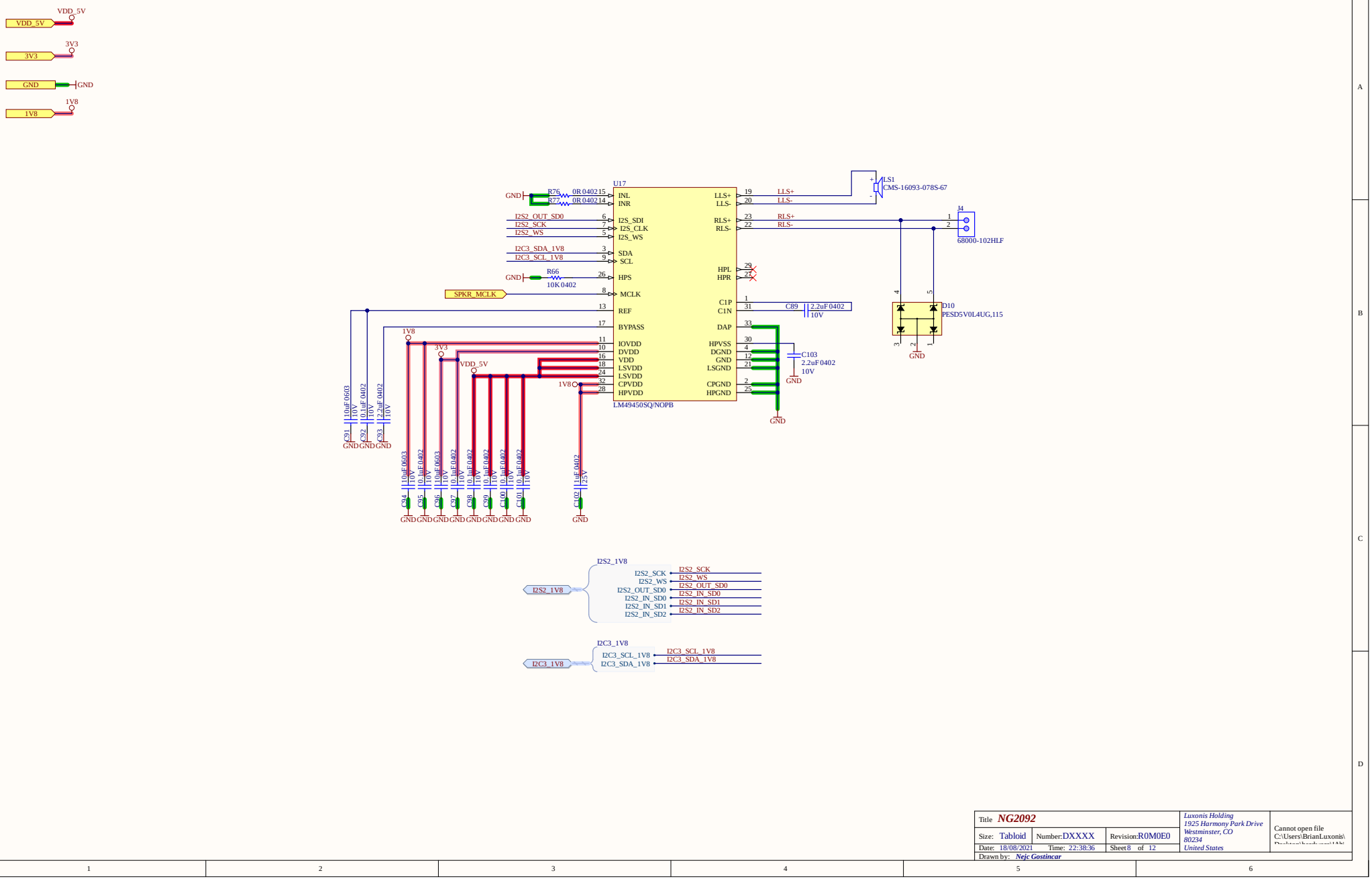

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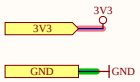

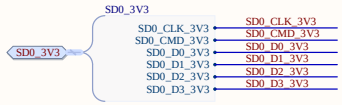

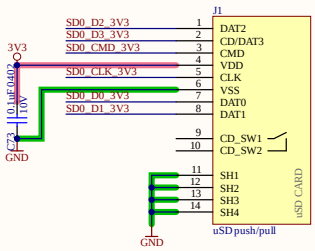

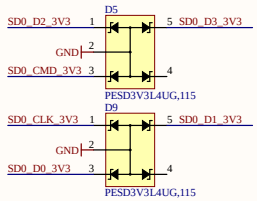

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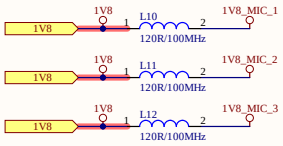

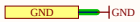

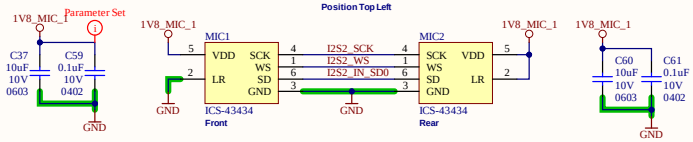

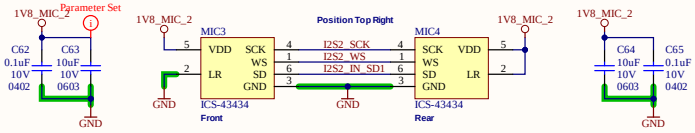

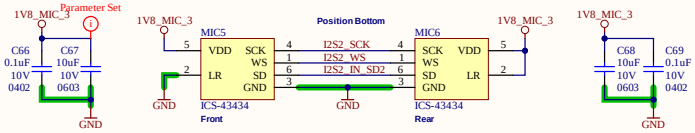

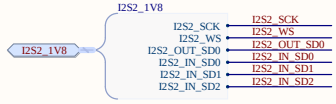

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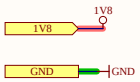

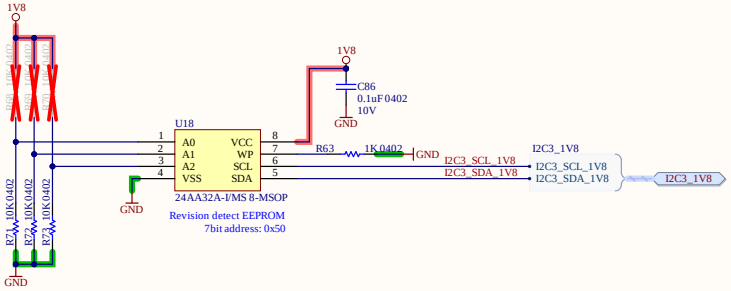

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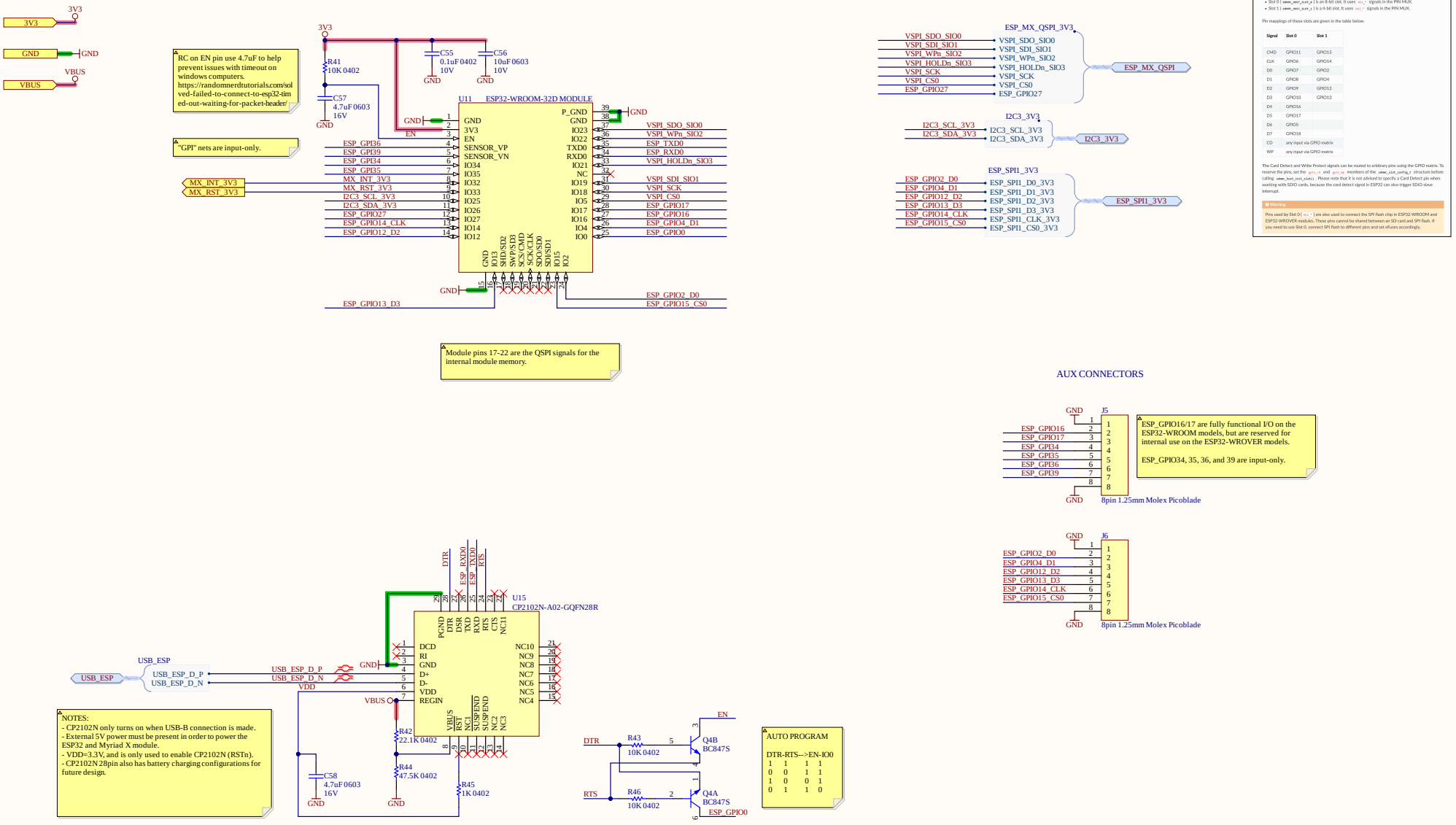
3V3
GND
VBUS
RC on EN pin use 4.7uF to help prevent issues with timeout on windows computers. https://randomnerdtutorials.com/solved-failed-to-connect-to-esp32-timed-out-waiting-for-packet-header/
R41 10K 0402
C55 0.1uF 0402 10V
C56 10uF 0603 10V
C57 4.7uF 0603 16V
"GPI" nets are input-only.
MX_INT_3V3
MX_RST_3V3
U11 ESP32-WROOM-32D MODULE
GND
3V3
EN
SENSOR_VP
SENSOR_VN
IO34
IO35
IO32
IO33
IO25
IO26
IO27
IO14
IO12
P_GND
IO23
IO22
TXD0
RXD0
IO21
NC
IO19
IO18
IO5
IO17
IO16
IO4
IO0
ESP_GPI36
ESP_GPI39
ESP_GPI34
ESP_GPI35
I2C3_SCL_3V3
I2C3_SDA_3V3
ESP_GPIO27
ESP_GPIO14_CLK
ESP_GPIO12_D2
ESP_GPIO13_D3
VSPI_SDO_SIO0
VSPI_WPn_SIO2
ESP_TXD0
ESP_RXD0
VSPI_HOLDn_SIO3
VSPI_SDI_SIO1
VSPI_SCK
VSPI_CS0
ESP_GPIO17
ESP_GPIO16
ESP_GPIO4_D1
ESP_GPIO0
ESP_GPIO2_D0
ESP_GPIO15_CS0
Module pins 17-22 are the QSPI signals for the internal module memory.
ESP_MX_QSPI_3V3
ESP_MX_QSPI
I2C3_3V3
ESP_SPI1_3V3
SDMMC Host Driver
Overview
ESP32's SDMMC host peripheral has two slots:
Slot 0 (sdmmc_host_slot_0) is an 8-bit slot. It uses sd1_* signals in the PIN MUX.
Slot 1 (sdmmc_host_slot_1) is a 4-bit slot. It uses sd2_* signals in the PIN MUX.
Pin mappings of these slots are given in the table below.
Signal | Slot 0 | Slot 1
CMD | GPIO11 | GPIO15
CLK | GPIO6 | GPIO14
D0 | GPIO7 | GPIO2
D1 | GPIO8 | GPIO4
D2 | GPIO9 | GPIO12
D3 | GPIO10 | GPIO13
D4 | GPIO16 |
D5 | GPIO17 |
D6 | GPIO5 |
D7 | GPIO18 |
CD | any input via GPIO matrix |
WP | any input via GPIO matrix
The Card Detect and Write Protect signals can be routed to arbitrary pins using the GPIO matrix. To reserve the pins, set the gpio_cd and gpio_wp members of the sdmmc_slot_config_t structure before calling sdmmc_host_init_slot() . Please note that it is not advised to specify a Card Detect pin when working with SDIO cards, because the card detect signal in ESP32 can also trigger SDIO slave interrupt.
Warning
Pins used by Slot 0 (sd1_*) are also used to connect the SPI flash chip in ESP32-WROOM and ESP32-WROVER modules. These pins cannot be shared between an SD card and SPI flash. If you need to use Slot 0, connect SPI flash to different pins and set eFuses accordingly.
AUX CONNECTORS
J5
ESP_GPIO16
ESP_GPIO17
ESP_GPI34
ESP_GPI35
ESP_GPI36
ESP_GPI39
8pin 1.25mm Molex Picoblade
ESP_GPIO16/17 are fully functional I/O on the ESP32-WROOM models, but are reserved for internal use on the ESP32-WROVER models.
ESP_GPIO34, 35, 36, and 39 are input-only.
J6
ESP_GPIO2_D0
ESP_GPIO4_D1
ESP_GPIO12_D2
ESP_GPIO13_D3
ESP_GPIO14_CLK
ESP_GPIO15_CS0
8pin 1.25mm Molex Picoblade
U15 CP2102N-A02-GQFN28R
PGND
DTR
DSR
TXD
RXD
RTS
CTS
NC11
DCD
RI
GND
D+
D-
VDD
REGIN
NC10
NC9
NC8
NC7
NC6
NC5
NC4
VBUS
RST
SUSPEND
SUSPEND
NC2
NC3
USB_ESP
USB_ESP_D_P
USB_ESP_D_N
R42 22.1K 0402
R44 47.5K 0402
R45 1K 0402
C58 4.7uF 0603 16V
R43 10K 0402
R46 10K 0402
Q4B BC847S
Q4A BC847S
AUTO PROGRAM
DTR-RTS-->EN-IO0
1 1 1 1
0 0 1 1
1 0 0 1
0 1 1 0
NOTES:
- CP2102N only turns on when USB-B connection is made.
- External 5V power must be present in order to power the ESP32 and Myriad X module.
- VDD=3.3V, and is only used to enable CP2102N (RSTn).
- CP2102N 28pin also has battery charging configurations for future design.
Title NG2092
Size: Tabloid
Number:DXXXX
Revision:R0M0E0
Date: 18/08/2021
Time: 22:38:37
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Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
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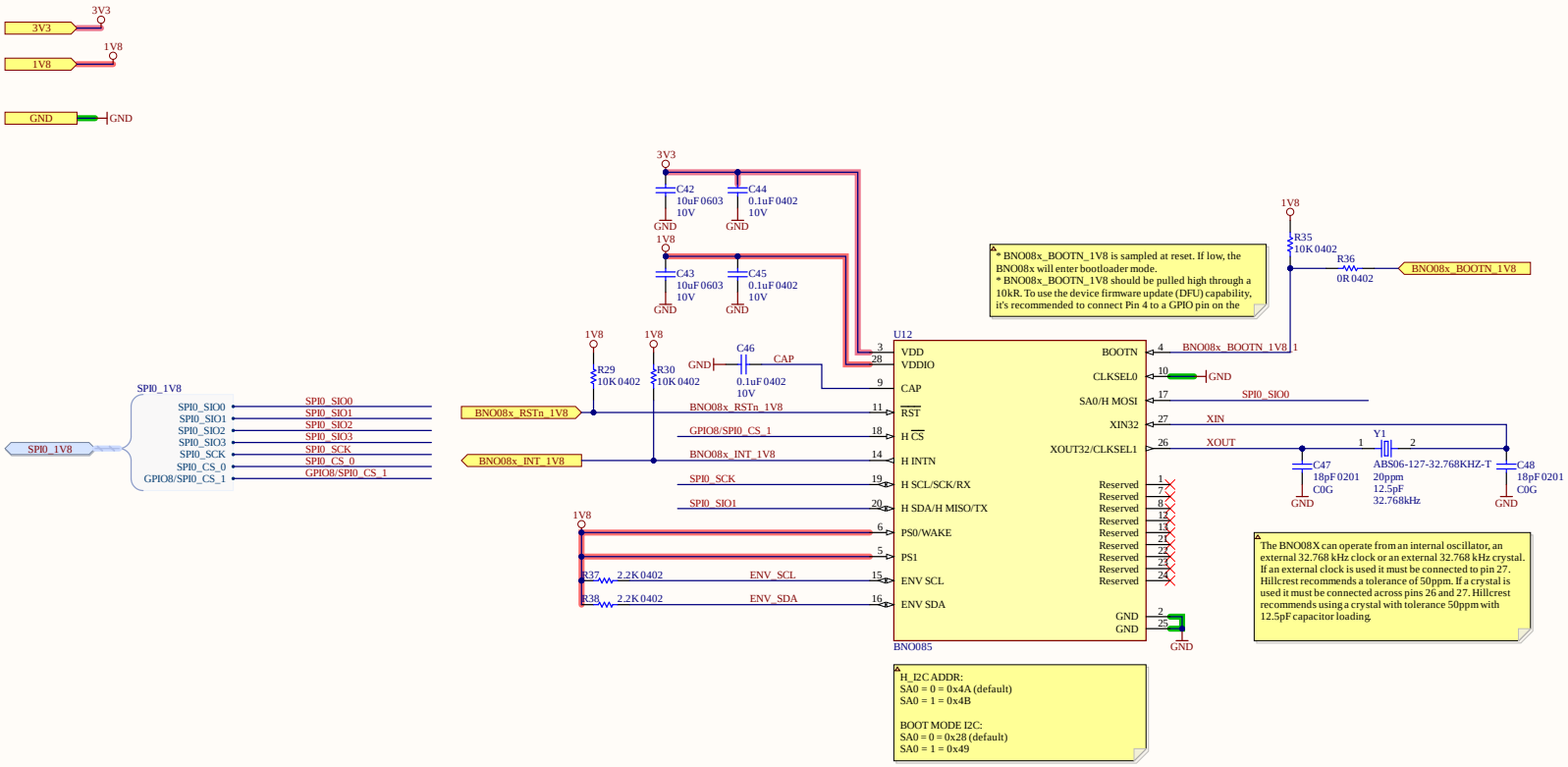

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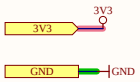

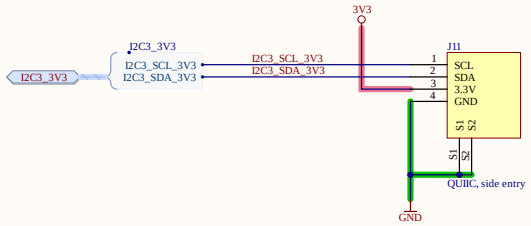

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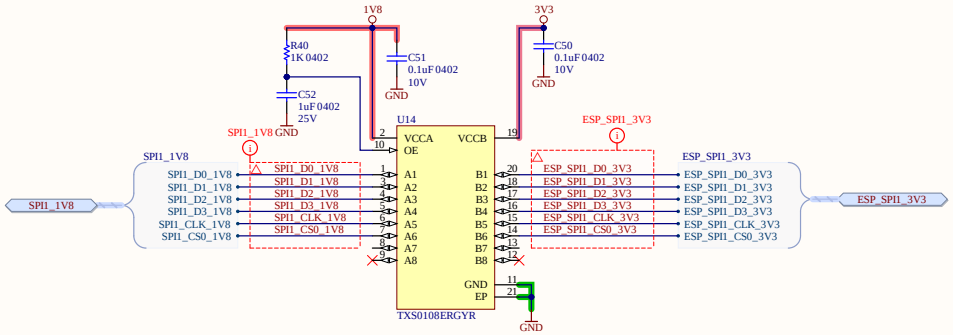
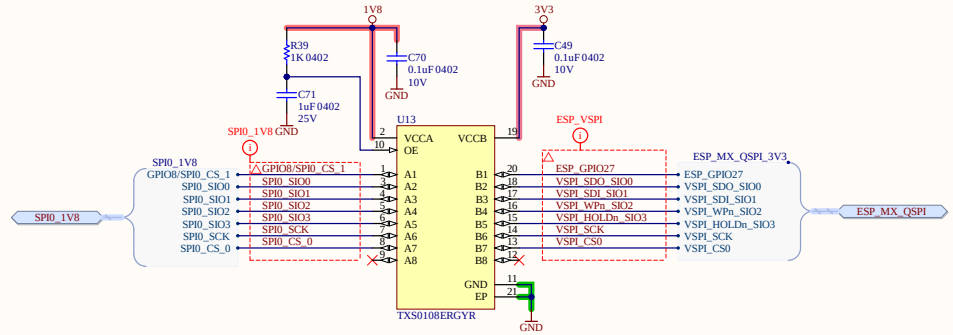
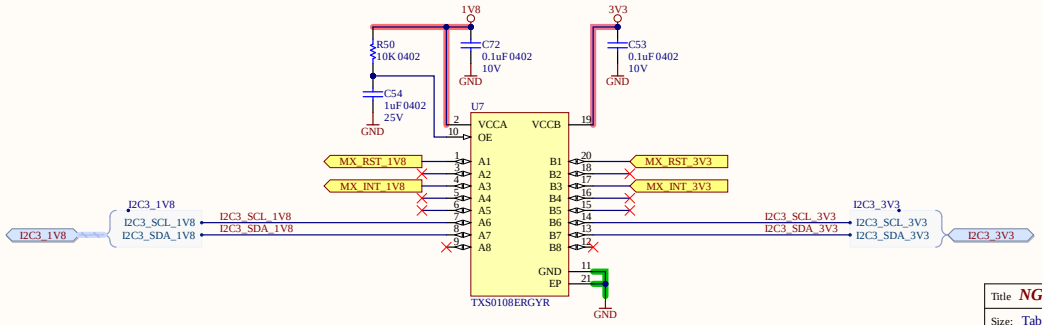




When driving high. TXS0108E ports have internal 4k pull ups to VCCA and VCCB, but when driving low, the pull up is 40k.

The TXS0101/2/4 translators have fixed 10-kΩ value pull-up resistors which provide dc-bias and dc current sourcing/drive capabilities to maintain a high signal. The TXS0108E translator reliably supports high-speed data rates in excess of 60Mbps, whereas the initial TXS series type translators supported slightly less than half this. The ability to translate down to the 1.2V operating-node is also supported in the TXS0108E device.



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