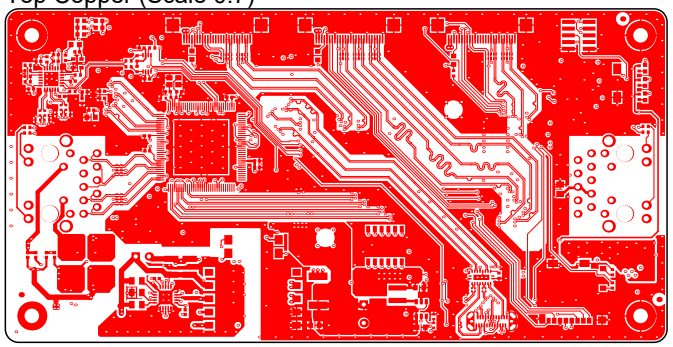
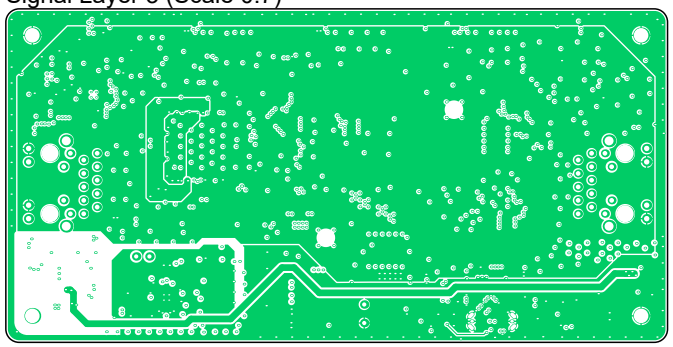
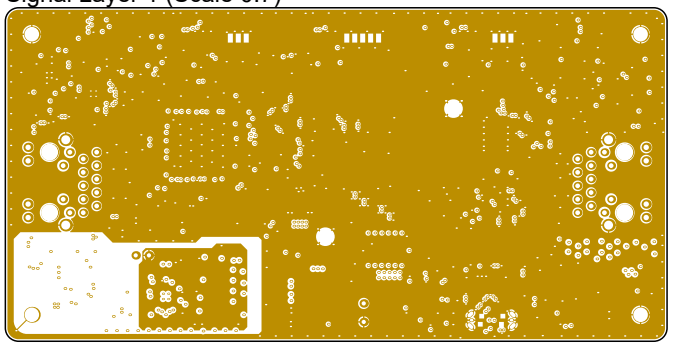
Top Copper (Scale 0.7)



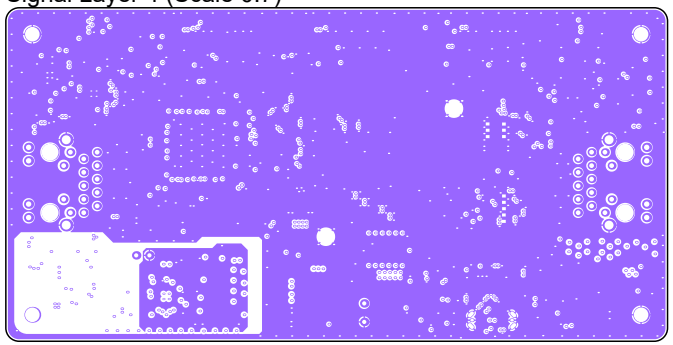
Signal Layer 3 (Scale 0.7)



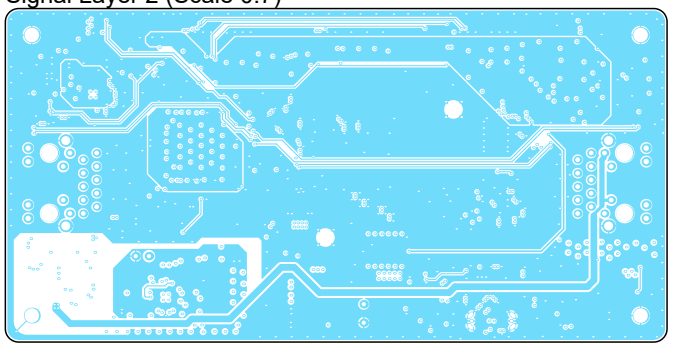
Signal Layer 1 (Scale 0.7)



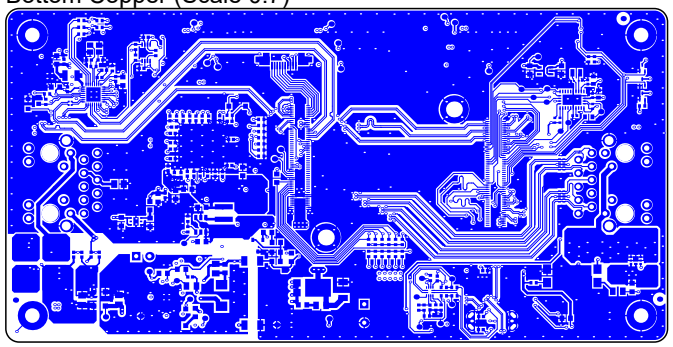
Signal Layer 4 (Scale 0.7)



Signal Layer 2 (Scale 0.7)



Bottom Copper (Scale 0.7)



**FABRICATION NOTES:**

**Fabricate per IPC-6011 & IPC-6012 CLASS 2**
**Inspect per IPC-A-600 CLASS 2**
**Test per IPC-TM-650**

*** PCB has 6 copper layers**
*** Copper thicknesses are finished and include base foil plus Cu plating on plated layers.**
*** PCB thickness: 63mil +/- 3mil**
*** Min. trace width/clearance: 4/4mil**
*** Min. hole drill/ring: 8mil/16mil**
*** All vias-in-pad shall be plugged and plated over (VIPPO)**
*** Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.**
*** Silkscreen, non-conductive epoxy ink, color: white**
*** Remove slikscreen as needed to prevent ink on any exposed copper**
*** Surface finish: ENIG**
*** Hole dimensions are finished size, +/-3mil**
*** Linear board dimension tolerance: +/-10mil**
*** Bow, twist, warp not to exceed 0.75% of greatest diagonal span**
*** PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0**
*** PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side**
*** All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.**

**Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.**

**Controlled impedance differential pairs shall be within +/-10% of target impedance. See sheets below for more detail.**

| | |
|---|---|
| Title: ***DD2088PoE_Daisy_Chain*** | LUXonis |
| Number: Revision: R0M0 E0 | |
| Date: 18-May-21 Sheet: 1 of 4 | PROPRIETARY AND CONFIDENTIAL |
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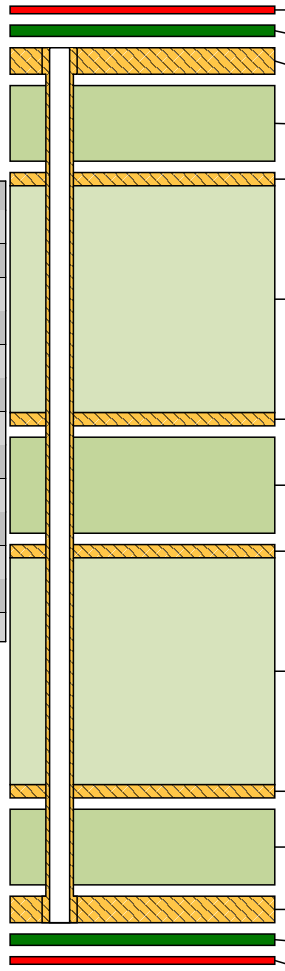
Drill Table

| Symbol | Count | Hole Size | Plated | Hole Tolerance |
|---|---|---|---|---|
| ⧈ | 8 | 8.00mil(0.203mm) | Plated | |
| ▽ | 879 | 10.00mil(0.254mm) | Plated | |
| ◎ | 2 | 11.81mil(0.300mm) | Plated | |
| ⛝ | 2 | 19.69mil(0.500mm) | Plated | |
| ✣ | 4 | 27.56mil(0.700mm) | Plated | |
| □ | 4 | 31.50mil(0.800mm) | Plated | |
| ✡ | 28 | 35.43mil(0.900mm) | Plated | |
| ☆ | 8 | 40.16mil(1.020mm) | Plated | |
| ✡ | 4 | 66.93mil(1.700mm) | Plated | |
| ○ | 4 | 108.27mil(2.750mm) | Plated | |
| ◇ | 2 | 118.11mil(3.000mm) | Plated | |
| ⛝ | 4 | 125.98mil(3.200mm) | Plated | +/-0.00mil(0.000mm) |
| | 949 Total | | | |

Layer Stack Legend



| Layer | Thickness | Type | Gerber | Df | Dk |
|---|---|---|---|---|---|
| Top Overlay | | Legend | GTO | | |
| Top Mask | 0.59mil(0.015mm) | Solder Mask | GTS | | 3.8 |
| Top Copper | 1.38mil(0.035mm) | Signal | GTL | | |
| | *3.94mil(0.100mm)* | *Dielectric* | | | *4.05* |
| Signal Layer 1 | 0.69mil(0.018mm) | Signal | G1 | | |
| | *22.24mil(0.565mm)* | *Dielectric* | | | *4.5* |
| Signal Layer 2 | 0.69mil(0.018mm) | Signal | G2 | | |
| | *5.00mil(0.127mm)* | *Dielectric* | | | *4.25* |
| Signal Layer 3 | 0.69mil(0.018mm) | Signal | G3 | | |
| | *22.24mil(0.565mm)* | *Dielectric* | | | *4.5* |
| Signal Layer 4 | 0.69mil(0.018mm) | Signal | G4 | | |
| | *3.94mil(0.100mm)* | *Dielectric* | | | *4.05* |
| Bottom Copper | 1.38mil(0.035mm) | Signal | GBL | | |
| Bottom Mask | 0.59mil(0.015mm) | Solder Mask | GBS | | 3.8 |
| Bottom Overlay | | Legend | GBO | | |

Total thickness: 64.06mil(1.627mm)

| | |
|---|---|
| Title: ***DD2088PoE_Daisy_Chain*** | LUXonjs |
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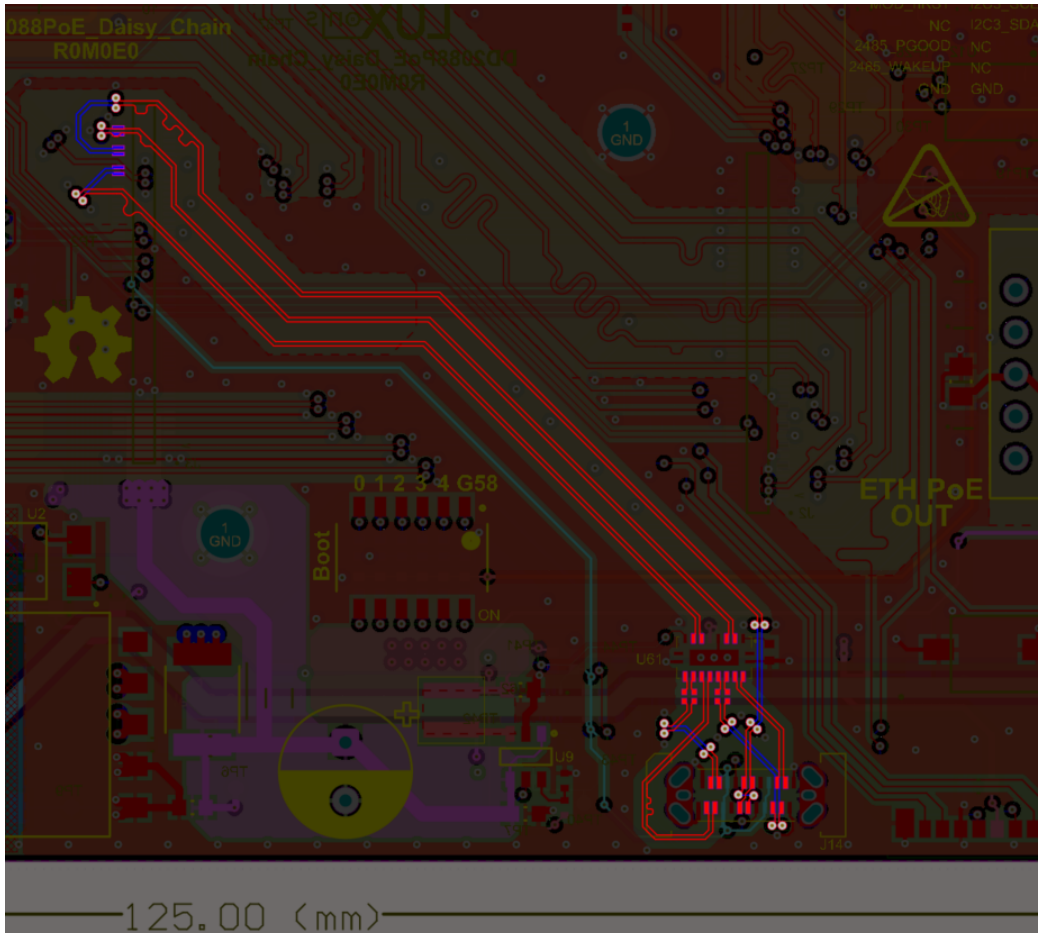
**90 OHM (+/-10%) DIFF PAIRS**

USB differential pairs




Transmission Line Structure Table

| Target Impedance | Calculated Impedance | Trace layer | Lower Trace Width | Upper Trace Width | Gap | Reference layers |
|---|---|---|---|---|---|---|
| 90 | 92.83 | Top Copper | 5.1mil(0.130mm) | 5.1mil(0.130mm) | 5.1mil(0.130mm) | Signal Layer 1 |
| 90 | 92.83 | Bottom Copper | 5.1mil(0.130mm) | 5.1mil(0.130mm) | 5.1mil(0.130mm) | Signal Layer 4 |

| | |
|---|---|
| Title: ***DD2088PoE_Daisy_Chain*** | LUXonjs |
| Number: Revision: R0M0 E0 | |
| Date: 18-May-21 Sheet: 3 of 4 | PROPRIETARY AND CONFIDENTIAL |
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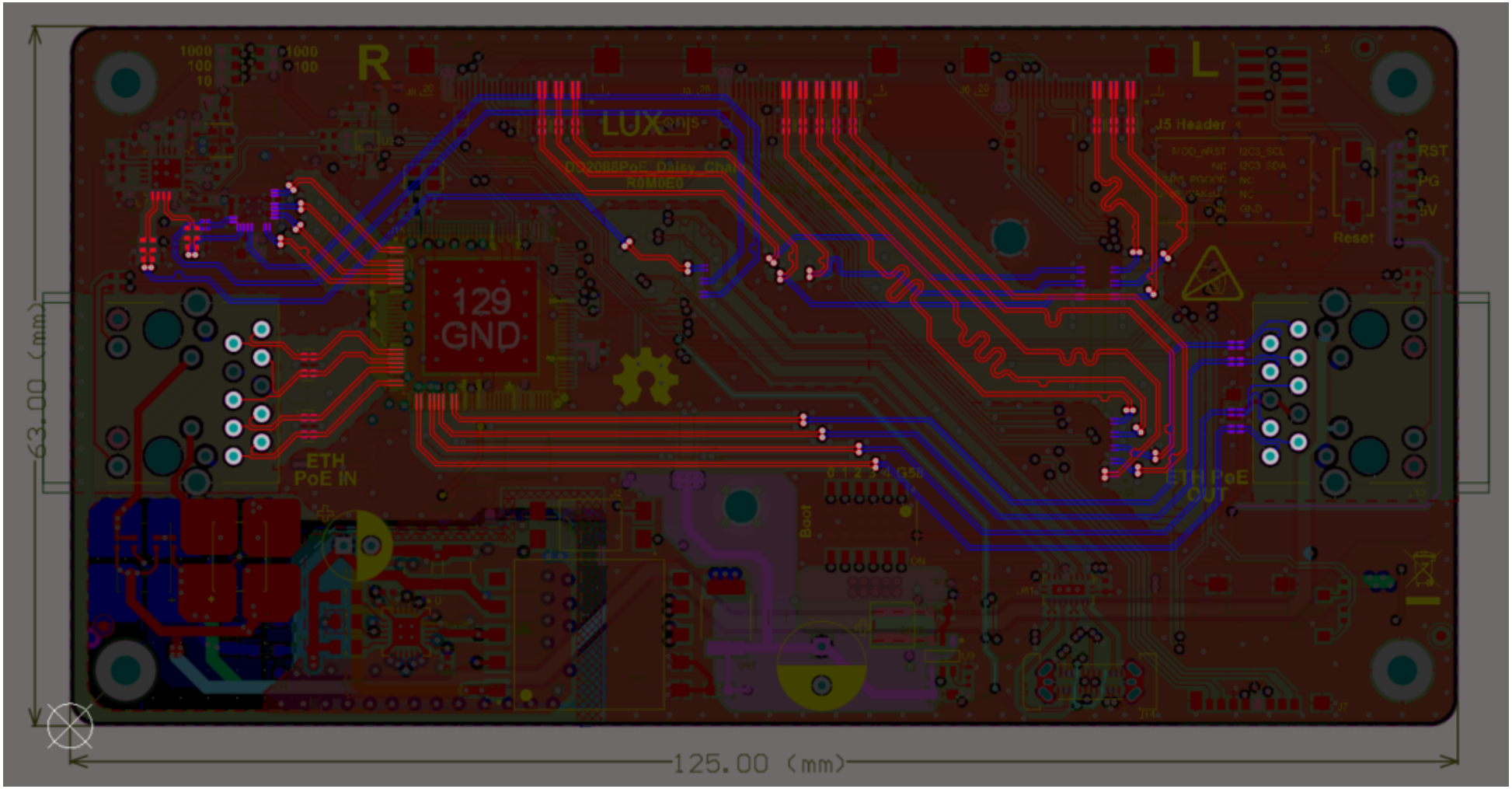
**100 OHM (+/-10%) DIFF PAIRS**




Transmission Line Structure Table

| Target Impedance | Calculated Impedance | Trace layer | Lower Trace Width | Upper Trace Width | Gap | Reference layers |
|---|---|---|---|---|---|---|
| 100 | 100.02 | Top Copper | 5.1mil(0.130mm) | 5.1mil(0.130mm) | 7.7mil(0.195mm) | Signal Layer 1 |
| 100 | 100.02 | Bottom Copper | 5.1mil(0.130mm) | 5.1mil(0.130mm) | 7.7mil(0.195mm) | Signal Layer 4 |

| | |
|---|---|
| Title: ***DD2088PoE_Daisy_Chain*** | LUXonjs |
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