

A

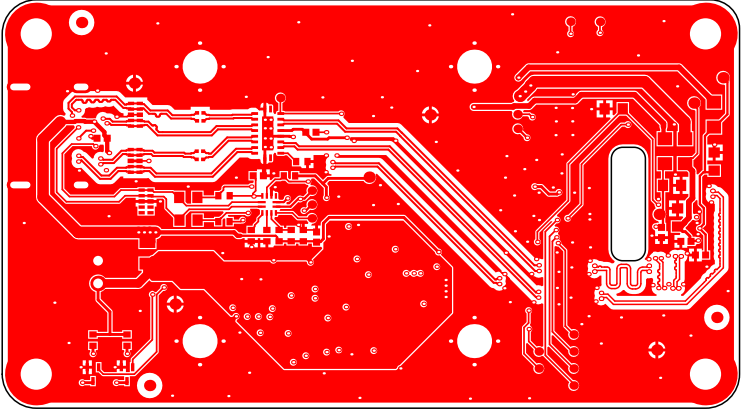
B

C

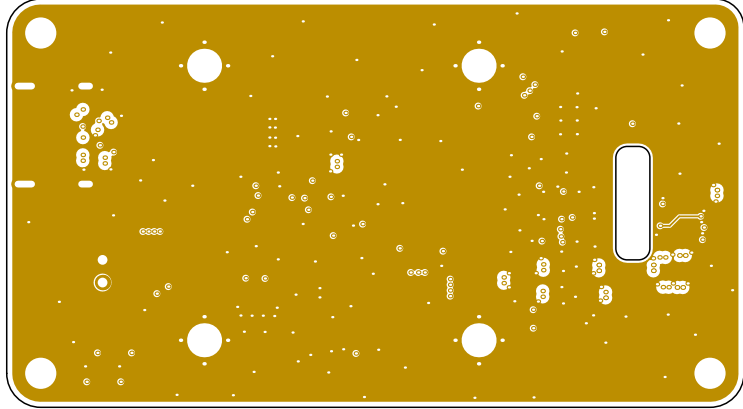
D

E

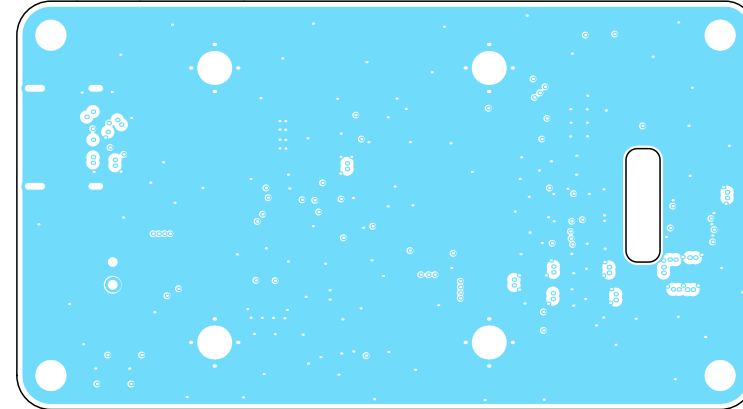
Top Layer (Scale 3:2)



Midlayer 1 (Scale 3:2)



Midlayer 2 (Scale 3:2)



FABRICATION NOTES:

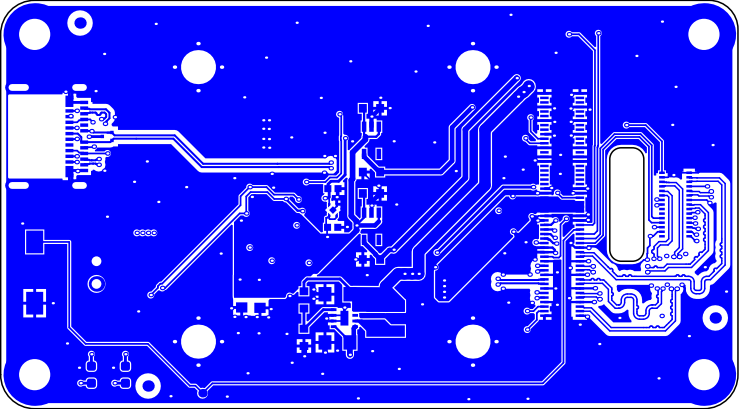
Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

PCB has 4 copper layers
Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
PCB thickness: 63mil +/- 3mil
Min. trace width/clearance: 4/4mil
Min. hole drill/ring: 8mil/16mil
Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
Silkscreen, non-conductive epoxy ink, color: white
Clip silkscreen as needed to prevent deposition on any exposed copper
Surface finish: ENIG
Hole dimensions are finished size, +/-3mil
Linear board dimension tolerance: +/-10mil
Bow, twist, warp not to exceed 0.75% of greatest diagonal span
PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Bottom Layer (Scale 3:2)



Title: BK1096	
Number: D000BK1096	Revision: R0M0 E0
Date: 10/3/2019	Sheet: 1 of 3
Drawn by: Blaž Kvas	

LUXonjs

PROPRIETARY AND CONFIDENTIAL
THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF LUXONIS HOLDING CORPORATION. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION IS PROHIBITED.

A

B

C

D

E

Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Solder	0.70mil(0.02mm)	Solder Mask	GTS	0.03	4
Top Layer	1.38mil(0.03mm)	Signal	GTL		
	7.87mil(0.20mm)	Dielectric		0.02	4.6
Midlayer 1	0.71mil(0.02mm)	Signal	G1		
	41.93mil(1.06mm)	Dielectric		0.02	4.6
Midlayer 2	0.71mil(0.02mm)	Signal	G2		
	7.87mil(0.20mm)	Dielectric		0.02	4.6
Bottom Layer	1.38mil(0.03mm)	Signal	GBL		
Bottom Solder	0.70mil(0.02mm)	Solder Mask	GBS	0.03	4
Bottom Overlay		Legend	GBO		
Total thickness: 63.25mil(1.61mm)					

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◇	133	7.87mil	Plated	None
☆	130	8.00mil	Plated	None
⊕	16	12.00mil	Plated	None
◇	4	23.62mil	Plated	None
⊗	2	33.86mil	Plated	None
○	4	108.27mil	Plated	None
□	4	118.11mil	Non-Plated	None
293 Total				

Title: **BK1096**

Number: D000BK1096 Revision: R0M0
E0

Date: 10/3/2019 Sheet: 2 of 3

Drawn by: Blaž Kvas

LUXonjs

PROPRIETARY AND CONFIDENTIAL

THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF LUXONIS HOLDING CORPORATION. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION IS PROHIBITED.

A

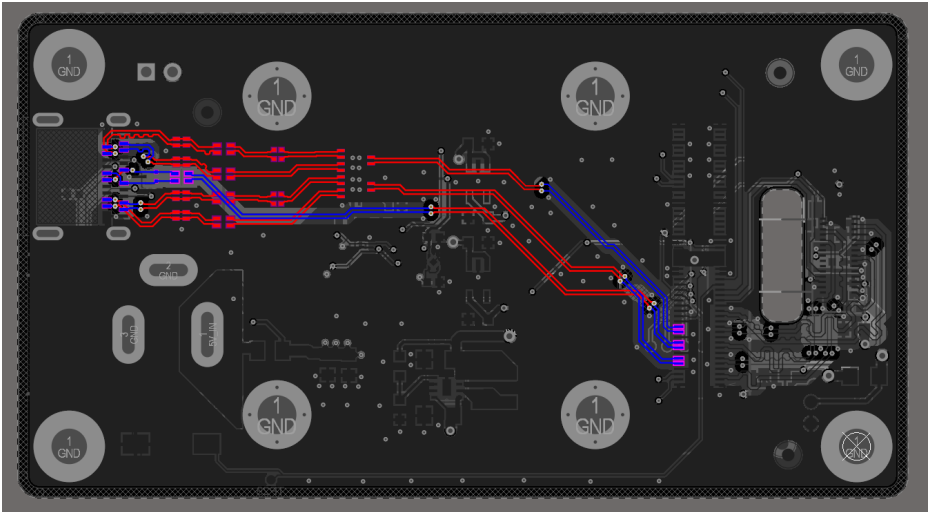
B

C

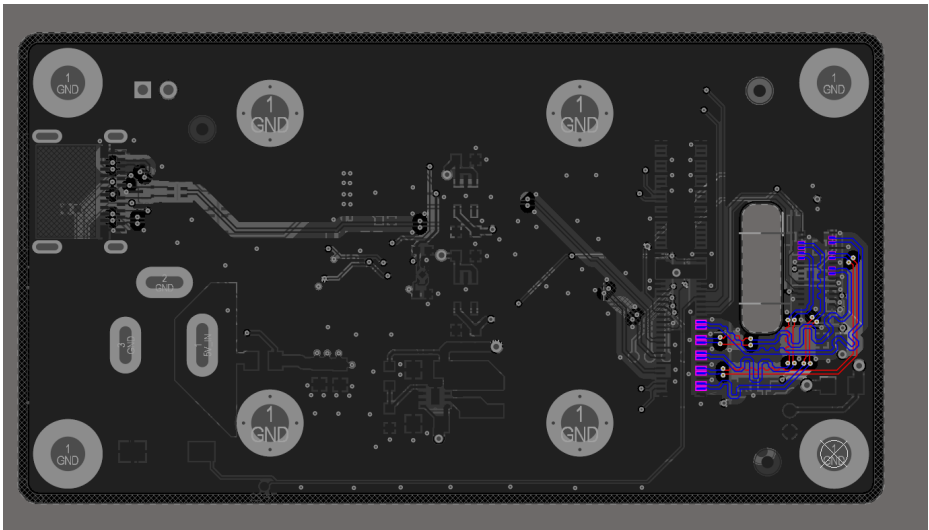
D

E

90 OHM (+/-10%) DIFF PAIRS



100 OHM (+/-10%) DIFF PAIRS



Transmission Line Structure Table

Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Trace Width	Gap	Reference layers
Edge-Coupled Coated Microstrip	90	89.99	Top Layer	0.18mm	0.11mm	Midlayer 1
Edge-Coupled Coated Microstrip	100	99.97	Top Layer	0.18mm	0.17mm	Midlayer 1
Edge-Coupled Coated Microstrip	90	89.99	Bottom Layer	0.18mm	0.11mm	Midlayer 2
Edge-Coupled Coated Microstrip	100	99.97	Bottom Layer	0.18mm	0.17mm	Midlayer 2

Title: BK1096	Revision: R0M0 E0
Number: D000BK1096	
Date: 10/3/2019	Sheet: 3 of 3
Drawn by: Blaž Kvas	



PROPRIETARY AND CONFIDENTIAL

THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF LUXONIS HOLDING CORPORATION. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION IS PROHIBITED.

A

B

C

D

E