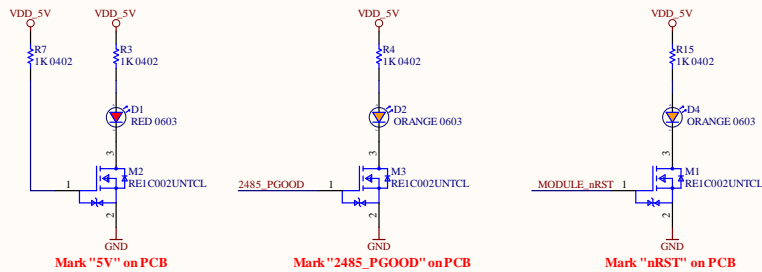


Project: *DM1098FFC*
Current Revision: *R0M0E0*

DM1098FFC Revision History:

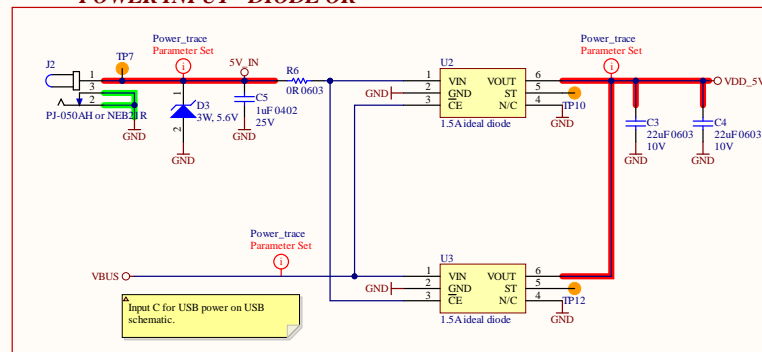
Date	Revision	Reason for Change	Changes Implemented
11/29/2019	R0M0E0 -> R1M1E1	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Standardize FFC connector alignment with edge of board when connector is closed 3) Existing design was not standardized on LuxonisMaster library format	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names. Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Moved each of the FFC connectors toward the board edge so that they are flush with edge when closed. 3) Updated schematic and component information to align with LuxonisMaster library system
8/3/2020	R1M1E1 -> R1M1E2	1) Shutter sync updated to ext_sirb	1) Removed R9, R14 (PN CRCW06030000Z0EA), added R10, R12 (PN CRCW06030000Z0EA)
12/28/2020	R1M1E2 -> R0M0E0	1) ESD protection 2) FFC connector stronger mechanics 3) Updating board with overvoltage protection and ideal diode to or USB VBUS and barrel jack 5V 4) Outdated stack 5) Unused reset circuit 6) Unused strobe configuration resistors	1) Added protection diodes to MIPI lines 2) Changed FFC with Molex 505278 series 3) Added ideal diodes and zener diode for protection 4) Standardized 4L stackup rerouted all differential pairs and tuned lengths 5) Deleted reset circuit and its components and rerouted signals 6) Deleted strobe configuration resistors with corresponding silk and tracks

Title <i>DM1098FFC</i>			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234		Cannot open file C:\Users\Brian.Luxonis\Documents\DM1098FFC.dwg
Size: <i>Tabloid</i>	Number: <i>D0000190</i>	Revision: <i>R0M0E0</i>			
Date: <i>4.01.2021</i>	Time: <i>17:58:44</i>	Sheet <i>1</i> of <i>5</i>	<i>United States</i>		
Drawn by: <i>David Malovich</i>					

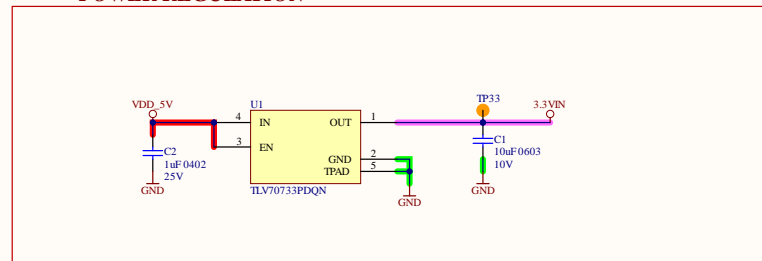


2485_PG00D and MODULE_nRST both have pull ups to 1.8V on 1099 module. 2485_PG00D is held low by open-drain output on 1099 PMIC until power is good. MODULE_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.

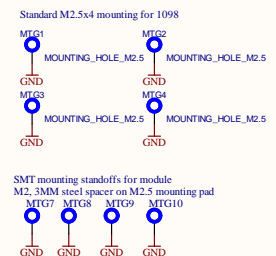
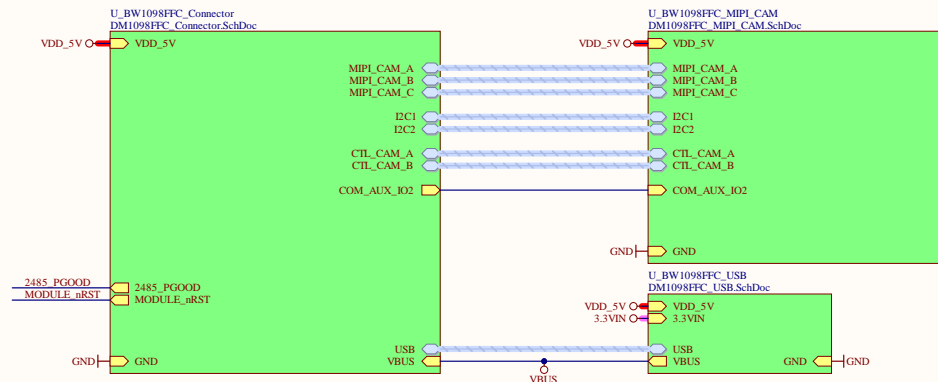
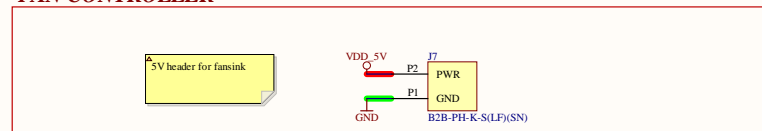
POWER INPUT - DIODE OR



POWER REGULATION



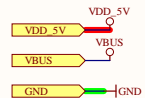
FAN CONTROLLER



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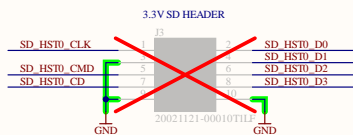
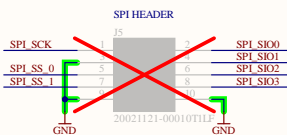
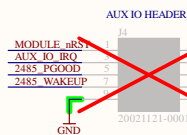
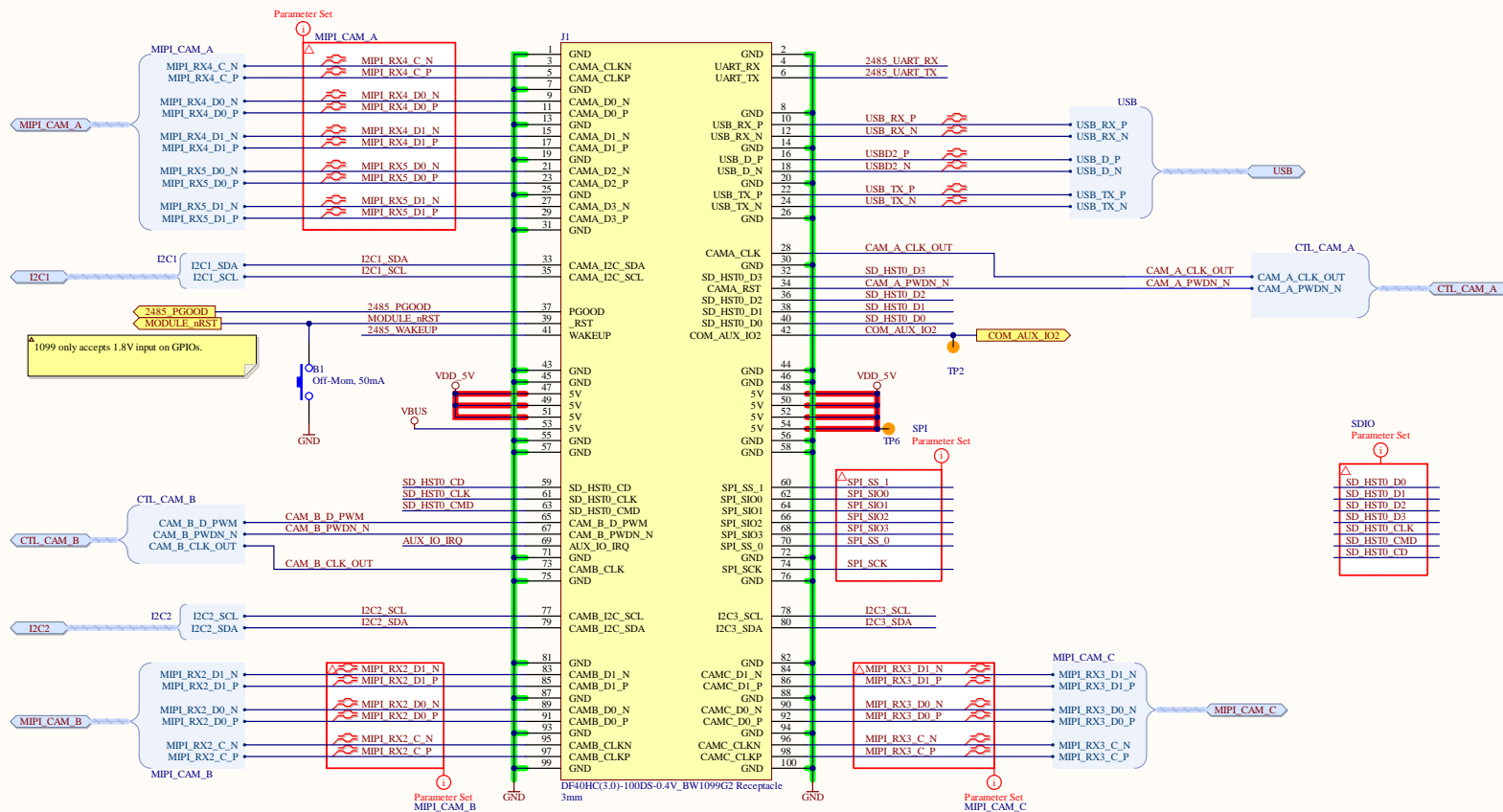


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Drawn by: David Malovich					



VDD_5V drawn by BW1099 can be up to 1A
VBUS on BW1099 is only sense input

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane



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MA2x8x Naming

IMX378 Naming

RGB
IMX378

J6

MP2

TOP CONTACT

MP1

CONN FEC TOP 26POS 0.50MM R/A
WM24290CT-ND

MA2x8x Pins:

- MIPI RX5_D0_P
- MIPI RX5_D0_N
- MIPI RX4_D0_P
- MIPI RX4_D0_N
- MIPI RX4_C_P
- MIPI RX4_C_N
- MIPI RX4_D1_P
- MIPI RX4_D1_N
- MIPI RX5_D1_P
- MIPI RX5_D1_N
- CAM_A_CLK_OUT
- CAM_A_PWD_N
- I2C1_SDA
- I2C1_SCL

IMX378 Pins:

- MIPI D2_P
- MIPI D2_N
- MIPI D0_P
- MIPI D0_N
- MIPI C_P
- MIPI C_N
- MIPI D1_N
- MIPI D1_P
- MIPI D3_P
- MIPI D3_N
- CAM_CLK
- CAM_RST
- I2C1_SDA
- I2C1_SCL
- AUX_IO1
- AUX_IO2
- VDD_5V_O

Legend:

- MIPI CAM A
- CTL CAM A
- I2C1

Note: keep 100 ohm diff. Impedance on MIPI lanes

Note: AUX_IO1/2 are not used on the BG0249, and on this design, their original source GPIO pins have been repurposed for a different output (SPI2).

D5

CAM L D0 P	1	I01	NC	10	CAM L D1 P
CAM L D1 N	2	I02	NC	9	CAM L D1 N
	3	GND	GND	8	
STEREO CLK	4	I03	NC	7	STEREO CLK
FSIN1	5	I04	NC	6	FSIN1

TPD4E02B04DQAR

D6

MIPI D2 P	1	I01	NC	10	MIPI D2 P
MIPI D2 N	2	I02	NC	9	MIPI D2 N
	3	GND	GND	8	
MIPI D0 N	4	I03	NC	7	MIPI D0 N
MIPI D0 N	5	I04	NC	6	MIPI D0 N

TPD4E02B04DQAR

D7

CAM L D0 P	1	I01	NC	10	CAM L D0 P
CAM L D0 N	2	I02	NC	9	CAM L D0 N
	3	GND	GND	8	
CAM L C P	4	I03	NC	7	CAM L C P
CAM L C N	5	I04	NC	6	CAM L C N

TPD4E02B04DQAR

D8

MIPI C P	1	I01	NC	10	MIPI C P
MIPI C N	2	I02	NC	9	MIPI C N
	3	GND	GND	8	
MIPI D1 N	4	I03	NC	7	MIPI D1 N
MIPI D1 P	5	I04	NC	6	MIPI D1 P

TPD4E02B04DQAR

D9

CAM R D0 P	1	I01	NC	10	CAM R D0 P
CAM R D0 N	2	I02	NC	9	CAM R D0 N
	3	GND	GND	8	
CAM R C P	4	I03	NC	7	CAM R C P
CAM R C N	5	I04	NC	6	CAM R C N

TPD4E02B04DQAR

D10

MIPI D3 P	1	I01	NC	10	MIPI D3 P
MIPI D3 N	2	I02	NC	9	MIPI D3 N
	3	GND	GND	8	
CAM_RST	4	I03	NC	7	CAM_RST
CAM_CLK	5	I04	NC	6	CAM_CLK

TPD4E02B04DQAR

D11

CAM R D1 P	1	I01	NC	10	CAM R D1 P
CAM R D1 N	2	I02	NC	9	CAM R D1 N
	3	GND	GND	8	
STEREO CLK	4	I03	NC	7	STEREO CLK
FSIN2	5	I04	NC	6	FSIN2

TPD4E02B04DQAR

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