Project: ***BW1097***
Current Revision: ***R2M2E3***

BW1097 Revision History:

Date	Revision	Reason for Change	Changes Implemented
8/2/2019	R0M0E0 -> R0M0E1	1) In Bom (Line 63 & 66), R28, R31, R32, R33, R35, R37 &R34, R36. Your PCB soldering pad is 0402 designed, but your Bom list in 0603 parts. 2) (Line 88) X1, ABM3B-25. It seems your PCB solder pad too small. 3) R48 was mistakenly placed as an 0402, but should have been an 0603.	1) Updated parts R28, R31, R32, R33, R35, R37 to 0402 parts with the same characteristics (10k 1%), and updated R35 and R27 to 0402 parts with same characteristics (0R) 2) Updated X1 to be either Epson FA-20H 25.0000MD30Y-C5 or TXC 8Z-25.000MAAJ-T, both of which are 2.5x2.0mm 3) Updated R48 with part of same characteristics, but in 0402 package. 4) Downsized the layout, making phsyical changes to the PCB, component, and mechnical locations.
8/30/2019	R0M0E1 -> R1M1E2	1) Power LED does not turn on, even though power is good. 2) MIC2026-2 was incorrectly used where MIC2026-1 should have been used. 3) RJ-45 connector footprint was wrong, preventing Ethernet from working. 4) Original BW1097 too large. 5) Audio buffer wrong component. Needs to be NC7WZ16P6X. 6) Existing barrel jack does not work well with reduced form factor PCBA due to large thru-holes interfering with SODIMM 7) Want to allow 4th USB port of LAN9514 to be routed to 4pin header as option for end users 8) Audio Left/Right outputs have wrong polarity 9) SDA/SCL lines for CM3 DSI/CSI are swapped 10) BW1099 Reset functionality needed for debug and end users, accessible from BW1097 board. 11) Vertical RaspPi CSI/DSI connectors are difficult to work with when flex is inserted and PCB is laying flat on table 12) Fansink for BW1099 will need 5V power from baseboard	1) Add 10k pull up to PGOOD 2) Replace MIC2026-2 with MIC2026-1 (changes on schematic and BOM) 3) Corrected RJ-45 footprint so that correct pins/nets are at the correct positions. 4) Form factor of PCBA minimized 5) Created new component for NC7WZ16P6X and added to schematic. No change to footprint (SC-70). 6) Added CUI PJ-036AH-SMT as new 5V barrel jack input 7) Added 4 pin, 0.100" pitch header to support auxiliary USB port (Port 5, LAN9514), along with 0R resistor connecting USB_AUX_VBUS directly to 5V. 8) Swapped polarity of L/R channels on AV schematic 9) Swapped polarity of SCL/SDA on SODIMM schematic 10) Added user button to press to put 1099 into RST, and added an open drain FET, controlled by CM3 GPIO33 (GPIO33 high -> 1099 RST) 11) Vertical CSI/DSI connectors removed, and right-angle FFC connectors added 12) Added JST connector for 5V fansink power
11/29/2019	R1M1E2 -> R2M2E3	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Header jumpers are unnecesary and expensive, and can be repalced with a simpler solution 3) Existing design was not standardized on LuxonisMaster library format 4) Series input power resistor is a sense resistor, but should be 0 ohm 5) The OV9282 LDOs have unncessary components compared to the most recent baseboards 6) Depopped R26 had no set component value. 7) HDMI connector footprint was found to be slightly crooked 8) PGOOD LED driver did not match other boards 9) DMG1012 FETs were automotive qualified, changed to non-automotive for entry into LuxonisMaster 10) Passive component equivalent part substitions as library was built up	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names, Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Removed header jumpers and exchanged with resistor jumper networks 3) Updated schematic and component information to align with LuxonisMaster library system. 4) Changed input series resistor to 0603 0ohm to match 1098OBC, 1098FFC, and 1094. 5) Removed RC circuit on OV9282 LDOs to match 1098OBC 6) Added 47K as default, but R26 remains depopulated 7) Corrected HDMI footprint to match recommended PCB layout from Wurth 685119134923 8) Changed transistor on PGOOD LED to be RE1C002UNTCL, to match other boards (Q5) 9) Changed from DMG1012TG-7 to DMG1012T-7 (Q1, Q2, Q3, Q4, Q6) 10) Many passive components did not exist in LuxonisMaster, so in some cases, equivalent from a different manufacturer are used. For 332R and 100K resistors, all were standardized to 0402, rather than a mix of sizes.

Title ***BW1097***				*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
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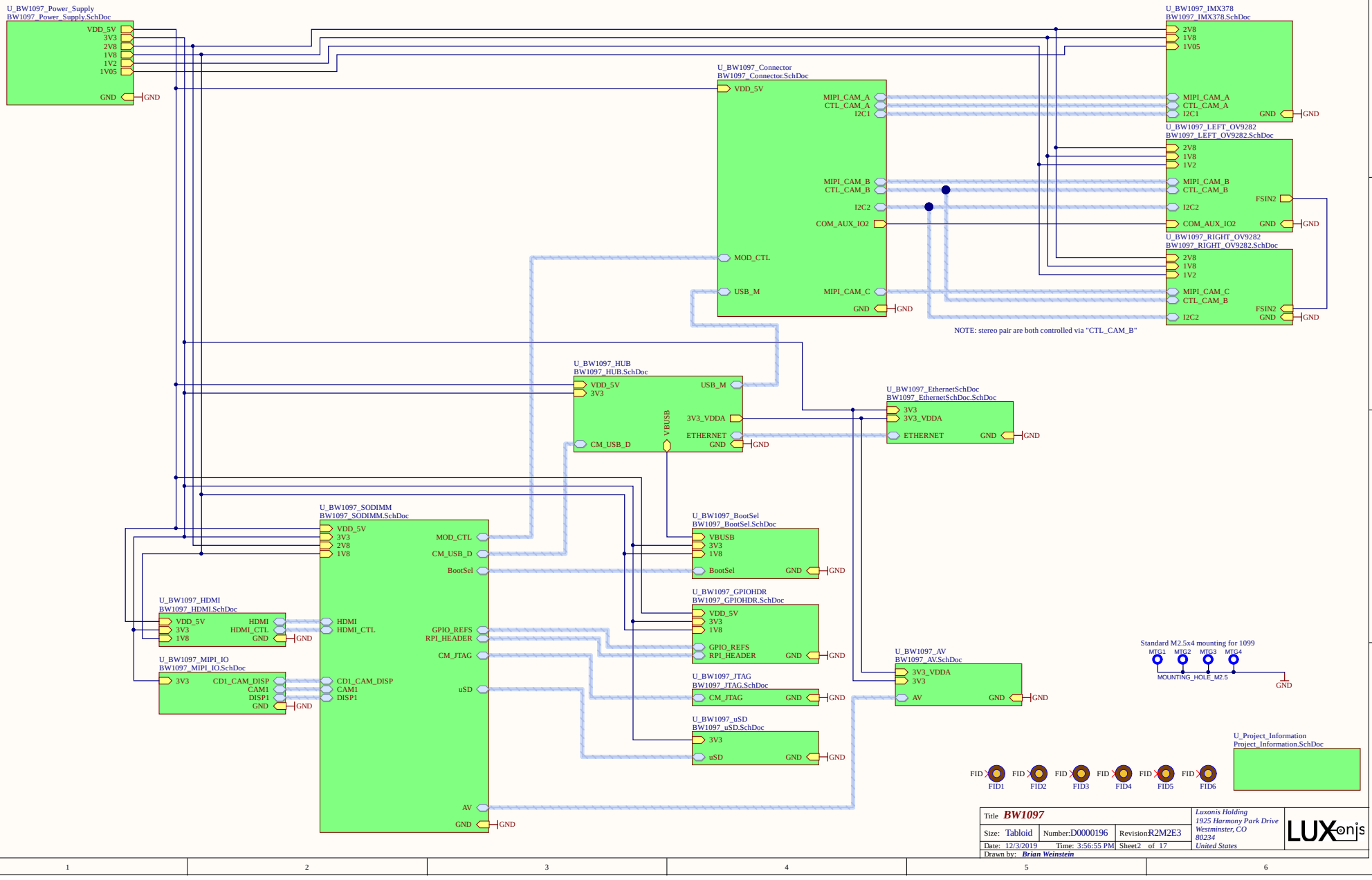
Drawn by: ***Brian Weinstein***				



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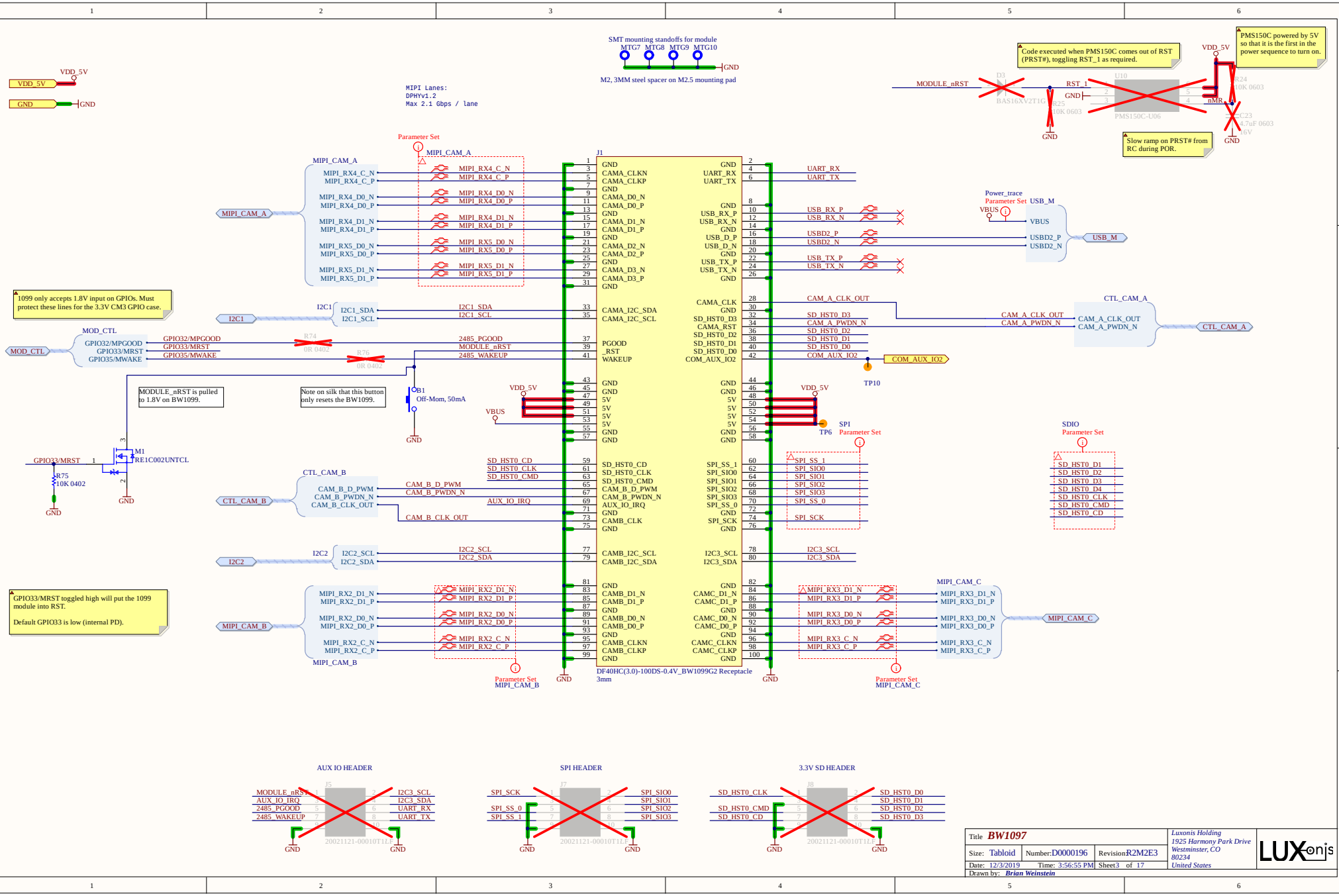
SMT mounting standoffs for module
MTG7 MTG8 MTG9 MTG10
GND
M2, 3MM steel spacer on M2.5 mounting pad
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane
Code executed when PMS150C comes out of RST (PRST#), toggling RST_1 as required.
PMS150C powered by 5V so that it is the first in the power sequence to turn on.
Slow ramp on PRST# from RC during POR.
MODULE_nRST
RST_1
PMS150C-U06
VDD_5V
GND
Parameter Set
MIPI_CAM_A
J1
DF40HC(3.0)-100DS-0.4V_BW1099G2 Receptacle
3mm
1099 only accepts 1.8V input on GPIOs. Must protect these lines for the 3.3V CM3 GPIO case.
MOD_CTL
GPIO32/MPGOOD
GPIO33/MRST
GPIO35/MWAKE
R74
0R 0402
R76
0R 0402
2485_PGOOD
MODULE_nRST
2485_WAKEUP
MODULE_nRST is pulled to 1.8V on BW1099.
Note on silk that this button only resets the BW1099.
B1
Off-Mom, 50mA
M1
RE1C002UNTCL
R75
10K 0402
I2C1
I2C1_SDA
I2C1_SCL
CTL_CAM_B
CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
AUX_IO_IRQ
I2C2
I2C2_SCL
I2C2_SDA
GPIO33/MRST toggled high will put the 1099 module into RST.
Default GPIO33 is low (internal PD).
MIPI_CAM_B
UART_RX
UART_TX
USB_RX_P
USB_RX_N
USB_M
USBD2_P
USBD2_N
USB_TX_P
USB_TX_N
Power_trace
Parameter Set
VBUS
CAM_A_CLK_OUT
CAM_A_PWDN_N
CTL_CAM_A
COM_AUX_IO2
TP10
TP6
SPI
Parameter Set
SPI_SS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3
SPI_SS_0
SPI_SCK
SDIO
Parameter Set
SD_HST0_D1
SD_HST0_D2
SD_HST0_D3
SD_HST0_D4
SD_HST0_CLK
SD_HST0_CMD
SD_HST0_CD
I2C3_SCL
I2C3_SDA
MIPI_CAM_C
MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P
AUX IO HEADER
SPI HEADER
3.3V SD HEADER
20021121-00010T1LF
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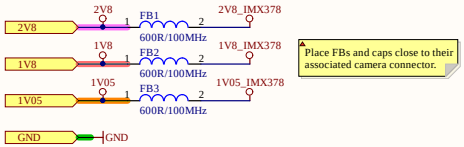
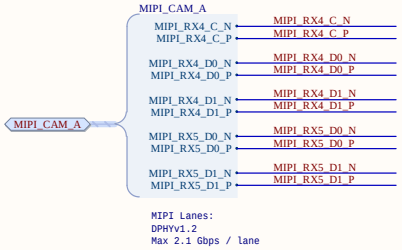
Westminster, CO
80234
United States
LUXonis



Place FBs and caps close to their associated camera connector.

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

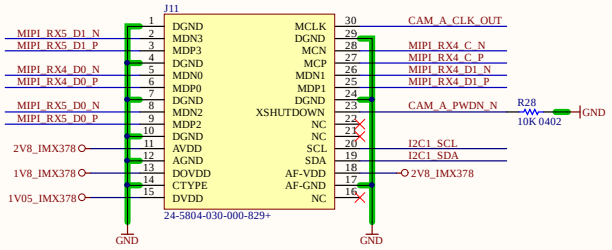
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

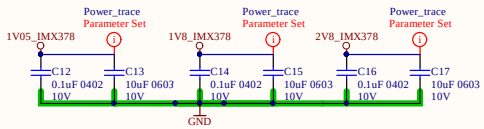


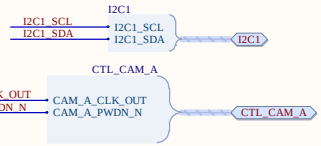
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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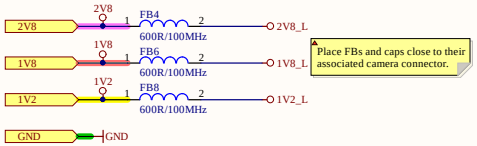
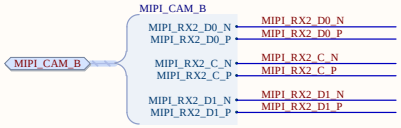
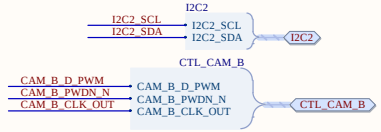


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN81V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

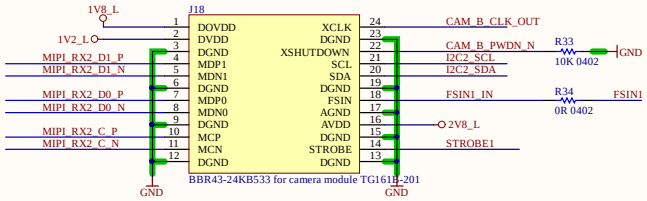
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

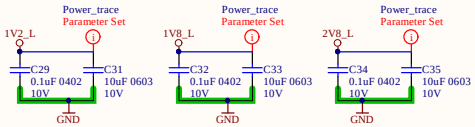


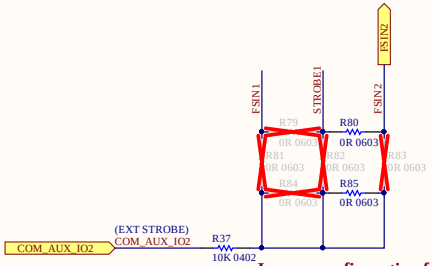


Mark "LEFT" on PCB

Place so that is the module's left camera.







Jumper configuration for FSIN and STROBE pins

PCB NOTE: Add below diagram to the PCB

Supported Modes of Operation

- NO SYNC
- NORMAL
- TIMING MASTER
- TIMING SLAVE

This header is used for configuring the STROBE signal direction between the camera boards by using jumpers. A strobe signal may drive FSIN signal for waking up a sensor from its low power mode. See the "Supported Modes of Operation" note for supported jumper settings.

- "NO SYNC" is the mode in which none of the camera modules is excited by any strobe signal.

- "NORMAL" mode means STROBE mechanism works only among the stereo cameras themselves. In this mode, CAM1 strobe is connected to the CAM2 FSIN input.

- "TIMING MASTER" mode means CAM1 STROBE signal drives the EXT_STROBE signal as well as the CAM2 FSIN input. EXT_STROBE signal circulates among the other camera ports so that one camera module can manage the timing of all cameras within the system.

- "TIMING SLAVE" mode uses external strobe signal which is driven externally by another camera. In this mode, CAM1 and CAM2 are excited by the EXT_STROBE signal.

Note that, at most only one camera can be in the "TIMING MASTER" mode at a time. STROBE generation and FSIN reception should be configured via software.

Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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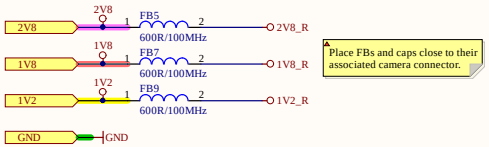
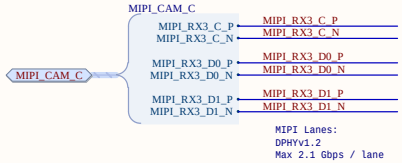


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

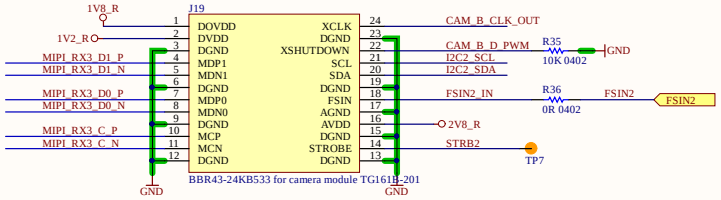
Supply Information

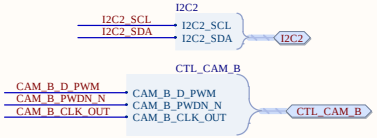
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

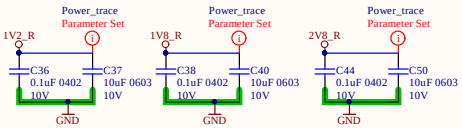


Mark "RIGHT" on PCB

Place so that is the module's right camera.







Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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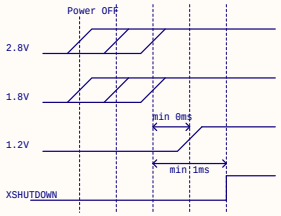
OV9282 POWER REQUIREMENTS

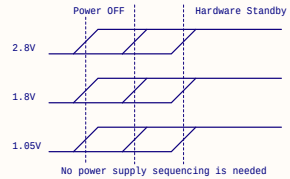


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

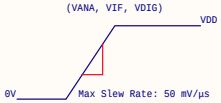
IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

Slew Rate Constraint (VANA, VIF, VDIG)

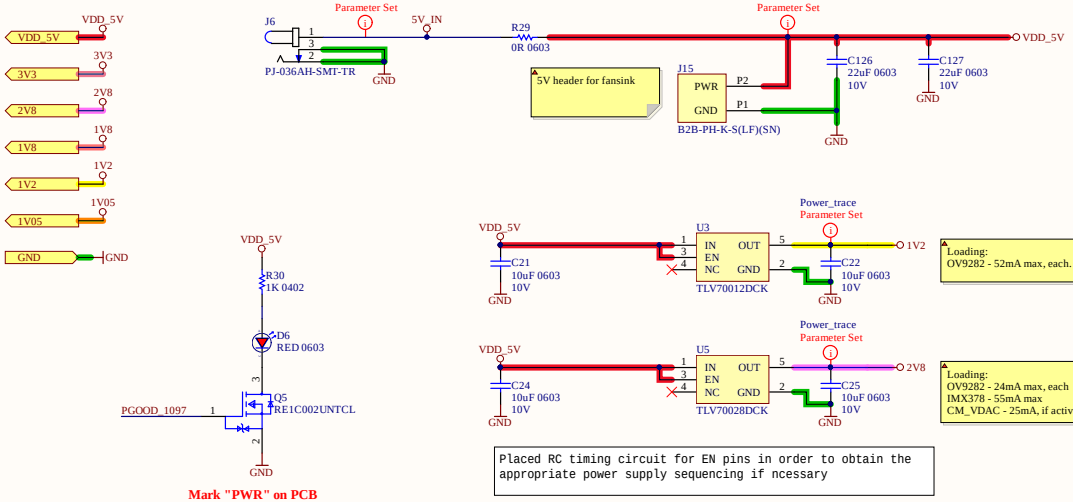


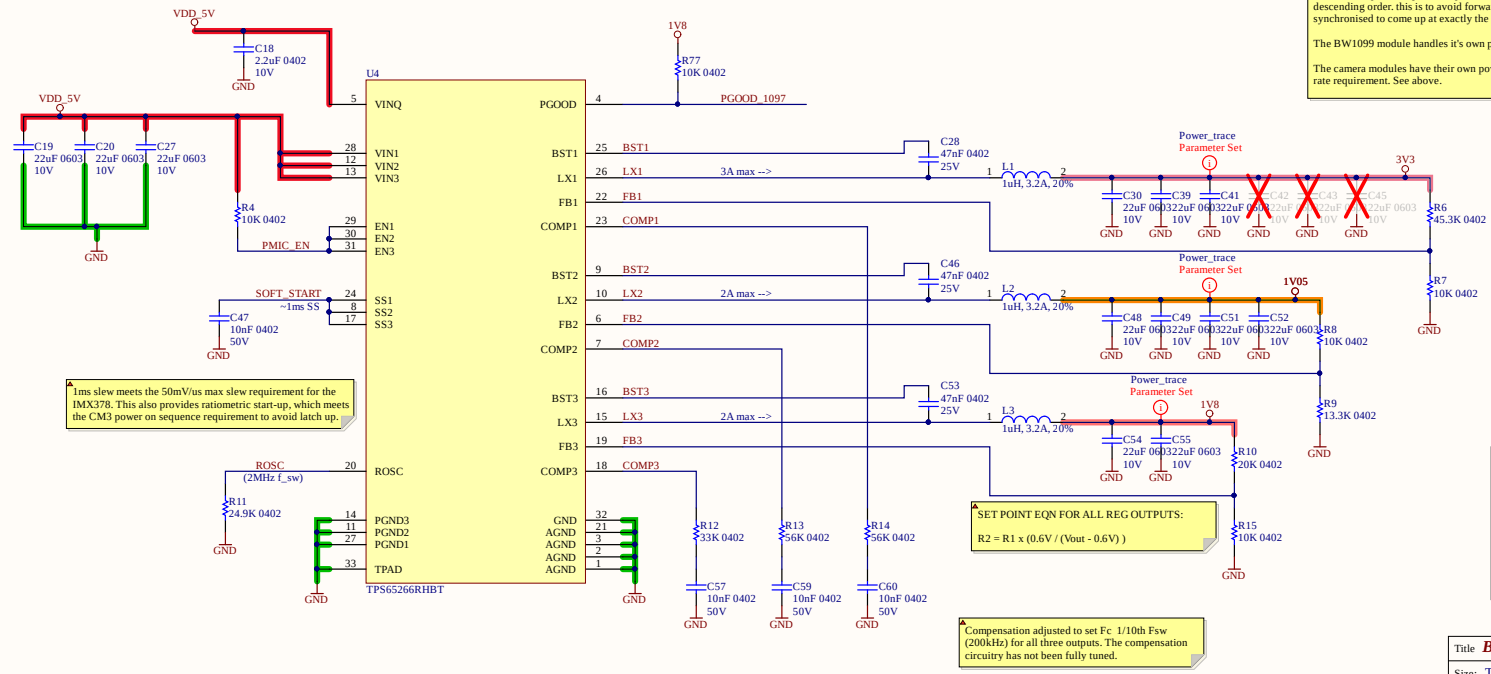
POWER SEQUENCING REQUIREMENTS:

The CM3 requests a power sequence such that, "supplies should be staggered so that the highest voltage comes up first, then the remaining voltages in descending order. this is to avoid forward biasing internal (on-chip) diodes between supplies, and causing latch-up. Alternatively supplies can be synchronised to come up at exactly the same time as long as at no point a lower voltages supply rail exceeeds a higher voltage supply rail."

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.





Effective capacitance targets for each rail, taking into account DC bias and other effects:
3.3V C_eff = 24uF
1.8V C_eff = 26uF
1.05V C_eff = 70uF

Voltage ripple and allowed voltage tolerance on all rails is +/-5%

Load step design assumptions, based on worst case rail loading:
3.3V - 2.5A step
1.8V - 1A step
1.05 - 0.5A step

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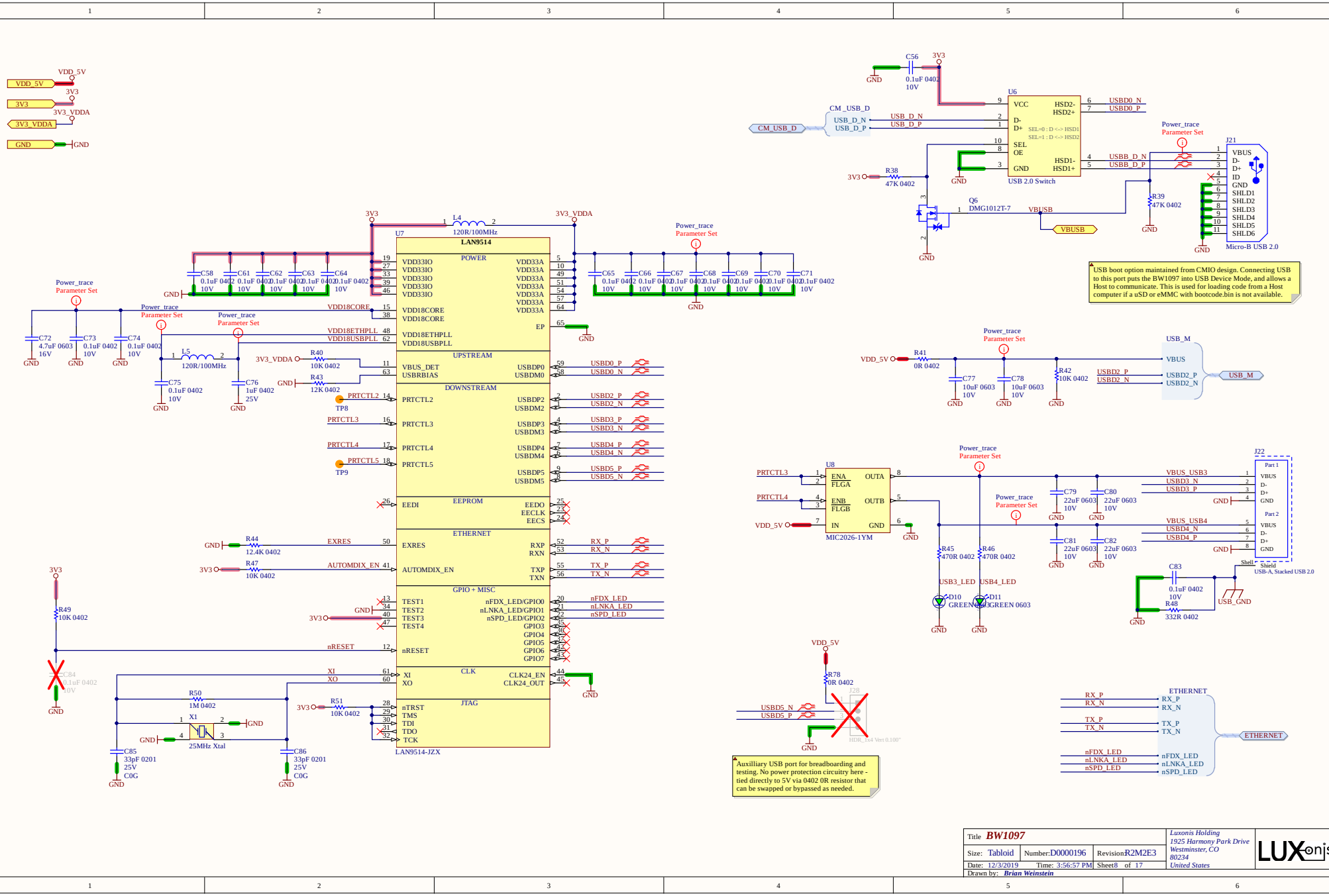

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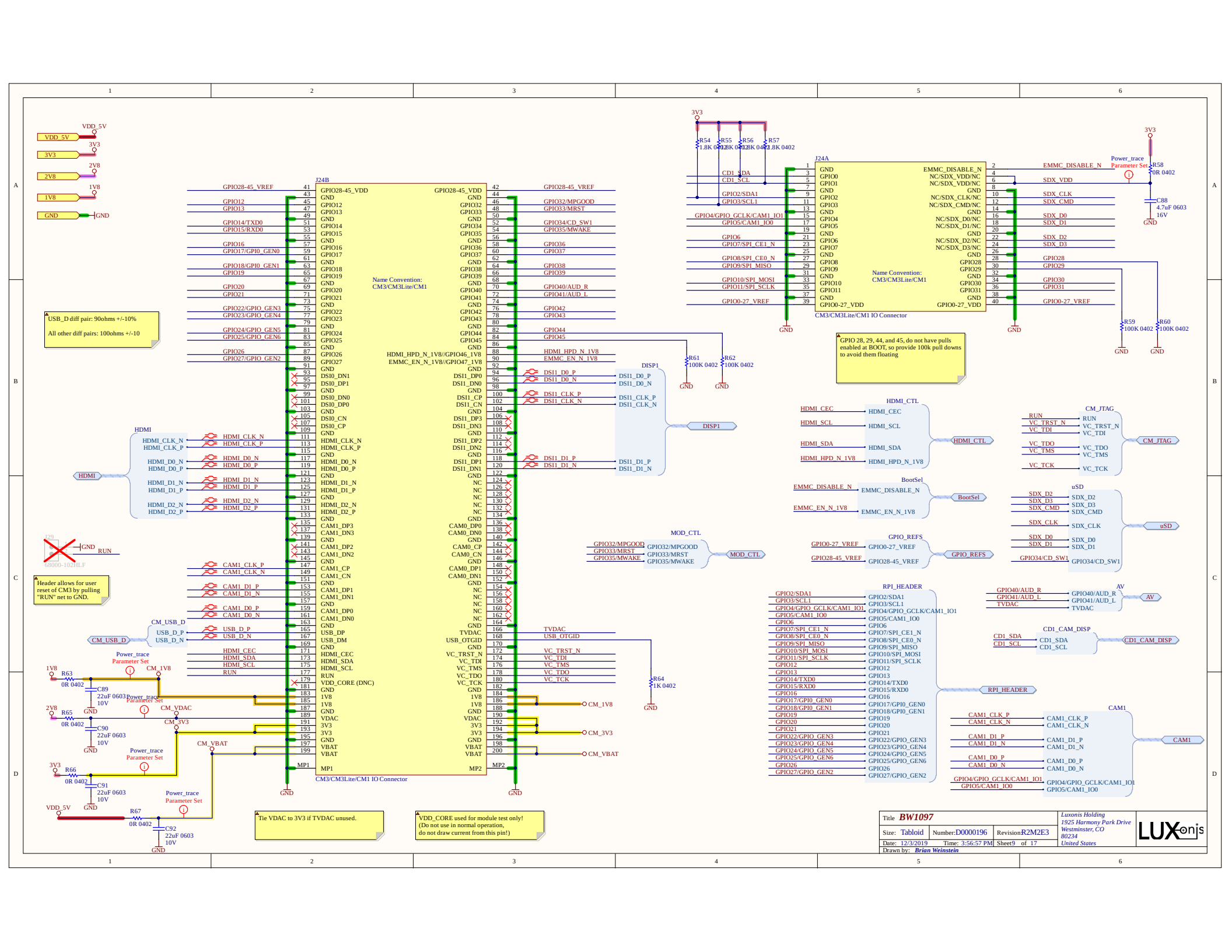
VDD_5V
3V3
2V8
1V8
GND
J24B
CM3/CM3Lite/CM1 IO Connector
Name Convention:
CM3/CM3Lite/CM1
J24A
CM3/CM3Lite/CM1 IO Connector
DISP1
HDMI
HDMI_CTL
CM_JTAG
BootSel
uSD
MOD_CTL
GPIO_REFS
RPI_HEADER
AV
CD1_CAM_DISP
CAM1
CM_USB_D
USB_D_P
USB_D_N
HDMI_CEC
HDMI_SDA
HDMI_SCL
RUN
USB_OTGID
TVDAC
VC_TRST_N
VC_TDI
VC_TMS
VC_TDO
VC_TCK
CM_1V8
CM_3V3
CM_VBAT
CM_VDAC
R54 1.8K 0402
R55 1.8K 0402
R56 1.8K 0402
R57 1.8K 0402
R58 0R 0402
R59 100K 0402
R60 100K 0402
R61 100K 0402
R62 100K 0402
R63 0R 0402
R64 1K 0402
R65 0R 0402
R66 0R 0402
R67 0R 0402
C88 4.7uF 0603 16V
C89 22uF 0603 10V
C90 22uF 0603 10V
C91 22uF 0603 10V
C92 22uF 0603 10V
J29
68000-102HLF
USB_D diff pair: 90ohms +/-10%
All other diff pairs: 100ohms +/-10
GPIO 28, 29, 44, and 45, do not have pulls enabled at BOOT, so provide 100k pull downs to avoid them floating
Header allows for user reset of CM3 by pulling "RUN" net to GND.
Tie VDAC to 3V3 if TVDAC unused.
VDD_CORE used for module test only! (Do not use in normal operation, do not draw current from this pin!)
Power_trace
Parameter Set
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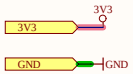
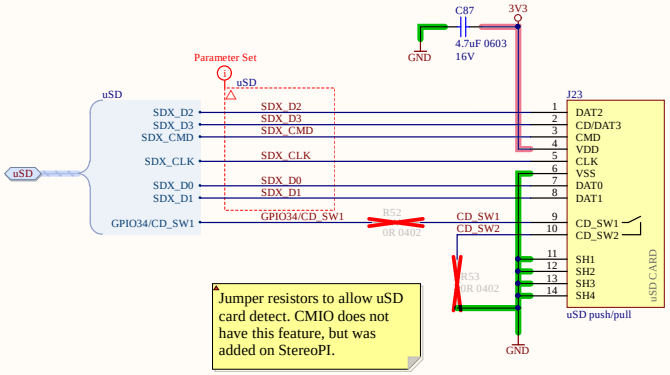
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
LUXonis



CMIO Note:

uSD is only used for modules with no on-board Flash (eMMC)



Jumper resistors to allow uSD card detect. CMIO does not have this feature, but was added on StereoPI.

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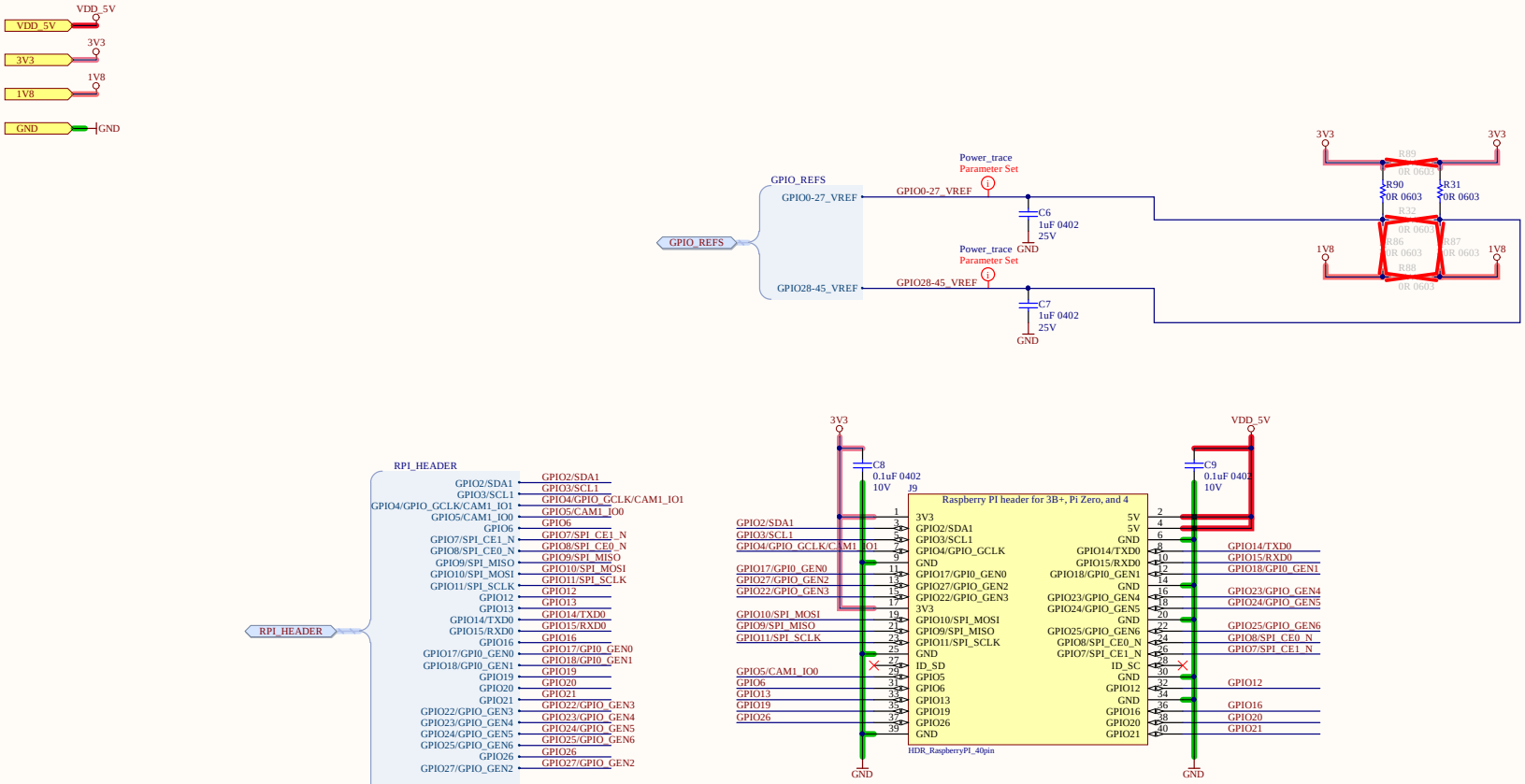

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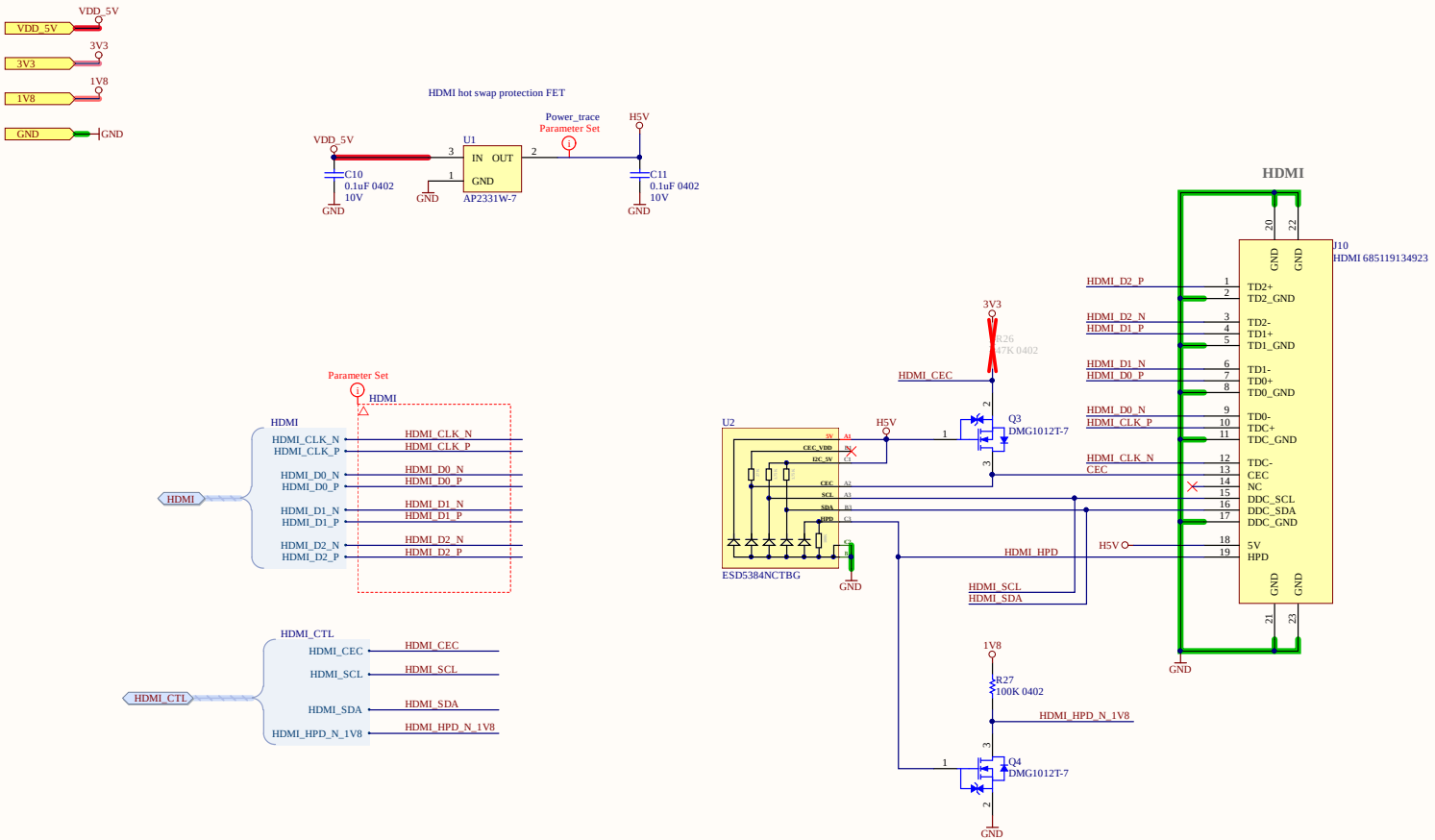

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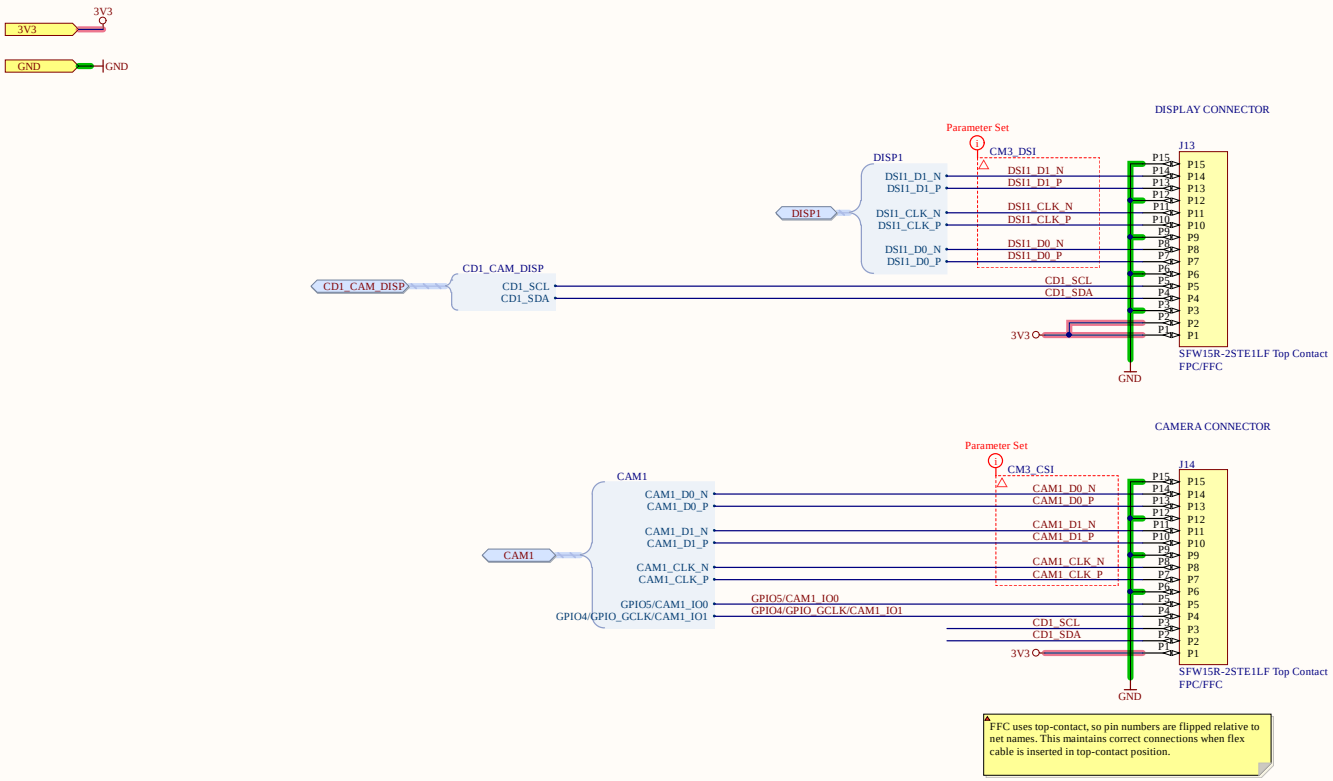

CMIO/CM3 guide for attaching display + camera (https://www.raspberrypi.org/documentation/hardware/computemodule/cmio-display.md) uses:

GPIO0 - CD1_SDA
GPIO1 - CD1_SCL
GPIO4 - CAM1_IO1
GPIO5 - CAM1_IO0

.dts file provided on that guide for this configuration.

NOTES:
(1) GPIO4/GPIO_GCLK and GPIO5 are also broken out to the standard 40-pin, 3B+-style header on this board.
(2) CAM1 and DISP1 are both 4-lane MIPI busses, but the 15-pin connectors only support 2-lane.

The PiCam V2.1 uses only the camera connector Pin 11 (CAM1_IO0) as an Enable pin, so this pin needs to be pulled high by default to enable camera usage, regardless of what GPIO it is connected to.

Both GPIO4 and GPIO5 are weakly pulled up by default in the BCM (see pg. 102 https://www.raspberrypi.org/app/uploads/2012/02/BCM2835-ARM-Peripherals.pdf)

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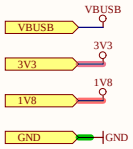
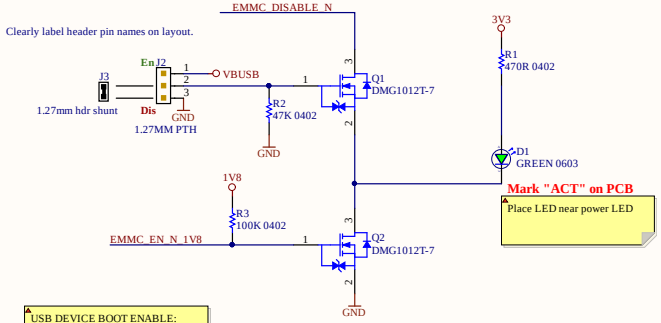


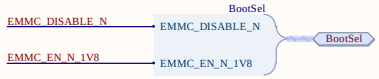
MODULE BOOT OPTIONS:

BCM2835 BootROM boot as USB Device (from Host):
- 3pin hdr set to enable USB Device Boot
- Plug host into micro USB socket (VBUSB=5V)
- EMMC_EN_N_1V8 high at boot (input with 1.8k pullup)
- EMMC_DISABLE_N therefore, LOW
- On power up, BCM283x USB Device Boot SW forces EMMC_EN_N_1V8 to enable access to eMMC

BCM2835 BootROM boot from eMMC:
- Nothing plugged into micro USB socket (VBUSB=0V) *OR* 3pin hdr set to disable USB Boot
- If line above is true, then EMMC_DISABLE_N is HIGH
- On power up, BCM283x boots from eMMC
- EMMC_EN_N_1V8 can be used as a status LED



USB DEVICE BOOT ENABLE:
Jumper positions:
1-2 = ENABLED
2-3 = DISABLED



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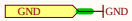

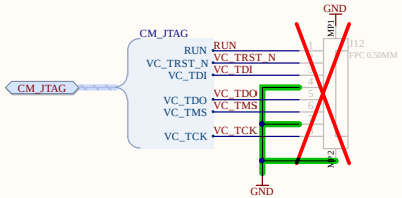

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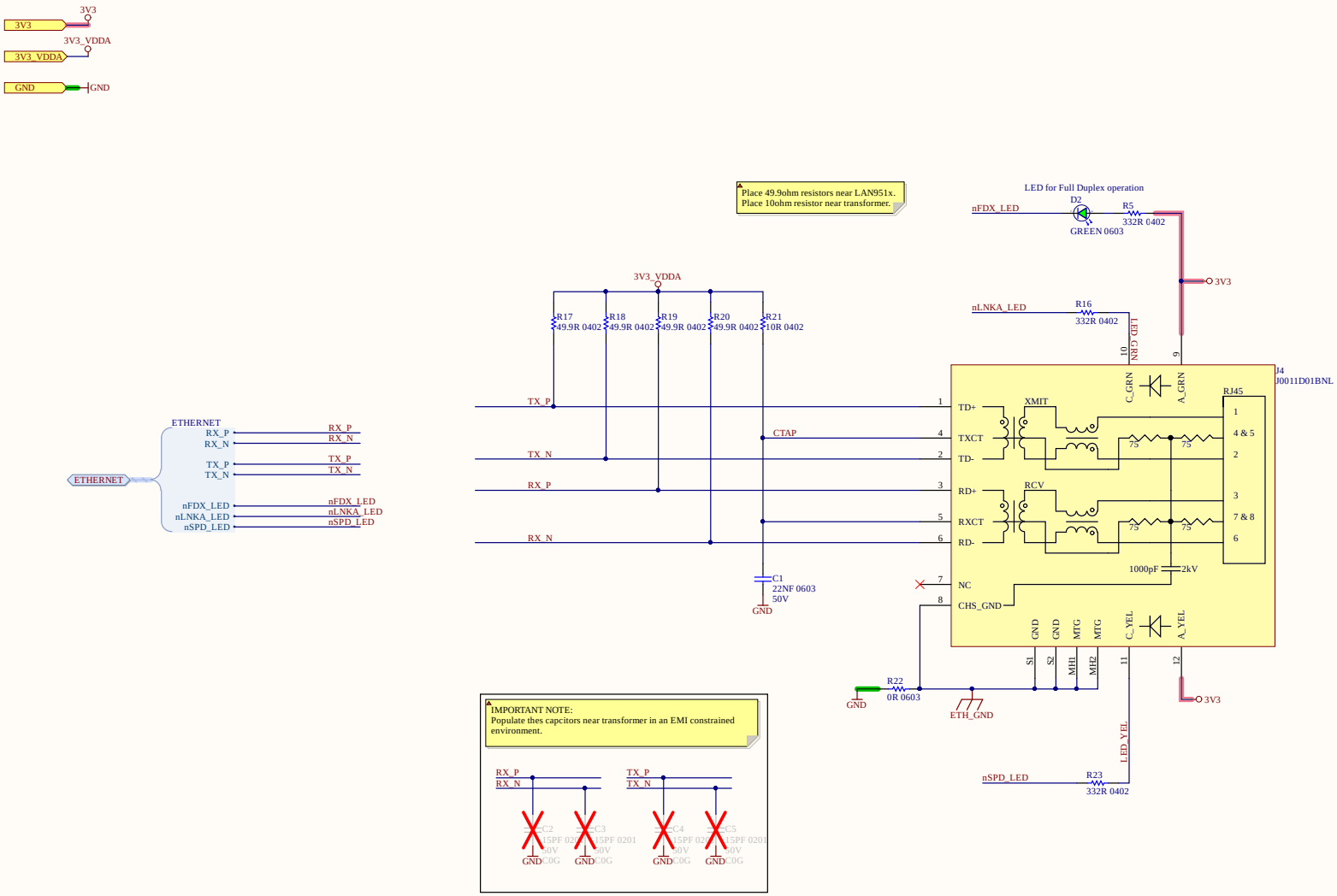

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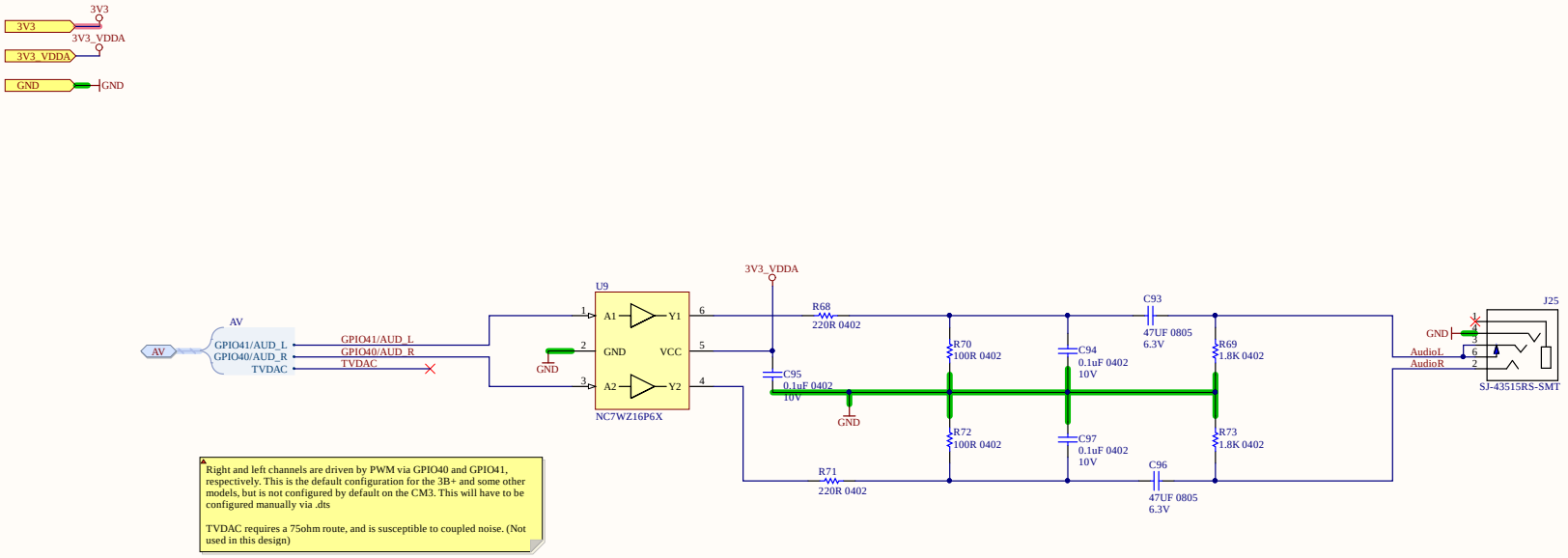

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