

BW1099 - Myriad X SoM Datasheet

1 Features

- Intel Movidius Myriad X VPU ma2485-C0
- 16MB QSPI NOR Flash (optional)
- 32Kb I2C EEPROM
- USB3.1, gen1 5gbps
- 1x 4-Lane MIPI CSI-2 D-PHY
- 2x 2-Lane MIPI CSI-2 D-PHY
- QSPI, SDIO, UART, I2C
- Boot Modes Supported: USB, NOR
- On-board power generation

MIPI CSI-2 D-PHY channel, allowing for multiple camera inputs.

Power-on Reset BOOT configuration can be modified with on-board resistor straps, and a 10-pin JTAG connector is also provided on-board to allow for debug without the need for a baseboard.

SoM power consumption is use-case dependent, but typical consumption is under 5W with thermal mitigation.

2 Applications

- Industrial automation
- Robotics and autonomy
- Security systems
- Remote intelligence

Device Information

PART NUMBER	SIZE (W x L x H) ¹
BW1099	40mm x 30mm x 17.5mm

1) Including components and heatsink

3 Description

The Luxonis BW1099 is a system-on-module (SoM) designed for integration into a top-level system with a need for a low-power, 4 TOPS AI vision system. The BW1099 interfaces with the system through a single 10-gbps-rated 100-pin DF40C-100DP-0.4V(51) board-to-board mezzanine connector which carries all signal I/O as well as 5V input. The on-board SMPS system regulates the 5V input and provides all necessary digital and analog power. An auxiliary power port is offered to interface without connection to a baseboard.

Core digital electronics on the BW1099 include the Movidius Myriad X VPU (MA2485-C0), a 16MB QSPI NOR flash, and 32kb EEPROM.

USB 3.1 Gen1, QSPI, UART, I2C, and SDIO are all broken out from the SoM and routed through the mezzanine connector to the system. Additionally, the BW1099 SoM exposes two 2-lane MIPI CSI-2 D-PHY channels and one 4-lane

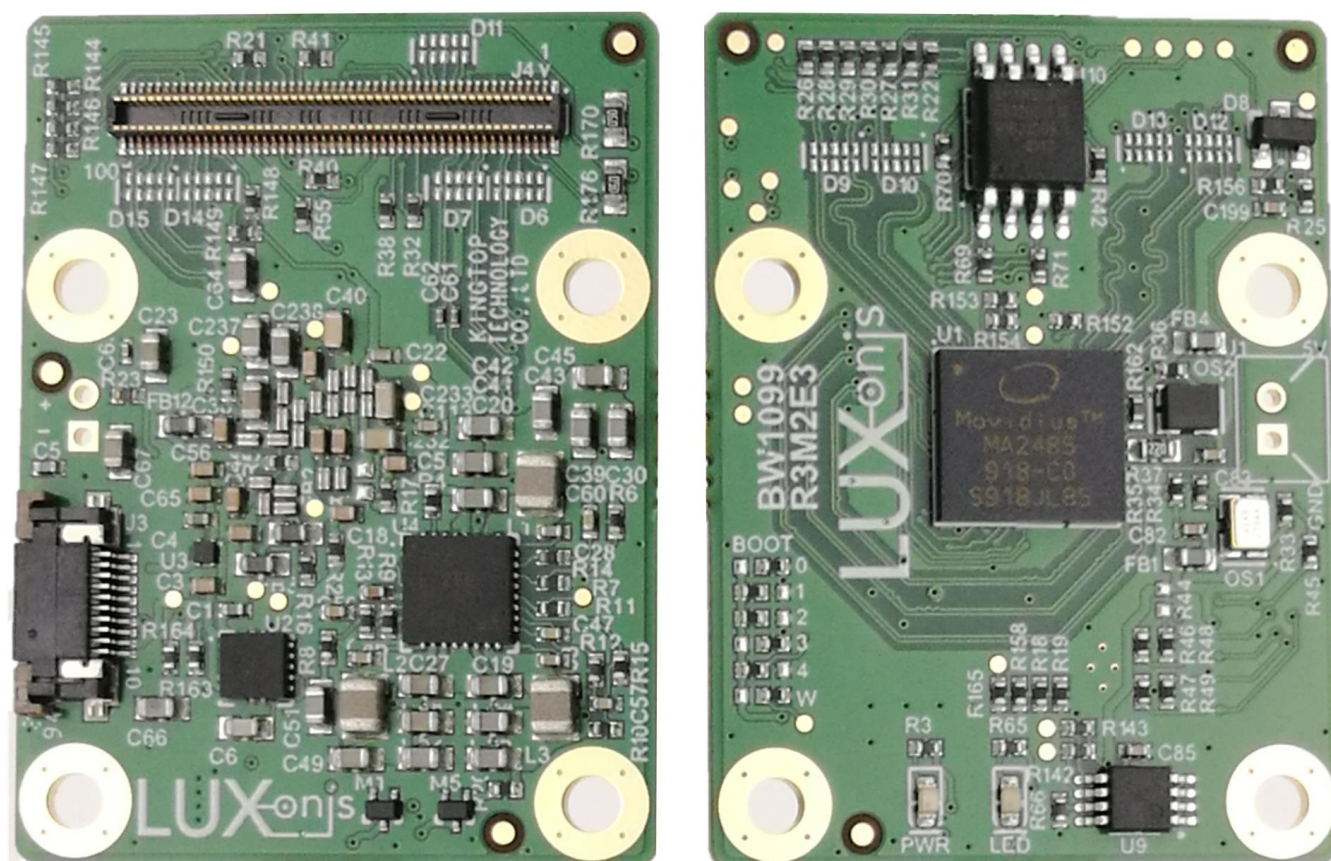


Figure 1 – Bottom and Top of BW1099 PCBA

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4 Block Diagram

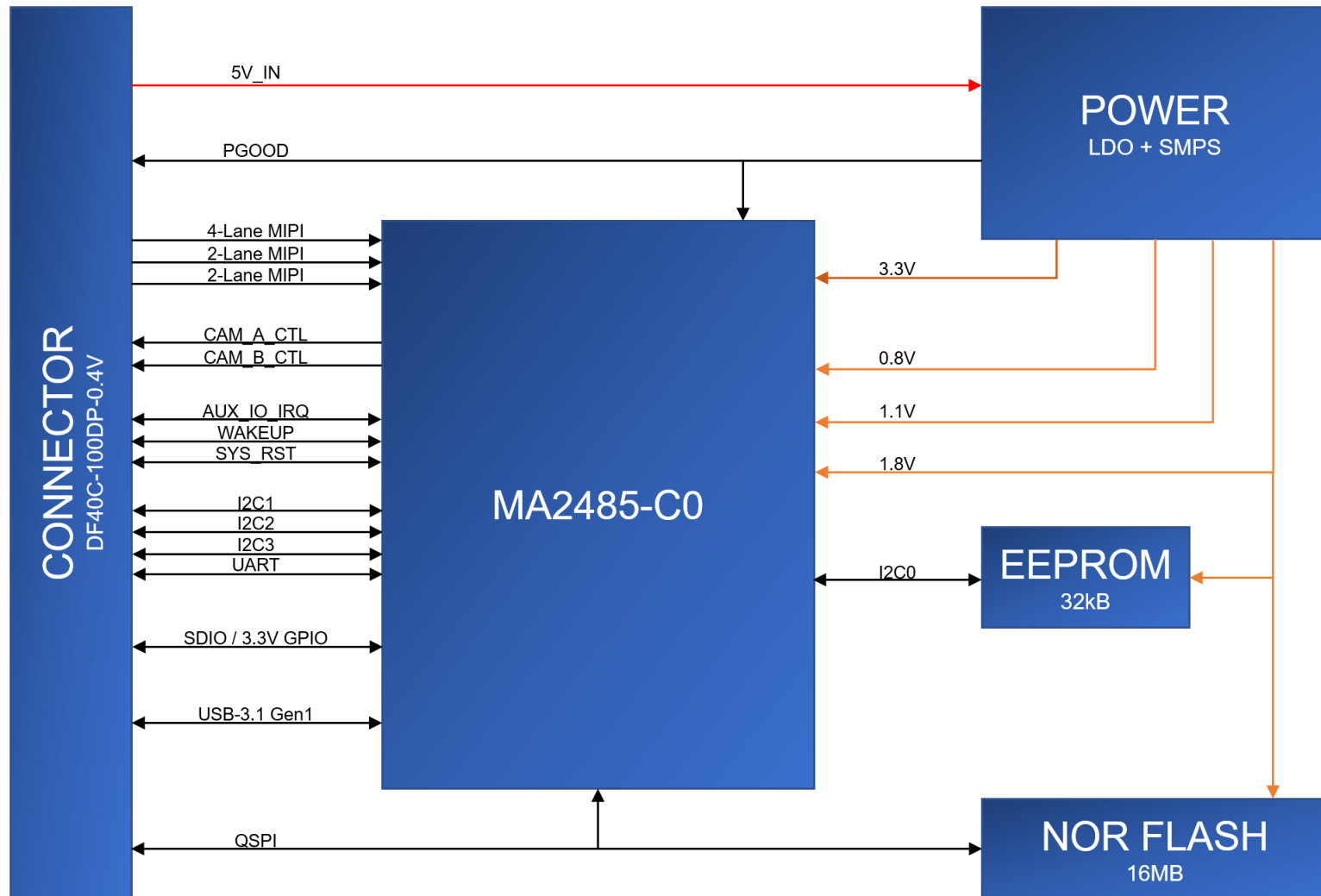


Figure 2 - Schematic Block Diagram

5 Electrical Characteristics

5.1 Absolute Maximum Ratings¹

SYMBOL	RATINGS	MIN	MAX	UNIT
V_{IN}	External input supply voltage range. ²	3.6	5.5	V
V_{I/O_1V8}	Input voltage SoM I/O for 1.8V logic	-0.3	2.0	V
V_{I/O_3V3}	Input voltage SoM I/O for 3.3V logic	-0.3	3.6	V
$I_{I/O}$	IO output current drive strength	2	12	mA
T_J	Junction temperature.		105	C
T_{STG}	Storage temperature.	-30	150	C

5.2 Recommended Operating Conditions

SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
V_{IN}	External input supply voltage range. ²	4.5	5.0	5.25	V
V_{I/O_1V8}	Input voltage SoM I/O for 1.8V logic	0		1.8	V
V_{I/O_3V3}	Input voltage SoM I/O for 3.3V logic	0		3.3	V
P_Q	Quiescent power draw ³		0.3		W
P_{IDLE}	Idle power draw ⁴		0.7		W
P_{INFR}	Inference power draw ⁵		2.48		W
T_A	Ambient operating temperature ⁶		25	50	°C
T_J	Junction temperature. ⁶			105	°C

- 1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2) Applies to 5V input pins only
- 3) With SoM in reset
- 4) Myriad X booted to base mode via USB
- 5) Mobilenet-SSDV2 detector, 30fps
- 6) With default Luxonis passive heatsink, running Mobilenet-SSDV2 30fps. Custom or active thermal solutions are recommended in ambient environments >50C, and/or for highly demanding inference operations >2.5W.

6 SoM Connector Interface

6.1 Pinout

The following contains the pinout of 100-pin Hirose DF40HC(3.0)-100DS-0.4V receptacle for the BW1099 SoM. The schematic symbol, footprint, and full IO pinout table can be found at the Luxonis Github repository.

J1			
1	GND	GND	2
3	CAMA_CLKN	SGPIO_1	4
5	CAMA_CLKP	SGPIO_2	6
7	GND		
9	CAMA_D0_N		
11	CAMA_D0_P	GND	8
13	GND	USB_RX_P	10
15	CAMA_D1_N	USB_RX_N	12
17	CAMA_D1_P	GND	14
19	GND	USB_D_P	16
21	CAMA_D2_N	USB_D_N	18
23	CAMA_D2_P	GND	20
25	GND	USB_TX_P	22
27	CAMA_D3_N	USB_TX_N	24
29	CAMA_D3_P	GND	26
31	GND		
		CAMA_CLK	28
33	CAMA_I2C_SDA	GND	30
35	CAMA_I2C_SCL	SGPIO_4_3V3	32
		CAMA_RST	34
		SGPIO_8_3V3	36
37	PGOOD	SGPIO_9_3V3	38
39	RST	SGPIO_10_3V3	40
41	WAKEUP	SGPIO_11	42
43	GND	GND	44
45	GND	GND	46
47	5V	5V	48
49	5V	5V	50
51	5V	5V	52
53	5V/VBUS	5V	54
55	GND	GND	56
57	GND	GND	58
59	SGPIO_12	SGPIO_13/SPIO_CS_1	60
61	SGPIO_14_3V3	SPIO_SIO0	62
63	SGPIO_16_3V3	SPIO_SIO1	64
65	CAM_B_D_PWM	SPIO_SIO2	66
67	CAM_B_PWDN_N	SPIO_SIO3	68
69	SGPIO_22	SPIO_CS_0	70
71	GND	GND	72
73	CAMB_CLK	SPIO_SCK	74
75	GND	GND	76
77	CAMB_I2C_SCL	SGPIO_27	78
79	CAMB_I2C_SDA	SGPIO_29	80
81	GND	GND	82
83	CAMB_D1_N	CAMC_D1_N	84
85	CAMB_D1_P	CAMC_D1_P	86
87	GND	GND	88
89	CAMB_D0_N	CAMC_D0_N	90
91	CAMB_D0_P	CAMC_D0_P	92
93	GND	GND	94
95	CAMB_CLKN	CAMC_CLKN	96
97	CAMB_CLKP	CAMC_CLKP	98
99	GND	GND	100

BW1099_Receptacle_DF40HC(3.0)-100DS-0.4V
3mm

Figure 3 - Schematic Symbol for BW1099 Baseboard Receptacle Connector

6.2 I2C

The BW1099 SoM offers two dedicated I2C interfaces, I2C1 (CAMA_I2C), I2C2 (CAMB_I2C), both with 2.2Kohm pull-up resistors (SDA & SCL) to the on-SoM 1.8V rail. For custom baseboard designs, each of the two I2C interfaces are available and are not in use for anything else on the SoM. On most Luxonis baseboards, such as the BW1098 family, the I2C1 interface is used for communication with the RGB color camera, the I2C2 interface is used to communicate with the pair of stereo cameras, and the I2C3 is typically unused but accessible through test points or connector pads.

6.2.1 RGB Camera I2C1 Address Usage

The IMX378 RGB camera on most Luxonis baseboards uses some specific addresses as seen in Figure 4. Use of the I2C1 interface on other components is possible, but with consideration of the existing usage of the RGB camera.

<i>IMX378 MODULE CONNECTOR</i>			
MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor)
			0x18 (VCM driver)
			0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz

Figure 4 - Baseboard I2C1 RGB Camera Module Usage

6.2.2 Stereo Camera I2C2 Address Usage

6.3 MIPI

Three MIPI CSI-2 DPHYv1.2 interfaces are available as input to the SoM. One is a 4-lane interface, and the other two interfaces are 2-lane each, all allowing a maximum of 2.1Gbps per lane.

For each of the three camera interfaces, the inter-pair delay of that interface is matched to the clock pair within +/-1ps, and all pairs are routed with 100ohm differential impedance.

6.4 PGOOD

PGOOD is a 1.8V open-drain output from the SoM PMIC and is pulled high when the PMIC evaluates power is good. PGOOD has a 10Kohm pull-up resistor to the on-SoM 1.8V rail.

This pin should be left floating if unused or tied to a high-impedance input to sense PGOOD. Do not pull or tie PGOOD to GND.

6.5 WAKEUP

WAKEUP is a 1.8V input to the SoM which is pulled to GND through a 10Kohm resistor. If driven high and sensed during the rising edge of _RST power-on-reset, the on-chip e-fuse is used for boot selection. At present, this functionality is not used on any Luxonis SoM.

The WAKEUP pin was originally intended for waking the SoM from deep sleep mode, but this functionality is not supported on Luxonis SoMs. However, any SGPIO can be used to trigger an interrupt and wake the SoM.

The WAKEUP should be left floating.

6.6 _RST

_RST is the active-low Myriad X reset input. _RST has a 1.8V 10Kohm pull-up resistor on the SoM, and can be driven low from the baseboard to reset the Myriad X.

6.7 Camera Reference Clocks

Two pins are used to provide a 24MHz reference clock to the image sensor ICs on the baseboard. These signals are on the CAMA_CLK and CAMB_CLK pins of the SoM interface connector. Each signal has a 121Kohm, pull down on the SoM. It is possible to create additional reference clocks for additional cameras by reconfiguring an SGPIO pin.

6.8 Camera Reset Signals

Three pins are used for individually resetting or powering down the RGB and stereo pair cameras. These signals are CAMA_RST, CAM_B_D_PWM, and CAM_B_PWDN_N, for the RGB, LEFT, and RIGHT cameras respectively. Each of these signals is 1.8V and are active-low. No pull-up or pull-down resistors are on these signals on the SoM.

6.9 1.8V Shared SPI0 (QSPI)

The signals with prefix "SPI0" are part of a QSPI bus which is shared with the optional on-SoM NOR flash. Note the signal configuration details in Table 1 (refer to the [BW1099 IO TABLE](#) for more details). All signals related to SPI0 are delay-matched on the SoM to +/-100ps to the connector interface.

Pin #	Pin name / Primary Function	SoM GPIO	Alt. 1	PU/PD on SoM	Pin Type	Description
60	SGPIO_13/SPI0_CS_1	SGPIO_13	SPI0_CS_1		1.8V GPIO	GPIO, or can be configured as second CS for SPI0, MX in Controller or Peripheral mode. / +/-100ps inter-SPI0
70	SPI0_CS_0	SGPIO_23		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR S# / +/-100ps inter-SPI0
74	SPI0_SCK	SGPIO_25			1.8V GPIO	Hardwired to 1099 on-board NOR C / +/-100ps inter-SPI0
62	SPI0_SIO0	SGPIO_15			1.8V GPIO	Hardwired to 1099 on-board NOR DQ0 / +/-100ps inter-SPI0
64	SPI0_SIO1	SGPIO_17			1.8V GPIO	Hardwired to 1099 on-board NOR DQ1 / +/-100ps inter-SPI0
66	SPI0_SIO2	SGPIO_19		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR W#/DQ2 / +/-100ps inter-SPI0
68	SPI0_SIO3	SGPIO_21		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR DQ3/HOLD# / +/-100ps inter-SPI0

Table 1 - SPI0 Pin Configuration

With the NOR flash unpopulated the SPI0 bus can be used by the Myriad X in either controller or peripheral mode. With the Myriad X in controller mode, SPI0_CS_0 and SPI0_CS_1 can be used as chip selects for any baseboard peripherals, and additional baseboard chip selects can be configured by

using SGPIOs, if required. With the Myriad X in peripheral mode, either the SPI0_CS_0 or SPI0_CS_1 can be used by the baseboard controller to select the Myriad X as a peripheral. Unlike for controller mode, in peripheral mode, SGPIOs cannot be configured as chip selects for the Myriad X, only SPI0_CS_0 and SPI0_CS_1 can be used for this purpose.

With the NOR flash populated, the SPI0 bus can still be used by the Myriad X in either controller or peripheral mode, but the NOR flash now occupies the SPI0_CS_0 location so some care must be taken to avoid contention. With the NOR flash populated, and the Myriad X is in controller mode, the SPI0_CS_0 selects the NOR flash. SPI0_CS_1 (or other reconfigured SGPIO) can be used as a second chip select for baseboard peripherals. When in peripheral mode SPI0_CS_1 should be used as the chip select for the peripheral Myriad X to avoid contention when communicating with NOR flash using SPI0_CS_0.

Note that when an external controller is accessing the NOR flash on the SoM, the Myriad X must not be allowed to access at the same time. Asserting _RST for the Myriad X is an option to prevent this contention.

6.10 3.3V SGPIO Bank

The SoM offers six SGPIO which are 3.3V signaling for easy interface to common peripherals and devices with 3.3V signaling. These SGPIO offer several configurations including SDIO, QSPI, UART, PWM, and I2C, along with general purpose IO and are listed in Table 2 (refer to the [BW1099 IO TABLE](#) for more details).

Pin #	Pin name / Primary Function	SoM GPIO	Alt. 1	Alt. 2	Alt. 3	Alt. 4	PU/PD on SoM	Pin Type	Description
40	SGPIO_10_3V3	SGPIO_10	sd_hst0_dat_0	spi2_dio_2	pwm_0	I2C3_SDA	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
61	SGPIO_14_3V3	SGPIO_14	sd_hst0_clk	spi2_dio_0_mosi			PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
63	SGPIO_16_3V3	SGPIO_16	sd_hst0_cmd	spi2_dio_1_miso		I2C3_SCL	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
32	SGPIO_4_3V3	SGPIO_4	sd_hst0_dat_3	spi2_cs_0	pwm_3	UART3_TX	PD: 300kR/GND	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
36	SGPIO_8_3V3	SGPIO_8	sd_hst0_dat_2	spi2_sclk			PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
38	SGPIO_9_3V3	SGPIO_9	sd_hst0_dat_1	spi2_dio_3		UART3_RX	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST

Table 2 - 3.3V SGPIO Pin Configuration

6.10.1 3.3V SGPIO Bank - SDIO

The 3.3V SGPIO bank is nominally configured for use with SDIO, as appropriate pull-up and pull-down resistors exist on the SoM. CLK, CMD, and DAT[0:3] are available for use. Optional signals such as card detect can be implemented using the 1.8V SGPIO.

6.10.2 3.3V SGPIO Bank – QSPI (SPI2)

The 3.3V SGPIO bank can be configured as a QSPI bus. The weak pull-up and pull-down resistors on the signal lines (for use as SDIO) are over driven when used as a QSPI interface, though maximum data rates are not guaranteed. Like the SPI0 bank, the 3.3V QSPI interface can operate as a controller or peripheral using the SPI2_CS_0 signal. Additional chip selects can be sent to baseboard peripherals with other 1.8v SGPIO, though the need to level shift from 1.8V to 3.3V may be necessary.

6.11 1.8V SGPIO

The default IO voltage for all SGPIO is 1.8V, with the exceptions of the 3.3V SGPIO listed in Table 2. Each SGPIO can be muxed to alternate functionality as described in Table 3 (refer to the [BW1099 IO TABLE](#) for more details). In addition to muxed functionality, each SGPIO is fully user-programmable with support for four output drive strengths (2mA, 4mA, 8mA, 12mA), selectable output slew-rate (slow/fast), open-drain output mode, LVCMOS/LVTTL compatible input modes with selectable hysteresis, programmable pull-up/pull-down input options, power-on-start capability, and no requirements for power sequencing. Additionally, 100MHz frequency can be achieved with less than 15pF external load, or up to 125MHz with less than 10pF external load.

Pin #	Pin name / Primary Function	SoM GPIO	Alt. 1	Alt. 2	PU/PD on SoM	Pin Type	Description
4	SGPIO_1	SGPIO_1	UART_RX	pwm3		1.8V GPIO	Typically labeled as UART_RX on Luxonis baseboards.
28	CAMA_CLK	SGPIO_3			PD: 121kR/GND	1.8V GPIO	24MHz reference clock for Camera A PLL
33	CAMA_I2C_SDA	SGPIO_5	pwm5		PU: 2.2kR/1.8V	1.8V GPIO	I2C data for Camera A
34	CAMA_RST	SGPIO_6				1.8V GPIO	Camera A reset/power down.
35	CAMA_I2C_SCL	SGPIO_7			PU: 2.2kR/1.8V	1.8V GPIO	I2C clock for Camera A
42	COM_AUX_IO2	SGPIO_11				1.8V GPIO	Auxiliary GPIO for cameras. Reserved for driving camera STROBE signal on Luxonis boards.
59	SGPIO_12	SGPIO_12			PU: 40.2kR/1.8V	1.8V GPIO	Configured for SDIO card detect, or as regular GPIO. Note 1.8V, 40.2k PU. / +/-100ps inter-SD_HST
60	SGPIO_13/SPI0_CS_1	SGPIO_13	SPI0_CS_1			1.8V GPIO	GPIO, or can be configured as second CS for SPI0, MX in Controller or Peripheral mode. / +/-100ps inter-SPI0
62	SPI0_SIO0	SGPIO_15				1.8V GPIO	Hardwired to 1099 on-board NOR DQ0 / +/-100ps inter-SPI0
64	SPI0_SIO1	SGPIO_17				1.8V GPIO	Hardwired to 1099 on-board NOR DQ1 / +/-100ps inter-SPI0
65	CAM_B_D_PWM	SGPIO_18				1.8V GPIO	Camera C reset/power down.
66	SPI0_SIO2	SGPIO_19			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR W#/DQ2 / +/-100ps inter-SPI0
67	CAM_B_PWDN_N	SGPIO_20				1.8V GPIO	Camera B reset/power down.
68	SPI0_SIO3	SGPIO_21			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR DQ3/HOLD# / +/-100ps inter-SPI0
70	SPI0_CS_0	SGPIO_23			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 1099 on-board NOR S# / +/-100ps inter-SPI0

73	CAMB_CLK	SGPIO_24			PD: 121kR/GND	1.8V GPIO	24MHz reference clock for Camera B PLL
74	SPI0_SCK	SGPIO_25				1.8V GPIO	Hardwired to 1099 on-board NOR C / +/-100ps inter-SPI0
77	CAMB_I2C_SCL	SGPIO_26			PU: 2.2kR/1.8V	1.8V GPIO	Camera B I2C SDA. Can be used as GPIO.
79	CAMB_I2C_SDA	SGPIO_28			PU: 2.2kR/1.8V	1.8V GPIO	Camera B I2C SCL. Can be used as GPIO.
6	SGPIO_2	SGPIO_2	UART_TX	pwm2		1.8V GPIO	Typically labeled as UART_TX on Luxonis baseboards.
69	SGPIO_22	SGPIO_22				1.8V GPIO	
78	SGPIO_27	SGPIO_27	I2C3_SDA		PU: 2.2kR/1.8V	1.8V GPIO	Camera C I2C SDA (if applicable). Can be used as GPIO
80	SGPIO_29	SGPIO_29	I2C3_SCL		PU: 2.2kR/1.8V	1.8V GPIO	Camera C I2C SCL (if applicable). Can be used as GPIO
59	SGPIO_12	SGPIO_12			PU: 40.2kR/1.8V	1.8V GPIO	Configured for SDIO card detect, or as regular GPIO. Note 1.8V, 40.2k PU. / +/-100ps inter-SD_HST

Table 3 - 1.8V SGPIO Pin Configuration

7 Mechanical Information

The following information is the most current data available for the designated device. This data is subject to change without notice and without revision of this document.

7.1 BW1099 Dimensions

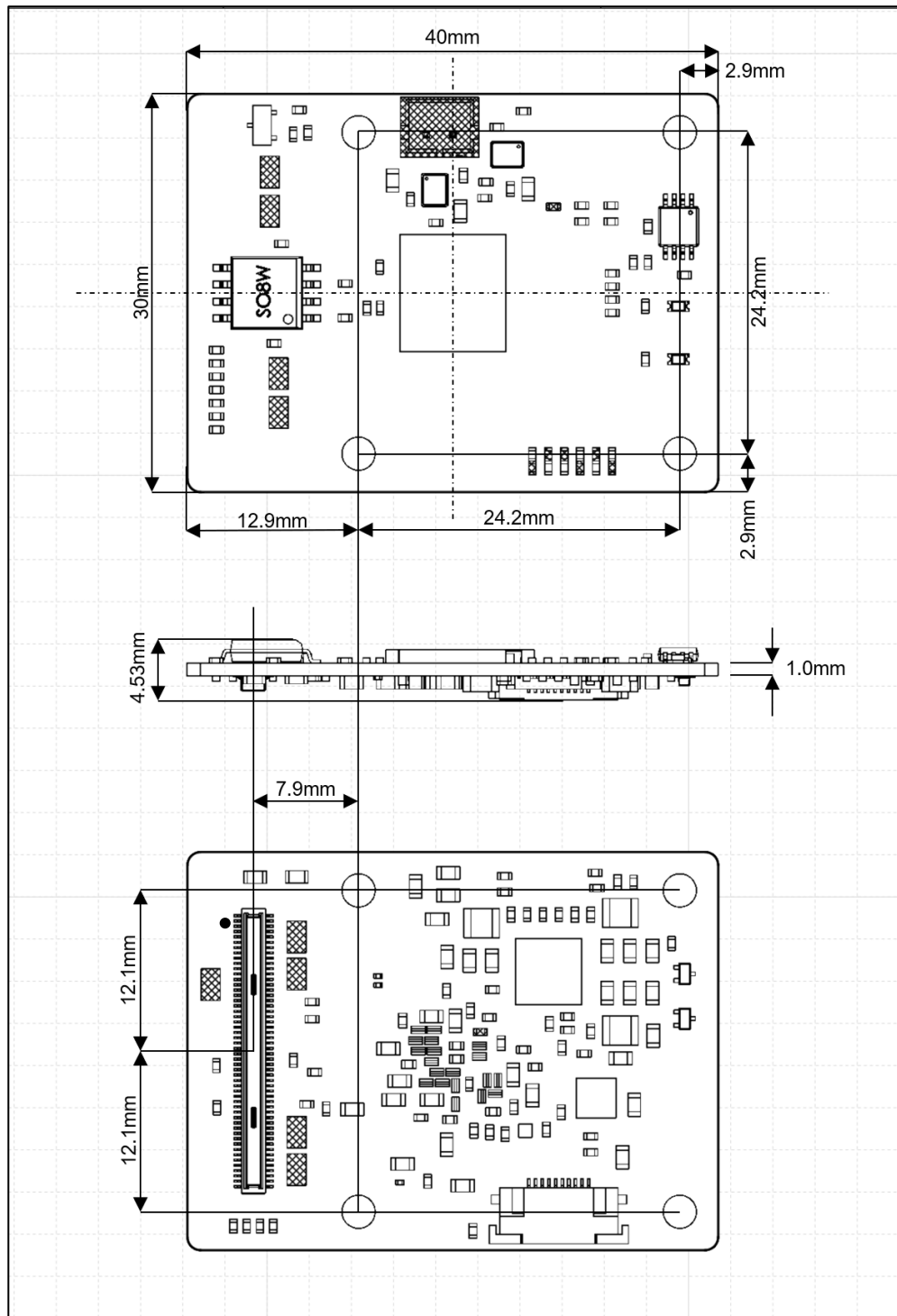


Figure 6 – Top, Side, and Bottom dimensions

7.2 Recommended Mounting Configuration

The BW1099 SoM is designed to be used with a 3mm mated-height connector and accompanying 3mm standoffs. The B2B connector plug is on the BW1099 (Hirose DF40C-100DP-0.4V), while the receptacle, which determines mated height, is on the baseboard (Hirose DF40HC(3.0)-100DS-0.4V). Würth Elektronik 9774030243R SMT standoffs are recommended.

7.3 BW1099 Mounting Holes

The BW1099 has 4 M2.5 mounting holes for securing the SoM. These mounting holes use a 2.6mm ID, and a 5.5mm OD pad, which is tied to SoM GND. M2-0.40 screws can be used with these pads to secure the SoM to the recommended Würth Elektronik 9774030243R SMT standoffs, or a custom solution using M2-0.40 or M2.5-0.45 screws can be used. Note that when using M2.5-0.45 screws, there is reduced tolerance between the B2B connector clocking and the screws' hole alignment. This must be accounted for to ensure proper connector mating.

7.4 SoM Clearance

3mm is the board-to-board standoff height when using the recommended mounting configuration, however, components on the underside of the BW1099 reduce this clearance. For highest design reliability, it is recommended not to place components on the baseboard underneath the SoM, but components with max height <1mm will have clearance.

In previous designs many components have been successfully placed on the baseboard beneath the SoM making careful use of the 3D STEP file of the SoM, which is available upon request.

8 Thermal Information

Power consumption can vary considerably depending on the application. A stereo vision application running Mobilenet-SSD V2 at 30fps typically consumes about 2.5W, but more aggressive applications can consume closer to 5W. Most of this power is consumed by the MA2485. While the VFBGA provides an excellent thermal path from the MA2485 to the SoM, the thermal sink is small, and the part temperature can quickly rise toward the 105C max die temperature.

Heatsinking of the MA2485 is required for most applications.

Table 4 details thermal parameters for the MA2485 simulated in a still air environment, an ambient temperature of 25C, 2W power dissipation, and under the test conditions described in JESD51-2A.

Parameter	Value (C/W)	Description
θ_{JB}	5.8	Junction-to-board thermal resistance (EIA/JESD51-8)
θ_{JC}	3.1	Junction-to-case thermal resistance
θ_{JA}	21.4	Junction-to-ambient thermal resistance (EIA/JESD51-2)

Table 4 - MA2485 Thermal Parameters

9 Revision History

- Initial Release – November 2020