

BW2099 - Myriad X SoM with eMMC Flash

1 Features

- Intel Movidius Myriad X VPU ma2485-C0
- 16GB eMMC 5.1
- 128MB QSPI NOR Flash
- 32Kb I2C EEPROM
- USB3.1, gen2 10gbps
- PCIe x1 (ext. ref clk)
- 2x 4-Lane MIPI CSI-2 D-PHY
- 2x 2-Lane MIPI CSI-2 D-PHY
- QSPI, SDIO, UART, I2C, I2S
- Boot Modes Supported: NOR, eMMC, USB, Ethernet (EEPROM)
- On-board power generation

2 Applications

- Industrial automation
- Robotics and autonomy
- Security systems
- Remote intelligence

3 Description

The Luxonis BW2099 is a system-on-module (SoM) designed for integration into a top-level system with a need for a low-power, 4 TOPS AI vision system. The BW2099 interfaces with the system through two 10-gbps-rated 100-pin DF40C-100DP-0.4V(51) board-to-board mezzanine connectors which carry all signal I/O as well as 5V input. The on-board SMPS system regulates the 5V input and provides all necessary digital and analog power. An auxiliary power port is offered to interface without connection to a baseboard.

Core digital electronics on the BW2099 include the Movidius Myriad X VPU (MA2485-C0), a 16GB eMMC 5.1 flash device, 128MB QSPI NOR flash, and 32kb EEPROM.

USB 3.1 Gen2, QSPI, UART, I2C, 1-lane PCIe, and SDIO are all broken out from the SoM and routed through the mezzanine connectors to the system. Additionally, the BW2099 SoM exposes

two 2-lane MIPI CSI-2 D-PHY channels and two 4-lane MIPI CSI-2 D-PHY channels, allowing for multiple camera inputs.

I2S interface with APB data 32 bit bus width is exposed; one output and 3 stereo inputs give the ability to connect multiple microphones and one external audio device.

GPIO Boot selection, JTAG, and additional Myriad X GPIOs are exposed as well. A 10-pin JTAG connector is also provided on-board to allow for debug without the need for a baseboard.

The SoM can be booted via USB, NOR flash, eMMC, SPI, and Ethernet (RTL8111HS driver in EEPROM).

SoM power consumption is use-case dependent, but typical consumption is under 5W with thermal mitigation.

Device Information

PART NUMBER	SIZE (W x L x H) ¹
BW2099	30mm x 45mm x 17.5mm

1) Including components and heatsink

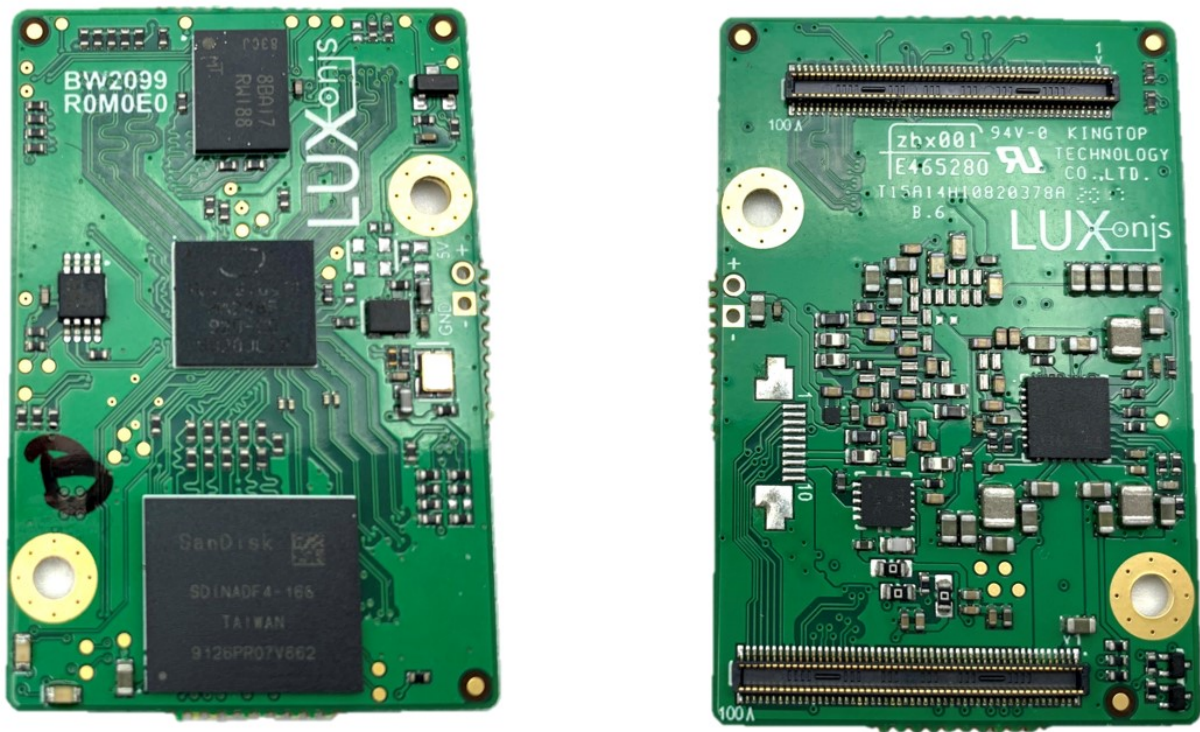


Figure 1 - Top and Bottom of BW2099 PCBA

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4 Block Diagram

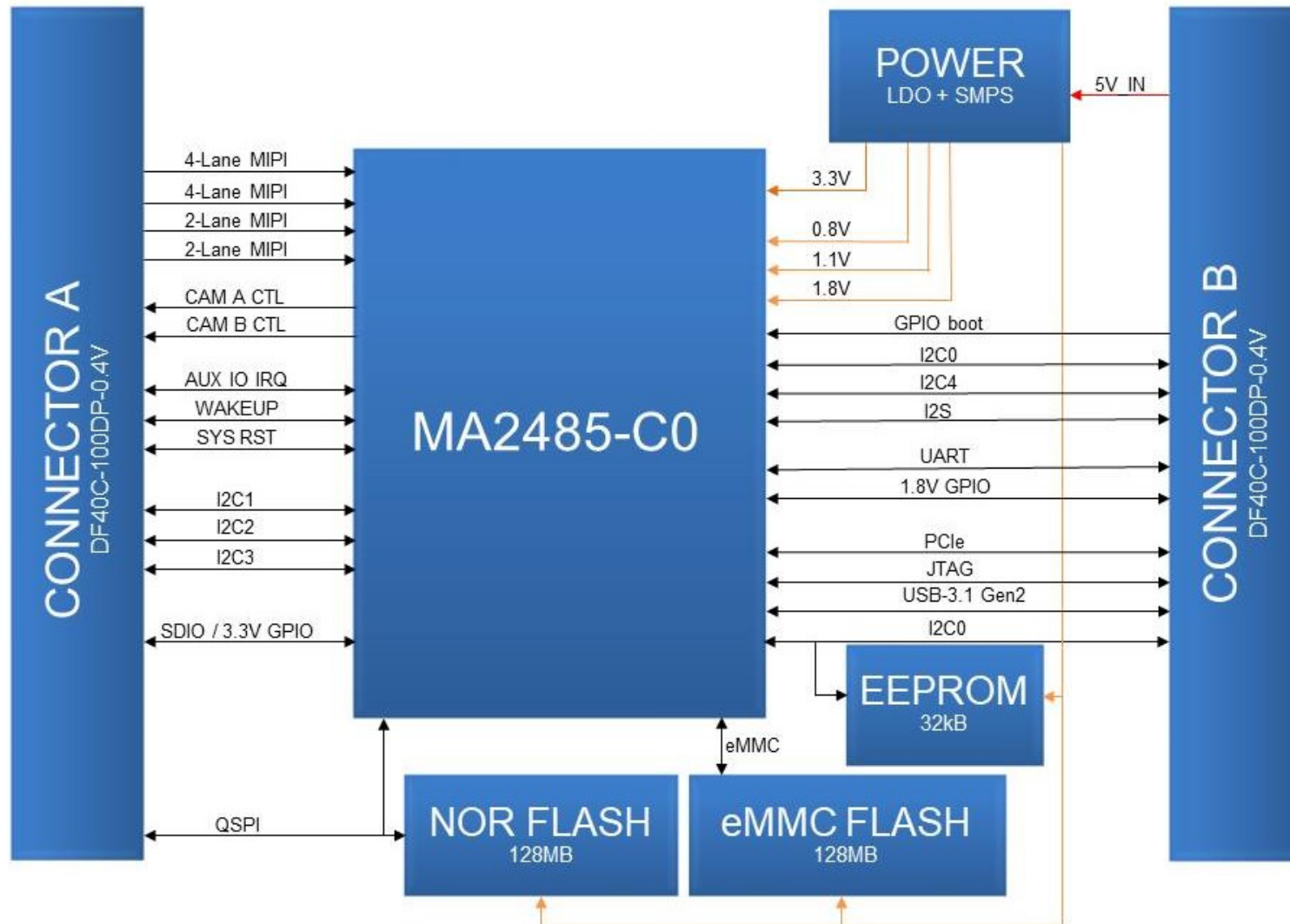


Figure 2 - Schematic Block Diagram

5 Electrical Characteristics

5.1 Absolute Maximum Ratings¹

SYMBOL	RATINGS	MIN	MAX	UNIT
V_{IN}	External input supply voltage range. ²	3.6	5.5	V
V_{I/O_1V8}	Input voltage SoM I/O for 1.8V logic	-0.3	2.0	V
V_{I/O_3V3}	Input voltage SoM I/O for 3.3V logic	-0.3	3.6	V
$I_{I/O}$	IO output current drive strength	2	12	mA
T_J	Junction temperature.		105	C
T_{STG}	Storage temperature.	-30	150	C

5.2 Recommended Operating Conditions

SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
V_{IN}	External input supply voltage range. ²	4.5	5.0	5.25	V
V_{I/O_1V8}	Input voltage SoM I/O for 1.8V logic	0		1.8	V
V_{I/O_3V3}	Input voltage SoM I/O for 3.3V logic	0		3.3	V
P_Q	Quiescent power draw ³		0.3		W
P_{IDLE}	Idle power draw ⁴		0.7		W
P_{INFR}	Inference power draw ⁵		2.48		W
T_A	Ambient operating temperature ⁶		25	50	°C
T_J	Junction temperature. ⁶			105	°C

- 1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2) Applies to 5V input pins only
- 3) With SoM in reset
- 4) Myriad X booted to base mode via USB
- 5) MobilenetSSDV2 detector, 30fps
- 6) With default Luxonis passive heatsink, running Mobilenet-SSDV2 30fps. Custom or active thermal solutions are recommended in ambient environments >50C, and/or for highly demanding inference operations >2.5W.

6 SoM Connector

6.1 Pinout

The following contains the pinout of 100-pin DF40C-100DP-0.4V(51) connector, A or designator J4.

S1			S2
1	GND	GND	2
3	CAMA_CLK_N	CAMD_CLK_N	4
5	CAMA_CLK_P	CAMD_CLK_P	6
7	GND		
9	CAMA_D0_N		8
11	CAMA_D0_P	GND	10
13	GND	CAMD_D0_N	12
15	CAMA_D1_N	CAMD_D0_P	14
17	CAMA_D1_P	GND	16
19	GND	CAMD_D1_N	18
21	CAMA_D2_N	CAMD_D1_P	20
23	CAMA_D2_P	GND	22
25	GND	CAMD_D2_N	24
27	CAMA_D3_N	CAMD_D2_P	26
29	CAMA_D3_P	GND	
31	GND		
		CAMA_CLK	28
33	CAMA_I2C_SDA	GND	30
35	CAMA_I2C_SCL	SGPIO_4_3V3	32
		CAMA_RST	34
37	PGOOD	SGPIO_8_3V3	36
39	RST	SGPIO_9_3V3	38
41	WAKEUP	SGPIO_10_3V3	40
		SGPIO_11	42
43	RFU	GND	44
45	RFU	CAMD_D3_N	46
47	RFU	CAMD_D3_P	48
49	RFU	GND	50
51	RFU	RFU	52
53	RFU	RFU	54
55	RFU	RFU	56
57	RFU	RFU	58
59	SGPIO_12	SGPIO_13/SPIO_CS_1	60
61	SGPIO_14_3V3	SPIO_SIO0	62
63	SGPIO_16_3V3	SPIO_SIO1	64
65	CAM_B_D_PWM	SPIO_SIO2	66
67	CAM_B_PWDN_N	SPIO_SIO3	68
69	SGPIO_22	SPIO_CS_0	70
71	GND	GND	72
73	CAMB_CLK	SPIO_SCK	74
75	GND	GND	76
77	CAMB_I2C_SCL	I2C3_SCL	78
79	CAMB_I2C_SDA	I2C3_SDA	80
81	GND	GND	82
83	CAMB_D1_N	CAMC_D1_N	84
85	CAMB_D1_P	CAMC_D1_P	86
87	GND	GND	88
89	CAMB_D0_N	CAMC_D0_N	90
91	CAMB_D0_P	CAMC_D0_P	92
93	GND	GND	94
95	CAMB_CLK_N	CAMC_CLK_N	96
97	CAMB_CLK_P	CAMC_CLK_P	98
99	GND	GND	100
S3			S4

Figure 3 - Schematic Pinout, Connector J4

The following contains the pinout of 100-pin DF40C-100DP-0.4V(51) connector, B or designator J2.

S1			S2
1	GND	GND	2
3	GND	GND	4
5	5V	5V	6
7	5V	5V	8
9	5V	5V	10
11	5V	5V	12
13	5V	5V	14
15	GND	GND	16
	GND	GND	
17	I2S2_SCK	BOOT4	18
19	I2S2_WS	BOOT3	20
21	I2S2_IN_SD0	BOOT2	22
23	I2S2_OUT_SD0	BOOT1	24
25	I2S2_IN_SD1	BOOT0	26
27	I2S2_IN_SD2	BOOT_AUX/PCIe_ISO_N	28
29	GND		
31	RFU	GND	30
33	RFU	GND	32
35	RFU		
37	RFU	I2C0_SCL	34
39	RFU	I2C0_SDA	36
41	RFU		
43	RFU	GND	38
45	RFU	GND	40
47	RFU		
49	RFU	SGPIO_1	42
51	RFU	SGPIO_2	44
53	RFU		
55	RFU	GND	46
		SGPIO_30	48
57	I2C4_SDA	SGPIO_31	50
59	I2C4_SCL	SGPIO_32	52
		SGPIO_33	54
61	GND	SGPIO_34	56
		SGPIO_35	58
63	PCIe_PERST	SGPIO_36	60
65	PCIe_CLKREQ_N	SGPIO_37	62
		SGPIO_38	64
67	GND	SGPIO_39	66
69	SDS_TXD_P	SGPIO_40	68
71	SDS_TXD_N	SGPIO_41	70
73	GND	SGPIO_42	72
75	SDS_RXD_P	SGPIO_43	74
77	SDS_RXD_N	RFU	76
79	GND		
81	SDS_IO_CLKI_N	GND	78
83	SDS_IO_CLKI_P	5V/VBUS	80
85	GND	GND	82
		USB_TX_N	84
		USB_TX_P	86
87	GND	GND	88
89	SYS_RST	USB_D_N	90
91	TDO	USB_D_P	92
93	TRST	GND	94
95	TDI	USB_RX_N	96
97	TCK	USB_RX_P	98
99	TMS	GND	100
83			S4

Figure 4 - Schematic Pinout, Connector J2

6.2 I2C

The BW2099 SoM offers five dedicated I2C interfaces, I2C0 (EEPROM I2C), I2C1 (CAMA_I2C), I2C2 (CAMB_I2C), I2C3 (CAMD_I2C), I2C4 (PCIe_CLK_I2C) all with 2.2Kohm pull-up resistors (SDA & SCL) to the on-SoM 1.8V rail. For custom baseboard designs, all four I2C interfaces are available and routed through the mezzanine connectors. I2C0 is already used for EEPROM which located on SoM. On most Luxonis baseboards, such as the SJ2088POE, the I2C1 interface is used for communication with the RGB color camera, the I2C2 interface is used to communicate with the pair of stereo cameras, the I2C4 is used for I2C programmability of PCIe clock generator and the I2C3 is typically unused but accessible through test points or connector pads.

6.2.1 EEPROM I2C0 Address Usage

The 32K I2C Serial EEPROM on most Luxonis baseboards is used for revision detect and a storage location for RTL8111HS driver if applicable. With functional address lines 7-bit address for EEPROM is set to 0x50. Use of the I2C0 interface on other components is possible, but with consideration of the existing usage of the EEPROM.

6.2.2 RGB Camera I2C1 Address Usage

The IMX378 RGB camera on most Luxonis baseboards uses some specific addresses as seen in Figure 5. Use of the I2C1 interface on other components is possible, but with consideration of the existing usage of the RGB camera.

IMX378 MODULE CONNECTOR			
MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C	I2C Address (8 bits)	0x34 (Sensor)
	12.3 Mega pixel CMOS		0x18 (VCM driver)
	1/2.3 inch		0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz

Figure 5 - Baseboard I2C1 RGB Camera Module Usage

6.2.3 Stereo Camera I2C2 Address Usage

The pair of OV9282 sensors comprising the stereo pair some Luxonis baseboards uses specific addresses as seen in Figure 6. Use of the I2C2 interface on other components is possible, but with consideration of the existing usage of the stereo camera.

MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A	I2C Address (8 bits)	0xC0(W) 0xC1(R)
	B&W 1 Mega pixel CMOS		
	1/4 inch		
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Figure 6 - Baseboard I2C2 Stereo Camera Module Usage

6.3 MIPI

Four MIPI CSI-2 DPHYv1.2 interfaces are available as input to the SoM. Two are 4-lane interfaces, and the other two interfaces are 2-lane each, all allowing a maximum of 2.1Gbps per lane.

For each of the four camera interfaces, the inter-pair delay of that interface is matched to the clock pair within +/-1ps, and all pairs are routed with 100ohm differential impedance.

6.4 I2S

Three stereo inputs for microphones and one audio output supporting I2S are available routed thorough mezzanine connector. With use of word select up to six microphones can be connected to the interface and two channel stereo audio device can be attached to the SoM.

Pin/ Conn. #	Pin name / Primary Function	SoM GPIO	Alt. 1	PU/PD on SoM	Pin Type	Description
21/B	I2S2_IN_SD0	SGPIO_46			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.
25/B	I2S2_IN_SD1	SGPIO_48			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.
27/B	I2S2_IN_SD2	SGPIO_49			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.
23/B	I2S2_OUT_SD0	SGPIO_47			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.
19/B	I2S2_WS 29	SGPIO_45			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.
17/B	I2S2_SCK	SGPIO_44			1.8V GPIO	Typically used for I2S interface but can be reconfigured to any other GPIO.

Table 1 – I2S Pin Configuration

6.5 PCIe

PCIe Gen 1 lane expansion bus is routed through mezzanine connector B. It supports all standard requirements of PCIe Rev 3.0, version 1.0. External reference clocking should be used for EP/RC applications. The reference clock signal used must be 100MHz.

6.6 USB3.1 Gen2

USB3.1 is exposed it can operate as a device. Maximum of 10Gbps serial data rate can be achieved.

6.7 eMMC

16GB eMMC with 5.1 host controller flash storage device on SoM can be used as a permanent storage medium. It can also be used as storage location for firmware boot images. Fastest recommended eMMC boot mode can be selected with boot mode number 0x1f. Using 8 parallel data lines you can achieve 3Gbits per second data rate and 1.5Gbits data rate for HS400 and HS200 mode respectively.

6.8 PGOOD

PGOOD is a 1.8V open-drain output from the SoM PMIC and is pulled high when the PMIC evaluates power is good. PGOOD has a 10Kohm pull-up resistor to the on-SoM 1.8V rail.

This pin should be left floating if unused or tied to a high-impedance input to sense PGOOD. Do not pull or tie PGOOD to GND.

6.9 WAKEUP

WAKEUP is a 1.8V input to the SoM which should be pulled to GND through a 10Kohm resistor on baseboard. If driven high and sensed during the rising edge of _RST power-on-reset, the on-chip e-fuse is used for boot selection. At present, this functionality is not used on any Luxonis SoM.

The WAKEUP pin was originally intended for waking the SoM from deep sleep mode, but this functionality is not supported on Luxonis SoMs. However, any SGPIO can be used to trigger an interrupt and wake the SoM.

The WAKEUP should be pulled to GND through a 10Kohm resistor on baseboard.

6.10 _RST

_RST is the active-low Myriad X reset input. _RST has a 1.8V 10Kohm pull-up resistor on the SoM, and can be driven low from the baseboard to reset the Myriad X.

6.11 Camera Reference Clocks

Two pins are used to provide a 24MHz reference clock to the image sensor ICs on the baseboard. These signals are on the CAMA_CLK and CAMB_CLK pins of the SoM interface connector. Each signal has a 121Kohm, pull down on the SoM. CAMA_CLK is meant to be used for RGB cameras and CAMB_CLK for grayscale stereo pair cameras. It is possible to create additional reference clocks for additional cameras by reconfiguring an SGPIO pin.

6.12 Camera Reset Signals

Three pins are used for individually resetting or powering down the RGB and stereo pair cameras. These signals are CAMA_RST, CAM_B_D_PWM, and CAM_B_PWDN_N, for both RGB, LEFT, and RIGHT cameras respectively. Each of these signals is 1.8V and are active-low. No pull-up or pull-down resistors are on these signals on the SoM.

6.13 1.8V Shared SPI0 (QSPI)

The signals with prefix "SPI0" are part of a QSPI bus which is shared with the optional on-SoM NOR flash. Note the signal configuration details in Table 2 (refer to the [BW2099 IO TABLE](#) for more details). All signals related to SPI0 are delay-matched on the SoM to +/-100ps to the connector interface.

Pin/ Conn. #	Pin name / Primary Function	SoM GPIO	Alt. 1	PU/PD on SoM	Pin Type	Description
60/A	SGPIO_13/SPI0_CS_1	SGPIO_13	SPI0_CS_1		1.8V GPIO	GPIO, or can be configured as second CS for SPI0, MX in Controller or Peripheral mode. / +/-100ps inter-SPI0
70/A	SPI0_CS_0	SGPIO_23		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR S# / +/-100ps inter-SPI0
74/A	SPI0_SCK	SGPIO_25			1.8V GPIO	Hardwired to 2099 on-board NOR C / +/-100ps inter-SPI0
62/A	SPI0_SIO0	SGPIO_15			1.8V GPIO	Hardwired to 2099 on-board NOR DQ0 / +/-100ps inter-SPI0
64/A	SPI0_SIO1	SGPIO_17			1.8V GPIO	Hardwired to 2099 on-board NOR DQ1 / +/-100ps inter-SPI0
66/A	SPI0_SIO2	SGPIO_19		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR W#/DQ2 / +/-100ps inter-SPI0
68/A	SPI0_SIO3	SGPIO_21		PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR DQ3/HOLD# / +/-100ps inter-SPI0

Table 2 - SPI0 Pin Configuration

With the NOR flash unpopulated the SPI0 bus can be used by the Myriad X in either controller or peripheral mode. With the Myriad X in controller mode, SPI0_CS_0 and SPI0_CS_1 can be used as chip selects for any baseboard peripherals, and additional baseboard chip selects can be configured by using SGPIOs, if required. With the Myriad X in peripheral mode, either the SPI0_CS_0 or SPI0_CS_1 can be used by the baseboard controller to select the Myriad X as a peripheral. Unlike for controller mode, in peripheral mode, SGPIOs cannot be configured as chip selects for the Myriad X, only SPI0_CS_0 and SPI0_CS_1 can be used for this purpose.

With the NOR flash populated, the SPI0 bus can still be used by the Myriad X in either controller or peripheral mode, but the NOR flash now occupies the SPI0_CS_0 location so some care must be taken to avoid contention. With the NOR flash populated, and the Myriad X is in controller mode, the SPI0_CS_0 selects the NOR flash. SPI0_CS_1 (or other reconfigured SGPIO) can be used as a second chip select for baseboard peripherals. When in peripheral mode SPI0_CS_1 should be used as the chip select for the peripheral Myriad X to avoid contention when communicating with NOR flash using SPI0_CS_0.

Note that when an external controller is accessing the NOR flash on the SoM, the Myriad X must not be allowed to access at the same time. Asserting _RST for the Myriad X is an option to prevent this contention.

6.14 3.3V SGPIO Bank

The SoM offers six SGPIO which are 3.3V signaling for easy interface to common peripherals and devices with 3.3V signaling. These SGPIO offer several configurations including SDIO, QSPI, UART, PWM, and I2C, along with general purpose IO and are listed in Table 3 (refer to the [BW2099 IO TABLE](#) for more details).

Pin/Conn. #	Pin name / Primary Function	SoM GPIO	Alt. 1	Alt. 2	Alt. 3	Alt. 4	PU/PD on SoM	Pin Type	Description
40/A	SGPIO_10_3V3	SGPIO_10	sd_hst0_dat_0	spi2_dio_2	pwm_0	I2C3_SDA	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
61/A	SGPIO_14_3V3	SGPIO_14	sd_hst0_clk	spi2_dio_0_mosi			PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
63/A	SGPIO_16_3V3	SGPIO_16	sd_hst0_cmd	spi2_dio_1_miso		I2C3_SCL	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
32/A	SGPIO_4_3V3	SGPIO_4	sd_hst0_dat_3	spi2_cs_0	pwm_3	UART3_TX	PD: 300kR/GND	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
36/A	SGPIO_8_3V3	SGPIO_8	sd_hst0_dat_2	spi2_sclk			PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST
38/A	SGPIO_9_3V3	SGPIO_9	sd_hst0_dat_1	spi2_dio_3		UART3_RX	PU: 40.2kR/1.8V	3.3V GPIO	3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD_HST

Table 3 - 3.3V SGPIO Pin Configuration

6.15.1 3.3V SGPIO Bank - SDIO

The 3.3V SGPIO bank is nominally configured for use with SDIO, as appropriate pull-up and pull-down resistors exist on the SoM. CLK, CMD, and DAT[0:3] are available for use. Optional signals such as card detect can be implemented using the 1.8V SGPIO.

6.15.2 3.3V SGPIO Bank – QSPI (SPI2)

The 3.3V SGPIO bank can be configured as a QSPI bus. The weak pull-up and pull-down resistors on the signal lines (for use as SDIO) are over driven when used as a QSPI interface, though maximum data rates are not guaranteed. Like the SPI0 bank, the 3.3V QSPI interface can operate as a controller or peripheral using the SPI2_CS_0 signal. Additional chip selects can be sent to baseboard peripherals with other 1.8V SGPIO, though the need to level shift from 1.8V to 3.3V may be necessary.

6.16 1.8V SGPIO

The default IO voltage for all SGPIO is 1.8V, with the exceptions of the 3.3V SGPIO listed in Table 3. Each SPGIO can be muxed to alternate functionality as described in Table 4 (refer to the [BW2099 IO TABLE](#) for more details). In addition to muxed functionality, each SGPIO is fully user-programmable with support of four output drive strengths (2mA, 4mA, 8mA, 12mA), selectable output slew-rate (slow/fast), open-drain output mode, LVCMOS/LVTTL compatible input modes with selectable hysteresis, programmable pull-up/pull-down input options, power-on-start capability, and no requirements for power sequencing. Additionally, 100MHz frequency can be achieved with less than 15pF external load, or up to 125MHz with less than 10pF external load.

Pin/Conn. #	Pin name / Primary Function	SoM GPIO	Alt. 1	Alt. 2	PU/PD on SoM	Pin Type	Description
28/A	CAMA_CLK	SGPIO_3			PD: 121kR/GND	1.8V GPIO	24MHz reference clock for Camera A PLL
33/A	CAMA_I2C_SDA	SGPIO_5	pwm5		PU: 2.2kR/1.8V	1.8V GPIO	I2C data for Camera A
34/A	CAMA_RST	SGPIO_6				1.8V GPIO	Camera A reset/power down.
35/A	CAMA_I2C_SCL	SGPIO_7			PU: 2.2kR/1.8V	1.8V GPIO	I2C clock for Camera A
42/A	COM_AUX_IO2	SGPIO_11				1.8V GPIO	Auxiliary GPIO for cameras sync/trigger. Reserved for interrupt FSIN (Frame sync input) for the cameras used.
59/A	SGPIO_12	SGPIO_12			PU: 40.2kR/1.8V	1.8V GPIO	Configured for SDIO card detect, or as regular GPIO. Note 1.8V, 40.2k PU. / +/-100ps inter-SD_HST
60/A	SGPIO_13/SPIO_CS_1	SGPIO_13	SPIO_CS_1			1.8V GPIO	GPIO, or can be configured as second CS for SPIO, MX in Controller or Peripheral mode. / +/-100ps inter-SPIO
62/A	SPIO_SIO0	SGPIO_15				1.8V GPIO	Hardwired to 2099 on-board NOR DQ0 / +/-100ps inter-SPIO
64/A	SPIO_SIO1	SGPIO_17				1.8V GPIO	Hardwired to 2099 on-board NOR DQ1 / +/-100ps inter-SPIO
65/A	CAM_B_D_PWM	SGPIO_18				1.8V GPIO	Camera C reset/power down.
66/A	SPIO_SIO2	SGPIO_19			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR W#/DQ2 / +/-100ps inter-SPIO
67/A	CAM_B_PWDN_N	SGPIO_20				1.8V GPIO	Camera B reset/power down.
68/A	SPIO_SIO3	SGPIO_21			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR DQ3/HOLD# / +/-100ps inter-SPIO
70/A	SPIO_CS_0	SGPIO_23			PU: 1kR/1.8V	1.8V GPIO	Hardwired to 2099 on-board NOR S# / +/-100ps inter-SPIO
73/A	CAMB_CLK	SGPIO_24			PD: 121kR/GND	1.8V GPIO	24MHz reference clock for Camera B PLL
74/A	SPIO_SCK	SGPIO_25				1.8V GPIO	Hardwired to 2099 on-board NOR C / +/-100ps inter-SPIO
77/A	CAMB_I2C_SCL	SGPIO_26			PU: 2.2kR/1.8V	1.8V GPIO	Camera B I2C SDA. Can be used as GPIO.
79/A	CAMB_I2C_SDA	SGPIO_28			PU: 2.2kR/1.8V	1.8V GPIO	Camera B I2C SCL. Can be used as GPIO.
69/A	SGPIO_22	SGPIO_22				1.8V GPIO	
78/A	SGPIO_27	SGPIO_27	I2C3_SCL		PU: 2.2kR/1.8V	1.8V GPIO	Camera C I2C SCL (if applicable). Can be used as GPIO
80/A	SGPIO_29	SGPIO_29	I2C3_SDA		PU: 2.2kR/1.8V	1.8V GPIO	Camera C I2C SDA (if applicable). Can be used as GPIO
59/A	SGPIO_12	SGPIO_12			PU: 40.2kR/1.8V	1.8V GPIO	Configured for SDIO card detect, or as regular GPIO. Note 1.8V, 40.2k PU. / +/-100ps inter-SD_HST

Table 4 - 1.8V SGPIO Pin Configuration (connector A)

28/B	SGPIO_50	SGPIO_50	UART_RX	pwm3		1.8V GPIO	Boot auxiliary GPIO for PCIe can be configured as PCIe_ISOLATE_N
34/B	SGPIO_51	I2C0_SCL			PU: 2.2kR/1.8V	1.8V GPIO	EEPROM I2C_SCL (if applicable). Can be used as GPIO
36/B	SGPIO_52	I2C0_SDA			PU: 2.2kR/1.8V	1.8V GPIO	EEPROM I2C_SDA (if applicable). Can be used as GPIO
42/B	SGPIO_1	SGPIO_1	UART_RX	pwm3		1.8V GPIO	Typically labeled as UART_RX on Luxonis baseboards.
44/B	SGPIO_2	SGPIO_2	UART_TX	pwm2		1.8V GPIO	Typically labeled as UART_TX on Luxonis baseboards.
48/B	SGPIO_30	SGPIO_30				1.8V GPIO	General purpose 1.8V IO
50/B	SGPIO_31	SGPIO_31				1.8V GPIO	General purpose 1.8V IO
52/B	SGPIO_32	SGPIO_32				1.8V GPIO	General purpose 1.8V IO
54/B	SGPIO_33	SGPIO_33				1.8V GPIO	General purpose 1.8V IO
56/B	SGPIO_34	SGPIO_34				1.8V GPIO	General purpose 1.8V IO
58/B	SGPIO_35	SGPIO_35				1.8V GPIO	General purpose 1.8V IO
60/B	SGPIO_36	SGPIO_36				1.8V GPIO	General purpose 1.8V IO
62/B	SGPIO_37	SGPIO_37				1.8V GPIO	General purpose 1.8V IO
64/B	SGPIO_38	SGPIO_38				1.8V GPIO	General purpose 1.8V IO
66/B	SGPIO_39	SGPIO_39				1.8V GPIO	General purpose 1.8V IO
68/B	SGPIO_40	SGPIO_40				1.8V GPIO	General purpose 1.8V IO
70/B	SGPIO_41	SGPIO_41				1.8V GPIO	General purpose 1.8V IO
72/B	SGPIO_42	SGPIO_42				1.8V GPIO	General purpose 1.8V IO
74/B	SGPIO_43	SGPIO_43				1.8V GPIO	General purpose 1.8V IO

Table 5 - 1.8V SGPIO Pin Configuration (connector B)

7 BOOT Modes

The boot signals are broken out from the SoM and routed through the mezzanine connector which offers the end user the option to easily configure the boot mode by setting the BOOT[4:0] bits high (1.8V) or low. These bits are sampled on the rising edge of _RST during power-on-reset, and allow for boot from USB, NOR flash, eMMC, SPI, and Ethernet (RTL8111HS driver in EEPROM).

To configure the NOR flash boot mode, set the bits to 0x8 [0b01000]. In this configuration, the Myriad X acts as an SPI controller on SPI0 to boot from the NOR flash with SPI settings: 24-bit address, Quad I/O, and at a rate of 50MHz. It is also possible to boot with the Myriad X configured as an SPI peripheral, but this feature is not yet fully supported.

To configure USB boot, set the bits to 0x16 [0b10110]. In this configuration, the Myriad X will boot using the USB 2 interface.

To configure eMMC boot, set the bits to 0x1f [0b11111]. In this configuration, the Myriad X will boot using the 8-bit, SDR104 mode in HS200 and HS400 mode.

To configure PCIe boot, set the bits to 0x14 [0b10100]. In this configuration, the Myriad X will boot using PCIe Gen 2 interface. With use of RTL8111HS Ethernet controller on baseboard device will boot from Ethernet interface.

Pin/ Conn. #	Pin name / Primary Function	SoM GPIO	Alt. 1	Alt. 2	PU/PD on SoM	Pin Type	Description
18/B	BOOT4					1.8V set BOOT pin	Boot register set pin bit 4 (MSB)
20/B	BOOT3					1.8V set BOOT pin	Boot register set pin bit 3
22/B	BOOT2					1.8V set BOOT pin	Boot register set pin bit 2
24/B	BOOT1					1.8V set BOOT pin	Boot register set pin bit 1
26/B	BOOT0					1.8V set BOOT pin	Boot register set pin bit 0 (LSB)

Table 6 - BOOT Pin Configuration

8 Mechanical Information

The following information is the most current data available for the designated device. This data is subject to change without notice and without revision of this document.

8.1 BW2099 Dimensions

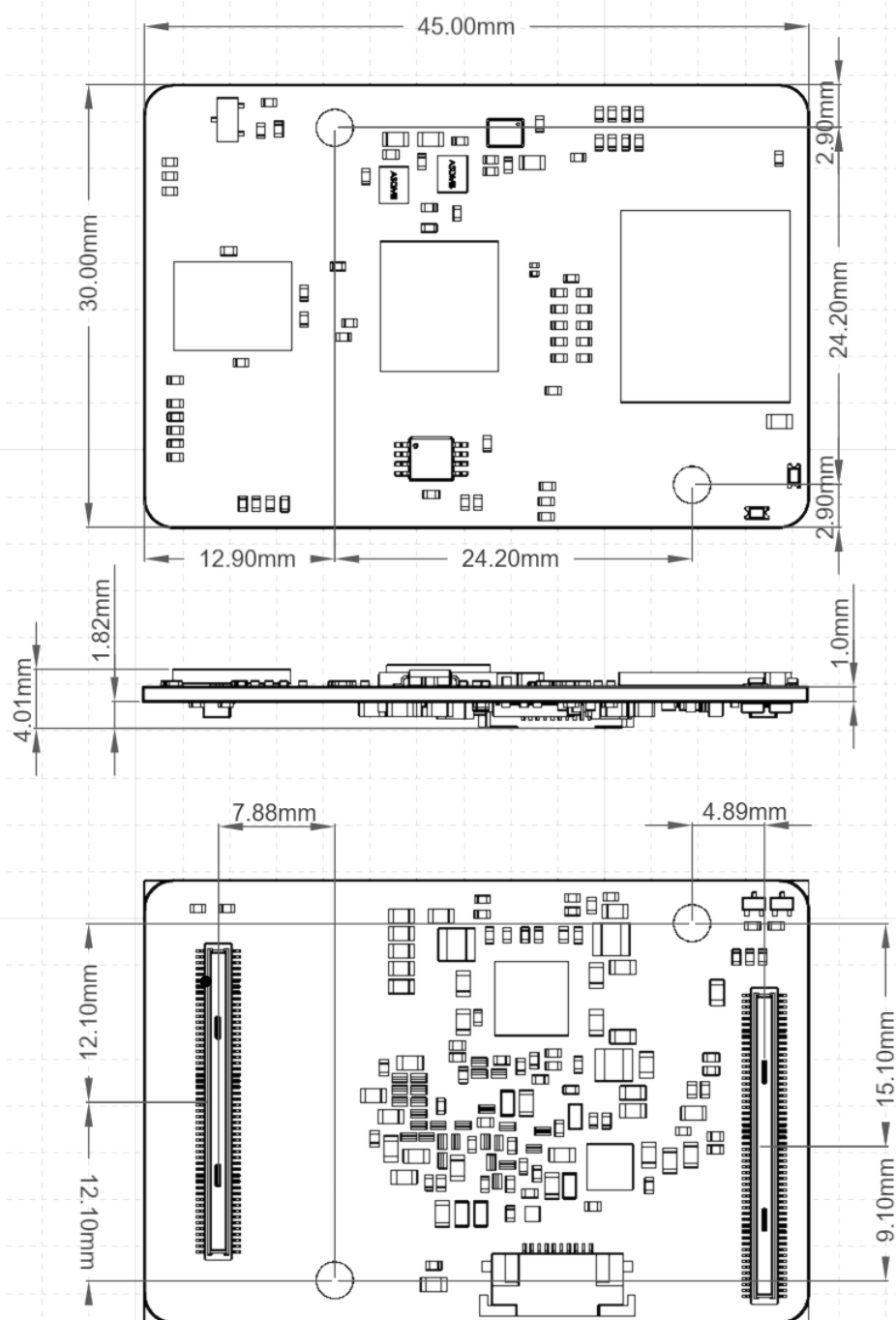


Figure 7 – Top, Side, and Bottom dimensions

8.2 Recommended Mounting Configuration

The BW2099 SoM is designed to be used with a 3mm mated-height connector and accompanying 3mm standoffs. The B2B connector plugs are on the BW2099 (Hirose DF40C-100DP-0.4V), while the receptacle, which determines mated height, is on the baseboard (Hirose DF40HC(3.0)-100DS-0.4V). Wuerth Elektronik 9774030243R SMT standoffs are recommended.

8.3 BW2099 Mounting Holes

The BW2099 has 2 M2.5 mounting holes for securing the SoM. These mounting holes use a 2.6mm ID, and a 5.5mm OD pad, which is tied to SoM GND. M2-0.40 screws can be used with these pads to secure the SoM to the recommended Wuerth Elektronik 9774030243R SMT standoffs, or a custom solution using M2-0.40 or M2.5-0.45 screws can be used. Note that when using M2.5-0.45 screws, there is reduced tolerance between the B2B connector clocking and the screws' hole alignment. This must be accounted for to ensure proper connector mating.

8.4 SoM Clearance

3mm is the board-to-board standoff height when using the recommended mounting configuration, however, components on the underside of the BW2099 reduce this clearance. For highest design reliability, it is recommended not to place components on the baseboard underneath the SoM, but components with max height <1mm will have clearance.

In previous designs many components have been successfully placed on the baseboard beneath the SoM making careful use of the 3D STEP file of the SoM, which is available online [here BW2099](#).

9 Thermal Information

Power consumption can vary considerably depending on the application. A stereo vision application running Mobilenet-SSD V2 at 30fps typically consumes about 2.5W, but more aggressive applications can consume closer to 5W. Most of this power is consumed by the MA2485. While the VFBGA provides an excellent thermal path from the MA2485 to the SoM, the thermal sink is small, and the part temperature can quickly rise toward the 105C max die temperature.

Heatsinking of the MA2485 is required for most applications.

Table 7 details thermal parameters for the MA2485 simulated in a still air environment, an ambient temperature of 25C, 2W power dissipation, and under the test conditions described in JESD51-2A.

Parameter	Value (C/W)	Description
θ_{JB}	5.8	Junction-to-board thermal resistance (EIA/JESD51-8)
θ_{JC}	3.1	Junction-to-case thermal resistance
θ_{JA}	21.4	Junction-to-ambient thermal resistance (EIA/JESD51-2)

Table 7 - MA2485 Thermal Parameters

10 Revision History

- Initial Release – June 2020
- Revision 0.1 – February 2021
 - Added block diagram
 - Added description for all interfaces
 - Updated connectors pinout and mechanical information