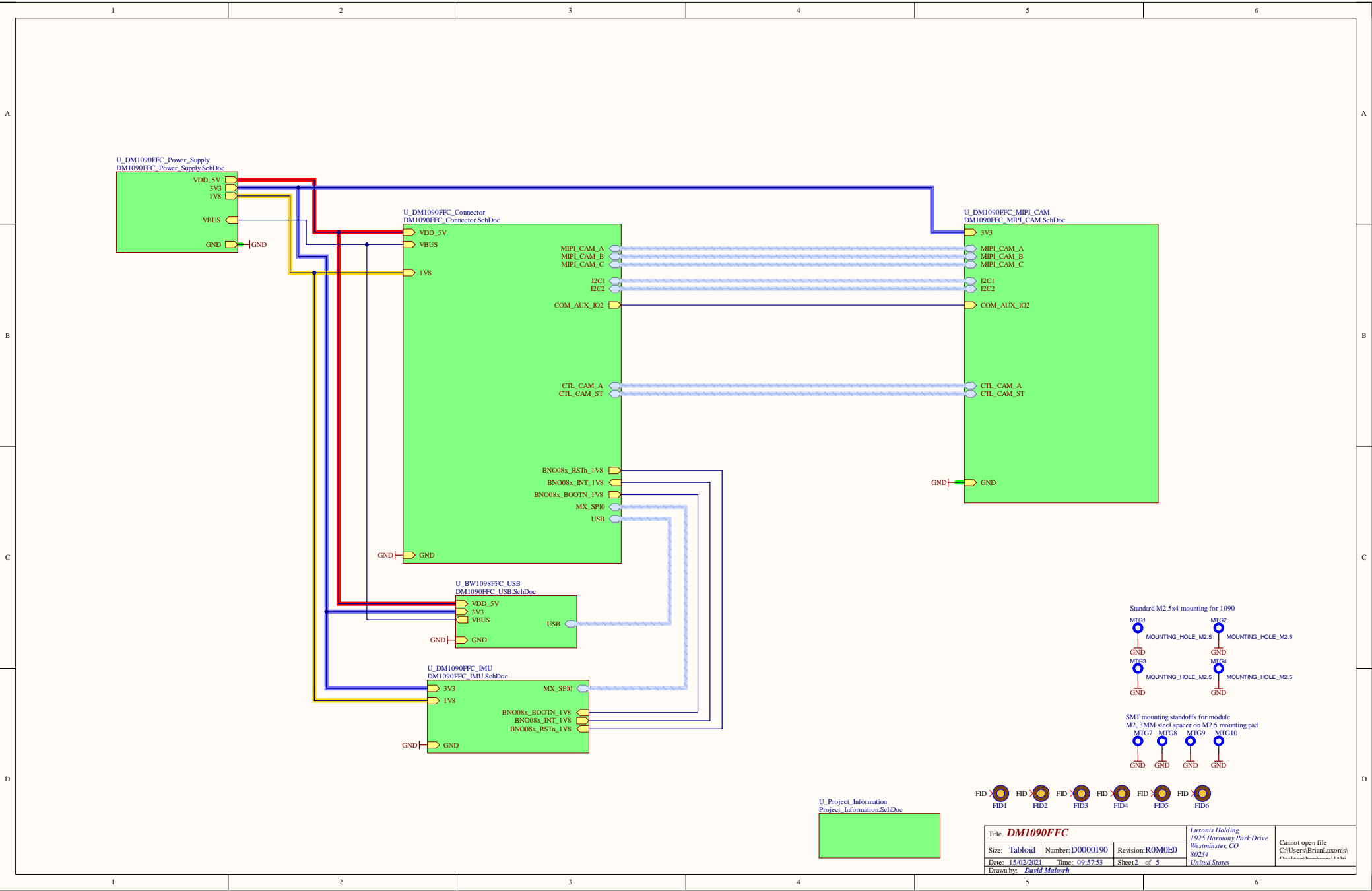


Project: *DM1090FFC*
Current Revision: *R0M0E0*

DM1090FFC Revision History:

Date	Revision	Reason for Change	Changes Implemented
12/28/2020	R1M1E2 -> R0M0E0	1) ESD protection 2) FFC connector stronger mechanics 3) Updating board with overvoltage protection and ideal diode to or USB VBUS and Barrel jack 5V 4) Outdated stack 5) Unused reset circuit 6) Unused strobe configuration resistors	1) Added protection diodes to MIPI lines 2) Changed FFC with Molex 505278 series 3) Added ideal diodes and zener diode for protection 4) Standardized 4L stackup rerouted all differential pairs and tuned lengths 5) Deleted reset circuit and its components and rerouted signals 6) Deleted strobe configuration resistors with corresponding silk and tracks
02/12/2020	DM1098FFC R0M0E0 -> DM1090FFC R0M0E0	1) Add IMU 2) Change FFC connectors type and pinout to ArduCam standard so that camera modules from Arducam can be connected directly without board adapter 3) Add BOOT_SEL button to PCB	1) Added IMU from OAK-D and modified length tuning for SPI to connector 2) Changed FFC connectors to ArduCam standard pinout, updated all connections to the connectors. Cameras from Arducam can be connected with same side dedicated FFC. Changed 3V3 power rail LDO with switcher with higher ampacity to supply camera modules 3) Added push-button connected to 1V8 and BOOT_SEL pin on BW1099 connector

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[illegible]

D6

CAM_L_D0_N	1	IO1	NC	10	CAM_L_D0_N
CAM_L_D0_P	2	IO2	NC	9	CAM_L_D0_P
	3	GND	GND	8	
CAM_L_D1_N	4	IO3	NC	7	CAM_L_D1_N
CAM_L_D1_P	5	IO4	NC	6	CAM_L_D1_P

TPD4E02B04DQAR

D7

CAM_L_C_N	1	IO1	NC	10	CAM_L_C_N
CAM_L_C_P	2	IO2	NC	9	CAM_L_C_P
	3	GND	GND	8	
CAM_L_PWDN	4	IO3	NC	7	CAM_L_PWDN
STEREO_CLK	5	IO4	NC	6	STEREO_CLK

TPD4E02B04DQAR

D6

MIPI_D0_N	1	IO1	NC	10	MIPI_D0_N
MIPI_D0_P	2	IO2	NC	9	MIPI_D0_P
	3	GND	GND	8	
MIPI_D1_N	4	IO3	NC	7	MIPI_D1_N
MIPI_D1_P	5	IO4	NC	6	MIPI_D1_P

TPD4E02B04DQAR

D7

MIPI_C_N	1	IO1	NC	10	MIPI_C_N
MIPI_C_P	2	IO2	NC	9	MIPI_C_P
	3	GND	GND	8	
MIPI_D2_N	4	IO3	NC	7	MIPI_D2_N
MIPI_D2_P	5	IO4	NC	6	MIPI_D2_P

TPD4E02B04DQAR

D9

CAM_R_D0_N	1	IO1	NC	10	CAM_R_D0_N
CAM_R_D0_P	2	IO2	NC	9	CAM_R_D0_P
	3	GND	GND	8	
CAM_R_D1_N	4	IO3	NC	7	CAM_R_D1_N
CAM_R_D1_P	5	IO4	NC	6	CAM_R_D1_P

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D10

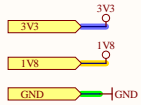
MIPI_D3_N	1	IO1	NC	10	MIPI_D3_N
MIPI_D3_P	2	IO2	NC	9	MIPI_D3_P
	3	GND	GND	8	
CAM_RST	4	IO3	NC	7	CAM_RST
CAM_CLK	5	IO4	NC	6	CAM_CLK

TPD4E02B04DQAR

D11

CAM_R_C_N	1	IO1	NC	10	CAM_R_C_N
CAM_R_C_P	2	IO2	NC	9	CAM_R_C_P
	3	GND	GND	8	
CAM_R_PWDN	4	IO3	NC	7	CAM_R_PWDN
STEREO_CLK	5	IO4	NC	6	STEREO_CLK

TPD4E02B04DQAR



* For the switching sequence of power supply VDD and VDDIO it is mandatory that VDD is powered on and driven to the specified level before or at the same time as VDDIO is powered ON. Otherwise there are no limitations on the voltage levels of both pins relative to each other as long as they are used within the specified operating range.

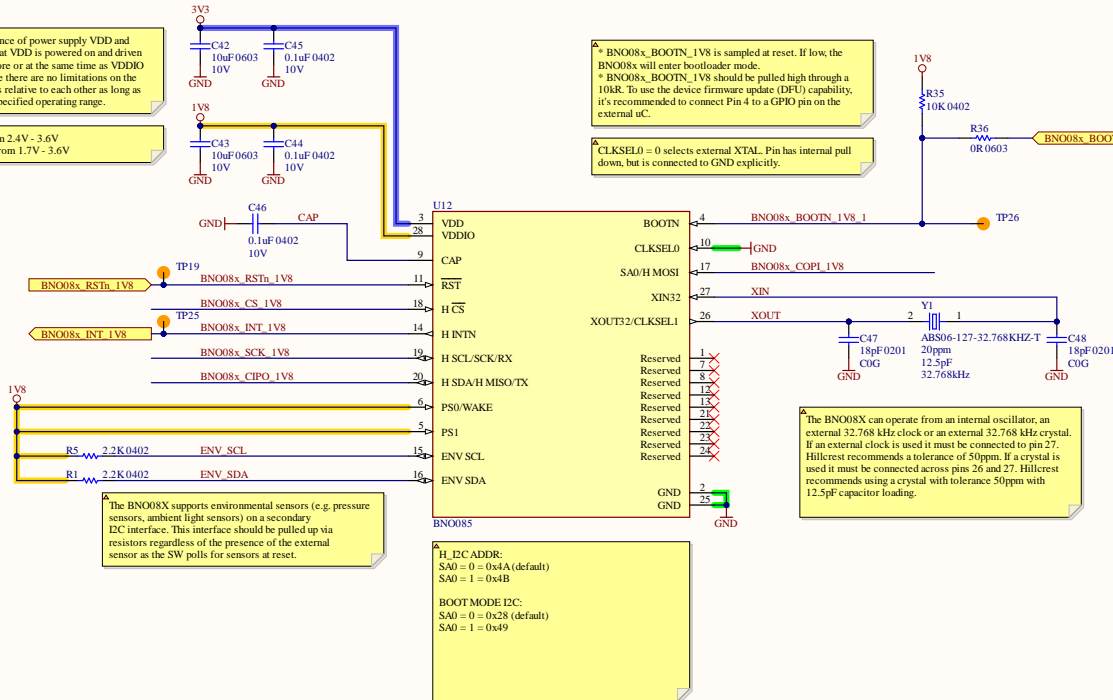
VDD can be powered from 2.4V - 3.6V
VDDIO can be powered from 1.7V - 3.6V

NRST is the reset line for the BNO08X and can be either driven by the application processor or the board reset.

The H_INTN pin is the application interrupt line that indicates the BNO08X requires attention. This should be tied to a GPIO with wake capability. The interrupt is active low. On the BNO085, if the host fails to respond to the assertion of H_INTN within approximately 10 ms, the BNO085 will timeout, deassert H_INTN and retry the operation.

Pin 5 (PS1) and Pin 6 (PS0/WAKE) are the host interface protocol selection pins. For SPI selection, both pins must be high (from before reset until after the first assertion of H_INTN to select the SPI interface. Pin 5 may be tied to VDDIO. Pin 6 must be connected to a GPIO so that the WAKE functionality can be performed.

After reset the PS0/WAKE signal is used as a 'wake' signal taking the BNO08X out of sleep if the host wants to initiate communication with the BNO08X.



* BNO08X_BOOTN_1V8 is sampled at reset. If low, the BNO08X will enter bootloader mode.
* BNO08X_BOOTN_1V8 should be pulled high through a 10kΩ. To use the device firmware update (DFU) capability, it's recommended to connect Pin 4 to a GPIO pin on the external uC.

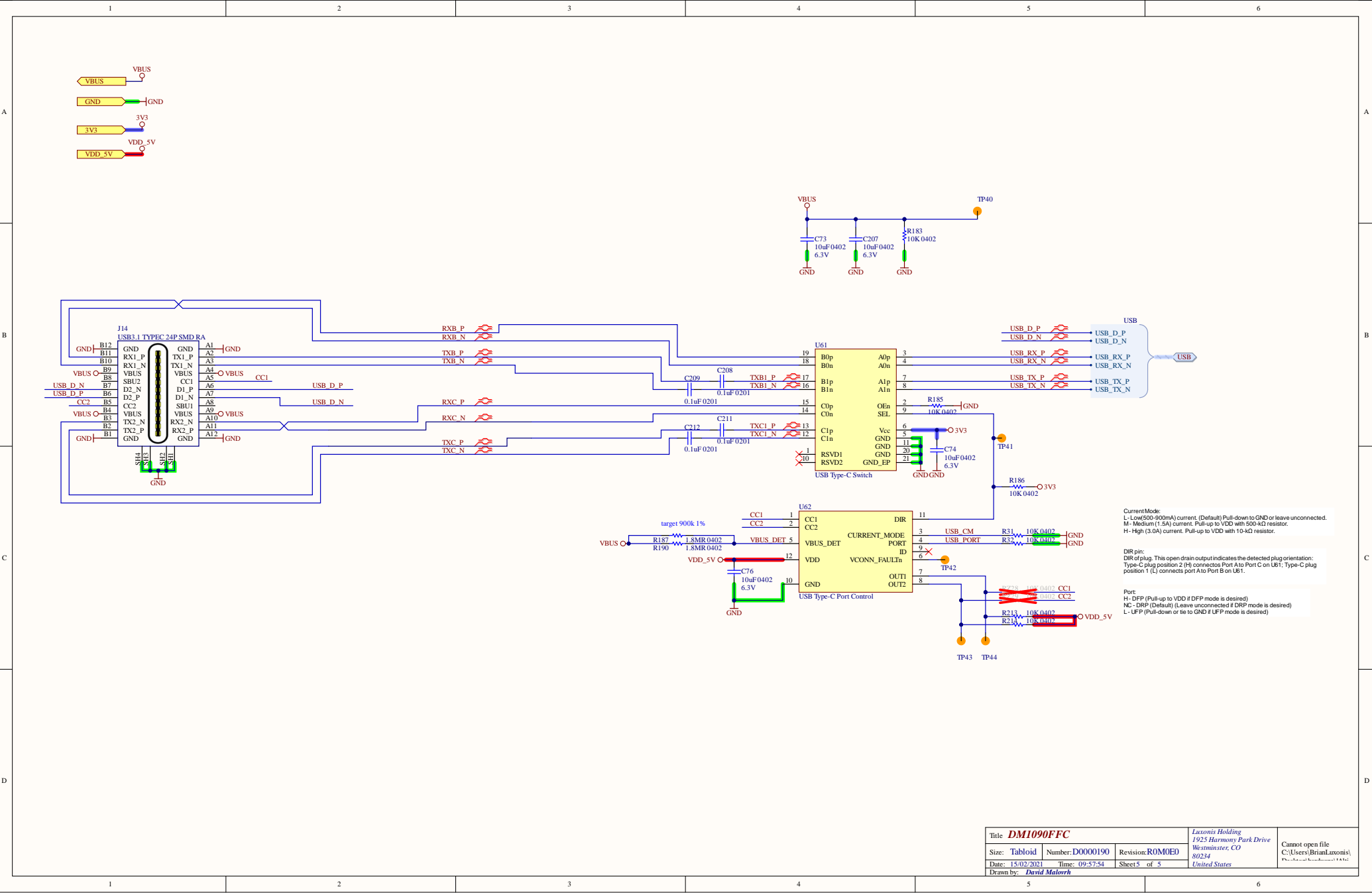
* CLKSEL0 = 0 selects external XTAL. Pin has internal pull down, but is connected to GND explicitly.

The BNO08X can operate from an internal oscillator, an external 32.768 kHz clock or an external 32.768 kHz crystal. If an external clock is used it must be connected to pin 27. Hillcrest recommends a tolerance of 50ppm. If a crystal is used it must be connected across pins 26 and 27. Hillcrest recommends using a crystal with tolerance 50ppm with 12.5pF capacitor loading.

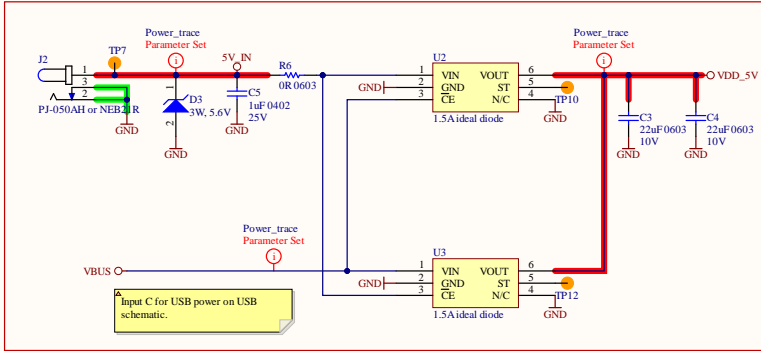
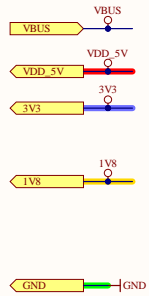
H_I2C-ADDR:
SA0 = 0 = 0x4A (default)
SA0 = 1 = 0x4B

BOOT MODE I2C:
SA0 = 0 = 0x28 (default)
SA0 = 1 = 0x49

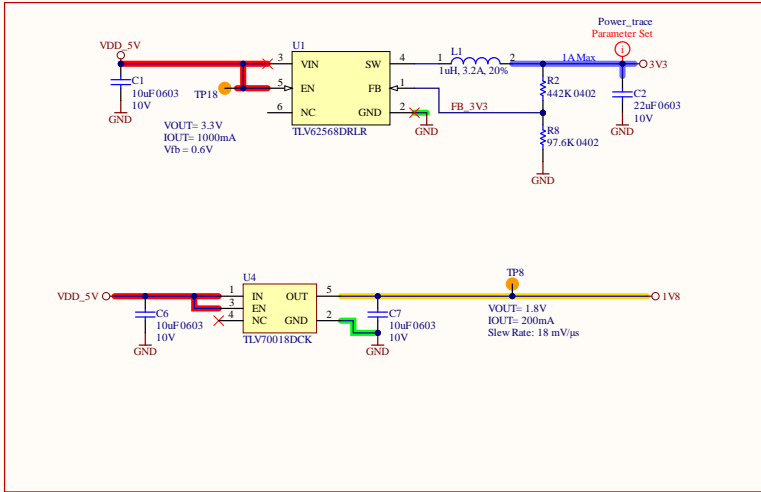
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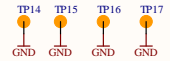
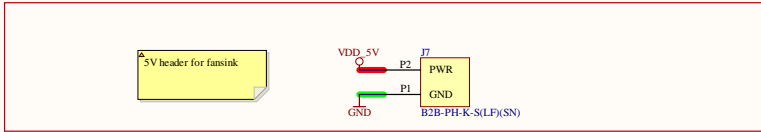
POWER INPUT - DIODE OR



POWER REGULATION



FAN CONTROLLER



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