Project: ***BW2098POE***
Current Revision: ***R3M1E3***

BW2098POE Revision History:

Date	Revision	Reason for Change	Changes Implemented
3/4/2020	Iniital Release -> R0M0E0		
5/29/2020	R0M0E0 --> R1M1E1	1) Pull up the EN pin on the 3.3V regulator 2) R1 should be depopulated (PU for MA2485 WAKEUP line) 3) Add ESD protection diodes to the Ethernet lines 4) LEDs labels for "nRST" and "5V" are switched. 5) Polygon 3V3_L01_P425 is underneath GND polygon on Layer 1 and didn't pour correctly (still electrically connected by tracing). 6) J5/J8 are a bit too close for both cable housings 7) RGB camera connector tab hard to get to as it's under the BW2099 8) Label the boot switches 9) KingTop doesn't like the L1 inductor. Says it's too fragile and hard to handle. Try to find alternate.	1) 3.3V regulator EN pin pulled high to 5V 2) Depopulated R1 on Production variant 3) Added pads for ESD protection diodes on ethernet diff pairs 4) Swapped "nRST" and "5V" labels on overlay and added netnames to LEDs in schematic to help prevent this in the future. 5) Removed polygon and thickened traces 6) Increased connector spacing by 50mils to allow clearance 7) Moved connector 2mm right to make it a bit easier to grab the latch. Still not great, but better. 8) Added overlay labeling for each BOOT[4:0] and GPIO58 9) Moved the L1 inductor to L1 on layout so it wasn't so exposed to impacts. Did not change PN or schematic.
7/23/2020	R1M1E1 --> R2M1E2	1) C35 preventing bridge from functioning properly. 2) Labeling of "GPIO6" is incorrect. Should be "GPIO8"	1) Removed C35 from PCB and BOM. 2) Changed references of GPIO6 to GPIO8. No physical change to PCB.
04/21/2021	R2M1E2 --> R3M1E3	1) Slow plug issue with USB type-C	1. Added 1uF capacitor to VBUS_DET updated PCB and fabrication files

Title ***BW2098POE***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number: D2098000	Revision: R3M1E3		
Date: 21/04/2021 Time: 12:04:26		Sheet 1 of 12		
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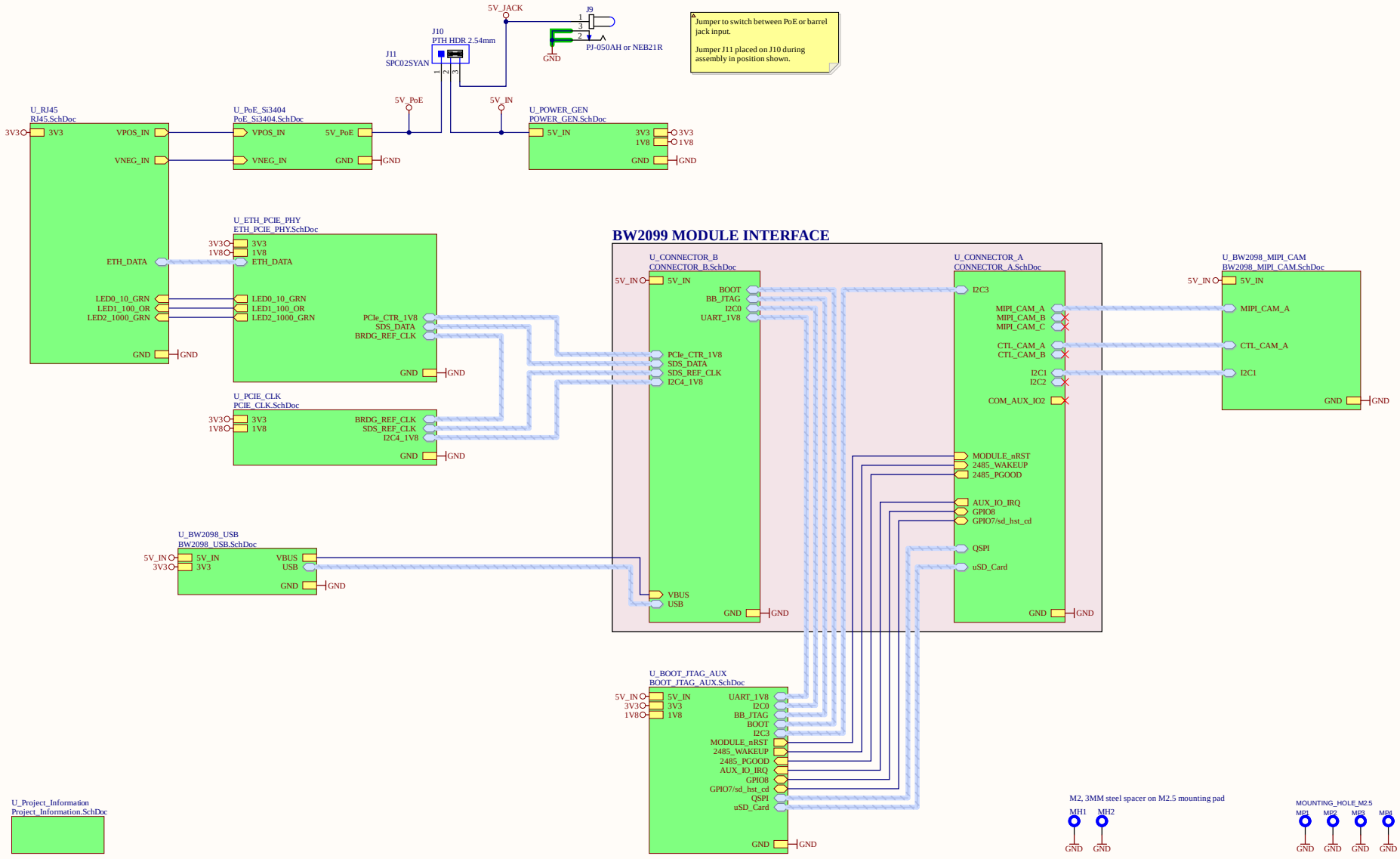
BW2099 MODULE INTERFACE
5V_JACK
J9
PJ-050AH or NEB21R
GND
J10
PTH HDR 2.54mm
J11
SPC02SYAN
Jumper to switch between PoE or barrel jack input.
Jumper J11 placed on J10 during assembly in position shown.
5V_PoE
5V_IN
U_RJ45
RJ45.SchDoc
3V3
VPOS_IN
VNEG_IN
GND
U_PoE_Si3404
PoE_Si3404.SchDoc
VPOS_IN
5V_PoE
VNEG_IN
GND
U_POWER_GEN
POWER_GEN.SchDoc
5V_IN
3V3
1V8
GND
U_ETH_PCIE_PHY
ETH_PCIE_PHY.SchDoc
3V3
1V8
ETH_DATA
LED0_10_GRN
LED1_100_OR
LED2_1000_GRN
PCIe_CTR_1V8
SDS_DATA
BRDG_REF_CLK
GND
U_PCIE_CLK
PCIE_CLK.SchDoc
3V3
1V8
BRDG_REF_CLK
SDS_REF_CLK
I2C4_1V8
GND
U_BW2098_USB
BW2098_USB.SchDoc
5V_IN
3V3
VBUS
USB
GND
U_CONNECTOR_B
CONNECTOR_B.SchDoc
5V_IN
BOOT
BB_JTAG
I2C0
UART_1V8
PCIe_CTR_1V8
SDS_DATA
SDS_REF_CLK
I2C4_1V8
VBUS
USB
GND
U_CONNECTOR_A
CONNECTOR_A.SchDoc
I2C3
MIPI_CAM_A
MIPI_CAM_B
MIPI_CAM_C
CTL_CAM_A
CTL_CAM_B
I2C1
I2C2
COM_AUX_IO2
MODULE_nRST
2485_WAKEUP
2485_PGOOD
AUX_IO_IRQ
GPIO8
GPIO7/sd_hst_cd
QSPI
uSD_Card
GND
U_BW2098_MIPI_CAM
BW2098_MIPI_CAM.SchDoc
5V_IN
MIPI_CAM_A
CTL_CAM_A
I2C1
GND
U_BOOT_JTAG_AUX
BOOT_JTAG_AUX.SchDoc
5V_IN
3V3
1V8
UART_1V8
I2C0
BB_JTAG
BOOT
I2C3
MODULE_nRST
2485_WAKEUP
2485_PGOOD
AUX_IO_IRQ
GPIO8
GPIO7/sd_hst_cd
QSPI
uSD_Card
GND
U_Project_Information
Project_Information.SchDoc
M2, 3MM steel spacer on M2.5 mounting pad
MH1
MH2
GND
MOUNTING_HOLE_M2.5
MP1
MP2
MP3
MP4
FID
FID1
FID2
FID3
FID4
FID5
FID6
Title BW2098POE
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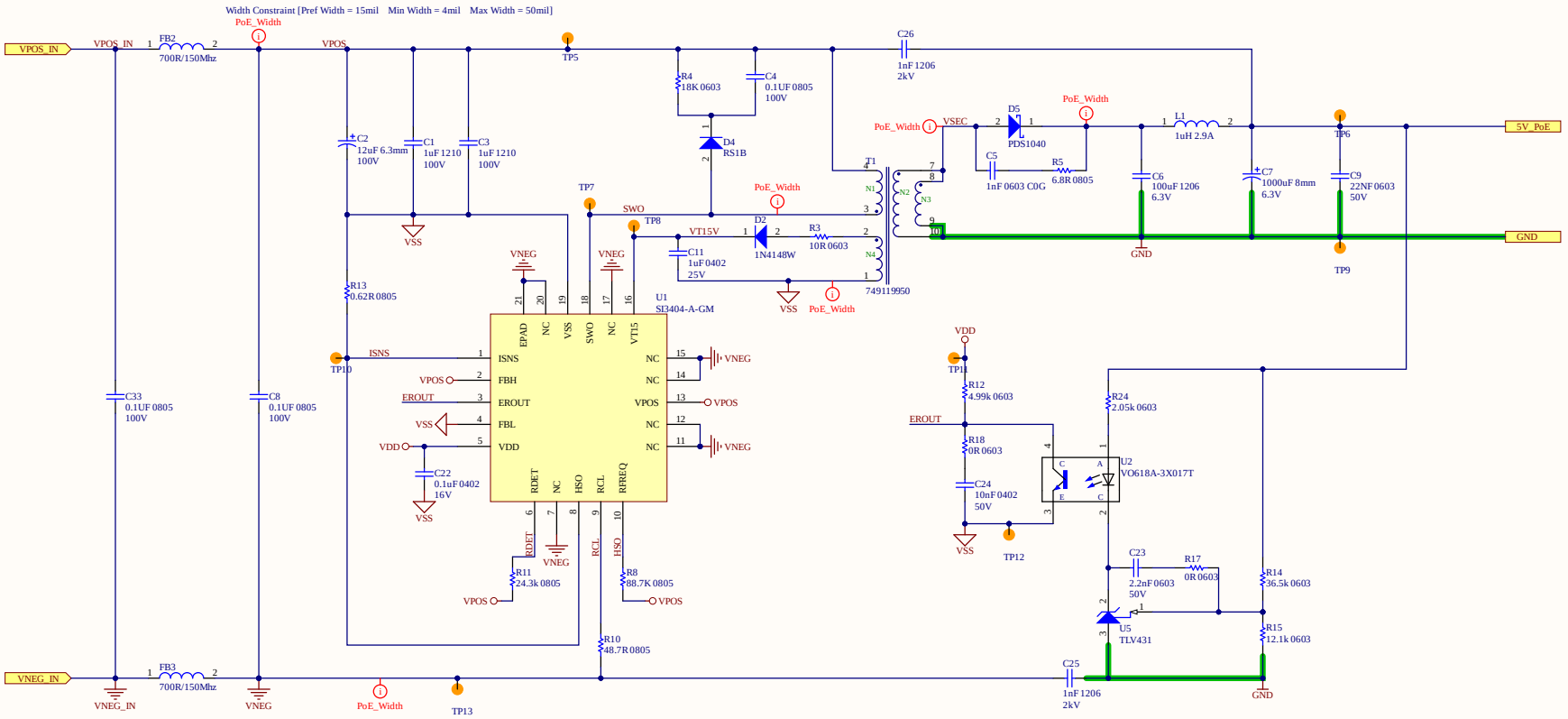
Width Constraint [Pref Width = 15mil Min Width = 4mil Max Width = 50mil]
PoE_Width
VPOS_IN
VPOS_IN
FB2
700R/150Mhz
VPOS
TP5
C26
1nF 1206
2kV
R4
18K 0603
C4
0.1UF 0805
100V
D4
RS1B
C2
12uF 6.3mm
100V
C1
1uF 1210
100V
C3
1uF 1210
100V
VSS
TP7
SWO
TP8
PoE_Width
D2
1N4148W
R3
10R 0603
VT15V
C11
1uF 0402
25V
VSS
PoE_Width
T1
749119950
N1
N2
N3
N4
PoE_Width
VSEC
D5
PDS1040
PoE_Width
L1
1uH 2.9A
C5
1nF 0603 C0G
R5
6.8R 0805
C6
100uF 1206
6.3V
C7
1000uF 8mm
6.3V
C9
22NF 0603
50V
TP6
TP9
5V_PoE
GND
GND
VNEG
VNEG
R13
0.62R 0805
U1
SI3404-A-GM
EPAD
NC
VSS
SWO
NC
VTI5
ISNS
FBH
EROUT
FBL
VDD
NC
NC
VPOS
NC
NC
RDET
NC
HSO
RCL
RFREQ
TP10
ISNS
VPOS
EROUT
VSS
VDD
C22
0.1uF 0402
16V
VSS
VNEG
VNEG
VNEG
VNEG
VPOS
VPOS
VPOS
RDET
RCL
HSO
R11
24.3k 0805
R8
88.7K 0805
R10
48.7R 0805
VDD
TP11
R12
4.99k 0603
EROUT
R18
0R 0603
C24
10nF 0402
50V
VSS
TP12
U2
VO618A-3X017T
R24
2.05k 0603
C23
2.2nF 0603
50V
R17
0R 0603
R14
36.5k 0603
U5
TLV431
R15
12.1k 0603
C33
0.1UF 0805
100V
C8
0.1UF 0805
100V
VNEG_IN
FB3
700R/150Mhz
VNEG_IN
VNEG
PoE_Width
TP13
C25
1nF 1206
2kV
GND
VNEG is a thermal plane as well as ESD and EML Use thermal vias to at least 1 inch square plane on backside.
Schematic based on the reference design for the SI3404 PoE.
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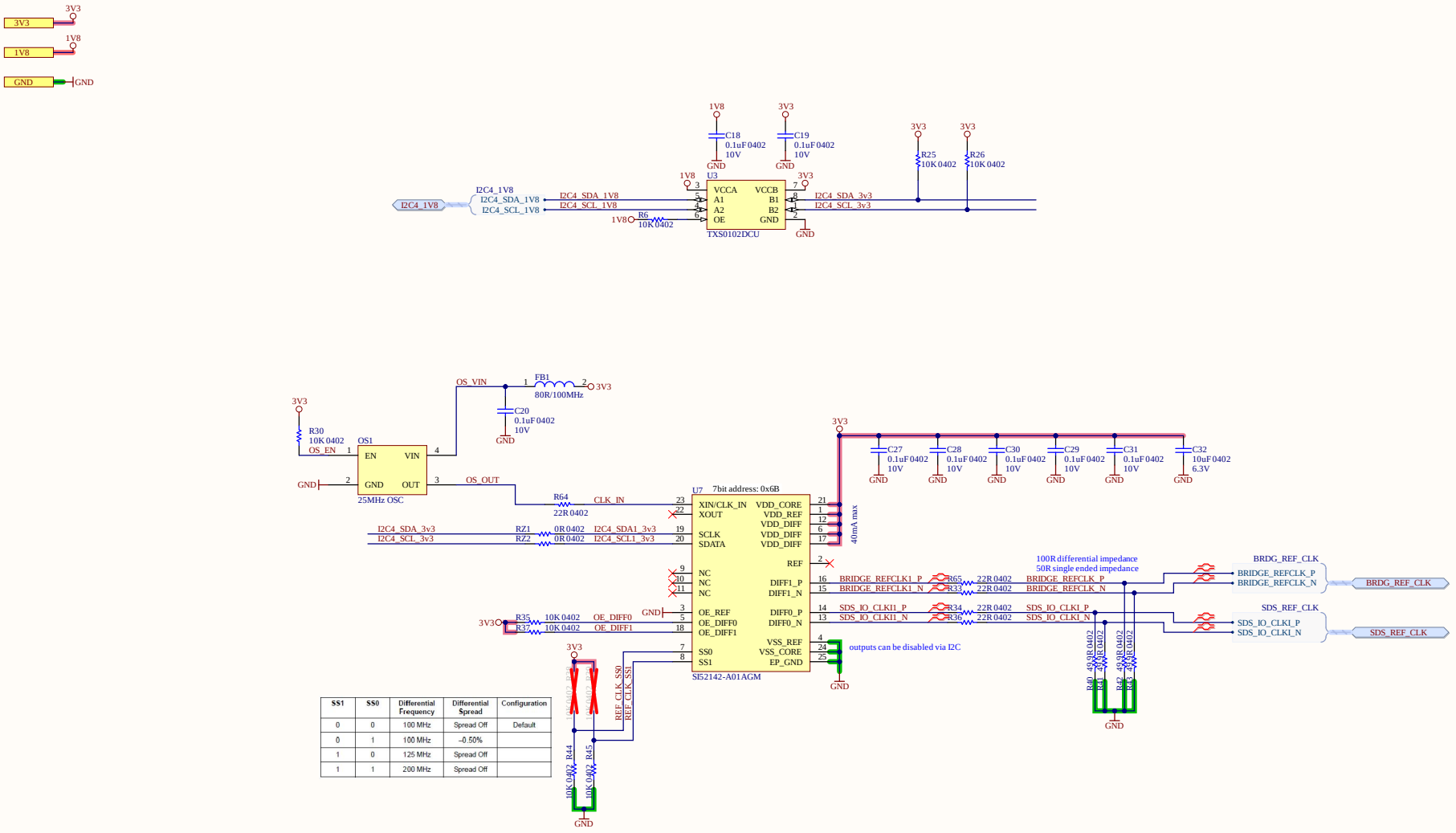

SS1	SS0	Differential Frequency	Differential Spread	Configuration
0	0	100 MHz	Spread Off	Default
0	1	100 MHz	-0.50%	
1	0	125 MHz	Spread Off	
1	1	200 MHz	Spread Off	

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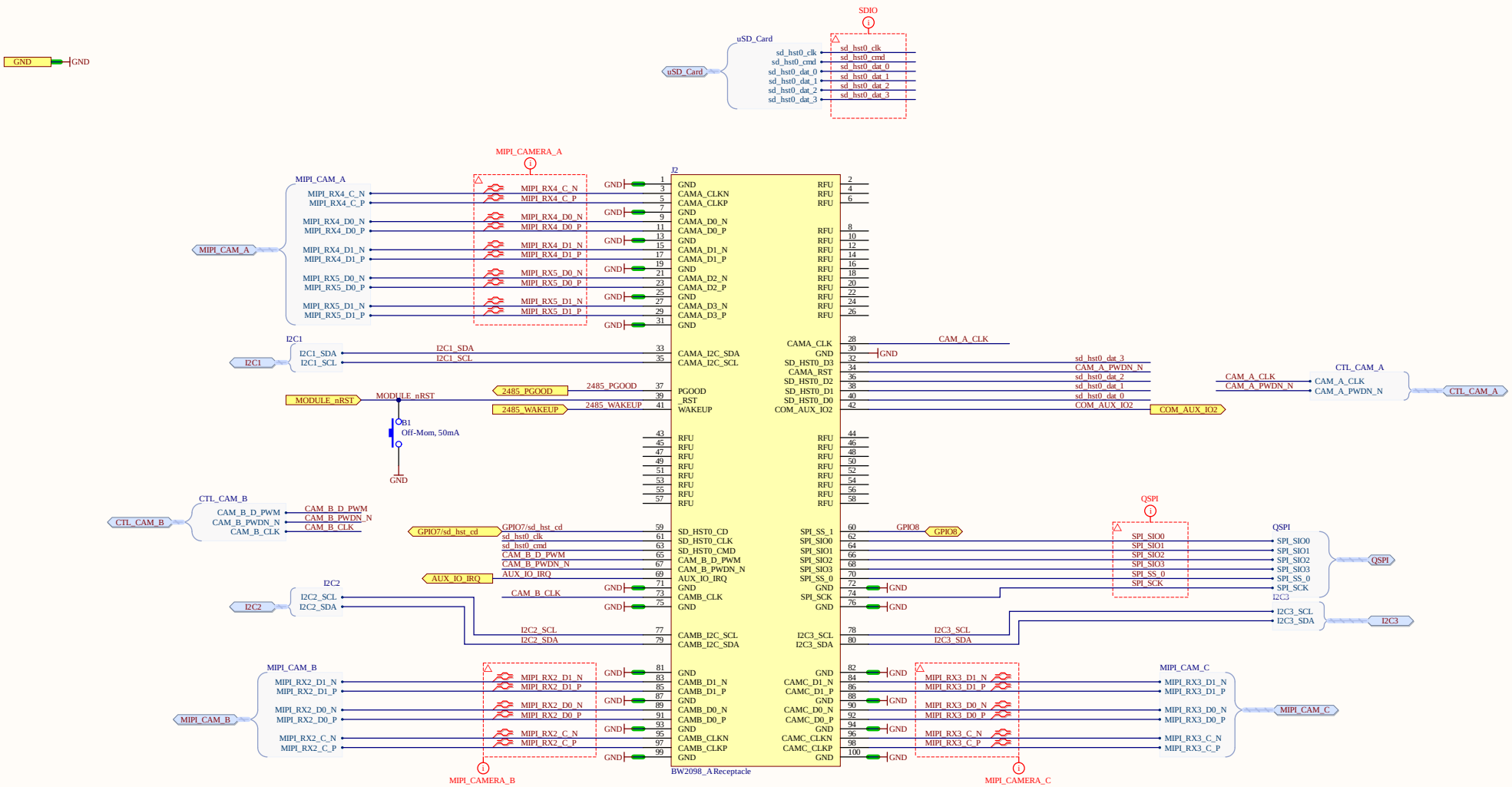

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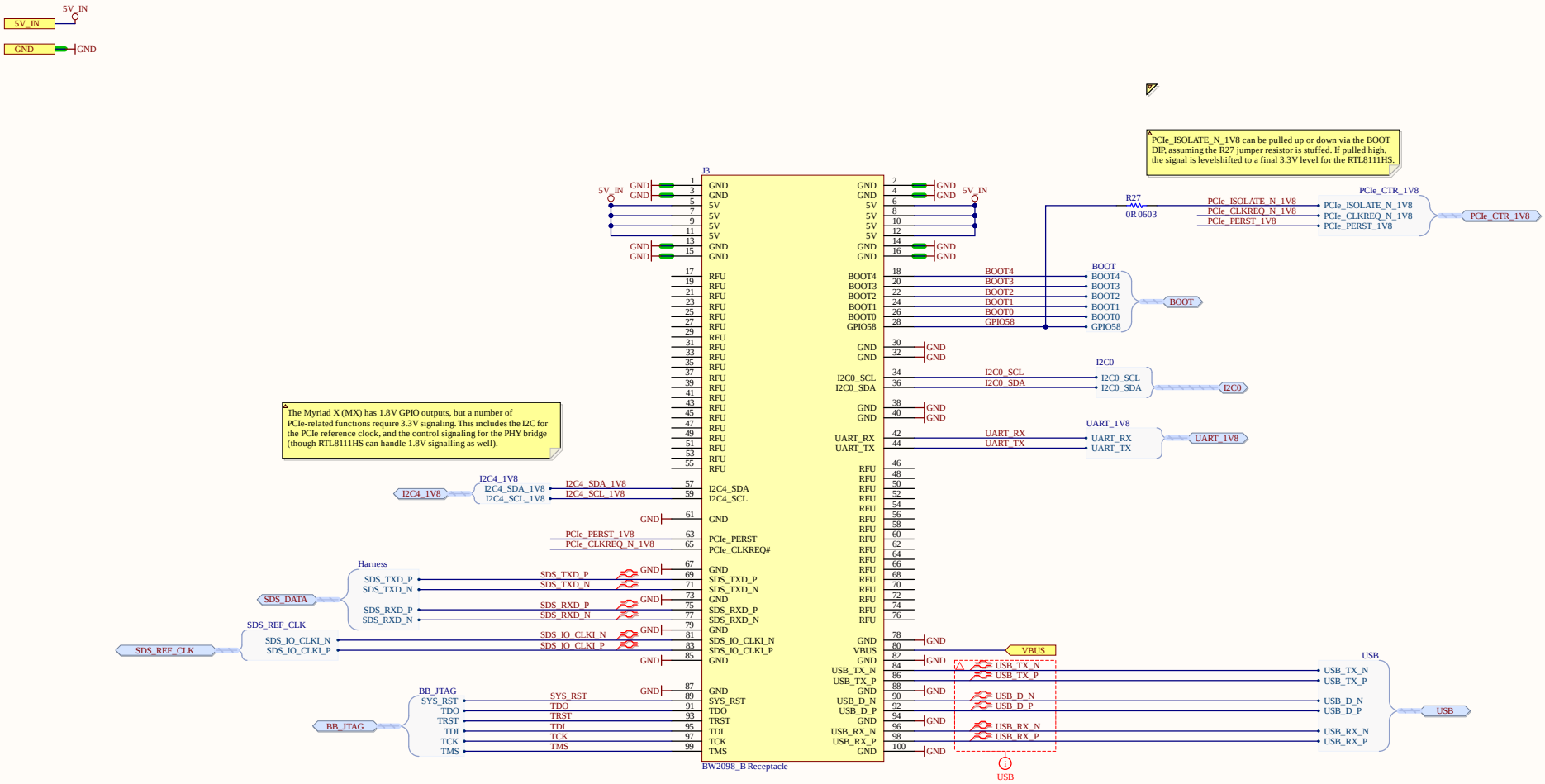

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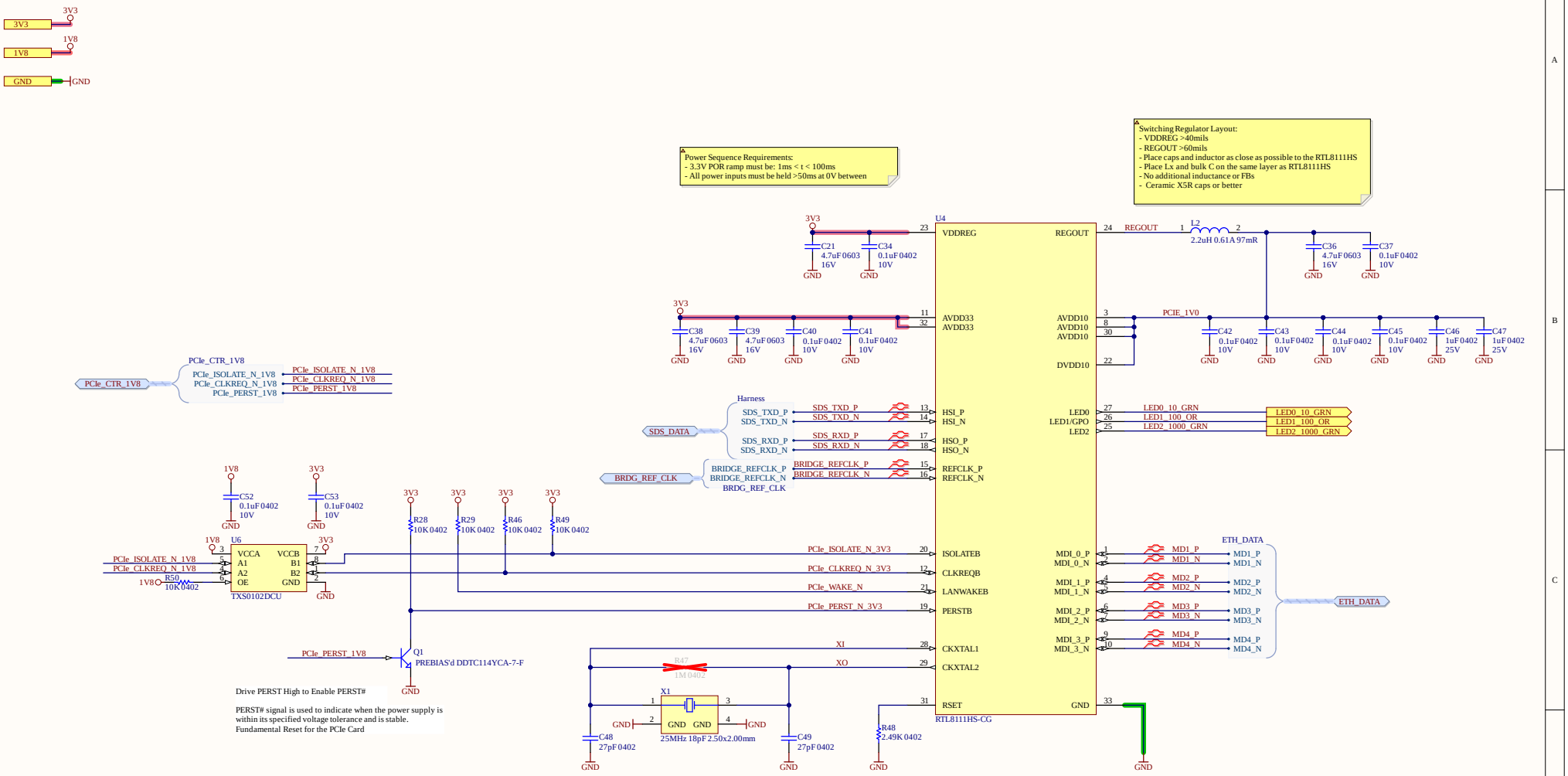

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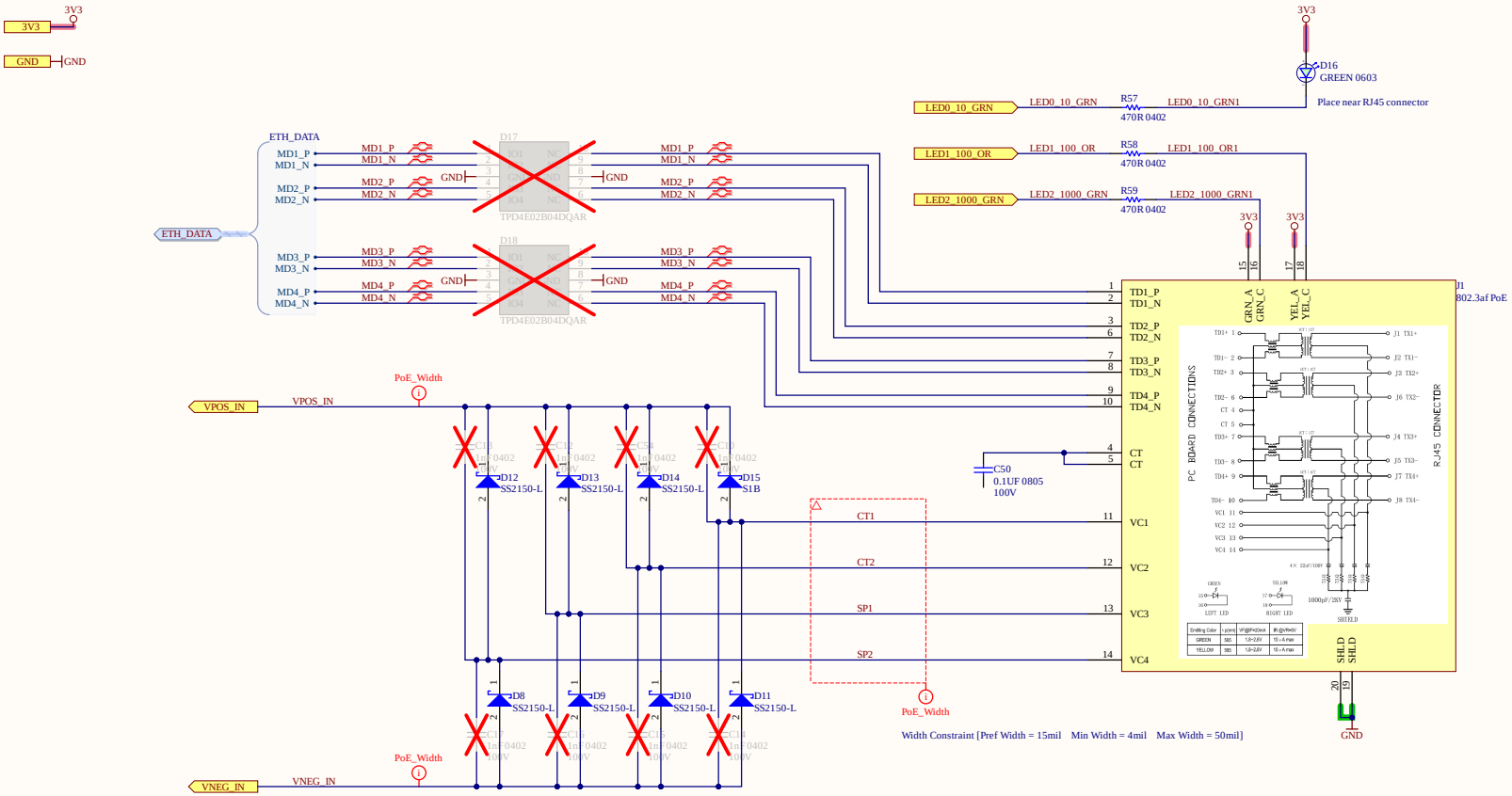

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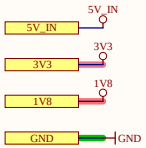
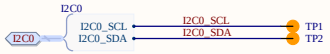
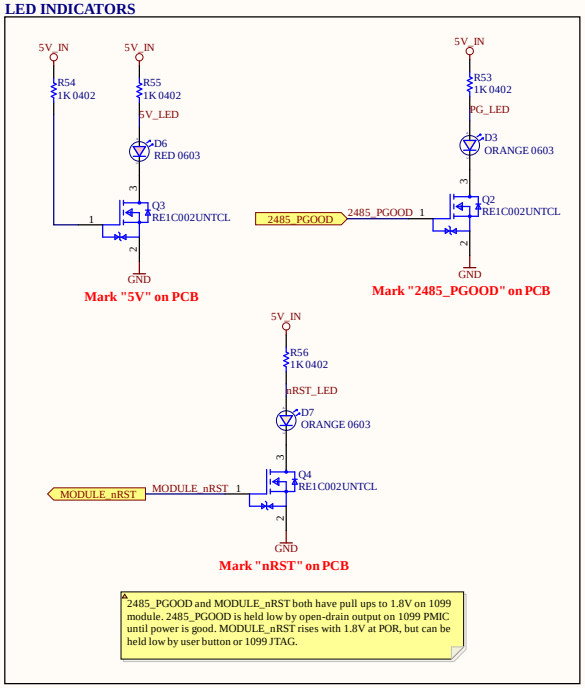




LED INDICATORS



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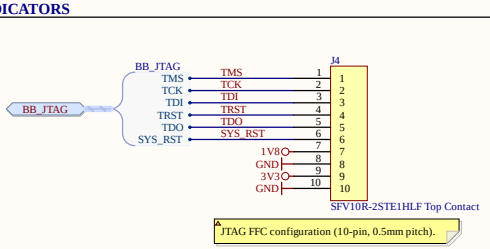
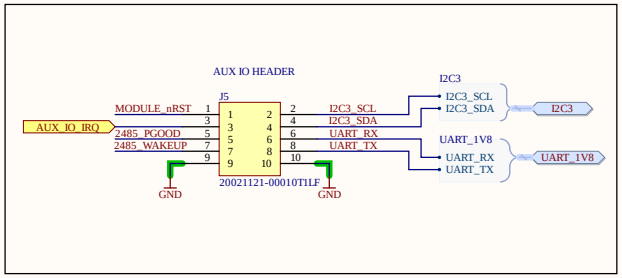
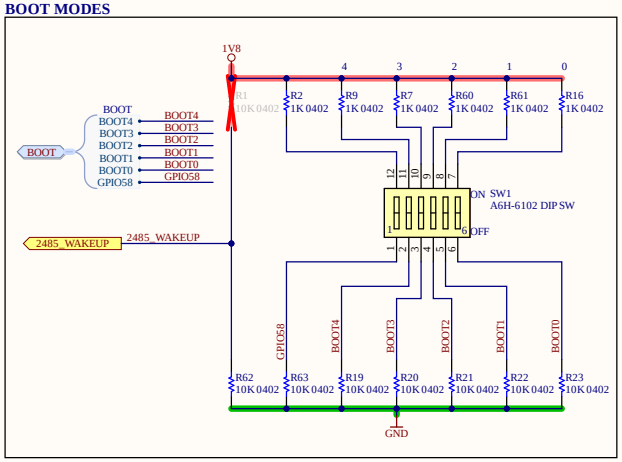


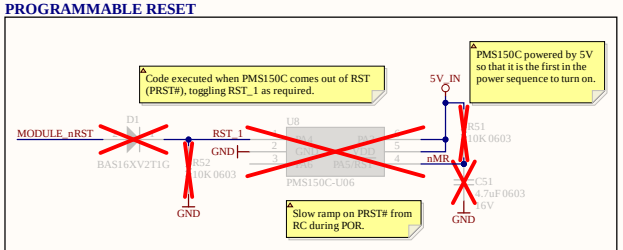
AUX IO HEADER



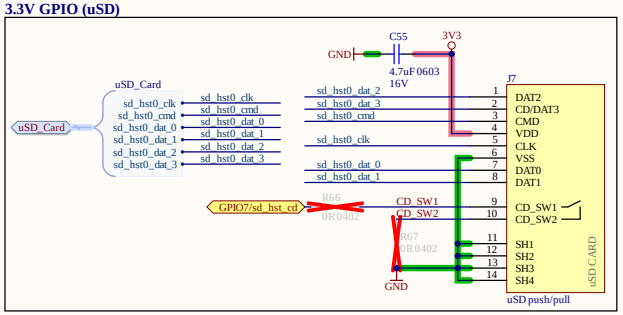
BOOT MODES



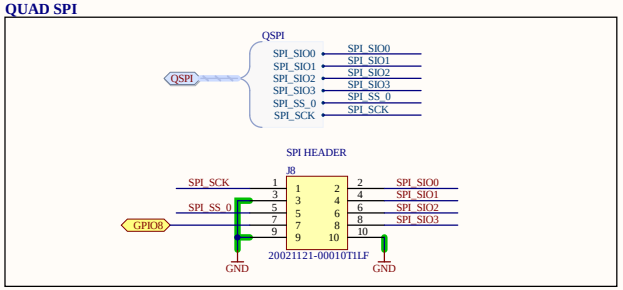
PROGRAMMABLE RESET



3.3V GPIO (uSD)



QUAD SPI



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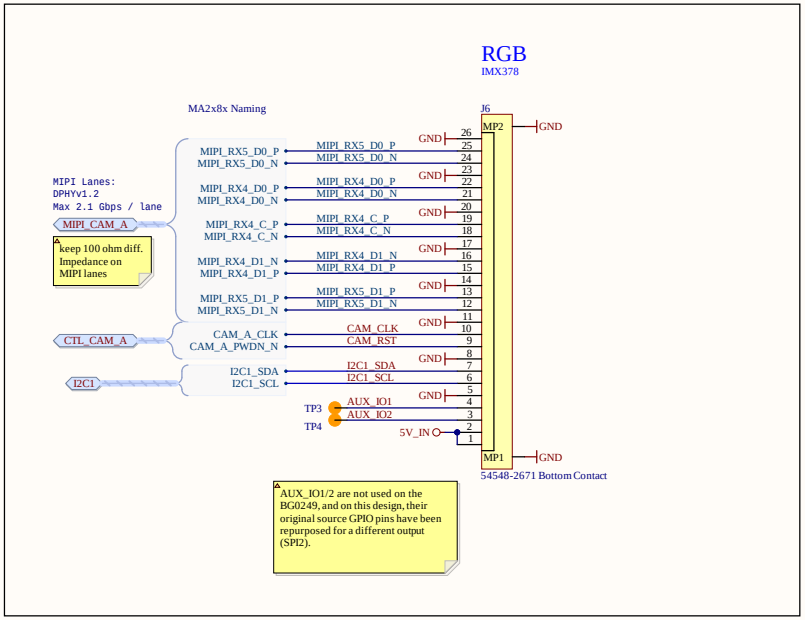
5V_IN

GND

RGB CAMERA



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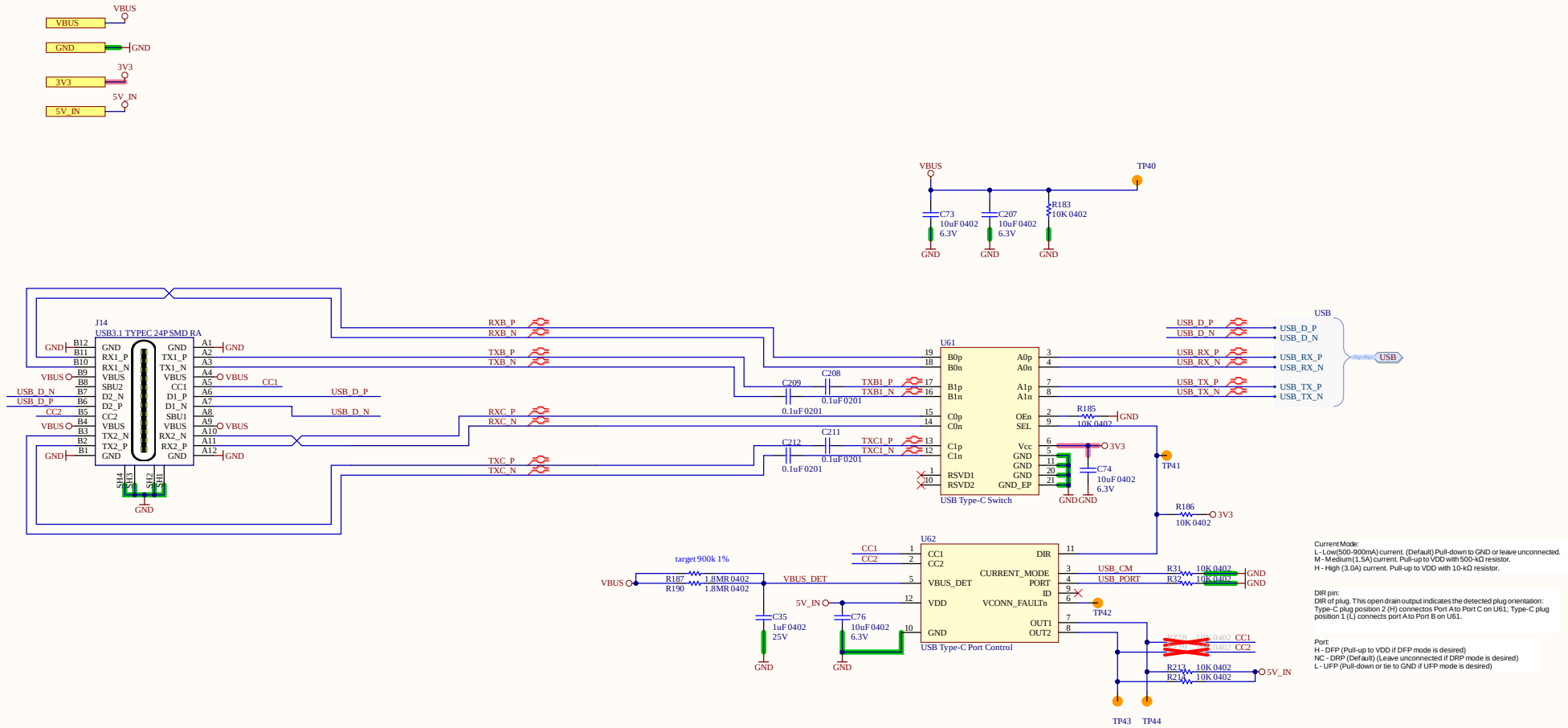

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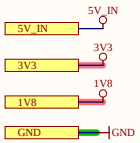

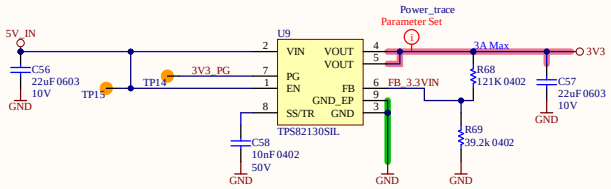

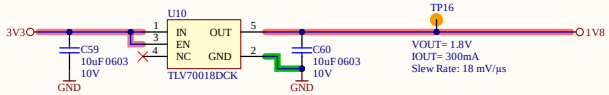

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