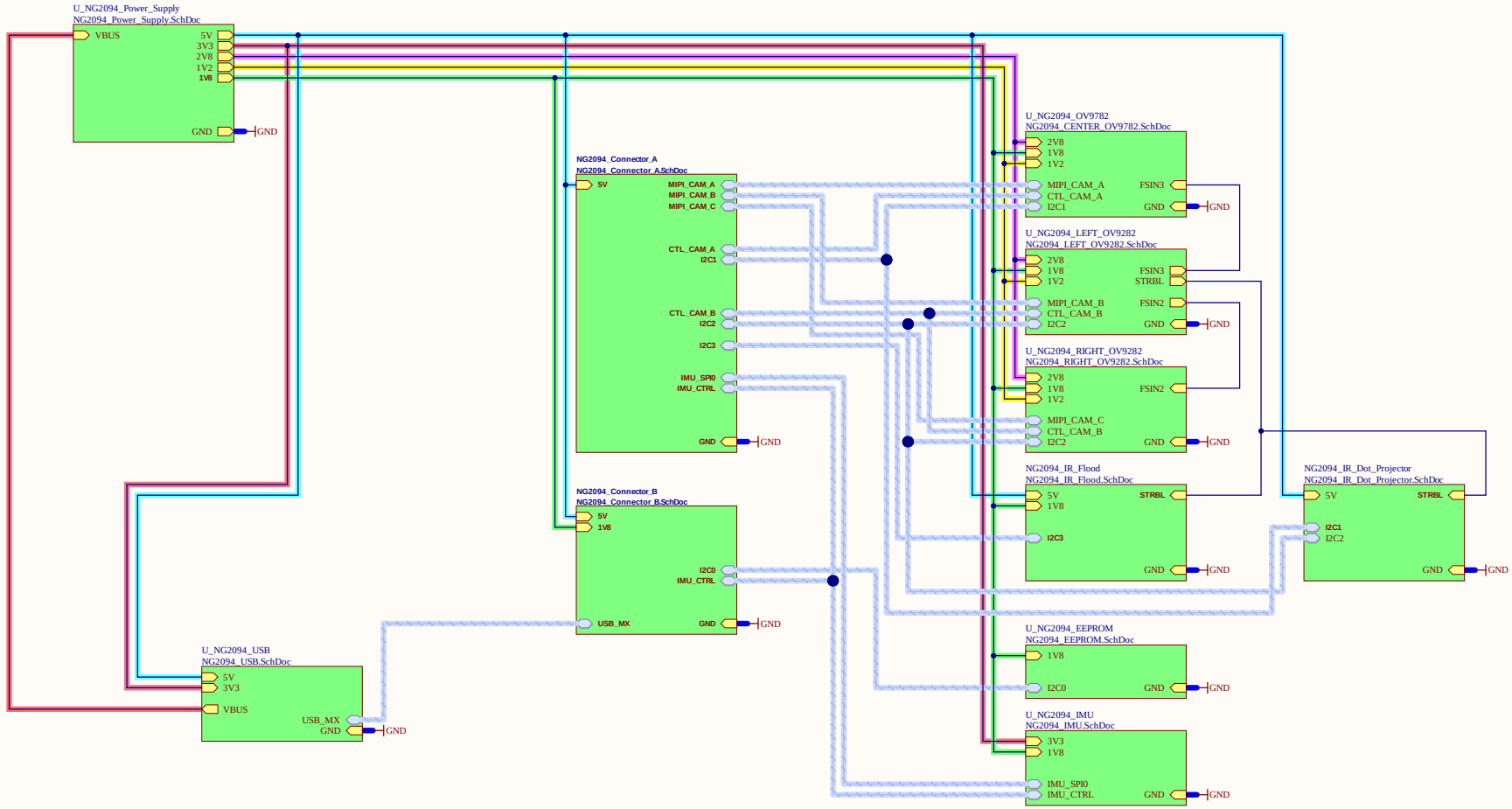
Project: ***NG2094***
Current Revision: ***R0M0E0***

NG2094 *Revision History:*

Date	Revision	Reason for Change	Changes Implemented
08/06/2021	Initial release		

Title *NG2094*			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number:DXXXX	Revision:R0M0E0		
Date: 30/09/2021 Time: 09:53:04		Sheet 1 of 9		
Drawn by: ***Nejc Gostincar***				


U_NG2094_Power_Supply
NG2094_Power_Supply.SchDoc
VBUS
5V
3V3
2V8
1V2
1V8
GND
U_NG2094_USB
NG2094_USB.SchDoc
USB_MX
NG2094_Connector_A
NG2094_Connector_A.SchDoc
MIPI_CAM_A
MIPI_CAM_B
MIPI_CAM_C
CTL_CAM_A
I2C1
CTL_CAM_B
I2C2
I2C3
IMU_SPI0
IMU_CTRL
NG2094_Connector_B
NG2094_Connector_B.SchDoc
I2C0
U_NG2094_OV9782
NG2094_CENTER_OV9782.SchDoc
FSIN3
U_NG2094_LEFT_OV9282
NG2094_LEFT_OV9282.SchDoc
FSIN2
STRBL
U_NG2094_RIGHT_OV9282
NG2094_RIGHT_OV9282.SchDoc
NG2094_IR_Flood
NG2094_IR_Flood.SchDoc
NG2094_IR_Dot_Projector
NG2094_IR_Dot_Projector.SchDoc
U_NG2094_EEPROM
NG2094_EEPROM.SchDoc
U_NG2094_IMU
NG2094_IMU.SchDoc
U_Project_Information
Project_Information.SchDoc
FID1
FID2
FID3
FID4
Title NG2094
Size: Tabloid
Number:DXXXX
Revision:R0M0E0
Date: 30/09/2021
Time: 09:53:04
Sheet 2 of 9
Drawn by: Nejc Gostincar
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
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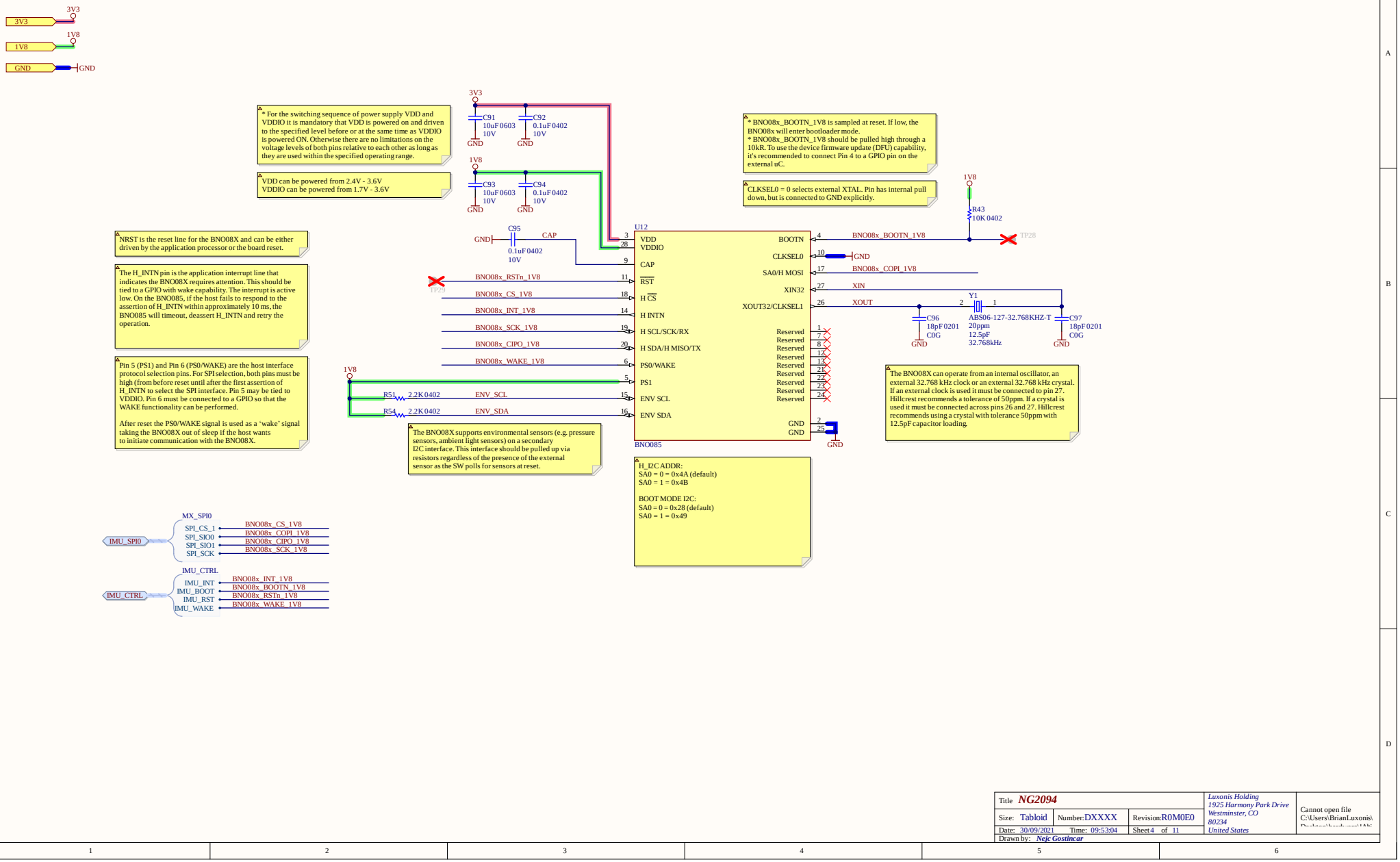
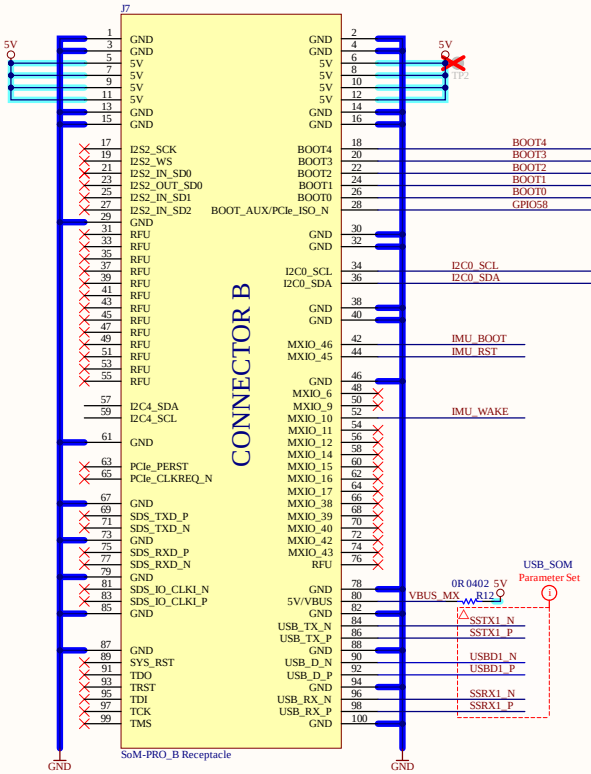


Title	NG2094		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: DXXXX	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 30/09/2021 Time: 09:53:04	Sheet 4 of 11		
Drawn by: Nejc Gostincar			

BW2099 CONNECTOR B



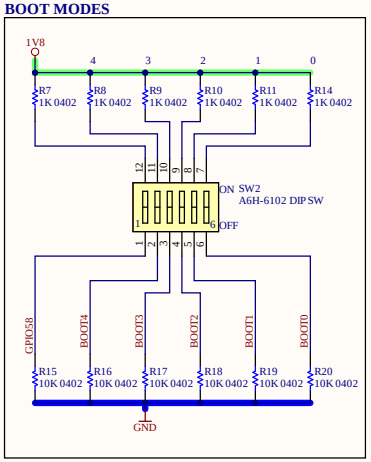
The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signalling as well).

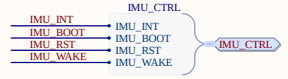
If WAKEUP pulled low when external reset is released, GPIO Configured Boot is selected. If pulled high, then eFuse Boot is selected.

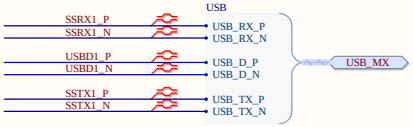
gpio59 --> Boot[0], LSB
gpio60 --> Boot[1]
gpio61 --> Boot[2]
gpio62 --> Boot[3]
gpio63 --> Boot[4], MSB

0x00 [0b00000] = Debug
0x07 [0b00111] = SPIME 24bit 100MHz, QUAD IO
0x16 [0b10110] =USBD Range_A 24MHz refclk0
See MyriadX datasheet for other options.

BOOT MODES







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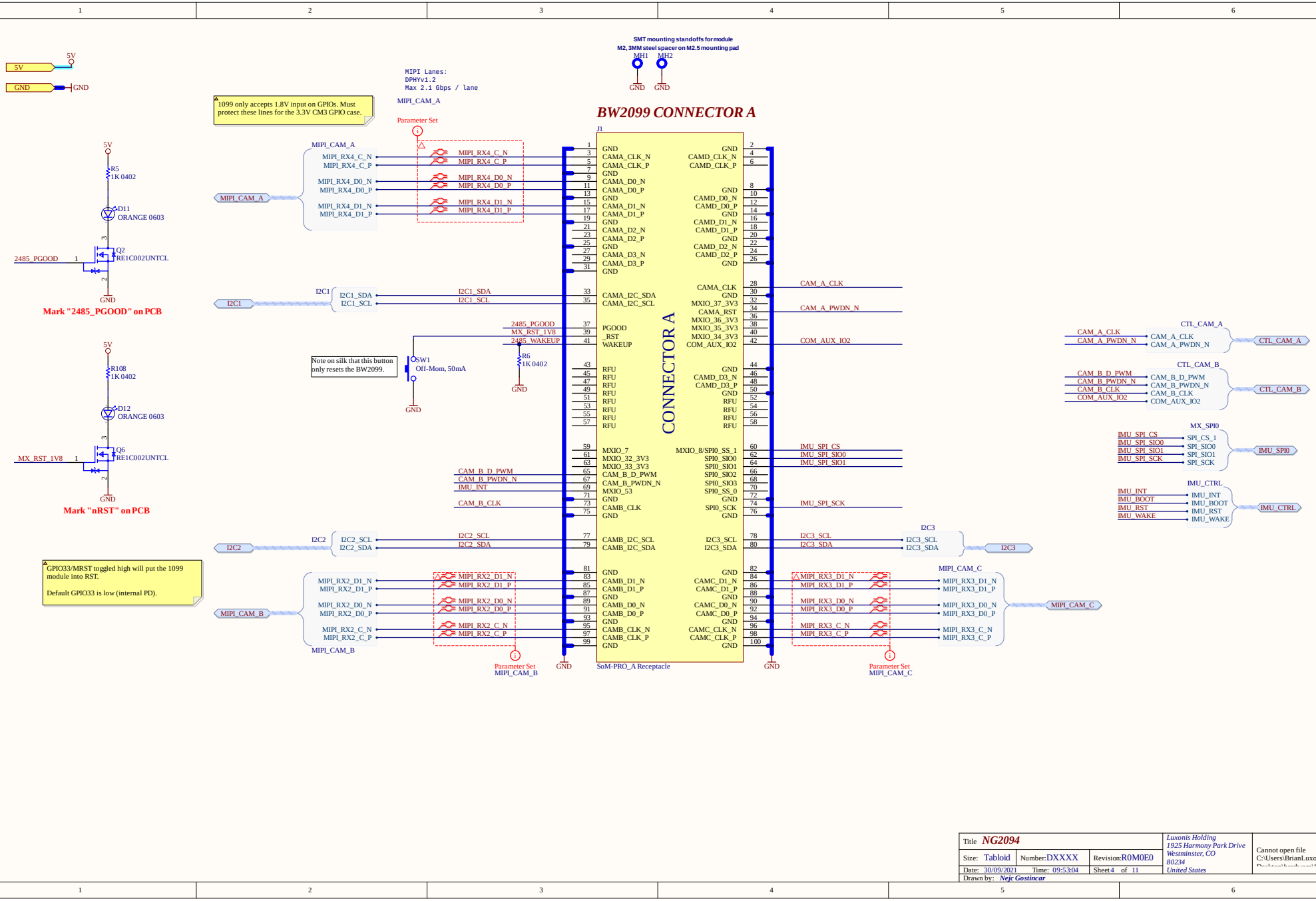
Size: Tabloid	Number:DXXXX	Revision:R0M0E0		
Date: 30/09/2021 Time: 09:53:04	Sheet 4 of 11			
Drawn by: Nejc Gostincar				



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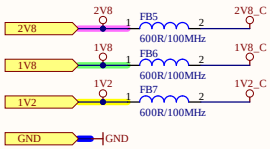
Drawn by: Nejc Gostincar			

Place FBs and caps close to their associated camera connector.

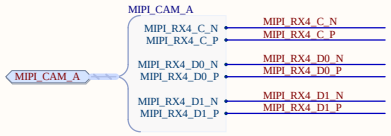


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	TBD kHz Max
SENSOR	OV09782 RGB 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xTBD(W) 0xTBD(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 27 MHz (24 MHz typ.)

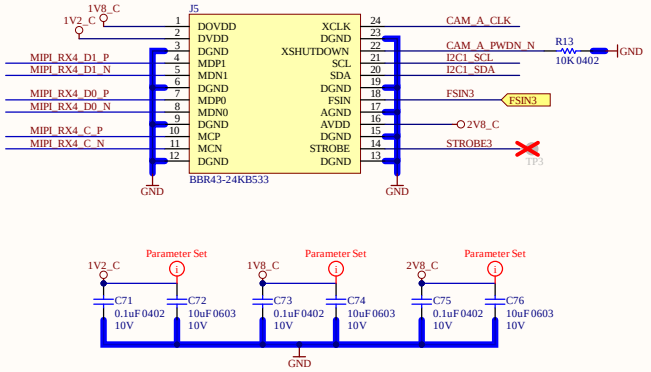
Supply Information

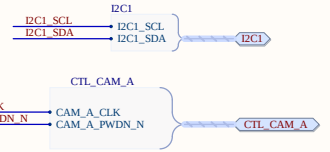
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane



OV9782 MODULE CONNECTOR





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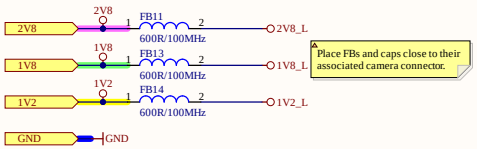
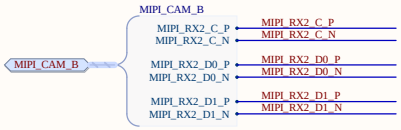
Size: Tabloid	Number: DXXXX	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 30/09/2021 Time: 09:53:04	Sheet 5 of 11		
Drawn by: Nejc Gostincar			



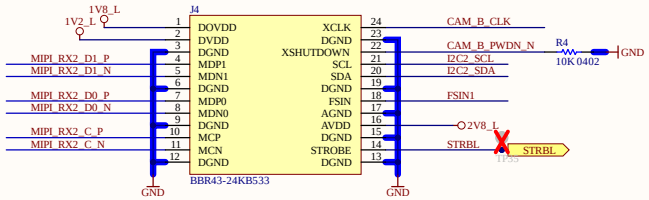
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

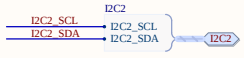
Supply Information

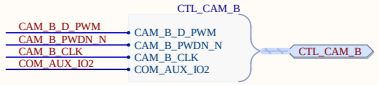
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

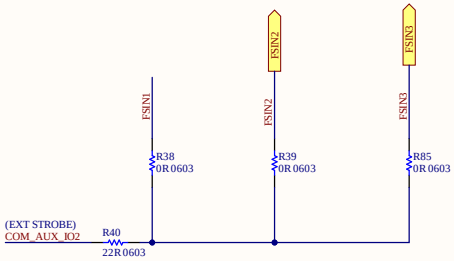


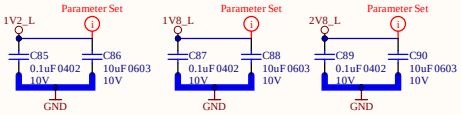
Mark "LEFT" on PCB
Place so that is the module's left camera.











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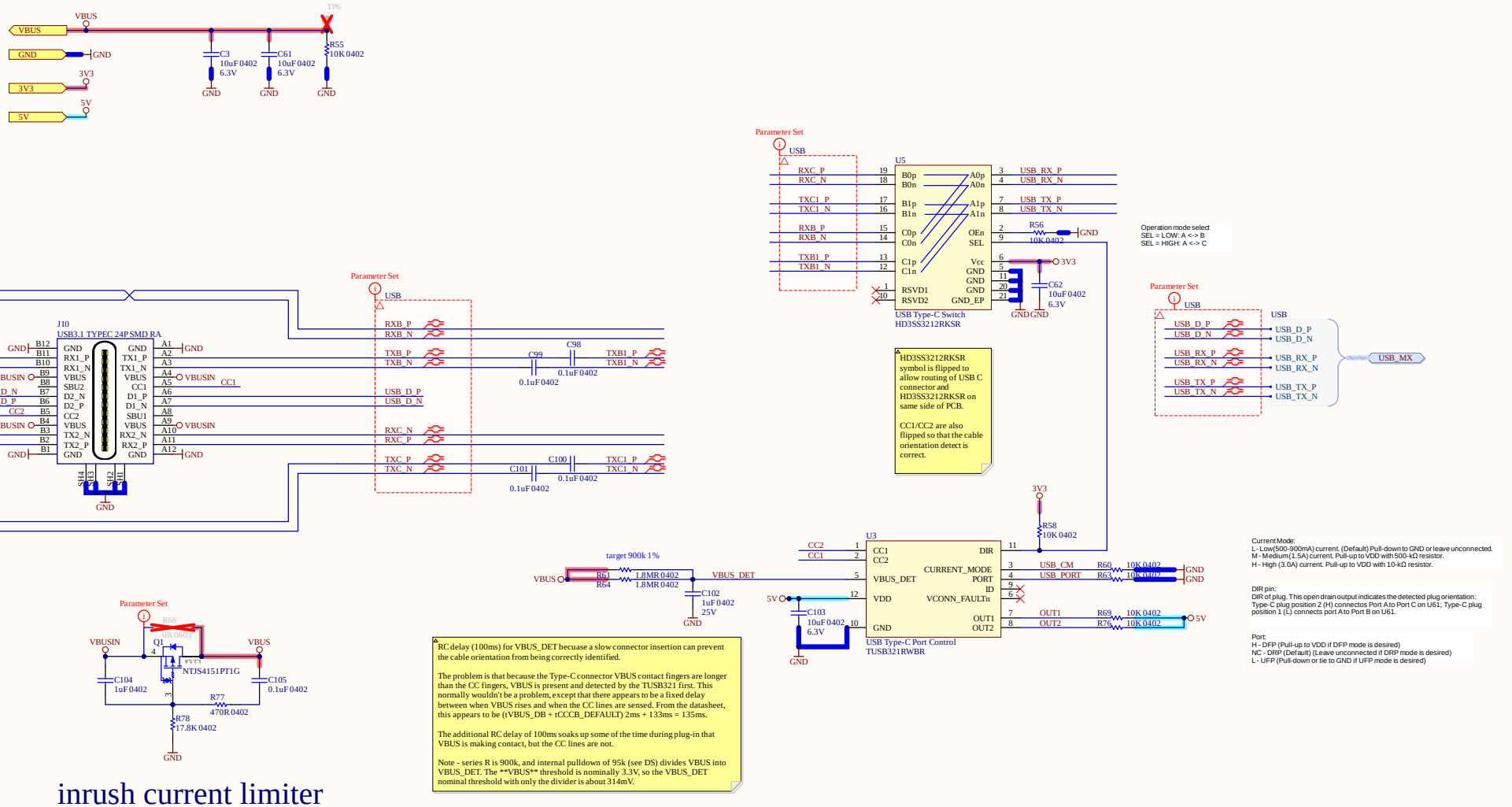
Drawn by: Nejc Gostincar			


VBUS
GND
3V3
5V
TP6
C3
10uF 0402
6.3V
C61
10uF 0402
6.3V
R55
10K 0402
Parameter Set
USB
J10
USB3.1 TYPEC 24P SMD RA
RXB_P
RXB_N
TXB_P
TXB_N
C99
0.1uF 0402
C98
0.1uF 0402
TXB1_P
TXB1_N
VBUSIN
CC1
USB_D_N
USB_D_P
CC2
RXC_N
RXC_P
TXC_P
TXC_N
C101
0.1uF 0402
C100
0.1uF 0402
TXC1_P
TXC1_N
U5
USB Type-C Switch
HD3SS3212RKSR
RXC_P
RXC_N
TXC1_P
TXC1_N
RXB_P
RXB_N
TXB1_P
TXB1_N
USB_RX_P
USB_RX_N
USB_TX_P
USB_TX_N
R56
10K 0402
C62
10uF 0402
6.3V
Operation mode select
SEL = LOW: A <-> B
SEL = HIGH: A <-> C
HD3SS3212RKSR symbol is flipped to allow routing of USB C connector and HD3SS3212RKSR on same side of PCB.
CC1/CC2 are also flipped so that the cable orientation detect is correct.
USB_D_P
USB_D_N
USB_RX_P
USB_RX_N
USB_TX_P
USB_TX_N
USB_MX
3V3
R58
10K 0402
U3
USB Type-C Port Control
TUSB321RWBR
CC2
CC1
VBUS_DET
VDD
GND
DIR
CURRENT_MODE
PORT
ID
VCONN_FAULTn
OUT1
OUT2
USB_CM
USB_PORT
R60
10K 0402
R63
10K 0402
R69
10K 0402
R76
10K 0402
C103
10uF 0402
6.3V
target 900k 1%
R61
1.8MR 0402
R64
1.8MR 0402
C102
1uF 0402
25V
Current Mode:
L - Low(500-900mA) current. (Default) Pull-down to GND or leave unconnected.
M - Medium(1.5A) current. Pull-up to VDD with 500-kΩ resistor.
H - High (3.0A) current. Pull-up to VDD with 10-kΩ resistor.
DIR pin:
DIR of plug. This open drain output indicates the detected plug orientation: Type-C plug position 2 (H) connectos Port A to Port C on U61; Type-C plug position 1 (L) connects port A to Port B on U61.
Port:
H - DFP (Pull-up to VDD if DFP mode is desired)
NC - DRP (Default) (Leave unconnected if DRP mode is desired)
L - UFP (Pull-down or tie to GND if UFP mode is desired)
R66
0R 0603
Q1
NTJS4151PT1G
C104
1uF 0402
C105
0.1uF 0402
R77
470R 0402
R78
17.8K 0402
RC delay (100ms) for VBUS_DET becuase a slow connector insertion can prevent the cable orientation from being correctly identified.
The problem is that because the Type-C connector VBUS contact fingers are longer than the CC fingers, VBUS is present and detected by the TUSB321 first. This normally wouldn't be a problem, except that there appears to be a fixed delay between when VBUS rises and when the CC lines are sensed. From the datasheet, this appears to be (tVBUS_DB + tCCCB_DEFAULT) 2ms + 133ms = 135ms.
The additional RC delay of 100ms soaks up some of the time during plug-in that VBUS is making contact, but the CC lines are not.
Note - series R is 900k, and internal pulldown of 95k (see DS) divides VBUS into VBUS_DET. The **VBUS** threshold is nominally 3.3V, so the VBUS_DET nominal threshold with only the divider is about 314mV.
inrush current limiter
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Drawn by: Nejc Gostincar
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
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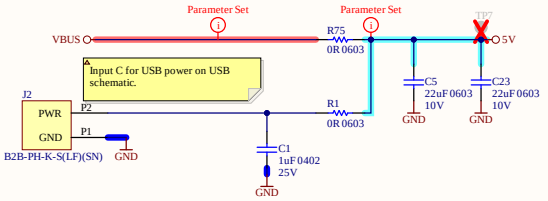
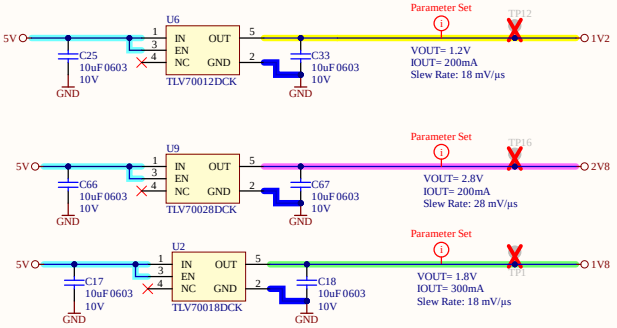
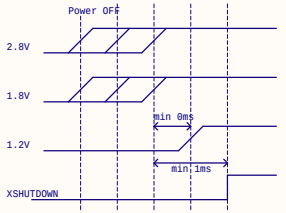
POWER INPUT



POWER SUPPLIES FOR CAMERA MODULES



OV9282 POWER REQUIREMENTS

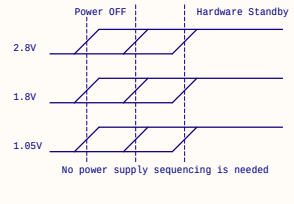


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

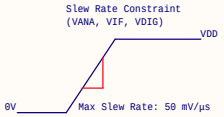
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

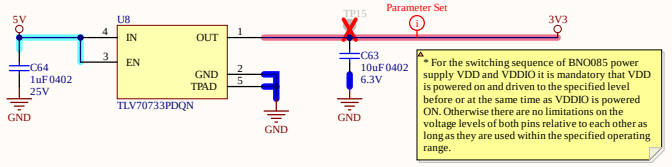


POWER SEQUENCING REQUIREMENTS:

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

3.3V USB SW POWER



TP18 TP19 TP25 TP26

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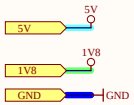
Drawn by: Nejc Gostincar			

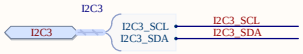


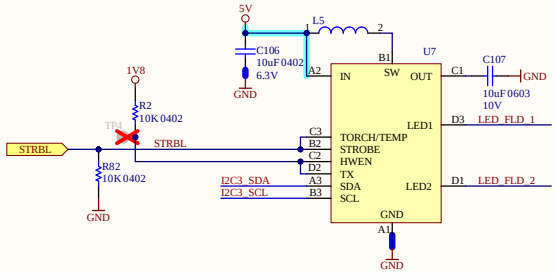
Only applicable if TORCH/TEMPT-STROBE and HWEN-TX are connected together to avoid using uVias:
To ensure that the LM3643/4/8 does not create a false TX or TORCH/TEMP event, the pin-enable bits for these functions must be disabled via I2C. Bit 7 and Bit 4 in register 0x01 must be set to logic 0 to disable the pin functionality.

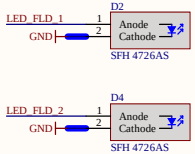
If anode and cathode connections are long they should be on separate layers and one routed above/below the other. GND should be connected together at LM3644 GND pin point.
Cathode coppper plane must be big enough to dissipate heat from projector.

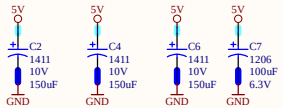
The resistive interlock is equivalent to a simple resistance as shown on the symbol.
Treshold set on 2.475V

$R_{Interlock}$	Resistance	At RT	10.8	13	21	kOhm









3.3 I2C Register Settings

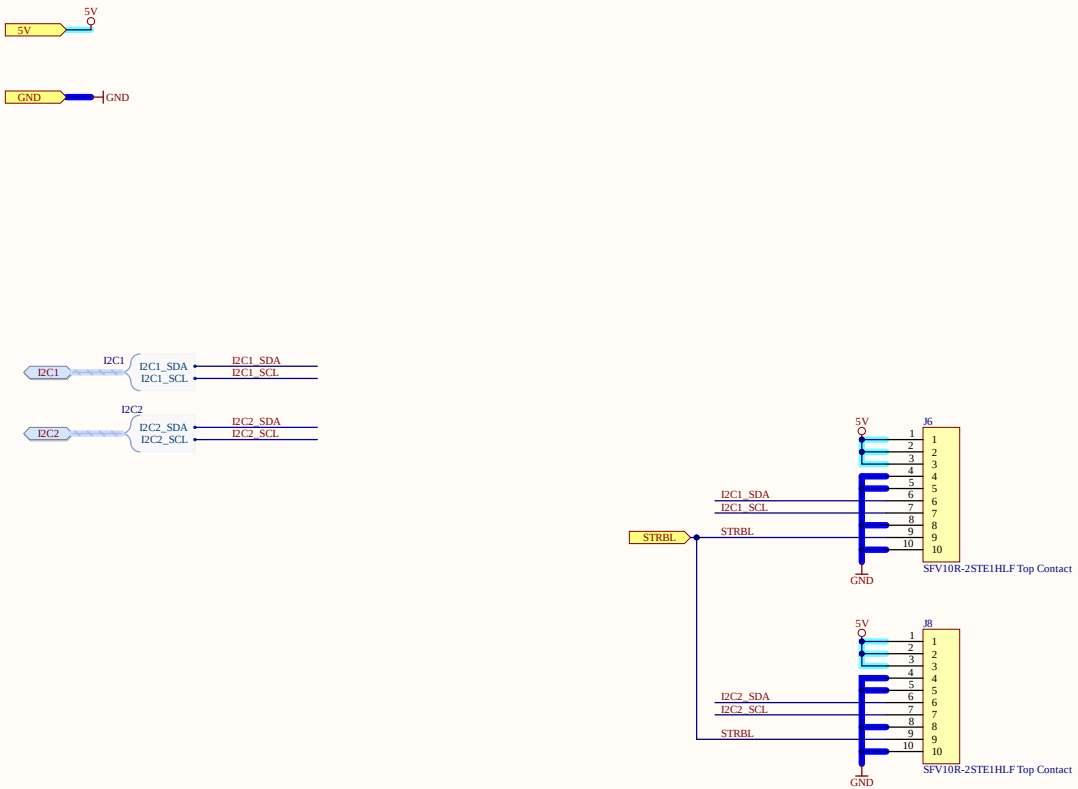
To ensure that the LM3643/4/8 does not create a false TX or TORCH/TEMP event, the pin-enable bits for these functions must be disabled via I2C. Bit 7 and Bit 4 in register 0x01 must be set to logic 0 to disable the pin functionality.

9.6.1 Enable Register (0x01)

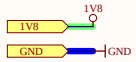
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX Pin Enable 0 = Disabled 1 = Enabled (Default)	**Strobe Type** 1 = Level Triggered (Default) 1 = Edge Triggered	**Strobe Enable** 0 = Disabled (Default) 1 = Enabled	**TORCH/TEMP Pin Enable** 0 = Disabled (Default) 1 = Enabled	**Mode Bits: M1, M0** '00' = Standby (Default) '01' = IR Drive '10' = Torch '11' = Flash		**LED2 Enable** 0 = OFF (Default) 1 = ON	**LED1 Enable** 0 = OFF (Default) 1 = ON

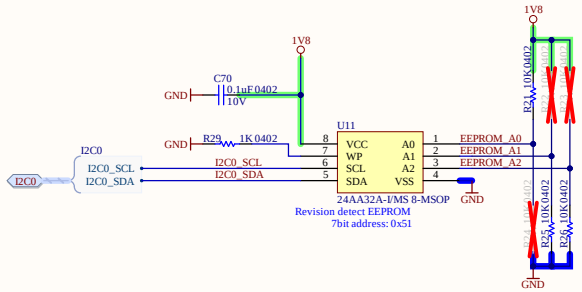
Figure 7. Enable Register Information

Title	**NG2094**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number:DXXXX	Revision:R0M0E0		Cannot open file C:\Users\BrianLuxonis\
Date: 30/09/2021	Time: 09:53:04	Sheet 9 of 10		
Drawn by: *Nejc Gostincar*				

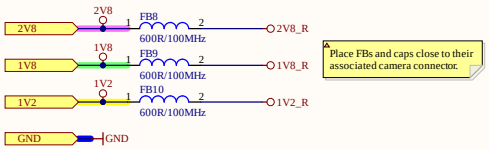


Title **NG2094**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: DXXXX	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 30/09/2021 Time: 09:53:04		Sheet 9 of 10	
Drawn by: ***Nejc Gostincar***			





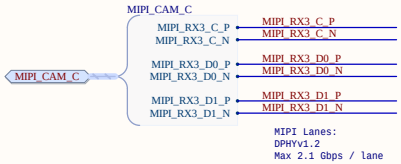
Title **NG2094**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: DXXXX	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 30/09/2021 Time: 09:53:04	Sheet 9 of 10		
Drawn by: ***Nejc Gostincar***			



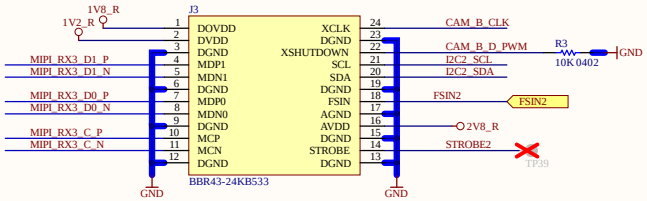
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

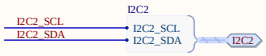
Supply Information

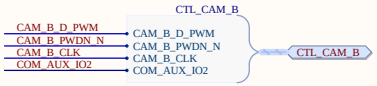
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

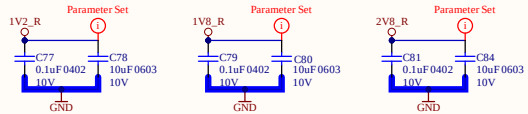


Mark "RIGHT" on PCB
Place so that this is the module's right camera.









Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if tl stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to tl sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title	NG2094		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
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Drawn by: Nejc Gostincar			

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