

Project: **SJ2096POE**  
Current Revision:

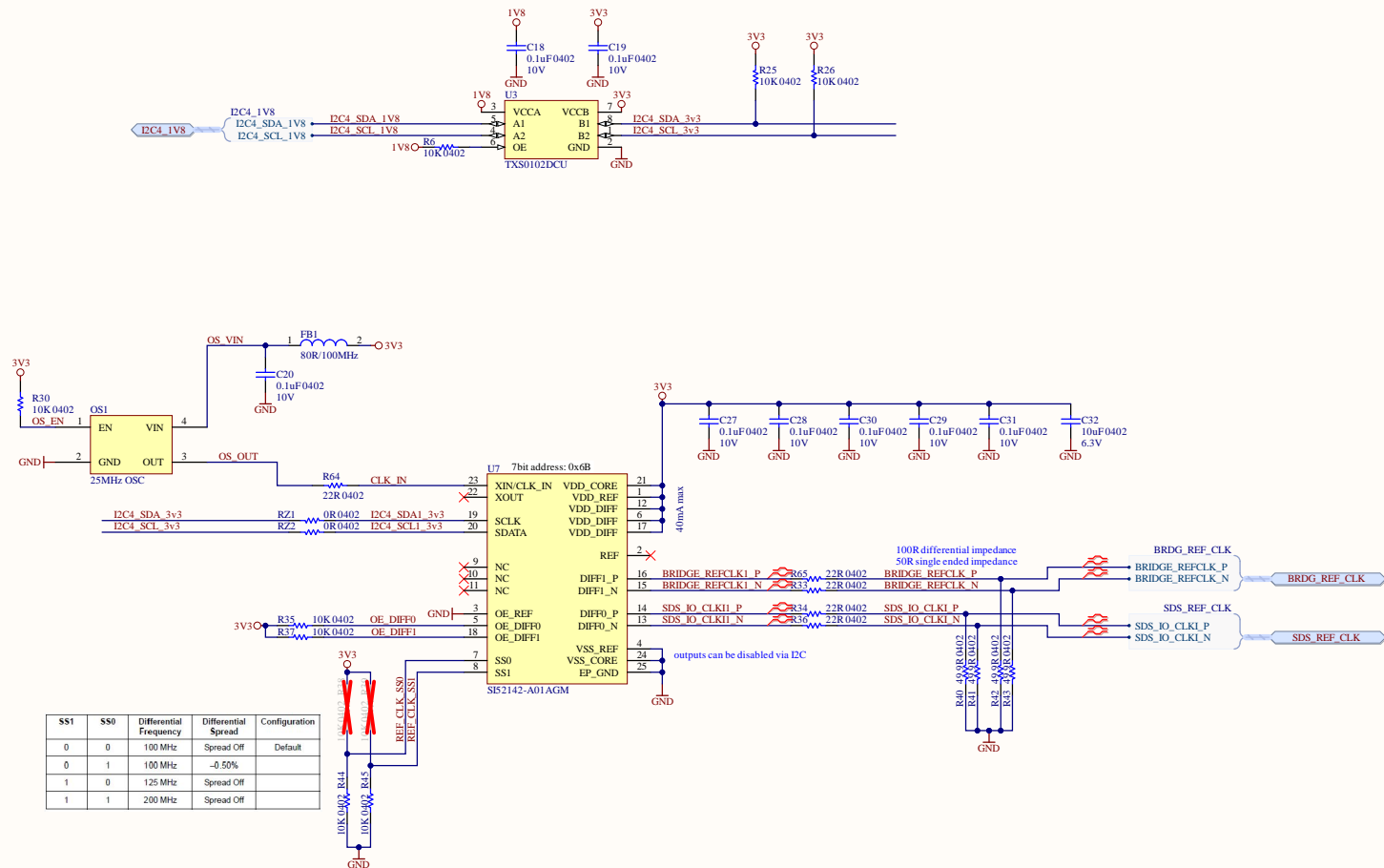
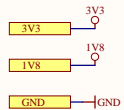
**SJ2096POE Revision History:**

Date	Revision	Reason for Change	Changes Implemented
3/4/2020	Initial Release -> R0M0E0		
5/29/2020	R0M0E0 --> R1M1E1	1) Pull up the EN pin on the 3.3V regulator 2) R1 should be depopulated (PU for MA2485 WAKEUP line) 3) Add ESD protection diodes to the Ethernet lines 4) LEDs labels for "nRST" and "5V" are switched. 5) Polygon 3V3_L01_P425 is underneath GND polygon on Layer 1 and didn't pour correctly (still electrically connected by tracing). 6) J5/J8 are a bit too close for both cable housings 7) RGB camera connector tab hard to get to as it's under the BW2099 8) Label the boot switches 9) KingTop doesn't like the L1 inductor. Says it's too fragile and hard to handle. Try to find alternate.	1) 3.3V regulator EN pin pulled high to 5V 2) Depopulated R1 on Production variant 3) Added pads for ESD protection diodes on ethernet diff pairs 4) Swapped "nRST" and "5V" labels on overlay and added netnames to LEDs in schematic to help prevent this in the future. 5) Removed polygon and thickened traces 6) Increased connector spacing by 50milis to allow clearance 7) Moved connector 2mm right to make it a bit easier to grab the latch. Still not great, but better. 8) Added overlay labeling for each BOOT[4:0] and GPIO58 9) Moved the L1 inductor to L1 on layout so it wasn't so exposed to impacts. Did not change PN or schematic.
7/23/2020	R1M1E1 --> R2M1E2	1) C25 preventing bridge from functioning properly. 2) Labeling of "GPIO6" is incorrect. Should be "GPIO8"	1) Removed C25 from PCB and BOM. 2) Changed references of GPIO6 to GPIO8. No physical change to PCB.
01/06/2021	BW2098POE_R1M1E1 --> SJ2096POE_R0M0E0	Moved from BW2098POE to SJ2096POE	1. Minor changes in schematic with power circuit arrangement. 2. Programmable reset circuit removed. 3. PCB Layout redone.
04/21/2021	R0M0E0 --> R1M0E1	1) Slow plug issue with USB type-C 2) BOM errors	1. Added 1uF capacitor to VBUS_DET updated PCB and fabrication files 2. Edited parameters for components

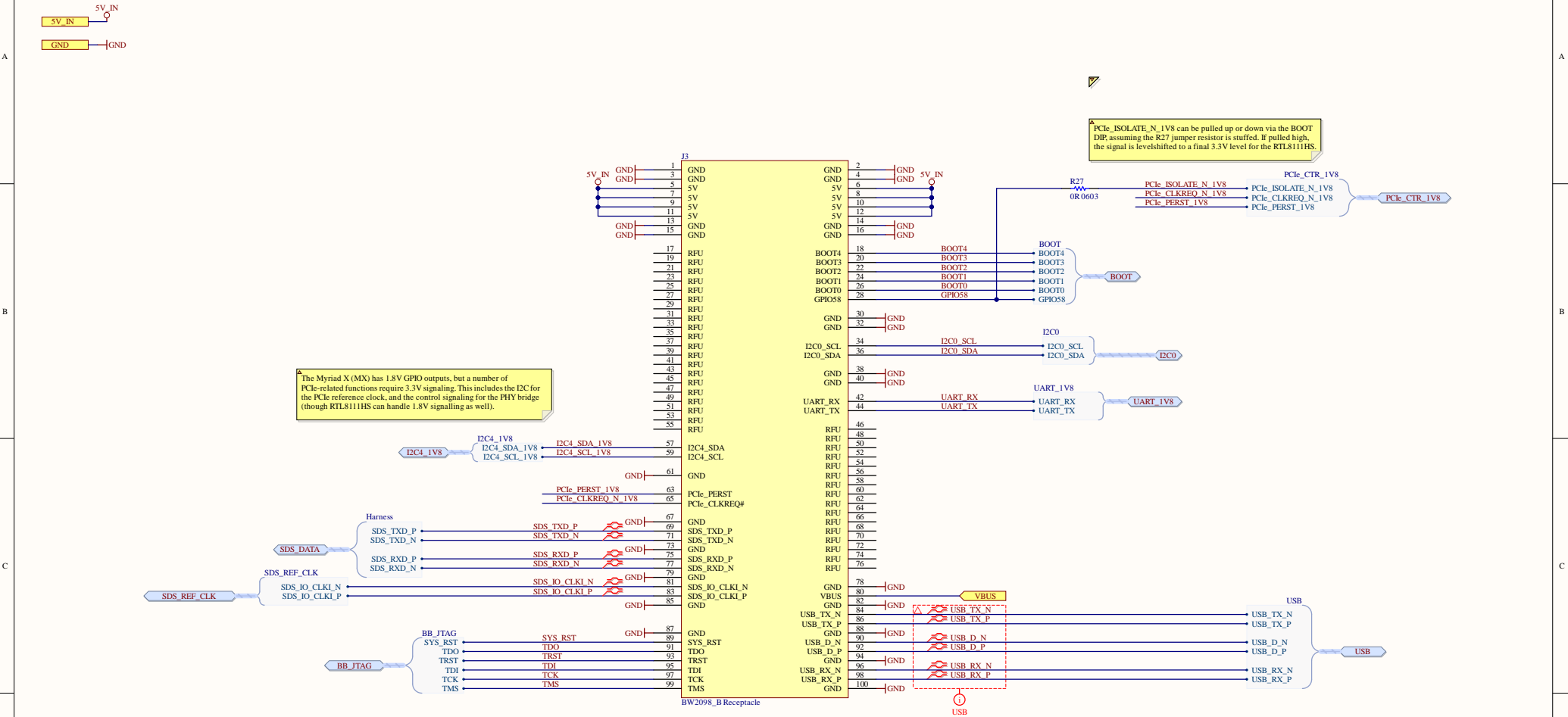
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Size: <b>Tabloid</b>	Number: <b>D2098000</b>	Revision:			
Date: <b>21/04/2021</b>	Time: <b>09:56:05</b>	Sheet <b>1</b> of <b>12</b>			
Drawn by: <b>BW/MB/SJ</b>					



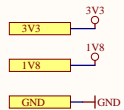






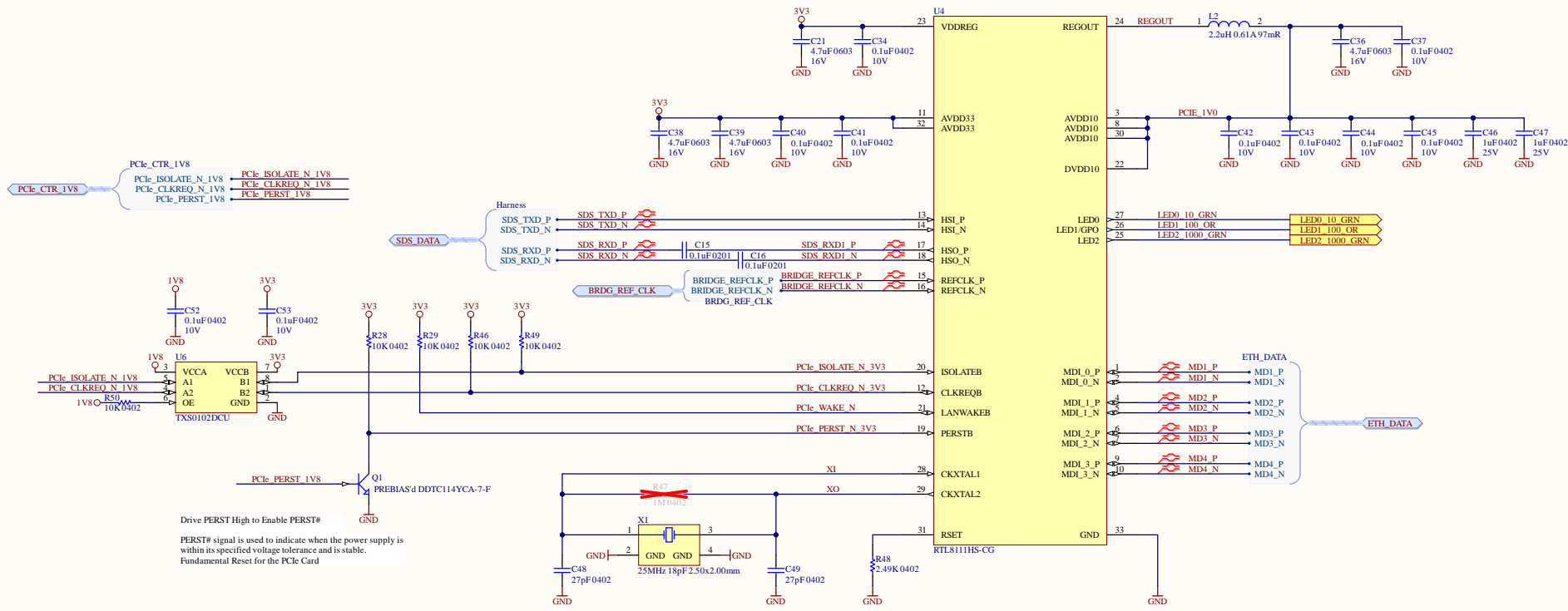


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Power Sequence Requirements:  
- 3.3V POR ramp must be:  $1\text{ms} < t < 100\text{ms}$   
- All power inputs must be held  $>50\text{ms}$  at 0V between

Switching Regulator Layout:  
- VDDREG  $>40\text{mils}$   
- REGOUT  $>60\text{mils}$   
- Place caps and inductor as close as possible to the RTL8111HS  
- Place Lx and bulk C on the same layer as RTL8111HS  
- No additional inductance or FBs  
- Ceramic X5R caps or better



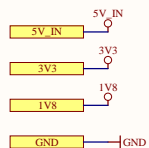
Drive PERST High to Enable PERST#  
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.  
Fundamental Reset for the PCIe Card

Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.

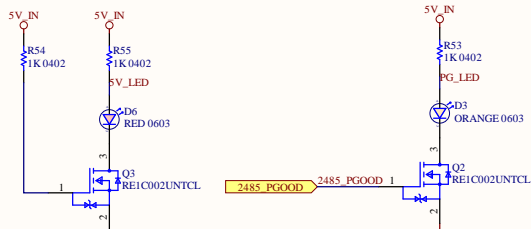
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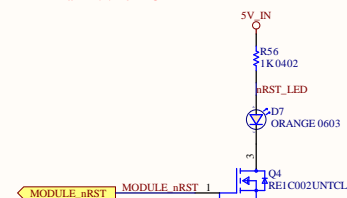


## LED INDICATORS



Mark "5V" on PCB

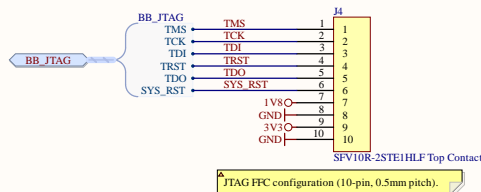
Mark "2485\_PGOOD" on PCB



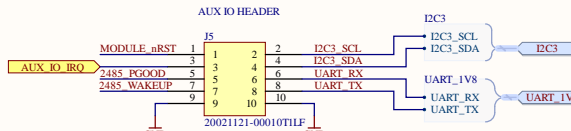
Mark "nRST" on PCB

2485\_PGOOD and MODULE\_nRST both have pull ups to 1.8V on 1099 module. 2485\_PGOOD is held low by open-drain output on 1099 PMIC until power is good. MODULE\_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.

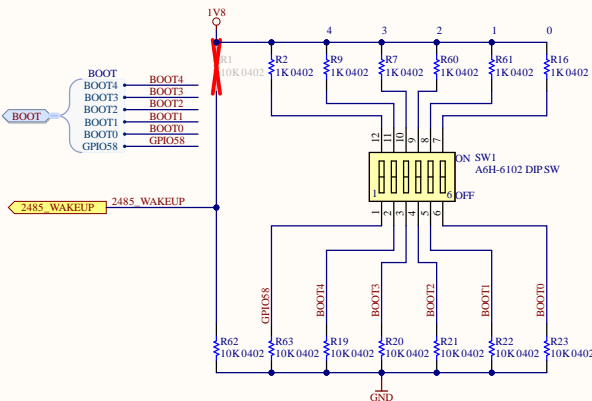
## LED INDICATORS



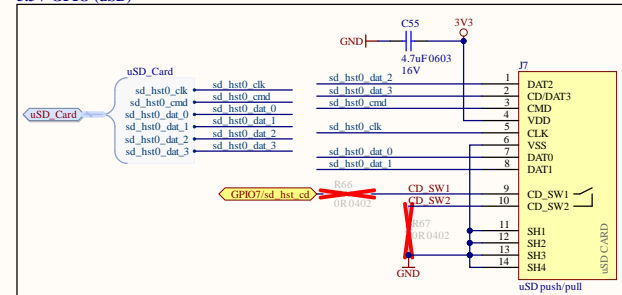
## AUX IO HEADER



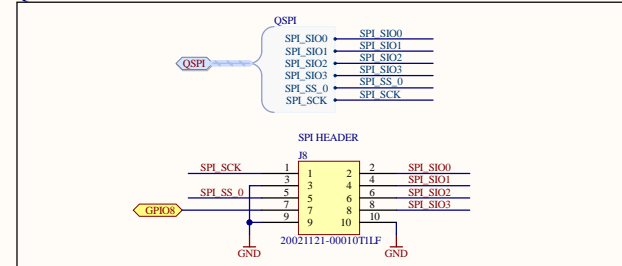
## BOOT MODES



## 3.3V GPIO (uSD)

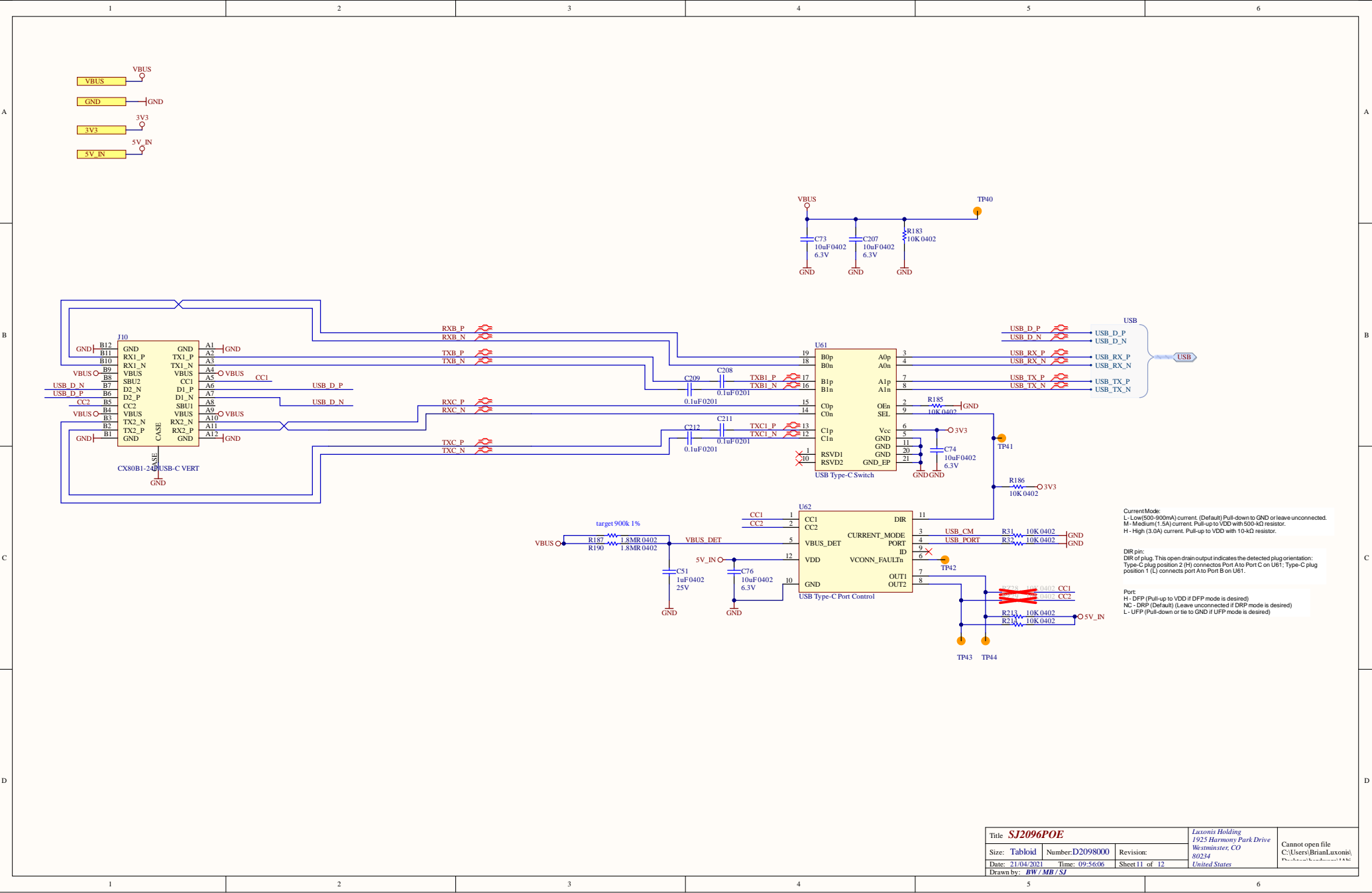


## QUAD SPI



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