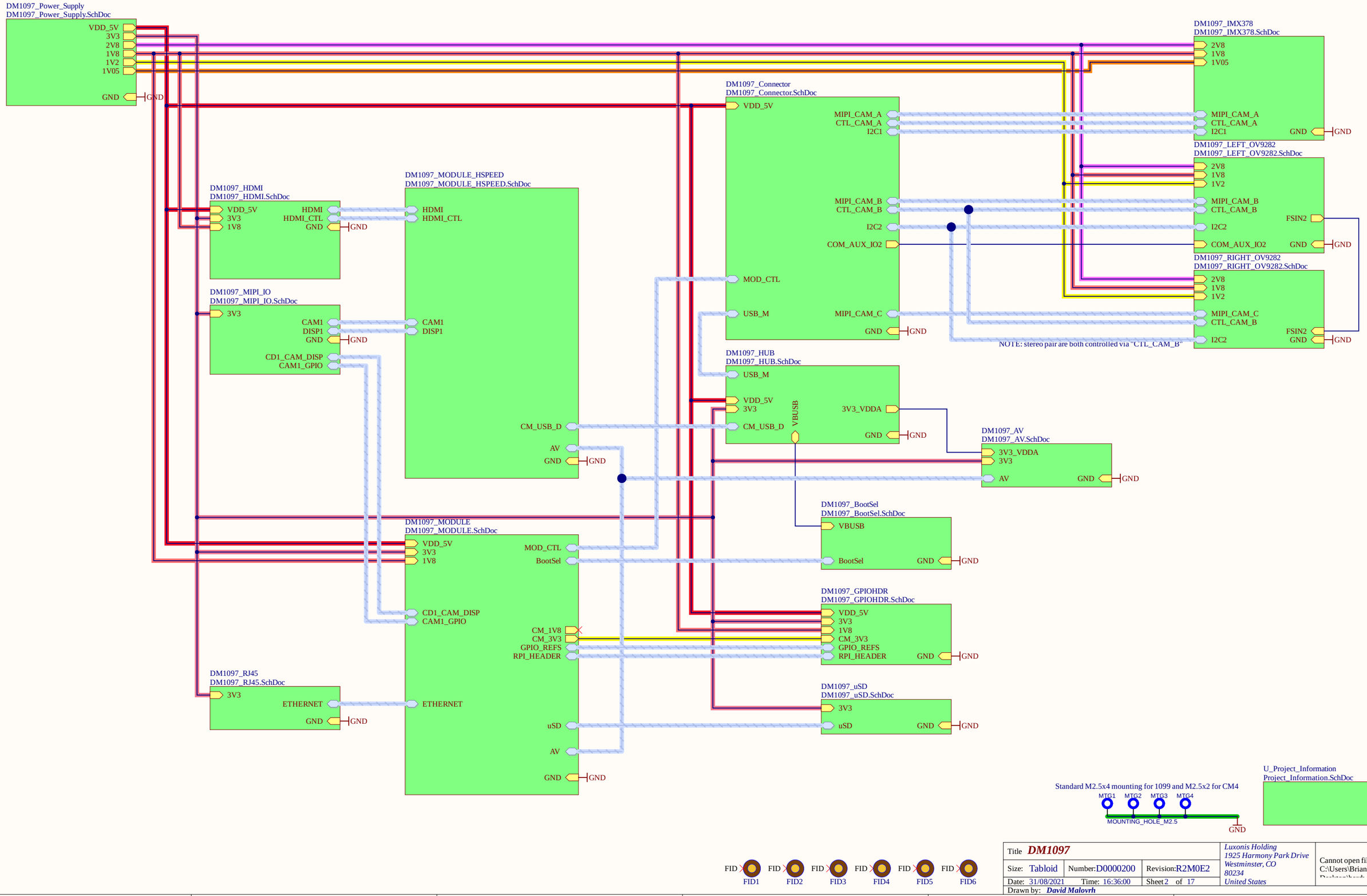
Project: ***DM1097***
Current Revision: ***R2M0E2***

BW1097 Revision History:

Date	Revision	Reason for Change	Changes Implemented
11/29/2019	R1M1E2 -> R2M2E3	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Header jumpers are unnecesary and expensive, and can be repalced with a simpler solution 3) Existing design was not standardized on LuxonisMaster library format 4) Series input power resistor is a sense resistor, but should be 0 ohm 5) The OV9282 LDOs have unncessary components compared to the most recent baseboards 6) Depopped R26 had no set component value. 7) HDMI connector footprint was found to be slightly crooked 8) PGOOD LED driver did not match other boards 9) DMG1012 FETs were automotive qualified, changed to non-automotive for entry into LuxonisMaster 10) Passive component equivalent part substitions as library was built up	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names, Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Removed header jumpers and exchanged with resistor jumper networks 3) Updated schematic and component information to align with LuxonisMaster library system. 4) Changed input series resistor to 0603 0ohm to match 1098OBC, 1098FFC, and 1094. 5) Removed RC circuit on OV9282 LDOs to match 1098OBC 6) Added 47K as default, but R26 remains depopulated 7) Corrected HDMI footprint to match recommended PCB layout from Wurth 685119134923 8) Changed transistor on PGOOD LED to be RE1C002UNTCL, to match other boards (Q5) 9) Changed from DMG1012TG-7 to DMG1012T-7 (Q1, Q2, Q3, Q4, Q6) 10) Many passive components did not exist in LuxonisMaster, so in some cases, equivalent from a different manufacturer are used. For 332R and 100K resistors, all were standardized to 0402, rather than a mix of sizes
	BW1097_R2M2E3 -> DM1097_R0M0E0	Initial design release supporting CM4 module	
	R0M0E1 -> R1M1E2	1) Corrected typo error in SDIO Net class 2) Changed configuration of populated shunt reistors on sync	1) Added SDIO0 to Net class and remover nonexisting SDIO4 Updated the PCB layout 2) Changed populated resistors on sync circuit so that R81 and R83 are populated

Title ***DM1097***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D0000200	Revision: R2M0E2	Cannot open file C:\Users\BrianLuxonis\
Date: 31/08/2021 Time: 16:36:00		Sheet 1 of 17	
Drawn by: ***David Malovrh***			


DM1097_Power_Supply
DM1097_Power_Supply.SchDoc
VDD_5V
3V3
2V8
1V8
1V2
1V05
GND
DM1097_IMX378
DM1097_IMX378.SchDoc
2V8
1V8
1V05
MIPI_CAM_A
CTL_CAM_A
I2C1
GND
DM1097_Connector
DM1097_Connector.SchDoc
VDD_5V
MIPI_CAM_A
CTL_CAM_A
I2C1
DM1097_LEFT_OV9282
DM1097_LEFT_OV9282.SchDoc
2V8
1V8
1V2
MIPI_CAM_B
CTL_CAM_B
I2C2
COM_AUX_IO2
FSIN2
DM1097_HDMI
DM1097_HDMI.SchDoc
VDD_5V
3V3
1V8
HDMI
HDMI_CTL
DM1097_MODULE_HSPEED
DM1097_MODULE_HSPEED.SchDoc
DM1097_RIGHT_OV9282
DM1097_RIGHT_OV9282.SchDoc
MOD_CTL
USB_M
MIPI_CAM_C
NOTE: stereo pair are both controlled via "CTL_CAM_B"
DM1097_MIPI_IO
DM1097_MIPI_IO.SchDoc
CAM1
DISP1
CD1_CAM_DISP
CAM1_GPIO
DM1097_HUB
DM1097_HUB.SchDoc
VBUSB
3V3_VDDA
CM_USB_D
AV
DM1097_AV
DM1097_AV.SchDoc
DM1097_BootSel
DM1097_BootSel.SchDoc
BootSel
DM1097_MODULE
DM1097_MODULE.SchDoc
CM_1V8
CM_3V3
GPIO_REFS
RPI_HEADER
DM1097_GPIOHDR
DM1097_GPIOHDR.SchDoc
DM1097_RJ45
DM1097_RJ45.SchDoc
ETHERNET
DM1097_uSD
DM1097_uSD.SchDoc
uSD
Standard M2.5x4 mounting for 1099 and M2.5x2 for CM4
MTG1
MTG2
MTG3
MTG4
MOUNTING_HOLE_M2.5
U_Project_Information
Project_Information.SchDoc
FID1
FID2
FID3
FID4
FID5
FID6
Title DM1097
Size: Tabloid
Number:D0000200
Revision:R2M0E2
Date: 31/08/2021
Time: 16:36:00
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80234
United States
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VDD_5V

GND

SMT mounting standoffs for module and for CM4

MTG7 MTG8 MTG9 MTG10 MTG5 MTG6

M2, 3MM steel spacer on M2.5 mounting pad

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

MISC1

Layout guide for BW1099

Code executed when PMS150C comes out of RST (PRST#), toggling RST_1 as required.

PMS150C powered by 5V so that it is the first in the power sequence to turn on.

Slow ramp on PRST# from RC during POR.

MODULE_nRST — D3 BAS16XV2T1G — RST_1 — R25 10K 0603 — GND

U10 PMS150C-U06 (PA4/RST, VDD, GND, PA5/RSTB)

nMR — R24 10K 0603 — C23 4.7uF 0603 16V — GND

1099 only accepts 1.8V input on GPIOs. Must protect these lines for the 3.3V CM3 GPIO case.

GPIO33/MRST toggled high will put the 1099 module into RST.

Default GPIO33 is low (internal PD).

MODULE_nRST is pulled to 1.8V on BW1099.

Note on silk that this button only resets the BW1099.

MOD_CTL — GPIO1/MRST — R18 470R 0402 — M1 RE1C002UNTCL — R75 10K 0402 — GND

B1 Off-Mom, 50mA

TP14 TP15

Parameter Set

MIPI_CAM_A

MIPI_RX4_C_N / MIPI_RX4_C_P
MIPI_RX4_D0_N / MIPI_RX4_D0_P
MIPI_RX4_D1_N / MIPI_RX4_D1_P
MIPI_RX5_D0_N / MIPI_RX5_D0_P
MIPI_RX5_D1_N / MIPI_RX5_D1_P

I2C1: I2C1_SDA, I2C1_SCL

2485_PGOOD, MODULE_nRST, 2485_WAKEUP

CTL_CAM_B: CAM_B_D_PWM, CAM_B_PWDN_N, CAM_B_CLK_OUT

AUX_IO_IRQ

I2C2: I2C2_SCL, I2C2_SDA

MIPI_CAM_B: MIPI_RX2_D1_N / MIPI_RX2_D1_P, MIPI_RX2_D0_N / MIPI_RX2_D0_P, MIPI_RX2_C_N / MIPI_RX2_C_P

J1

1 GND	CAMA_CLKN 3	5 CAMA_CLKP	7 GND
9 CAMA_D0_N	11 CAMA_D0_P	13 GND	15 CAMA_D1_N
17 CAMA_D1_P	19 GND	21 CAMA_D2_N	23 CAMA_D2_P
25 GND	27 CAMA_D3_N	29 CAMA_D3_P	31 GND
33 CAMA_I2C_SDA	35 CAMA_I2C_SCL	37 PGOOD	39 _RST
41 WAKEUP	43 GND	45 GND	47 5V
49 5V	51 5V	53 5V	55 GND
57 GND	59 SD_HST0_CD	61 SD_HST0_CLK	63 SD_HST0_CMD
65 CAM_B_D_PWM	67 CAM_B_PWDN_N	69 AUX_IO_IRQ	71 GND
73 CAMB_CLK	75 GND	77 CAMB_I2C_SCL	79 CAMB_I2C_SDA
81 GND	83 CAMB_D1_N	85 CAMB_D1_P	87 GND
89 CAMB_D0_N	91 CAMB_D0_P	93 GND	95 CAMB_CLKN
97 CAMB_CLKP	99 GND		

2 GND	4 UART_RX	6 UART_TX	8 GND
10 USB_RX_P	12 USB_RX_N	14 GND	16 USB_D_P
18 USB_D_N	20 GND	22 USB_TX_P	24 USB_TX_N
26 GND	28 CAMA_CLK	30 GND	32 SD_HST0_D3
34 CAMA_RST	36 SD_HST0_D2	38 SD_HST0_D1	40 SD_HST0_D0
42 COM_AUX_IO2	44 GND	46 GND	48 5V
50 5V	52 5V	54 5V	56 GND
58 GND	60 SPI_SS_1	62 SPI_SIO0	64 SPI_SIO1
66 SPI_SIO2	68 SPI_SIO3	70 SPI_SS_0	72 GND
74 SPI_SCK	76 GND	78 I2C3_SCL	80 I2C3_SDA
82 GND	84 CAMC_D1_N	86 CAMC_D1_P	88 GND
90 CAMC_D0_N	92 CAMC_D0_P	94 GND	96 CAMC_CLKN
98 CAMC_CLKP	100 GND		

DF40HC(3.0)-100DS-0.4V_BW1099G2 Receptacle 3mm

UART_RX, UART_TX

USB_RX_P / USB_RX_N, USBD2_P / USBD2_N, USB_TX_P / USB_TX_N

Power_trace
Parameter Set
VBUS — USB_M — USBD2_P / USBD2_N

CAM_A_CLK_OUT, CAM_A_PWDN_N, SD_HST0_D3, SD_HST0_D2, SD_HST0_D1, SD_HST0_D0, COM_AUX_IO2

CTL_CAM_A — CAM_A_CLK_OUT / CAM_A_PWDN_N

TP10 COM_AUX_IO2

VDD_5V, VBUS

TP6

SPI
Parameter Set
SPI_SS_1, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3, SPI_SS_0, SPI_SCK

SDIO
Parameter Set
SD_HST0_D0, SD_HST0_D1, SD_HST0_D2, SD_HST0_D3, SD_HST0_CLK, SD_HST0_CMD, SD_HST0_CD

MIPI_CAM_C — MIPI_RX3_D1_N / MIPI_RX3_D1_P, MIPI_RX3_D0_N / MIPI_RX3_D0_P, MIPI_RX3_C_N / MIPI_RX3_C_P

Parameter Set MIPI_CAM_B

Parameter Set MIPI_CAM_C

AUX IO HEADER

J5 (20021121-00010T1LF)

MODULE_nRST 1	2 I2C3_SCL	AUX_IO_IRQ 3	4 I2C3_SDA
2485_PGOOD 5	6 UART_RX	2485_WAKEUP 7	8 UART_TX
9 GND	10 GND		

SPI HEADER

J7 (20021121-00010T1LF)

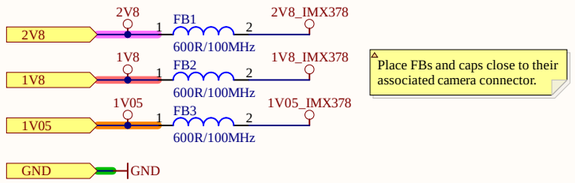
SPI_SCK 1	2 SPI_SIO0	3	4 SPI_SIO1
SPI_SS_0 5	6 SPI_SIO2	SPI_SS_1 7	8 SPI_SIO3
9 GND	10 GND		

3.3V SD HEADER

J8 (20021121-00010T1LF)

SD_HST0_CLK 1	2 SD_HST0_D0	3	4 SD_HST0_D1
SD_HST0_CMD 5	6 SD_HST0_D2	SD_HST0_CD 7	8 SD_HST0_D3
9 GND	10 GND		

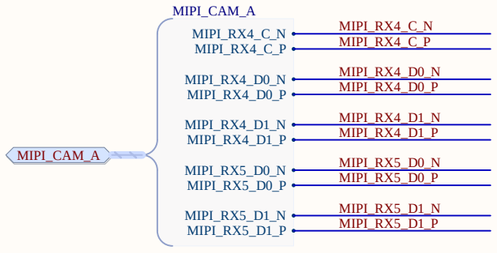
Title: DM1097			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D0000200	Revision: R2M0E2	Cannot open file C:\Users\BrianLuxonis\
Date: 31/08/2021	Time: 16:36:00	Sheet 3 of 17	
Drawn by: David Malovrh			



Place FBs and caps close to their associated camera connector.

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

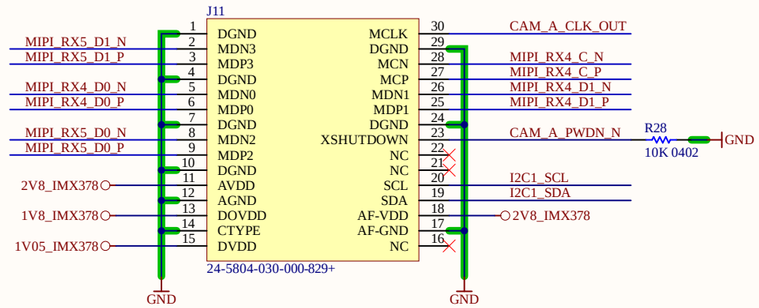
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

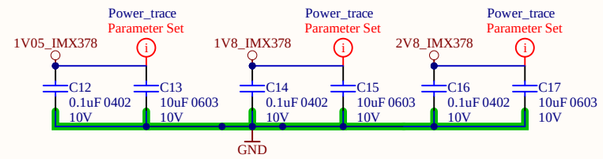


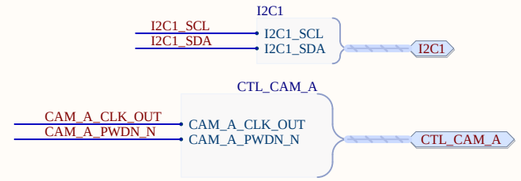
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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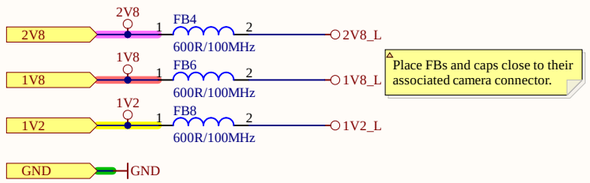
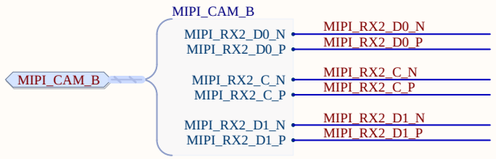
Date: 31/08/2021 Time: 16:36:00	Sheet 4 of 17		
Drawn by: ***David Malovrh***			

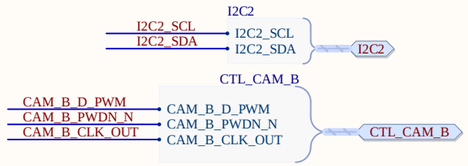


MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

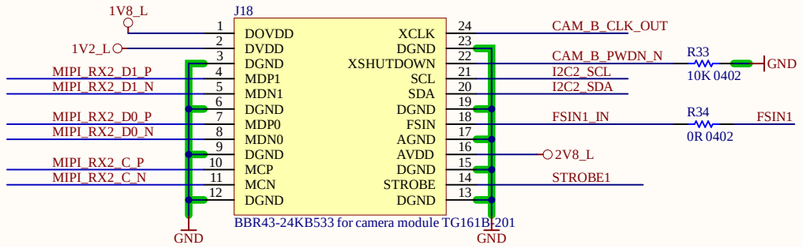
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

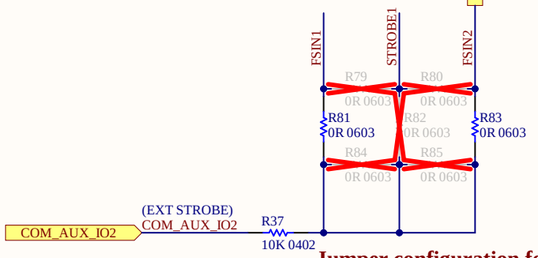


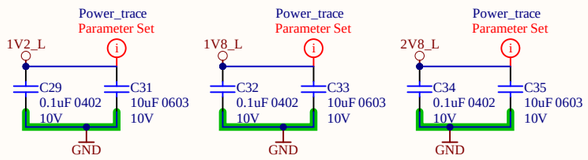


Mark "LEFT" on PCB

Place so that is the module's left camera.







PCB NOTE: Add below diagram to the PCB

Supported Modes of Operation

NO SYNC

NORMAL

TIMING MASTER

TIMING SLAVE

Jumper configuration for FSIN and STROBE pins

This header is used for configuring the STROBE signal direction between the camera boards by using jumpers. A strobe signal may drive FSIN signal for waking up a sensor from its low power mode. See the "Supported Modes of Operation" note for supported jumper settings.

- "NO SYNC" is the mode in which none of the camera modules is excited by any strobe signal.

- "NORMAL" mode means STROBE mechanism works only among the stereo cameras themselves. In this mode, CAM1 strobe is connected to the CAM2 FSIN input.

- "TIMING MASTER" mode means CAM1 STROBE signal drives the EXT_STROBE signal as well as the CAM2 FSIN input. EXT_STROBE signal circulates among the other camera ports so that one camera module can manage the timing of all cameras within the system.

- "TIMING SLAVE" mode uses external strobe signal which is driven externally by another camera. In this mode, CAM1 and CAM2 are excited by the EXT_STROBE signal.

Note that, at most only one camera can be in the "TIMING MASTER" mode at a time. STROBE generation and FSIN reception should be configured via software.

Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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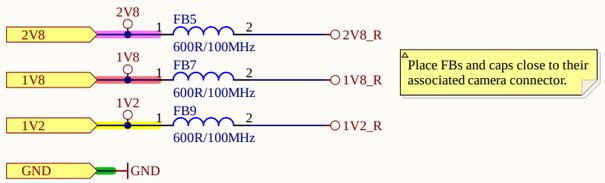

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MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

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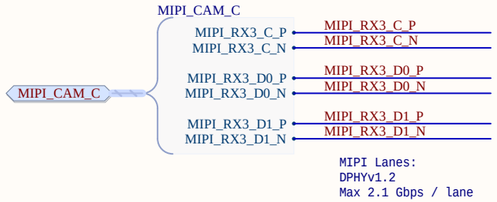
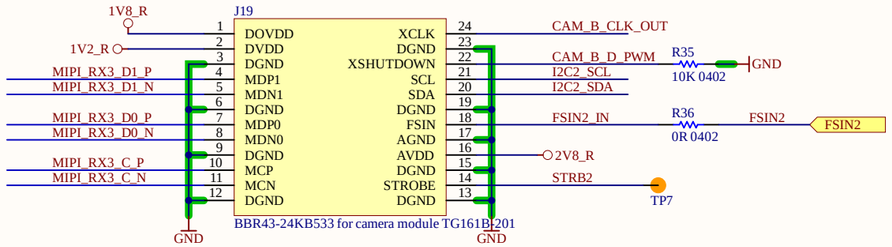
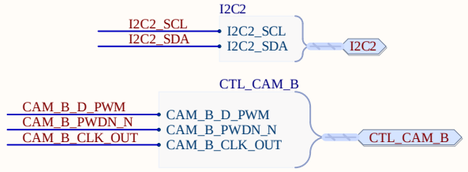
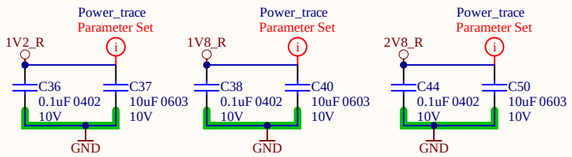


Mark "RIGHT" on PCB
Place so that is the module's right camera.







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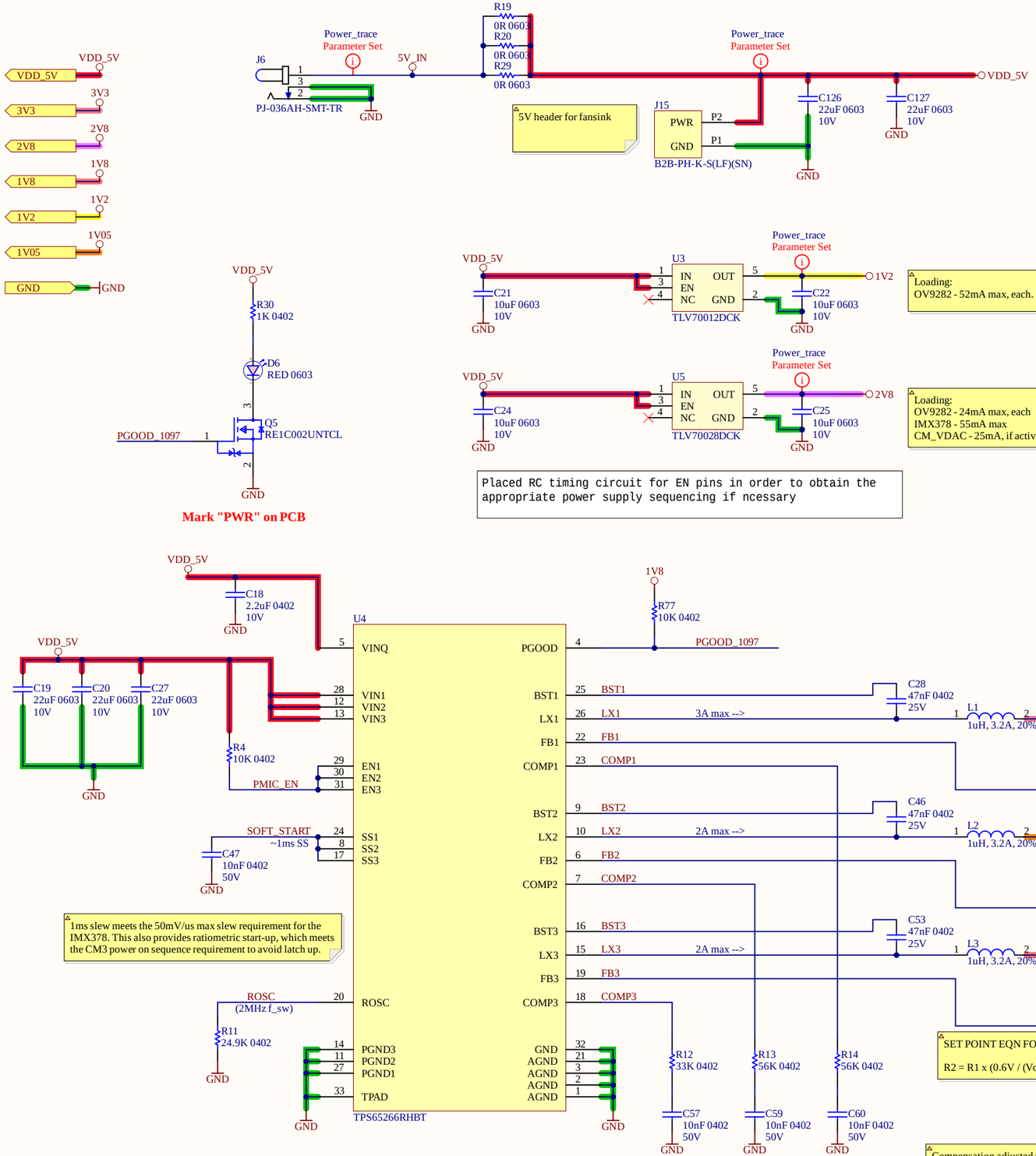
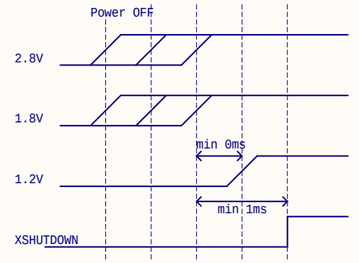
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title: DM1097			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D0000200	Revision: R2M0E2	Cannot open file C:\Users\BrianLuxonis\
Date: 31/08/2021	Time: 16:36:00	Sheet 6 of 17	
Drawn by: David Malovrh			



OV9282 POWER REQUIREMENTS

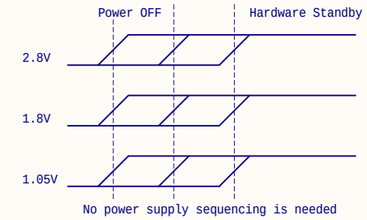


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

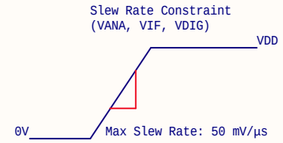
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA



POWER SEQUENCING REQUIREMENTS:

The CM3 reqeuests a power sequence such that, "supplies should be staggered so that the highest voltage comes up first, then the remaining voltages in descending order. this is to avoid forward biasing internal (on-chip) diodes between supplies, and causing latch-up. Alternatively supplies can be synchronised to come up at exactly the same time as long as at no point a lower voltages supply rail exceeeds a higher voltage supply rail."

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

Effective capacitance targets for each rail, taking into account DC bias and other effects:
3.3V C_eff = 24uF
1.8V C_eff = 26uF
1.05V C_eff = 70uF

Voltage ripple and allowed voltage tolerance on all rails is +/-5%

Load step design assumptions, based on worst case rail loading:
3.3V - 2.5A step
1.8V - 1A step
1.05 - 0.5A step

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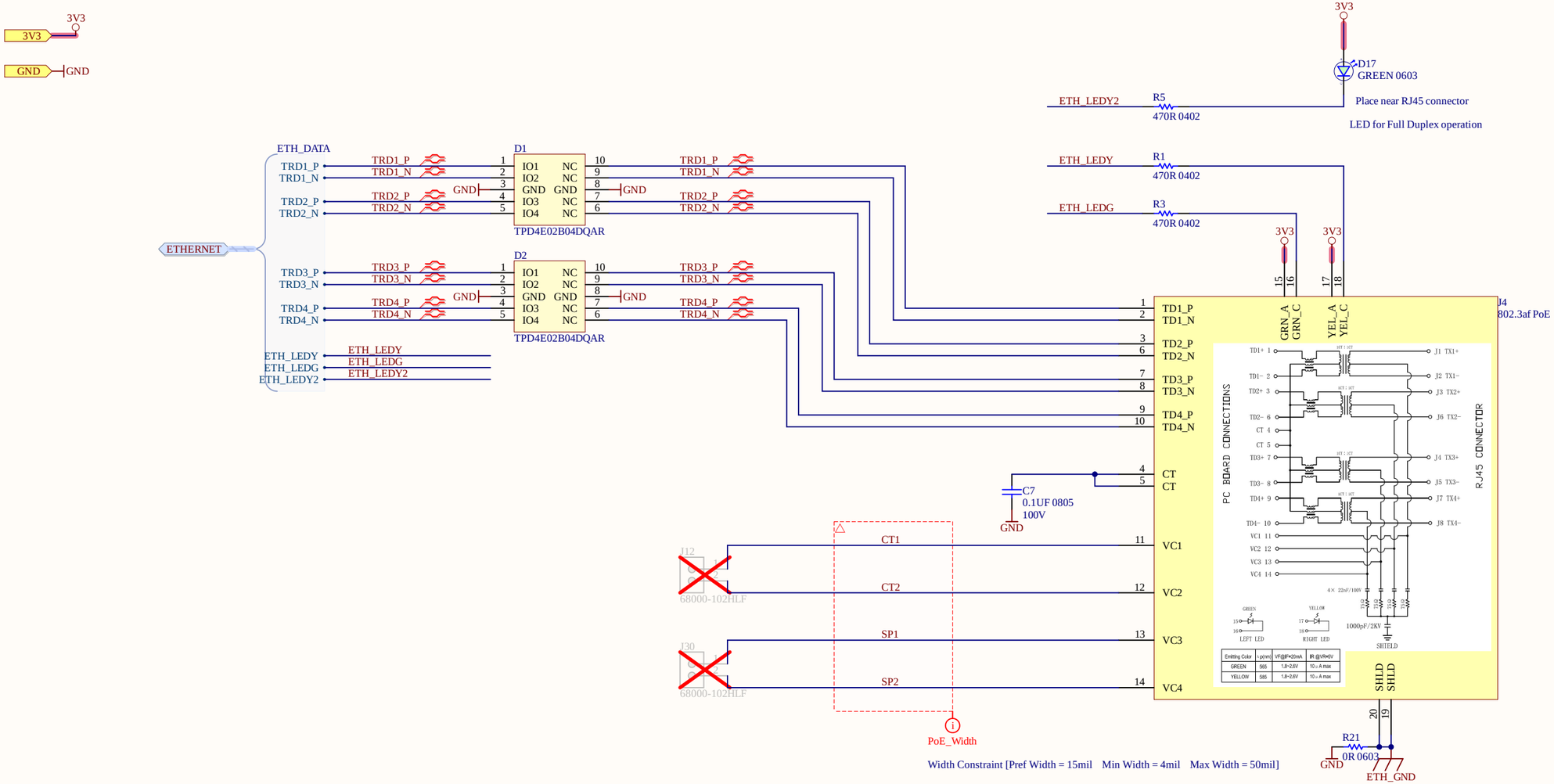
Date: 31/08/2021 Time: 16:36:01	Sheet 7 of 17		
Drawn by: ***David Malovrh***			



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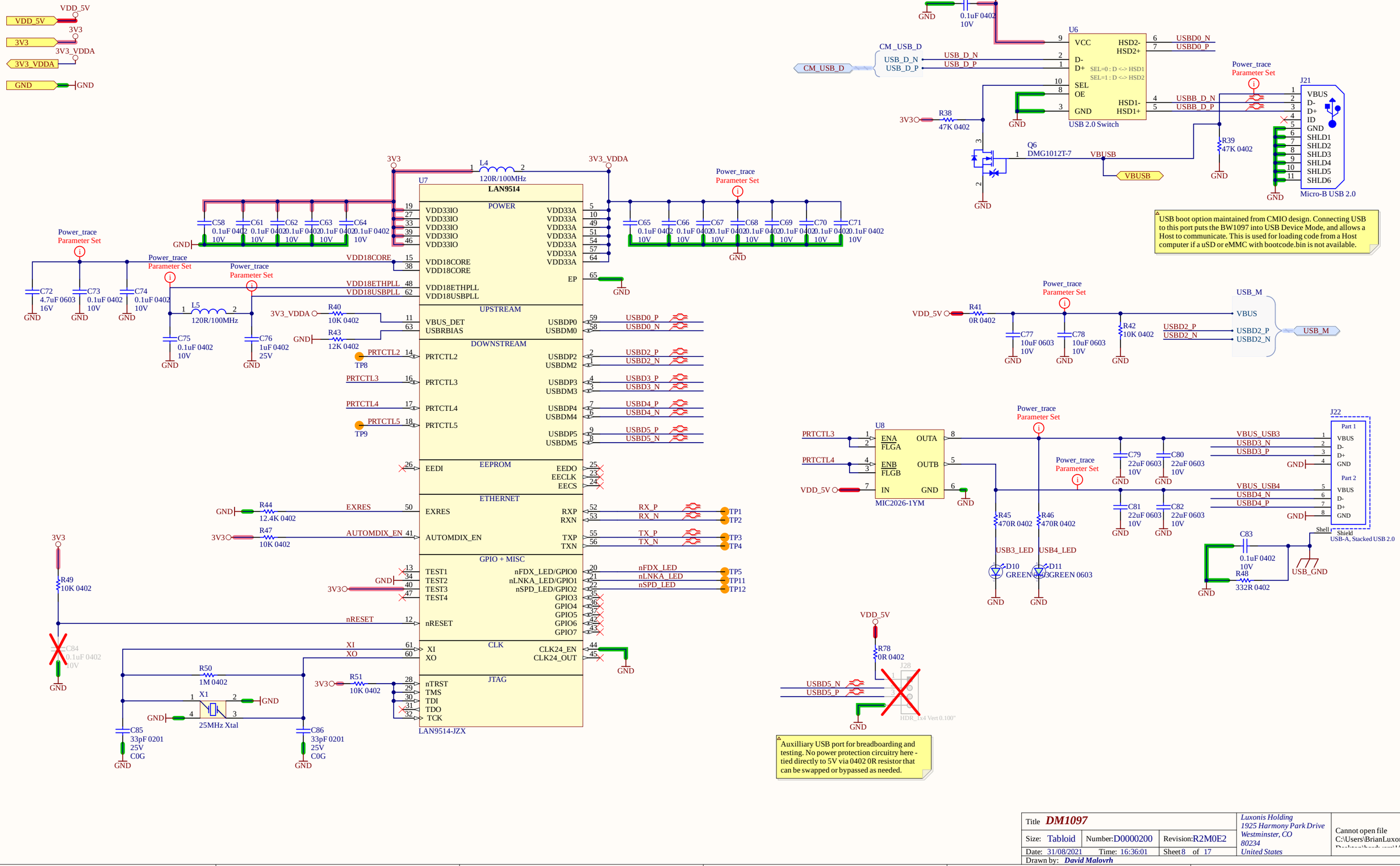
Drawn by: David Malovrh				



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Drawn by: *David Malovrh*			

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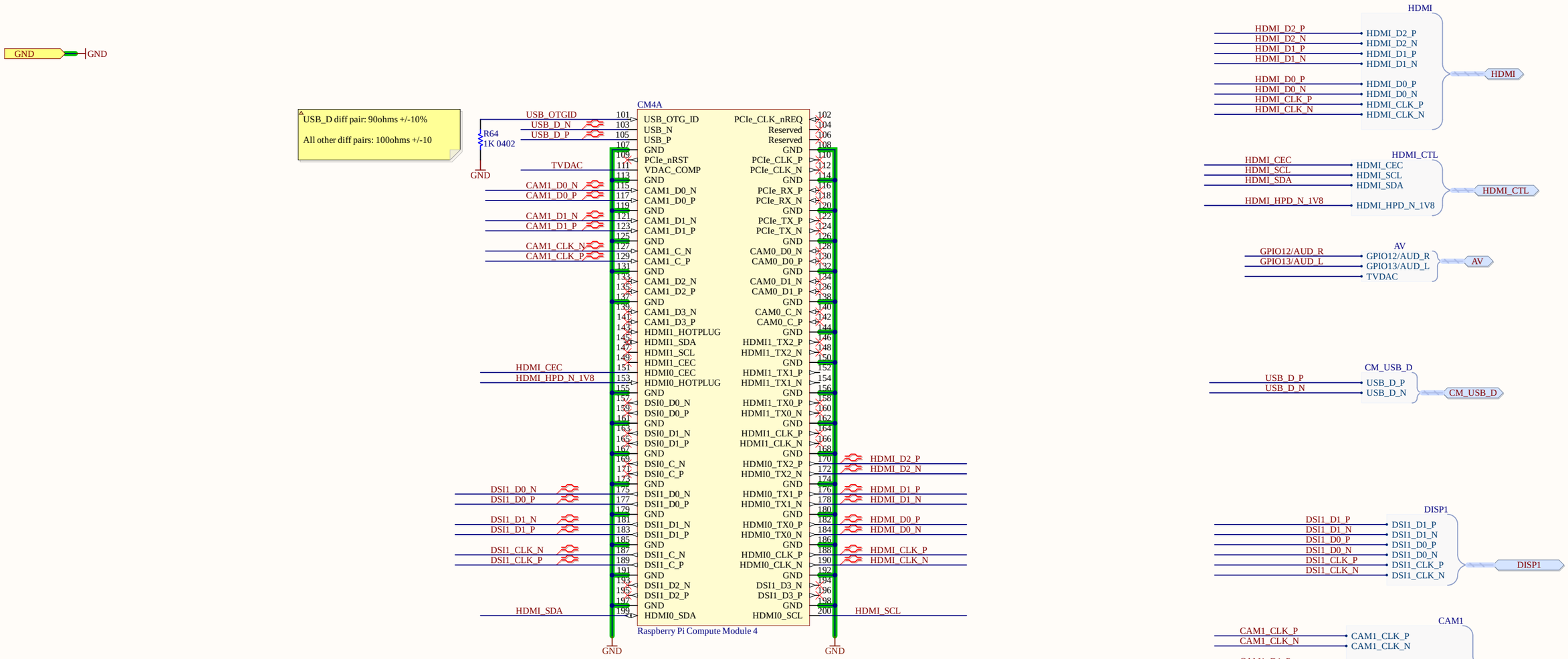

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Date: 31/08/2021	Time: 16:36:01	Sheet 9 of 17	
Drawn by: ***David Malovrh***			

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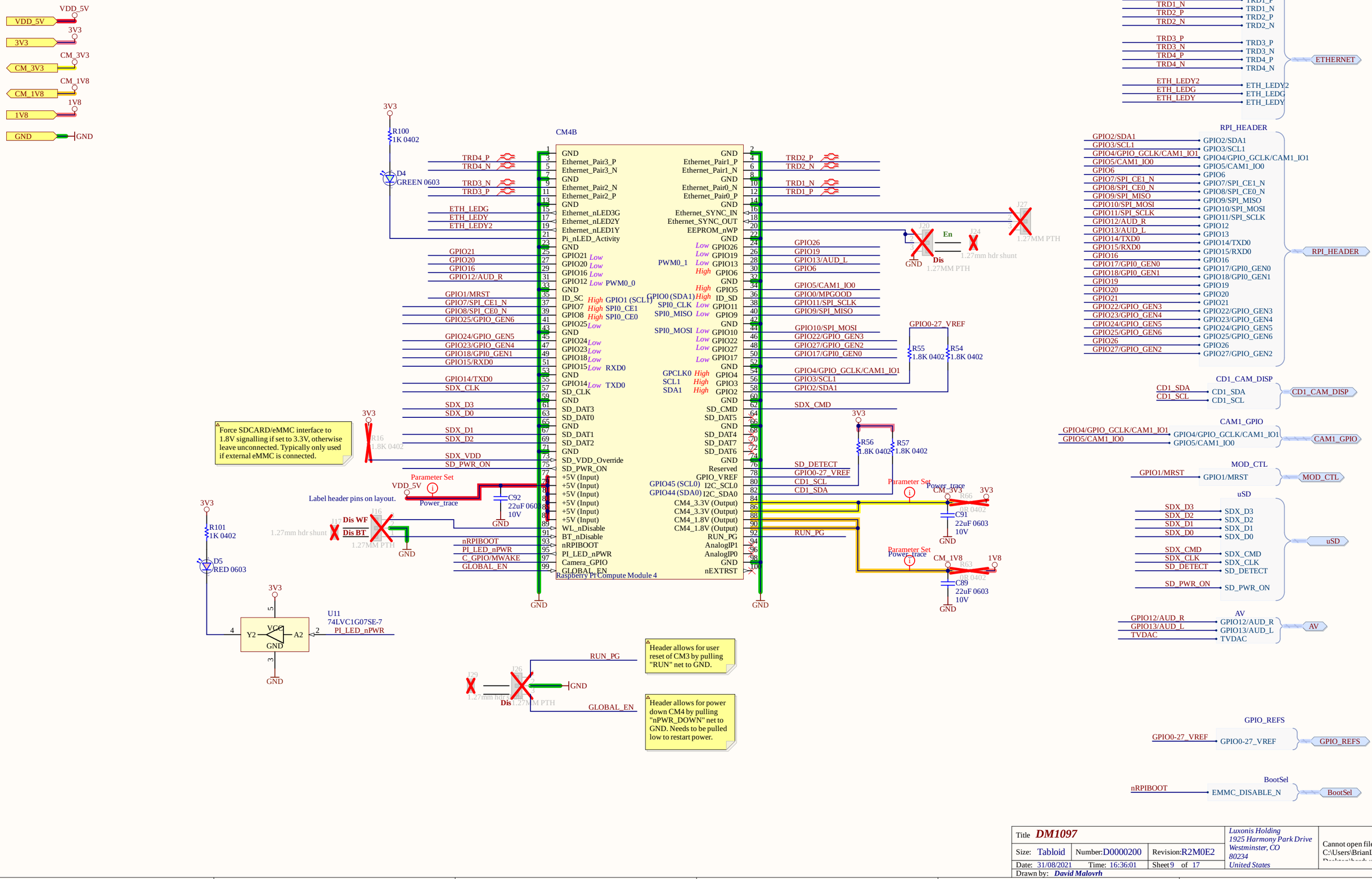

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Number	D0000200
Revision	R2M0E2
Date	31/08/2021
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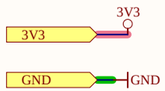
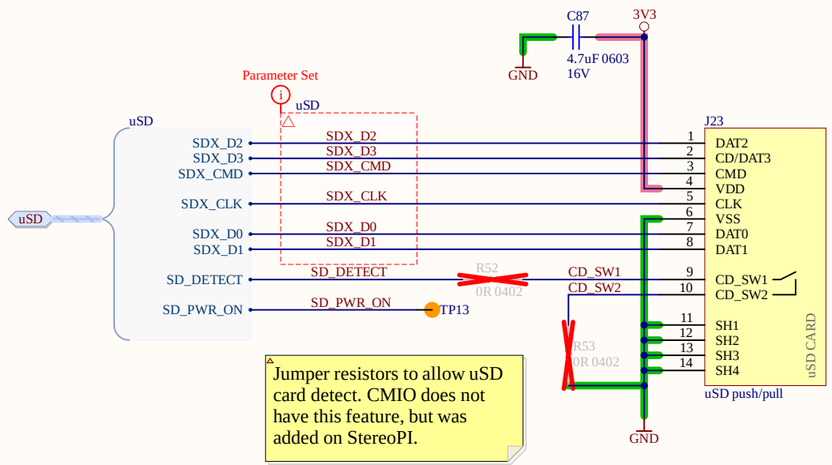


CMIO Note:

uSD is only used for modules with no on-board Flash (eMMC)



Jumper resistors to allow uSD card detect. CMIO does not have this feature, but was added on StereoPI.

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Date: 31/08/2021 Time: 16:36:01	Sheet 10 of 17		
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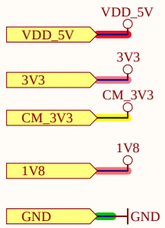

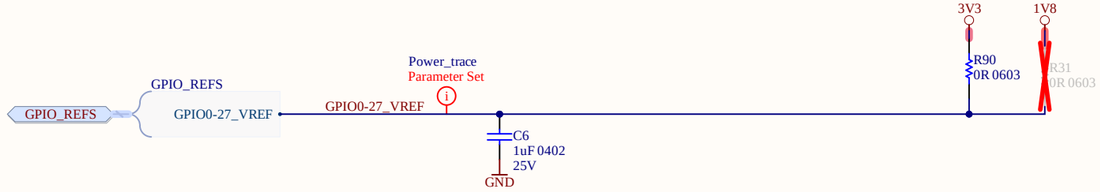

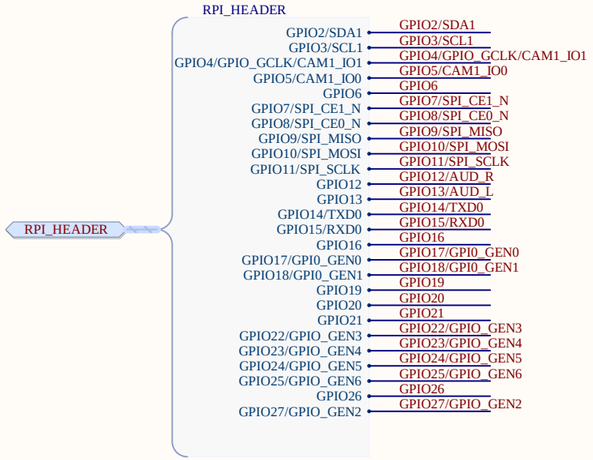

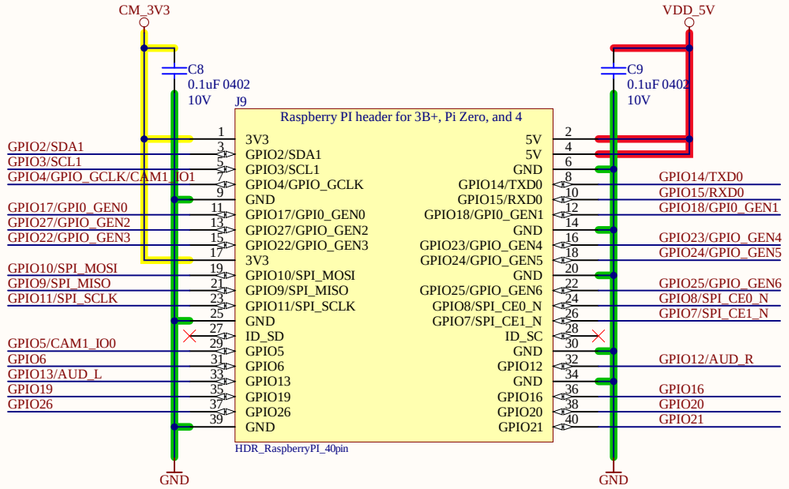

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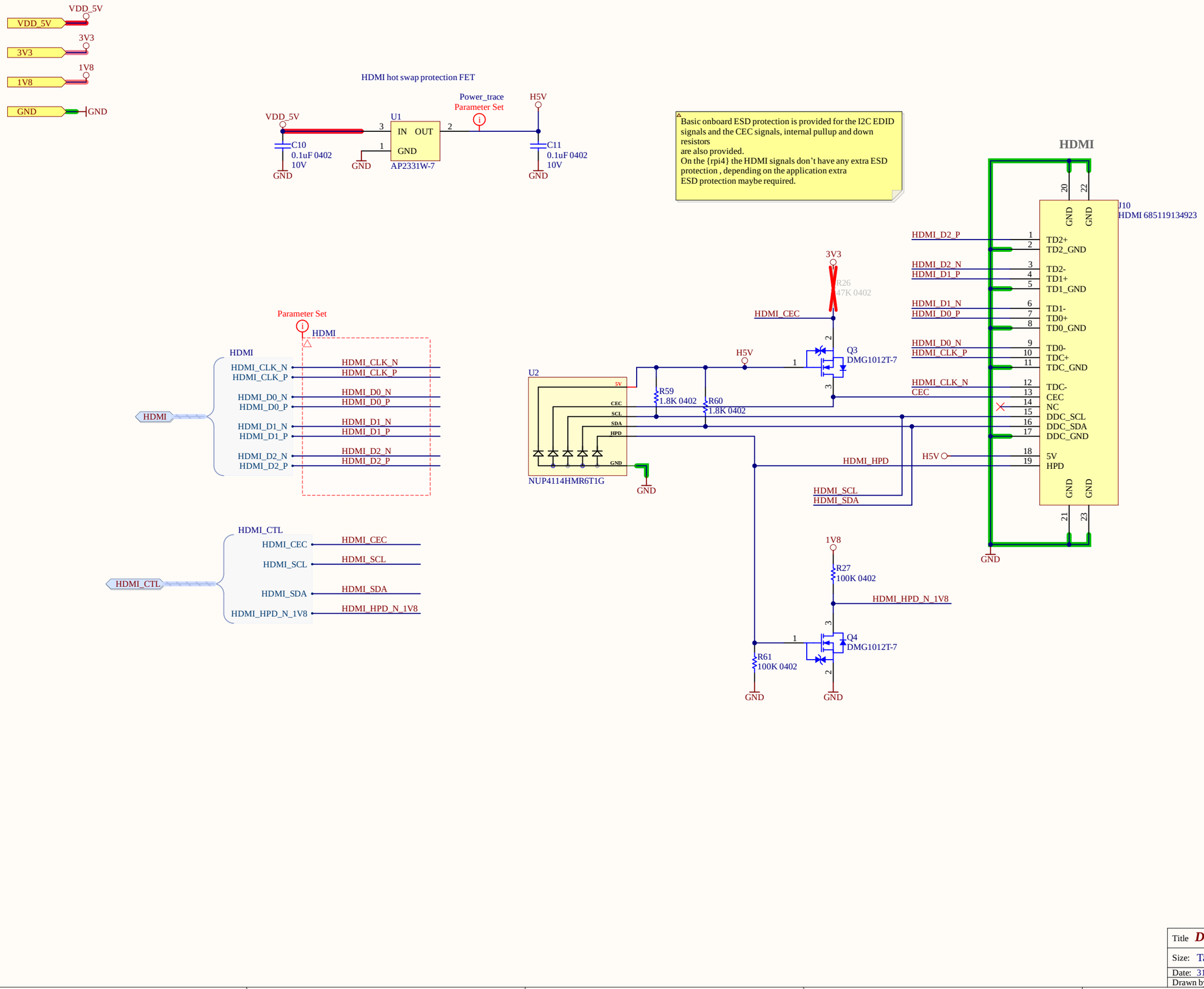

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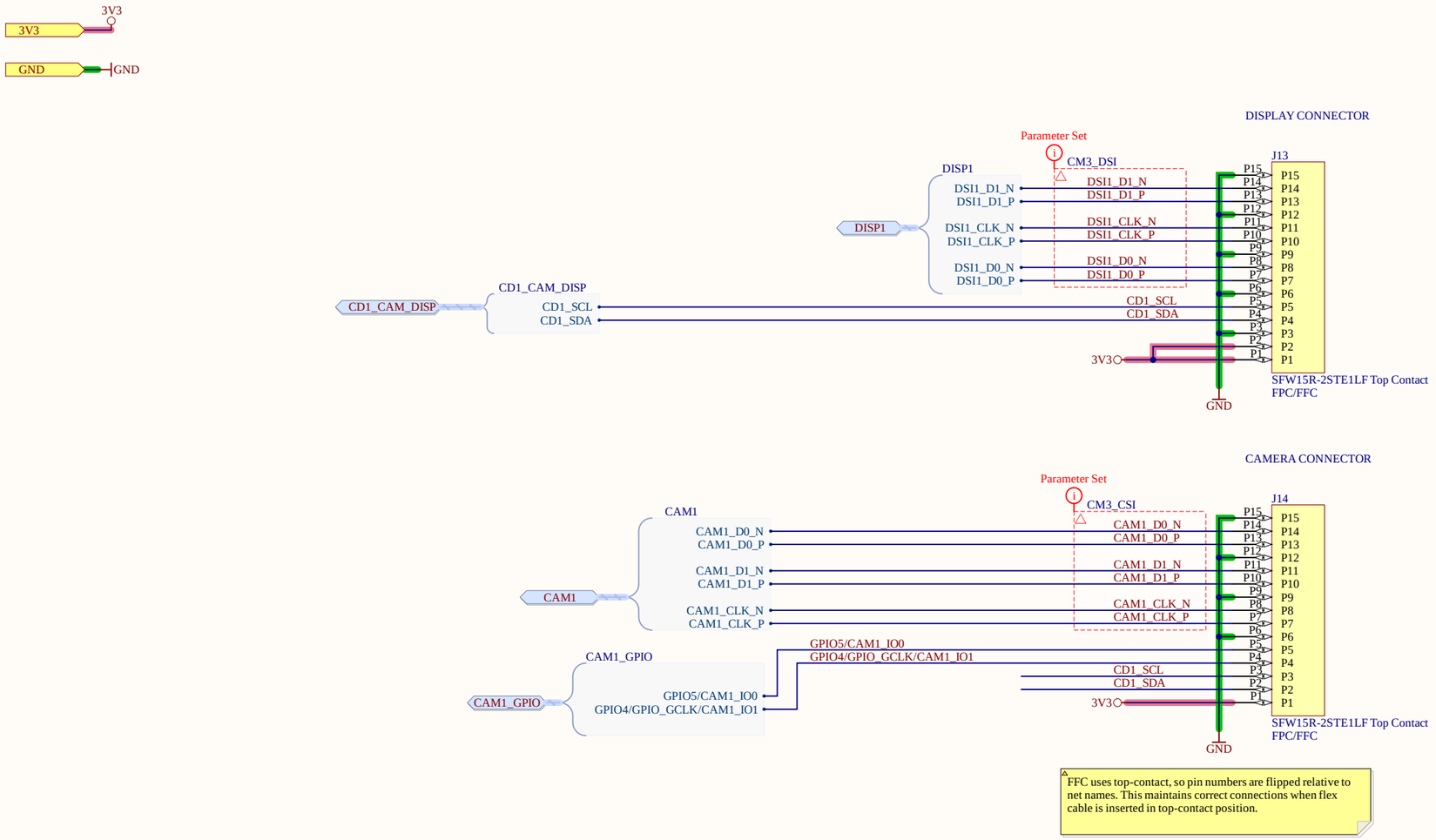

CMIO/CM3 guide for attaching display + camera (https://www.raspberrypi.org/documentation/hardware/computemodule/cmio-display.md) uses:

GPIO0 - CD1_SDA
GPIO1 - CD1_SCL
GPIO4 - CAM1_IO1
GPIO5 - CAM1_IO0

.dts file provided on that guide for this configuration.

NOTES:
(1) GPIO4/GPIO_GCLK and GPIO5 are also broken out to the standard 40-pin, 3B+-style header on this board.
(2) CAM1 and DISP1 are both 4-lane MIPI busses, but the 15-pin connectors only support 2-lane.

The PiCam V2.1 uses only the camera connector Pin 11 (CAM1_IO0) as an Enable pin, so this pin needs to be pulled high by default to enable camera usage, regardless of what GPIO it is connected to.

Both GPIO4 and GPIO5 are weakly pulled up by default in the BCM (see pg. 102 https://www.raspberrypi.org/app/uploads/2012/02/BCM2835-ARM-Peripherals.pdf)

FFC uses top-contact, so pin numbers are flipped relative to net names. This maintains correct connections when flex cable is inserted in top-contact position.

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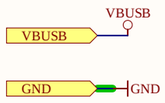
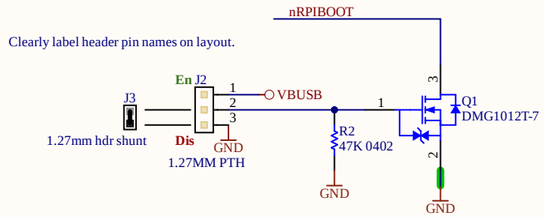


MODULE BOOT OPTIONS:

Short the nRPIBOOT pin to ground to force USB boot mode. The CM4IO board has a jumper for nRPIBOOT This can be
used to enable different boot modes (e.g. network) and enable UART logging.



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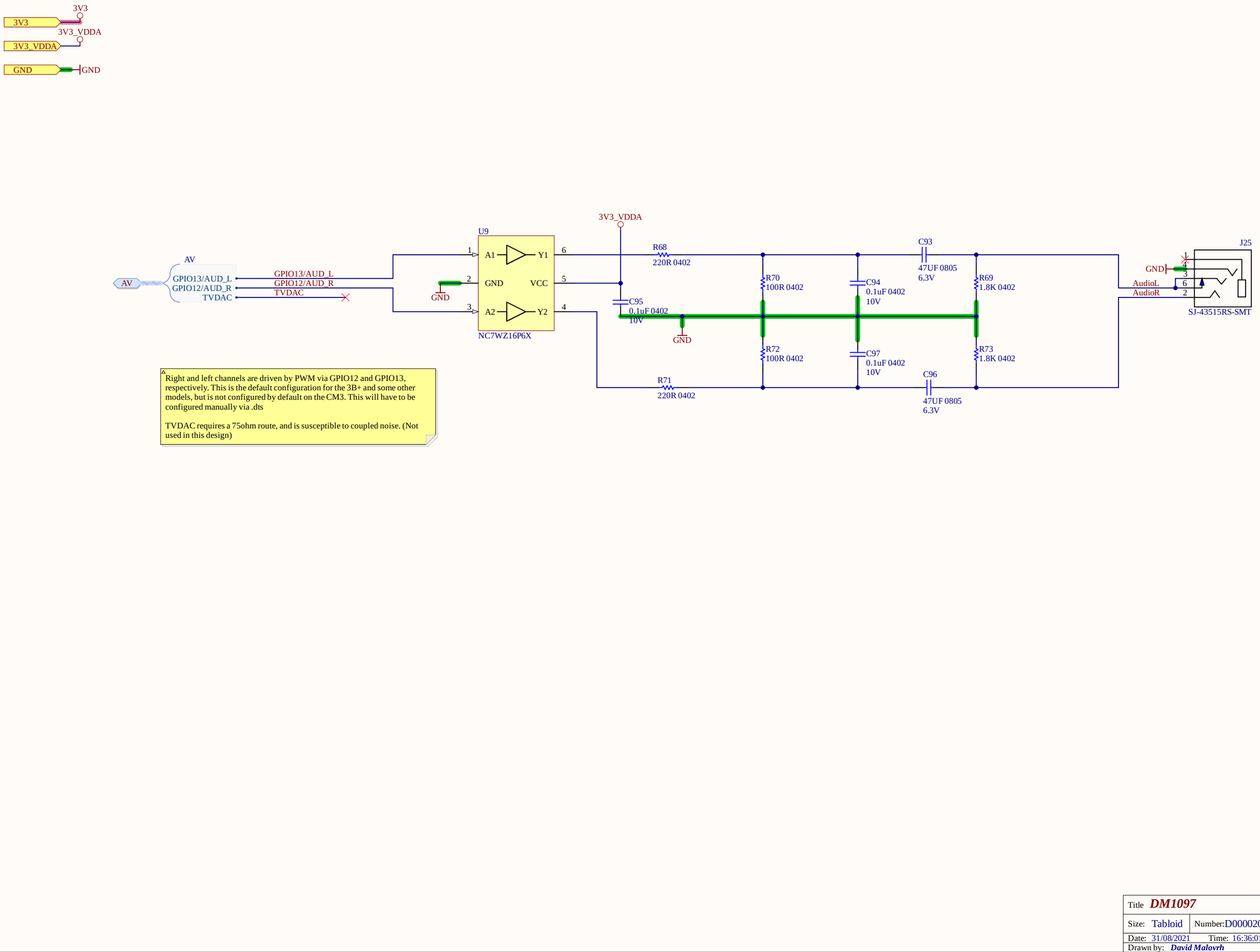

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