

A

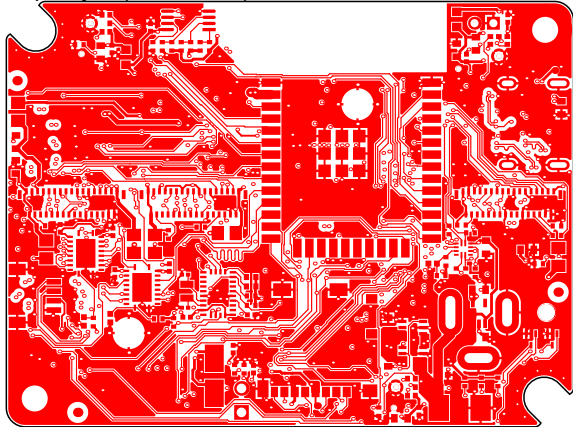
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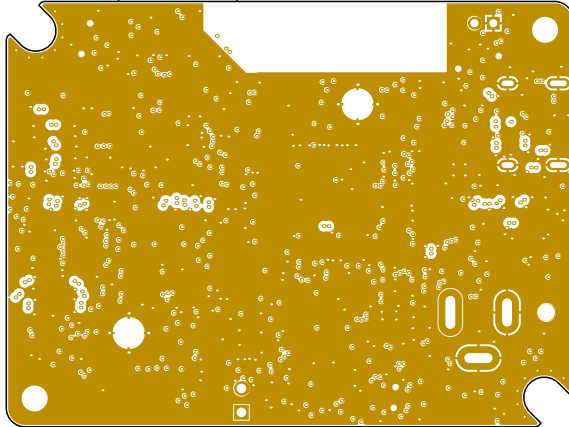
D

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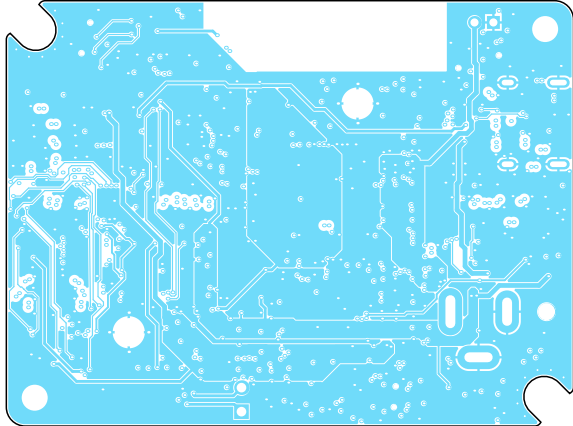
Top Layer (Scale 1.25)



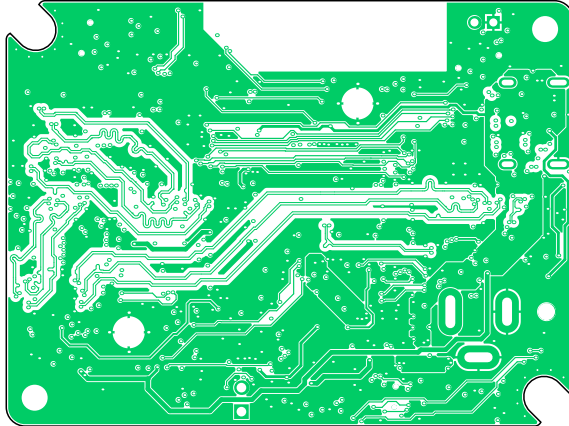
Ground 1 (Scale 1.25)



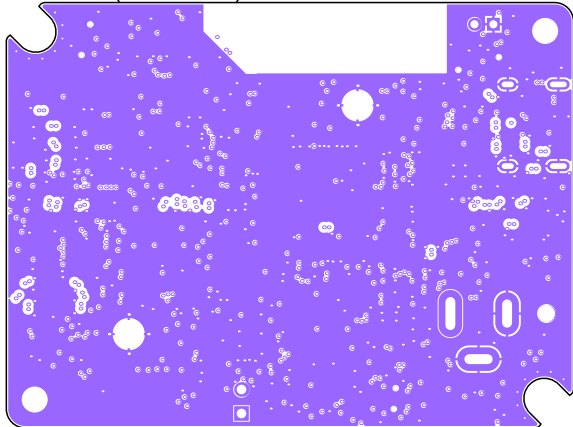
Inner Layer 1 (Scale 1.25)



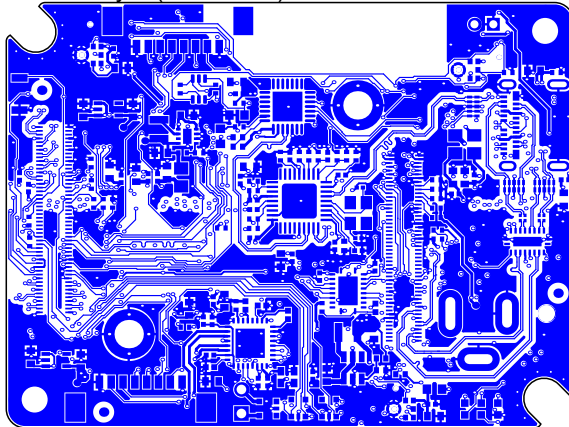
Inner Layer 2 (Scale 1.25)



Ground 2 (Scale 1.25)



Bottom Layer (Scale 1.25)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

- * PCB has 6 copper layers
- * Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- * PCB thickness: Please refer to the Board layer stack legend
- * Min. trace width/clearance: 4/4mil
- * Min. hole drill/ring: 8mil/16mil
- * Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- * Silkscreen, non-conductive epoxy ink, color: white
- * Solder mask color: green
- * Remove silkscreen as needed to prevent ink on any exposed copper
- * Surface finish: ENIG
- * Hole dimensions are finished size, +/-3mil
- * Linear board dimension tolerance: +/-10mil
- * Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- * PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- * PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- * All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.
- * GM1 shall be used as a board outline

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: **NG2092**

Number: DXXXX

Revision: R0M0
E0

Date: 18/08/2021

Sheet: 1 of 3

Drawn by: Nejc Gostincar

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Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊗	748	7.99mil(0.203mm)	Plated	
▽	8	10.00mil(0.254mm)	Plated	
□	6	19.69mil(0.500mm)	Non-Plated	
⊛	4	23.62mil(0.600mm)	Plated	
○	2	33.86mil(0.860mm)	Plated	
☆	2	40.16mil(1.020mm)	Plated	
✧	3	41.34mil(1.050mm)	Plated	
☆	1	70.87mil(1.800mm)	Non-Plated	
⊕	2	108.27mil(2.750mm)	Plated	
◇	2	118.11mil(3.000mm)	Plated	
	778 Total			

Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.59mil(0.015mm)	Solder Mask	GTS		3,8
Top Layer	1.38mil(0.035mm)	Signal	GTL		
	3.94mil(0.100mm)	Dielectric			4,05
Inner Layer 1	0.71mil(0.018mm)	Signal	G1		
	22.24mil(0.565mm)	Dielectric			4,5
Ground 1	0.71mil(0.018mm)	Signal	G2		
	5.00mil(0.127mm)	Dielectric			4,25
Inner Layer 2	0.71mil(0.018mm)	Signal	G3		
	22.24mil(0.565mm)	Dielectric			4,5
Ground 2	0.71mil(0.018mm)	Signal	G4		
	3.94mil(0.100mm)	Dielectric			4,05
Bottom Layer	1.38mil(0.035mm)	Signal	GBL		
Bottom Mask	0.59mil(0.015mm)	Solder Mask	GBS		3,8
Bottom Overlay		Legend	GBO		
Total thickness: 64.14mil(1.629mm)					

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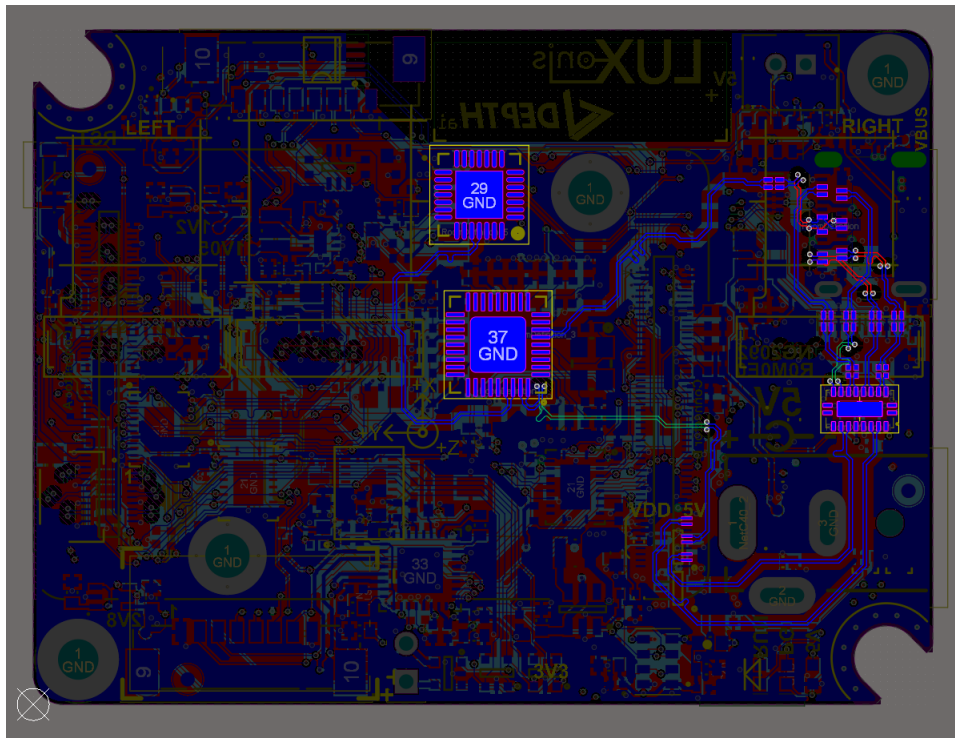
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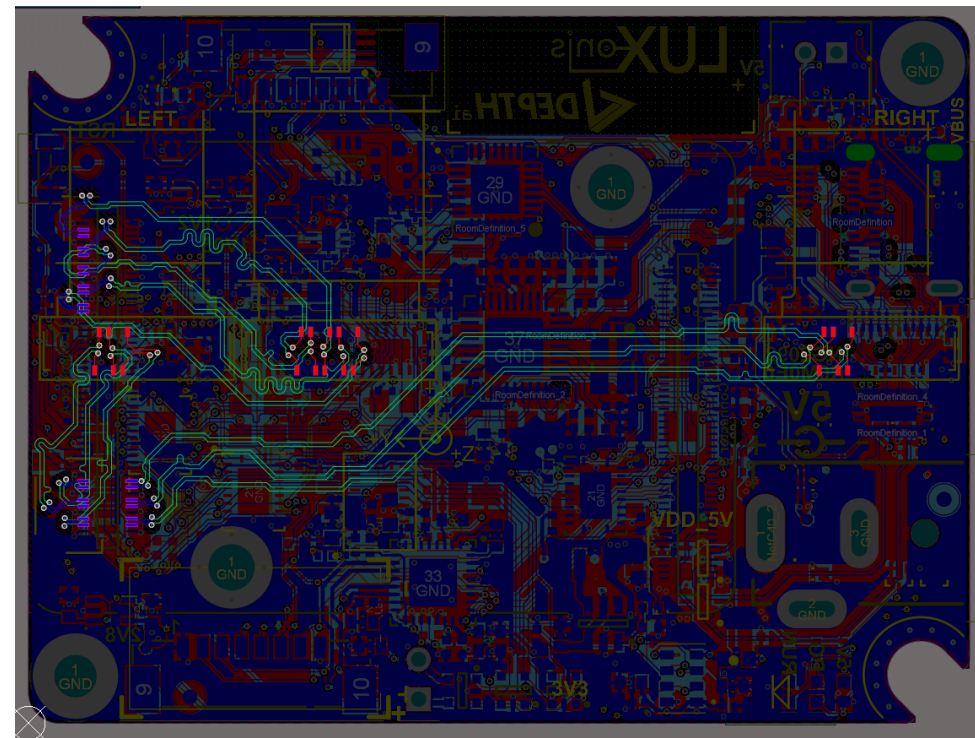
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90 OHM (+/-10%) DIFF PAIRS



100 OHM (+/-10%) DIFF PAIRS

Transmission Line Structure Table

Impedance Id	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
1	90	90.88	Top Layer	0.13mm(5.00mil)	0.11mm(4.45mil)	0.10mm(4.00mil)	Inner Layer 1
2	100	101.51	Top Layer	0.10mm(4.00mil)	0.09mm(3.45mil)	0.11mm(4.50mil)	Inner Layer 1
3	50	56.74	Top Layer	0.13mm(4.92mil)	0.13mm(4.92mil)		Inner Layer 1
4	50	50.00	Inner Layer 1	0.13mm(5.00mil)	0.13mm(5.00mil)		Top Layer,Ground 1
6	90	90.04	Inner Layer 2	0.10mm(3.94mil)	0.10mm(3.94mil)	0.10mm(3.99mil)	Ground 1,Ground 2
7	100	100.65	Inner Layer 2	0.10mm(4.00mil)	0.09mm(3.72mil)	0.15mm(6.00mil)	Ground 1,Ground 2
8	50	50.00	Inner Layer 2	0.16mm(6.19mil)	0.16mm(6.19mil)		Ground 1,Ground 2
10	90	90.88	Bottom Layer	0.13mm(5.00mil)	0.11mm(4.45mil)	0.10mm(4.00mil)	Ground 2
11	100	101.51	Bottom Layer	0.10mm(4.00mil)	0.09mm(3.45mil)	0.11mm(4.50mil)	Ground 2
12	50	56.75	Bottom Layer	0.13mm(4.92mil)	0.13mm(4.92mil)		Ground 2

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