Project: DM1092
Current Revision: R2M2E2

DM1092 Revision History:

Date	Revision	Reason for Change	Changes Implemented
December 7th, 2020	BW1092_R0M0E0 -> DM1092_R0M0E0	1. IMU data transfer maximum 1kHz rate over I2C 2. Issues with floating lines (to weak MX pull-up) 3. No everse polarity protection 4. No tooling holes 5. Camera sync text and resistor selection depricated 6. IMX camera flat cable to short for 1.6mm PCB	1. Changed power supply from 3V3 to 1V8 for IO, removed INT, RSTn and BOOTN from level shifter. Removed I2C3_3V3 interface added SPI0 connected directly to MX bus. Corrected chip setup for SPI. Updated routing and matched signals. 2. Added 10k pullups to BNO08x_INT_1V8 and BNO08x_RSTn_1V8 3. Added rev. polarity protection from OAK-D 4. Added two 2mm non-plated tooling holes 5. Remved unnecessary camera sync text and resistor options 6. Updated footprint
February 3rd, 2021	DM1092_R0M0E0 -> DM1092_R1M1E1	1. Improve antenna keepout 2. Remove ENV_I2C due to wrong routing and currently no use case on field	1. Extended copper keepout around antenna and moved traces form that zone 2. Removed QWIIC connector J12 and its circuitry from PCB and schematic
June 26th, 2021	DM1092_R1M1E1 -> DM1092_R2M2E2	1. Arducam CCM is to big so more clearance must be ensured between the CCM and ESP32 2. Correct annotation table content	1. Moved ESP32 away from RGB CCM and updated layout 2. Corrected annotation table on this page, PUs for 3V3 bank connected to 3V3 rail

ESP32 WROOM IO_MUX															DM1092				BW1099EMB		
ESP32 Pin	ESP32-WROOM-32D PIN	Analog Function1	Analog Function2	Analog Function3	RTC Function1	RTC Function2	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	At RST	After RST	DM1092 NET NAME	Level Shift	Level Shifted NET NAME	QUIIC / AUX connector	1099 Connector PIN	1099 NET NAME	1099 PU/PD
5	4	ADC_H	ADC1_CH0		RTC_GPIO0		GPIO36		GPIO36				oe=0,ie=0	oe=0,ie=0	ESP_GPI36	no	n/a	AUX: J5,6			
8	5	ADC_H	ADC1_CH3		RTC_GPIO3		GPIO39		GPIO39				oe=0,ie=0	oe=0,ie=0	ESP_GPI39	no	n/a	AUX: J5,7			
10	6		ADC1_CH6		RTC_GPIO4		GPIO34		GPIO34				oe=0,ie=0	oe=0,ie=0	ESP_GPI34	no	n/a	AUX: J5,4			
11	7		ADC1_CH7		RTC_GPIO5		GPIO35		GPIO35				oe=0,ie=0	oe=0,ie=0	ESP_GPI35	no	n/a	AUX: J5,5			
12	8	XTAL_32K_P	ADC1_CH4	TOUCH9	RTC_GPIO9		GPIO32		GPIO32				oe=0,ie=0	oe=0,ie=0	MX_INT_3V3	3.3V <-> 1.8V	MX_INT_1V8		59	GPIO_7	40.2kR/1.8V
13	9	XTAL_32K_N	ADC1_CH5	TOUCH8	RTC_GPIO8		GPIO33		GPIO33				oe=0,ie=0	oe=0,ie=0	MX_RST_3V3	3.3V <-> 1.8V	MX_RST_1V8		39	SYS_RST	10kR/1.8V
14	10	DAC_1	ADC2_CH8		RTC_GPIO6		GPIO25		GPIO25			EMAC_RXD0	oe=0,ie=0	oe=0,ie=0	I2C3_SCL_3V3	3.3V <-> 1.8V	I2C3_SCL_1V8	QUIIC: J11,1	78	GPIO_24	2.2kR/1.8V
15	11	DAC_2	ADC2_CH9		RTC_GPIO7		GPIO26		GPIO26			EMAC_RXD1	oe=0,ie=0	oe=0,ie=0	I2C3_SDA_3V3	3.3V <-> 1.8V	I2C3_SDA_1V8	QUIIC: J11,2	80	GPIO_25	2.2kR/1.8V
16	12		ADC2_CH7	TOUCH7	RTC_GPIO17		GPIO27		GPIO27			EMAC_RX_DV	oe=0,ie=0	oe=0,ie=1	ESP_GPIO27	no	n/a		60	GPIO_8	no
17	13		ADC2_CH6	TOUCH6	RTC_GPIO16		MTMS	HSPICLK	GPIO14	HS2_CLK	SD_CLK	EMAC_TXD2	oe=0,ie=0	oe=0,ie=1	ESP_GPIO14	no	n/a	AUX: J6,6	36	GPIO_36_3V3	40.2kR/3.3V
18	14		ADC2_CH5	TOUCH5	RTC_GPIO15		MTDI	HSPIQ	GPIO12	HS2_DATA2	SD_DATA2	EMAC_TXD3	oe=0,ie=1,wpd	oe=0,ie=1,wpd	ESP_GPIO12	no	n/a	AUX: J6,4	63	GPIO_33_3V3	40.2kR/3.3V
20	16		ADC2_CH4	TOUCH4	RTC_GPIO14		MTCK	HSPID	GPIO13	HS2_DATA3	SD_DATA3	EMAC_RX_ER	oe=0,ie=0	oe=0,ie=1	ESP_GPIO13	no	n/a	AUX: J6,5	61	GPIO_32_3V3	40.2kR/3.3V
21	23		ADC2_CH3	TOUCH3	RTC_GPIO13	I2C_SDA	MTDO	HSPICS0	GPIO15	HS2_CMD	SD_CMD	EMAC_RXD3	oe=0,ie=1,wpu	oe=0,ie=1,wpu	ESP_GPIO15	no	n/a	AUX: J6,7	32	GPIO_37_3V3	300kR/GND
22	24		ADC2_CH2	TOUCH2	RTC_GPIO12	I2C_SCL	GPIO2	HSPIWP	GPIO2	HS2_DATA0	SD_DATA0		oe=0,ie=1,wpd	oe=0,ie=1,wpd	ESP_GPIO2	no	n/a	AUX: J6,2	40	GPIO_34_3V3	40.2kR/3.3V
23	25		ADC2_CH1	TOUCH1	RTC_GPIO11	I2C_SDA	GPIO0	CLK_OUT1	GPIO0			EMAC_TX_CLK	oe=0,ie=1,wpu	oe=0,ie=1,wpu	ESP_GPIO0	no	n/a				
24	26		ADC2_CH0	TOUCH0	RTC_GPIO10	I2C_SCL	GPIO4	HSPIHD	GPIO4	HS2_DATA1	SD_DATA1	EMAC_TX_ER	oe=0,ie=1,wpd	oe=0,ie=1,wpd	ESP_GPIO4	no	n/a	AUX: J6,3	38	GPIO_35_3V3	40.2kR/3.3V
25	27						GPIO16	GPIO16	HS1_DATA4	U2RXD		EMAC_CLK_OUT	oe=0,ie=0	oe=0,ie=1	ESP_GPIO16	no	n/a	AUX: J5,2			
27	28						GPIO17	GPIO17	HS1_DATA5	U2TXD		EMAC_CLK_OUT_180	oe=0,ie=0	oe=0,ie=1	ESP_GPIO17	3.3V <-> 1.8V	GPIO8/SPI0_CS_1	AUX: J5,3			
34	29						GPIO5	VSPICS0	GPIO5	HS1_DATA6		EMAC_RX_CLK	oe=0,ie=1,wpu	oe=0,ie=1,wpu	VSPI_CS0	3.3V <-> 1.8V	SPI0_CS_0		70	SPI_SS_0	1kR/1.8V
35	30						GPIO18	VSPICLK	GPIO18	HS1_DATA7			oe=0,ie=0	oe=0,ie=1	VSPI_SCK	3.3V <-> 1.8V	SPI0_SCK		74	SPI0_SCK	no
38	31						GPIO19	VSPIQ	GPIO19	U0CTS		EMAC_TXD0	oe=0,ie=0	oe=0,ie=1	VSPI_SDI_SIO1	3.3V <-> 1.8V	SPI0_SIO1		64	SPI0_SIO1	no
42	33						GPIO21	VSPIHD	GPIO21			EMAC_TX_EN	oe=0,ie=0	oe=0,ie=1	VSPI_HOLDn_SIO3	3.3V <-> 1.8V	SPI0_SIO3		68	SPI0_SIO3	1kR/1.8V
40	34				U0RXD		CLK_OUT2	GPIO3					oe=0,ie=1,wpu	oe=0,ie=1,wpu	ESP_RXD0	no	n/a				
41	35				U0TXD		CLK_OUT3	GPIO1				EMAC_RXD2	oe=0,ie=1,wpu	oe=0,ie=1,wpu	ESP_TXD0	no	n/a				
39	36						GPIO22	VSPIWP	GPIO22	U0RTS		EMAC_TXD1	oe=0,ie=0	oe=0,ie=1	VSPI_WPn_SIO2	3.3V <-> 1.8V	SPI0_SIO2		66	SPI0_SIO2	1kR/1.8V
36	37						GPIO23	VSPID	GPIO23	HS1_STROBE			oe=0,ie=0	oe=0,ie=1	VSPI_SDO_SIO0	3.3V <-> 1.8V	SPI0_SIO0		62	SPI0_SIO0	no

NOTE:
Green boxes are intended primary usage.

BNO085	DM1092				BW1099EMB		
BNO085 PIN	DM1092 NET NAME	Level Shift	Level Shifted NET NAME	QUIIC / IO connector	1099 Connector PIN	1099 NET NAME	1099 PU/PD
11	BNO08x_RSTn_1V8	no	n/a		6	UART_TX	no
14	BNO08x_INT_1V8	no	n/a		69	GPIO_53	no
18	GPIO8/SPI0_CS_1	3.3V <-> 1.8V	ESP_GPIO27 (ESP_MX_QSPI)		60	GPIO_8	no
19	SPI0_SCK	3.3V <-> 1.8V	VSPI_SCK (ESP_MX_QSPI)		74	SPI0_SCK	no
17	SPI0_SIO0	3.3V <-> 1.8V	VSPI_SDO_SIO0 (ESP_MX_QSPI)		64	SPI0_SIO1	no
20	SPI0_SIO1	3.3V <-> 1.8V	VSPI_SDI_SIO1 (ESP_MX_QSPI)		62	SPI0_SIO0	no
15	ENV_SCL	no	n/a	nc	nc		
16	ENV_SDA	no	n/a	nc	nc		
4	BNO08x_BOOTN_1V8	no	n/a		4	UART_RX	no

NOTE:
Green boxes are intended primary usage.

Title: *DM1092*		*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
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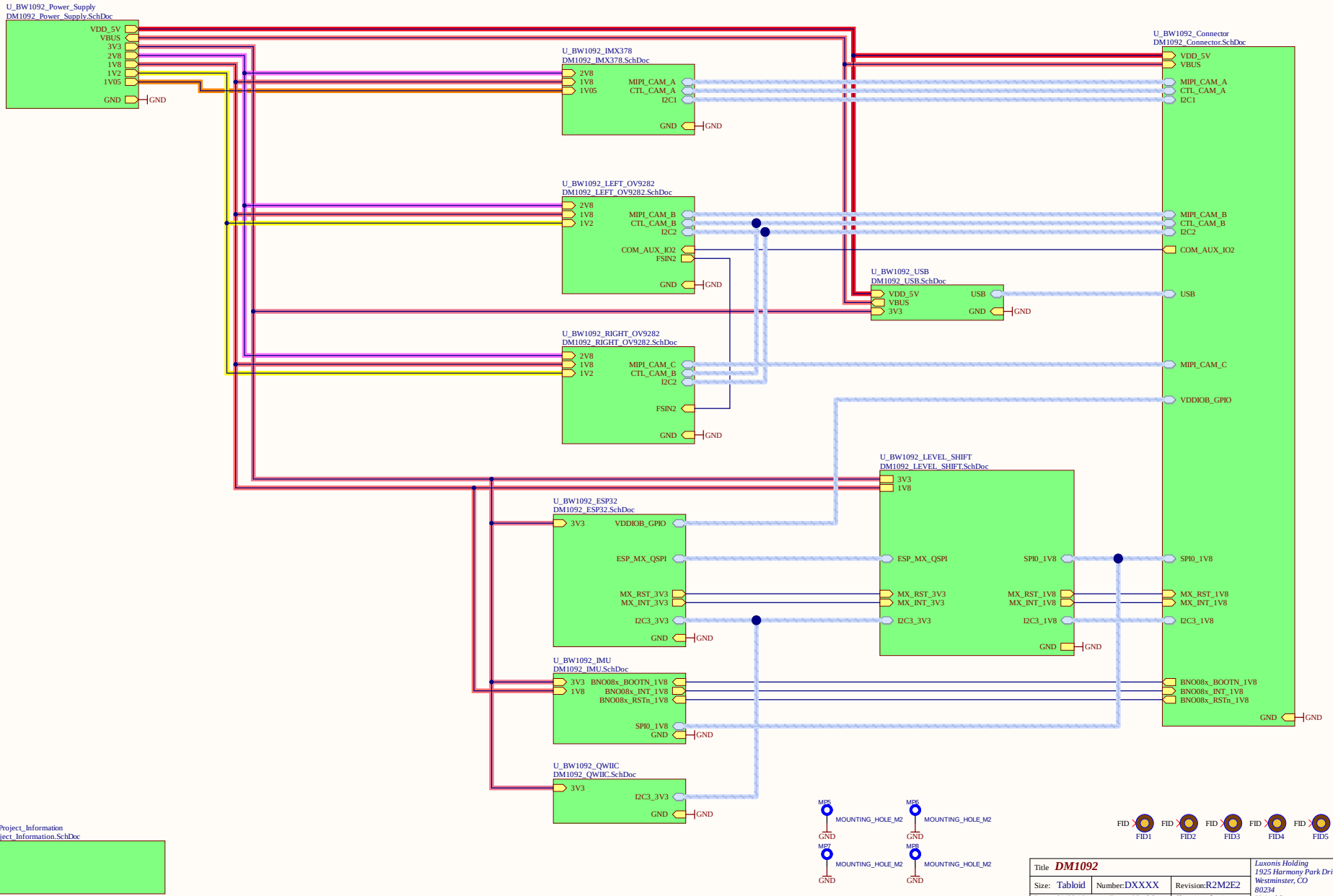
Date: 02/08/2021	Time: 08:43:31	Sheet 1 of 12	
Drawn by: *David Malovrh*			


U_BW1092_Power_Supply
DM1092_Power_Supply.SchDoc
VDD_5V
VBUS
3V3
2V8
1V8
1V2
1V05
GND
U_BW1092_IMX378
DM1092_IMX378.SchDoc
2V8
1V8
1V05
MIPI_CAM_A
CTL_CAM_A
I2C1
GND
U_BW1092_LEFT_OV9282
DM1092_LEFT_OV9282.SchDoc
2V8
1V8
1V2
MIPI_CAM_B
CTL_CAM_B
I2C2
COM_AUX_IO2
FSIN2
GND
U_BW1092_RIGHT_OV9282
DM1092_RIGHT_OV9282.SchDoc
2V8
1V8
1V2
MIPI_CAM_C
CTL_CAM_B
I2C2
FSIN2
GND
U_BW1092_USB
DM1092_USB.SchDoc
VDD_5V
VBUS
3V3
USB
GND
U_BW1092_LEVEL_SHIFT
DM1092_LEVEL_SHIFT.SchDoc
3V3
1V8
ESP_MX_QSPI
SPI0_1V8
MX_RST_3V3
MX_INT_3V3
I2C3_3V3
MX_RST_1V8
MX_INT_1V8
I2C3_1V8
GND
U_BW1092_ESP32
DM1092_ESP32.SchDoc
3V3
VDDIOB_GPIO
ESP_MX_QSPI
MX_RST_3V3
MX_INT_3V3
I2C3_3V3
GND
U_BW1092_IMU
DM1092_IMU.SchDoc
3V3
1V8
BNO08x_BOOTN_1V8
BNO08x_INT_1V8
BNO08x_RSTn_1V8
SPI0_1V8
GND
U_BW1092_QWIIC
DM1092_QWIIC.SchDoc
3V3
I2C3_3V3
GND
U_BW1092_Connector
DM1092_Connector.SchDoc
VDD_5V
VBUS
MIPI_CAM_A
CTL_CAM_A
I2C1
MIPI_CAM_B
CTL_CAM_B
I2C2
COM_AUX_IO2
USB
MIPI_CAM_C
VDDIOB_GPIO
SPI0_1V8
MX_RST_1V8
MX_INT_1V8
I2C3_1V8
BNO08x_BOOTN_1V8
BNO08x_INT_1V8
BNO08x_RSTn_1V8
GND
U_Project_Information
Project_Information.SchDoc
MP5
MP6
MP7
MP8
MOUNTING_HOLE_M2
GND
FID
FID1
FID2
FID3
FID4
FID5
FID6
Title DM1092
Size: Tabloid
Number:DXXXX
Revision:R2M2E2
Date: 02/08/2021
Time: 08:43:31
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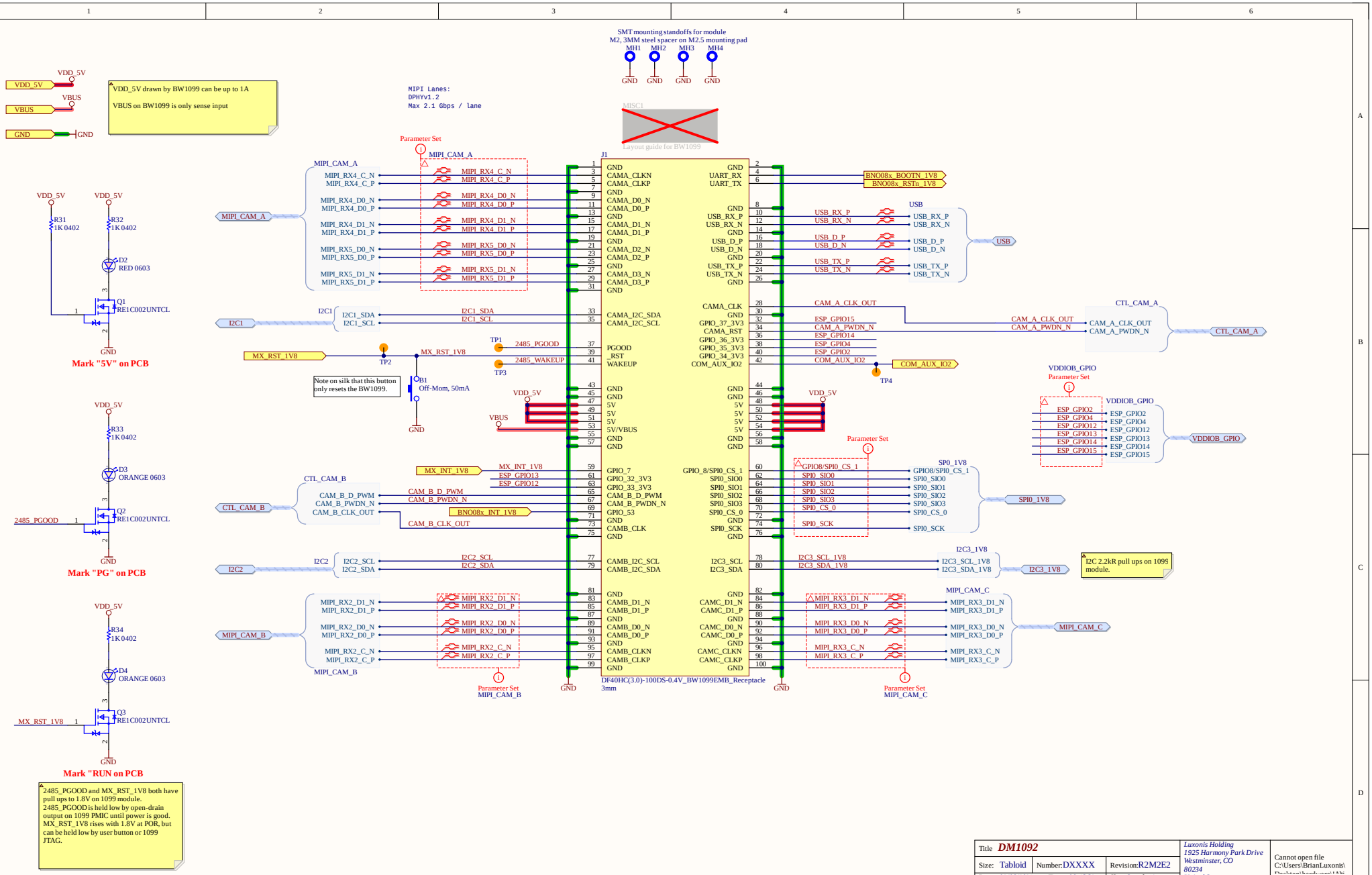
SMT mounting standoffs for module
M2, 3MM steel spacer on M2.5 mounting pad
MH1 MH2 MH3 MH4
GND GND GND GND
VDD_5V
VBUS
GND
VDD_5V drawn by BW1099 can be up to 1A
VBUS on BW1099 is only sense input
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane
MISC1
Layout guide for BW1099
Parameter Set
MIPI_CAM_A
J1
MIPI_RX4_C_N
MIPI_RX4_C_P
MIPI_RX4_D0_N
MIPI_RX4_D0_P
MIPI_RX4_D1_N
MIPI_RX4_D1_P
MIPI_RX5_D0_N
MIPI_RX5_D0_P
MIPI_RX5_D1_N
MIPI_RX5_D1_P
GND
CAMA_CLKN
CAMA_CLKP
CAMA_D0_N
CAMA_D0_P
CAMA_D1_N
CAMA_D1_P
CAMA_D2_N
CAMA_D2_P
CAMA_D3_N
CAMA_D3_P
UART_RX
UART_TX
BNO08x_BOOTN_1V8
BNO08x_RSTn_1V8
USB_RX_P
USB_RX_N
USB_D_P
USB_D_N
USB_TX_P
USB_TX_N
USB
CAMA_CLK
CAM_A_CLK_OUT
CAMA_I2C_SDA
CAMA_I2C_SCL
GPIO_37_3V3
ESP_GPIO15
CAM_A_PWDN_N
CAMA_RST
ESP_GPIO14
GPIO_36_3V3
ESP_GPIO4
GPIO_35_3V3
ESP_GPIO2
GPIO_34_3V3
COM_AUX_IO2
CTL_CAM_A
I2C1
I2C1_SDA
I2C1_SCL
MX_RST_1V8
TP1
TP2
TP3
TP4
2485_PGOOD
2485_WAKEUP
PGOOD
_RST
WAKEUP
B1
Off-Mom, 50mA
Note on silk that this button only resets the BW1099.
5V
5V/VBUS
VDDIOB_GPIO
ESP_GPIO2
ESP_GPIO4
ESP_GPIO12
ESP_GPIO13
ESP_GPIO14
ESP_GPIO15
GPIO_7
GPIO_32_3V3
GPIO_33_3V3
GPIO_53
GPIO_8/SPI0_CS_1
SPI0_SIO0
SPI0_SIO1
SPI0_SIO2
SPI0_SIO3
SPI0_CS_0
SPI0_SCK
SPI0_1V8
CTL_CAM_B
CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
BNO08x_INT_1V8
MX_INT_1V8
ESP_GPIO13
ESP_GPIO12
CAMB_I2C_SCL
CAMB_I2C_SDA
I2C2
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C3_SCL_1V8
I2C3_SDA_1V8
I2C3_1V8
I2C 2.2kR pull ups on 1099 module.
MIPI_CAM_B
CAMB_D1_N
CAMB_D1_P
CAMB_D0_N
CAMB_D0_P
CAMB_CLKN
CAMB_CLKP
MIPI_RX2_D1_N
MIPI_RX2_D1_P
MIPI_RX2_D0_N
MIPI_RX2_D0_P
MIPI_RX2_C_N
MIPI_RX2_C_P
MIPI_CAM_C
CAMC_D1_N
CAMC_D1_P
CAMC_D0_N
CAMC_D0_P
CAMC_CLKN
CAMC_CLKP
MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P
DF40HC(3.0)-100DS-0.4V_BW1099EMB_Receptacle
3mm
Parameter Set
MIPI_CAM_B
Parameter Set
MIPI_CAM_C
R31 1K 0402
R32 1K 0402
D2 RED 0603
Q1 RE1C002UNTCL
Mark "5V" on PCB
R33 1K 0402
D3 ORANGE 0603
Q2 RE1C002UNTCL
Mark "PG" on PCB
R34 1K 0402
D4 ORANGE 0603
Q3 RE1C002UNTCL
Mark "RUN on PCB
2485_PGOOD and MX_RST_1V8 both have pull ups to 1.8V on 1099 module.
2485_PGOOD is held low by open-drain output on 1099 PMIC until power is good.
MX_RST_1V8 rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.
Title DM1092
Size: Tabloid
Number:DXXXX
Revision:R2M2E2
Date: 02/08/2021
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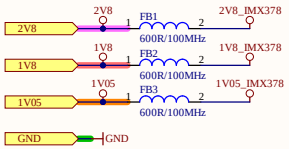
Place FBs and caps close to their associated camera connector.



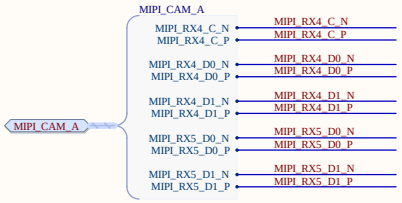
Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

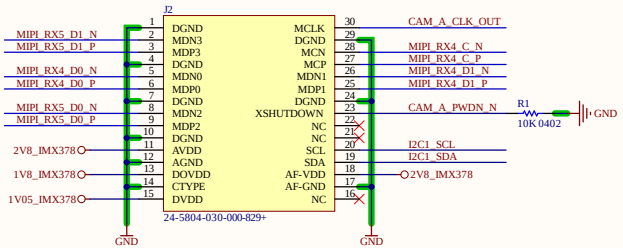
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

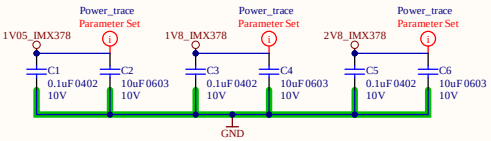
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

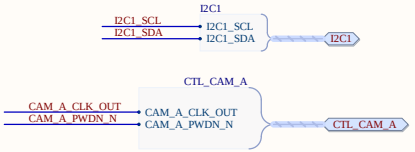


IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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Size: Tabloid	Number: DXXXX	Revision: R2M2E2	Cannot open file C:\Users\BrianLuxonis\
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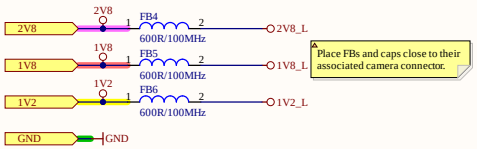
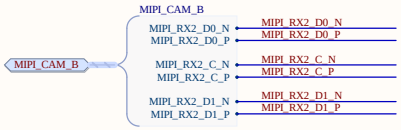


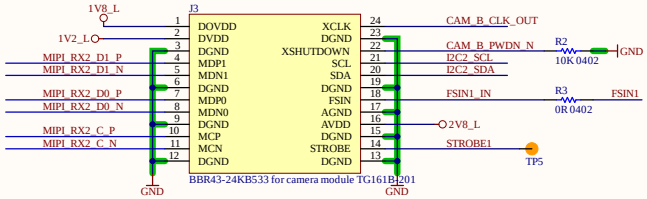
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

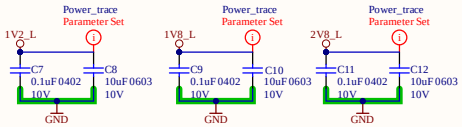
Supply Information

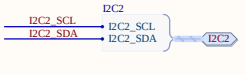
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

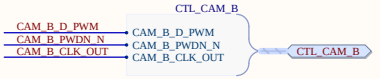


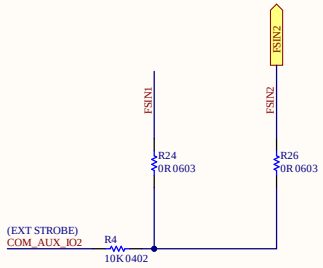
Mark "LEFT" on PCB
Place so that is the module's left camera.











Camera timing Sync Option

Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to th sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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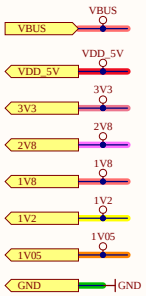
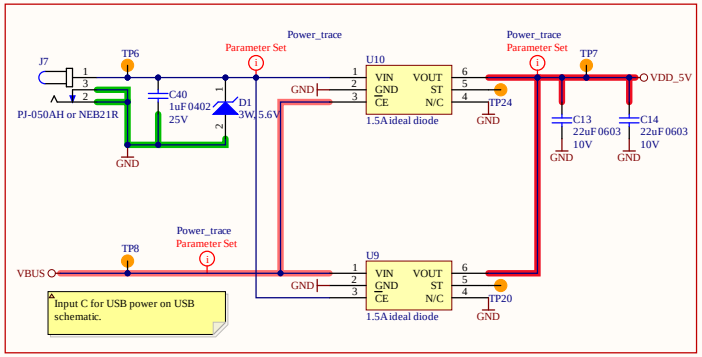
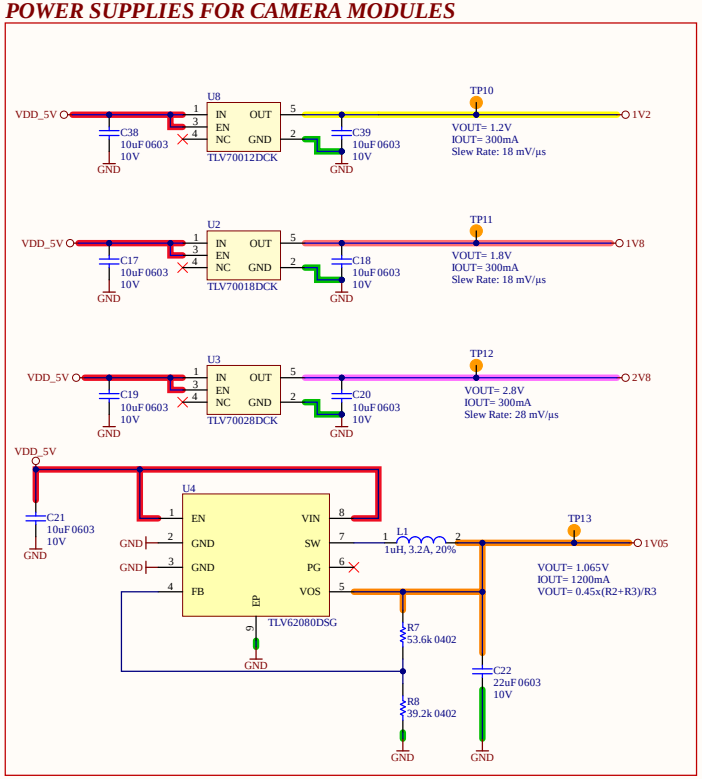
Drawn by: David Malovrh			



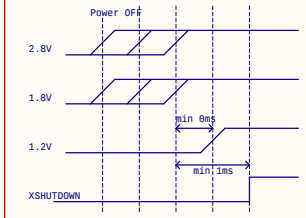
POWER INPUT



POWER SUPPLIES FOR CAMERA MODULES



OV9282 POWER REQUIREMENTS

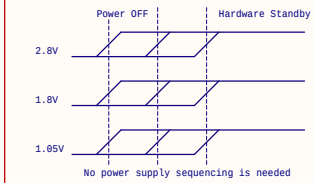


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

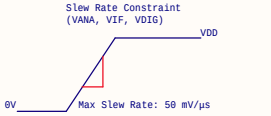
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

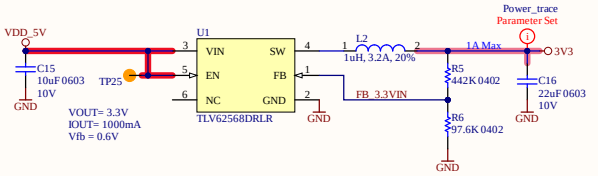


POWER SEQUENCING REQUIREMENTS:

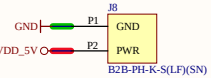
The BW1099 module handles it's own power sequencing on-board.

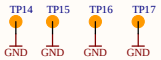
The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

3.3V USB SW POWER



FAN CONTROLLER





Title: DM1092			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
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Drawn by: David Malovrh			

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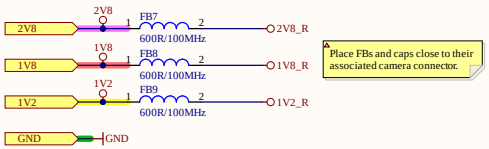

Place FBs and caps close to their associated camera connector.

MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
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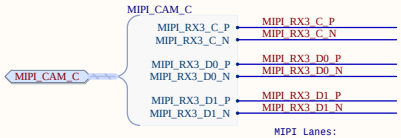
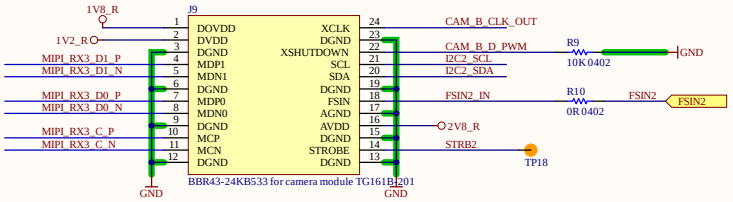
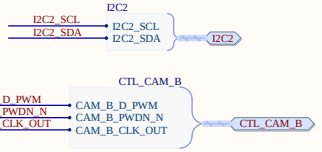
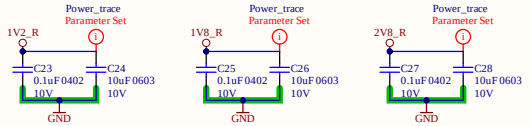


MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

Mark "RIGHT" on PCB
Place so that this is the module's right camera.







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CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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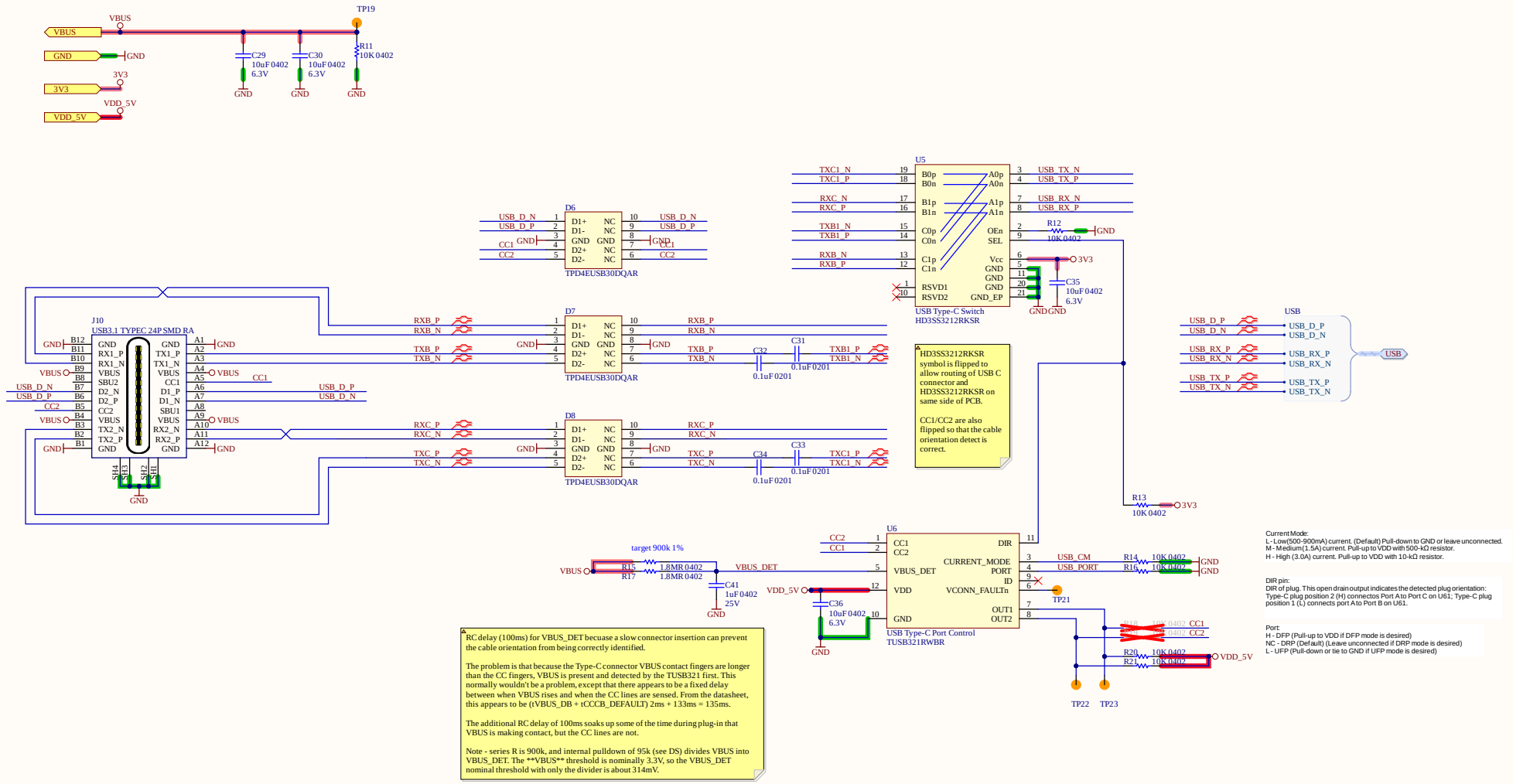
Drawn by: David Malovrh			



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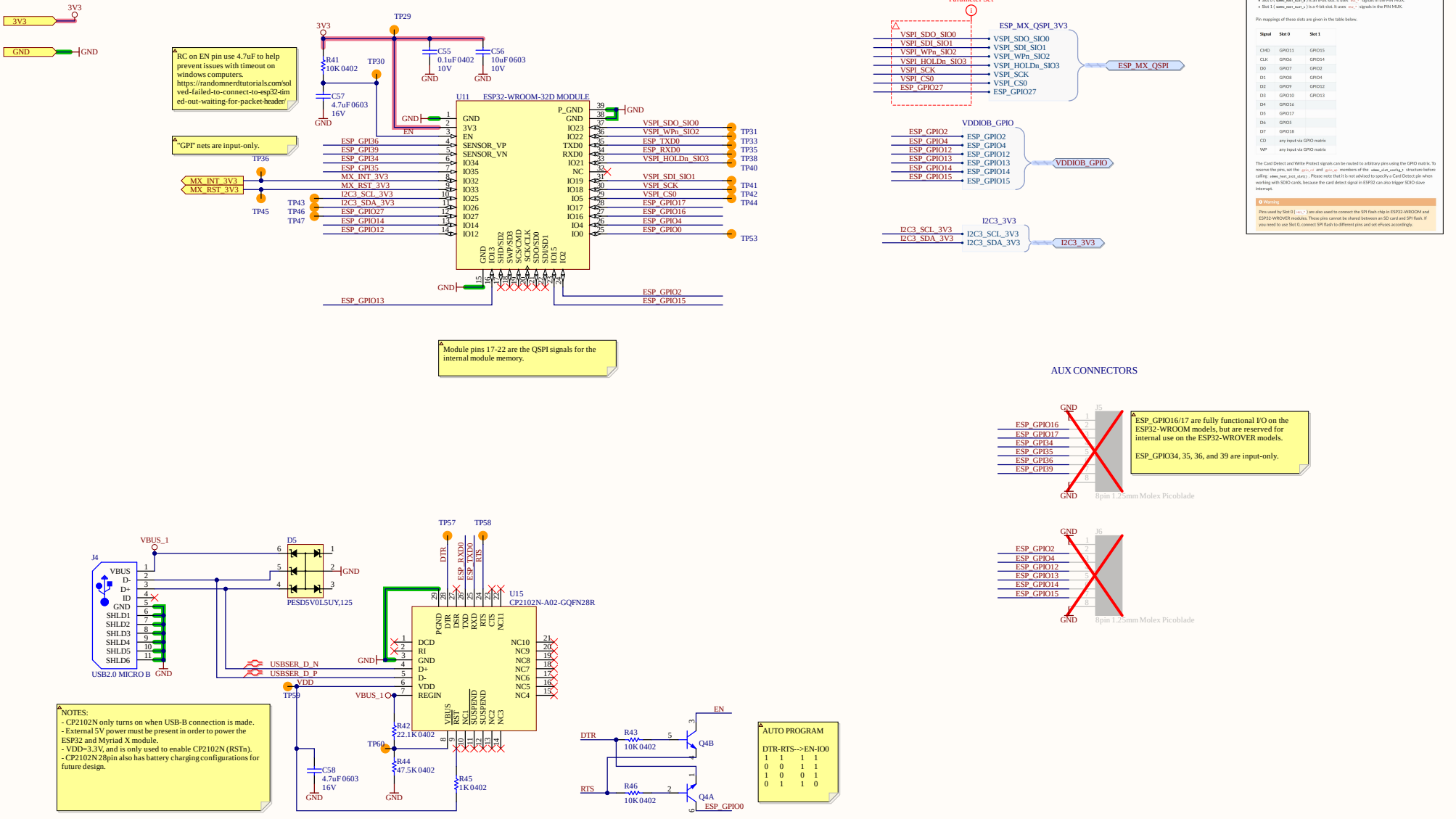

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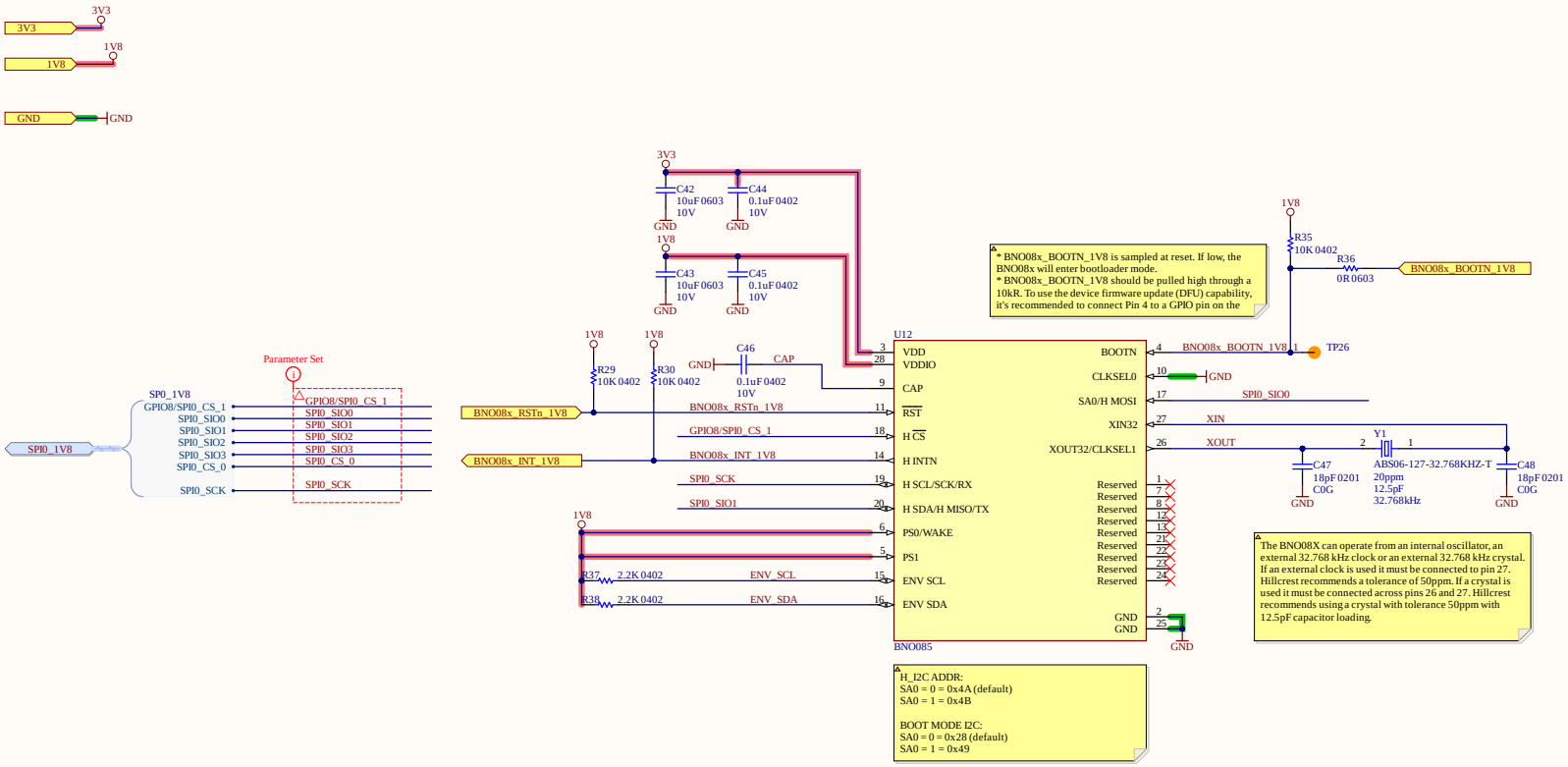

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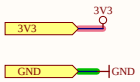

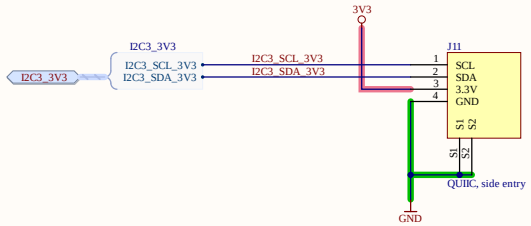

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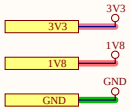
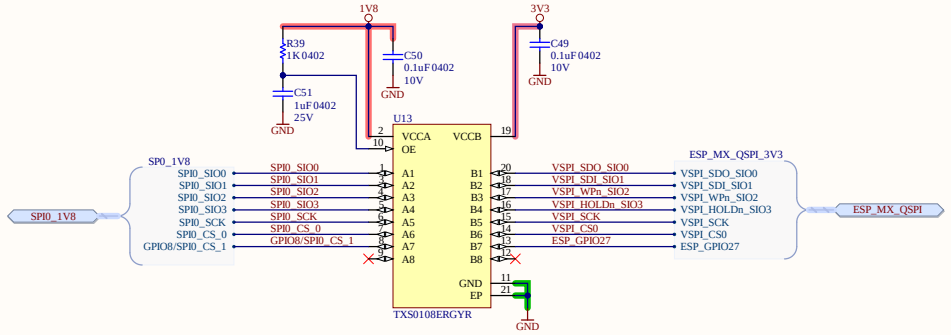
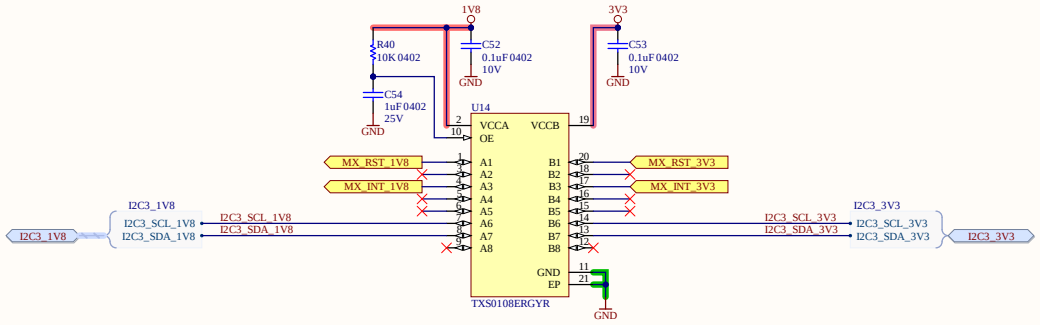
Date: 02/08/2021 Time: 08:43:32		Sheet 11 of 12		
Drawn by: ***David Malovrh***				





When driving high. TXS0108E ports have internal 4k pull ups to VCCA and VCCB, but when driving low, the pull up is 40k.

The TXS0101/2/4 translators have fixed 10-kΩ value pull-up resistors which provide dc-bias and dc current sourcing/drive capabilities to maintain a high signal. The TXS0108E translator reliably supports high-speed data rates in excess of 60Mbps, whereas the initial TXS series type translators supported slightly less than half this. The ability to translate down to the 1.2V operating-node is also supported in the TXS0108E device.



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