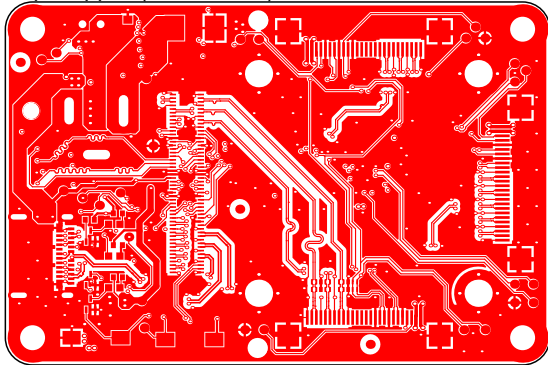
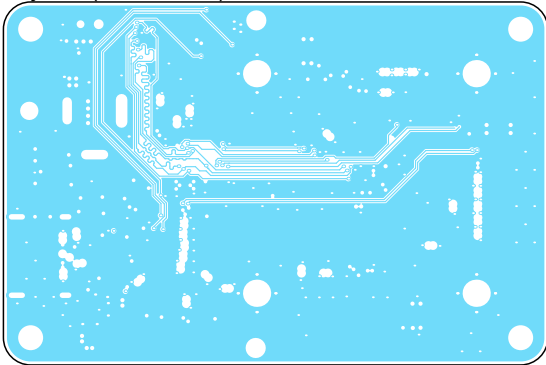


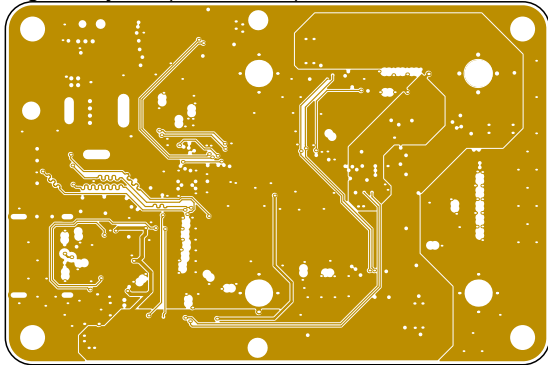
Top Copper (Scale 1.2:1)



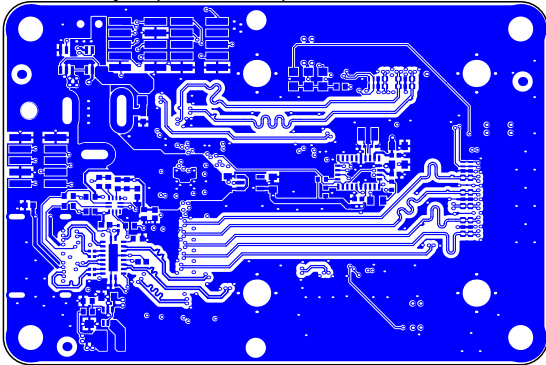
Layer 1 (Scale 1.2:1)



Signal Layer 1 (Scale 1.2:1)



Bottom Layer (Scale 1.2:1)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

- * PCB has 4 copper layers
- * Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- * PCB thickness: 63mil +/- 3mil
- * Min. trace width/clearance: 0.1mm/0.1mm
- * Min. hole drill/ring: 8mil/16mil
- * Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- * Silkscreen, non-conductive epoxy ink, color: black
- * Solder mask color: white
- * Remove silkscreen as needed to prevent ink on any exposed copper
- * Surface finish: ENIG
- * Hole dimensions are finished size, +/-3mil
- * Linear board dimension tolerance: +/-10mil
- * Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- * PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- * PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- * All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.
- * GM1 shall be used as PCB outline.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: DM1090	
Number: DXXXX	Revision: R3M0 E3
Date: 14/02/2022	Sheet: 1 of 3
Drawn by: David Malovrh	



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Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.71mil(0.018mm)	Solder Mask	GTS		4,2
Top Copper	1.40mil(0.036mm)	Signal	GTL		
	7.09mil(0.180mm)	Dielectric		0,02	4,2
Signal Layer 1	1.40mil(0.036mm)	Signal	G1		
	43.31mil(1.100mm)	Dielectric		0,02	4,2
Layer 1	1.40mil(0.036mm)	Signal	G2		
	7.09mil(0.180mm)	Dielectric		0,02	4,2
Bottom Layer	1.40mil(0.036mm)	Signal	GBL		
Bottom Solder	0.71mil(0.018mm)	Solder Mask	GBS		4,2
Bottom Overlay		Legend	GBO		
Total thickness: 64.50mil(1.638mm)					

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
☆	381	8.00mil(0.203mm)	Plated	
☆	63	10.00mil(0.254mm)	Plated	
◇	4	23.62mil(0.600mm)	Plated	
⊠	2	33.86mil(0.860mm)	Plated	
✕	3	41.34mil(1.050mm)	Plated	
⊞	1	70.87mil(1.800mm)	Non-Plated	
☆	2	78.74mil(2.000mm)	Non-Plated	
○	4	108.27mil(2.750mm)	Plated	
□	4	118.11mil(3.000mm)	Plated	
464 Total				

Title: **DM1090**

Number: DXXXX

Revision: R3M0
E3

Date: 14/02/2022

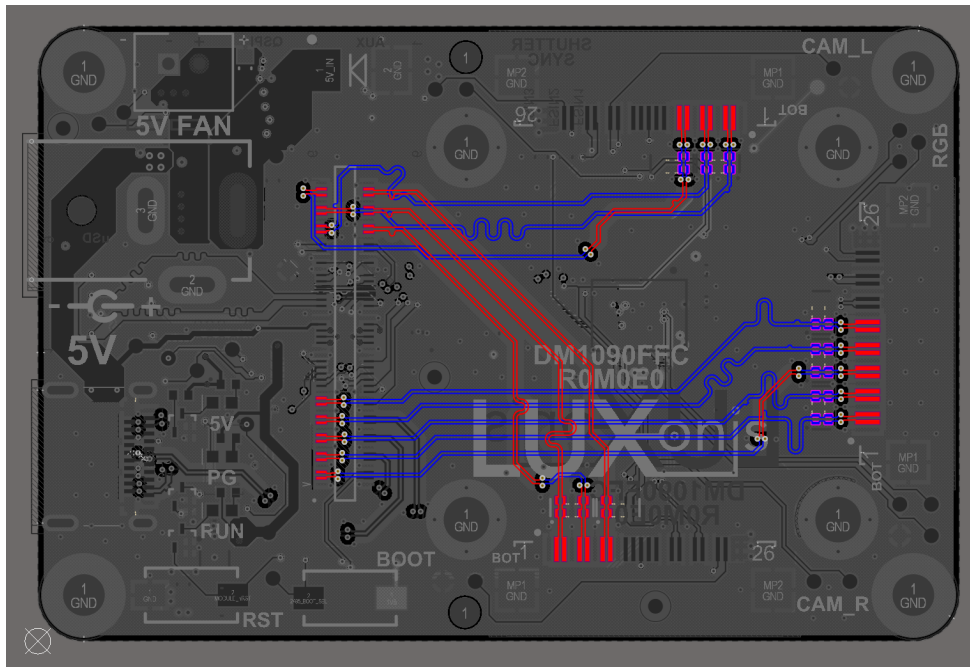
Sheet: 2 of 3

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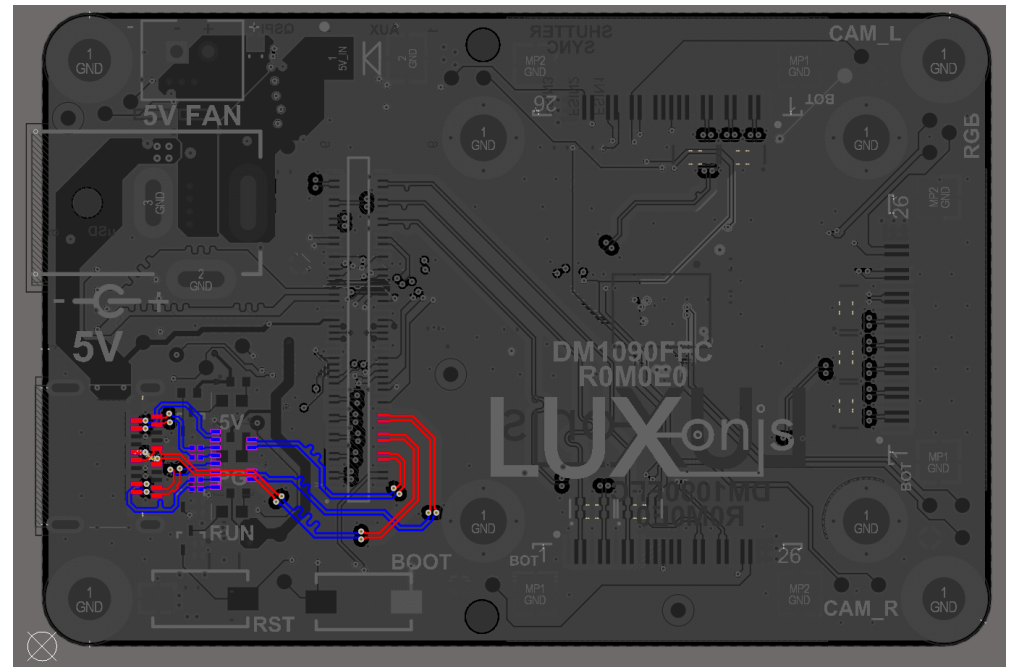
LUXonjs

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100 OHM (+/-10%) DIFF PAIRS



90 OHM (+/-10%) DIFF PAIRS

Transmission Line Structure Table

Impedance Id	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
1	100	101.48	Top Copper	5.0mil(0.127mm)	4.2mil(0.106mm)	4.0mil(0.102mm)	Signal Layer 1
2	90	91.35	Top Copper	7.0mil(0.178mm)	6.2mil(0.157mm)	4.0mil(0.102mm)	Signal Layer 1
3	100	101.48	Bottom Layer	5.0mil(0.127mm)	4.2mil(0.106mm)	4.0mil(0.102mm)	Layer 1
4	90	91.35	Bottom Layer	7.0mil(0.178mm)	6.2mil(0.157mm)	4.0mil(0.102mm)	Layer 1

Title: DM1090		
Number: DXXXX	Revision: R3M0 E3	
Date: 14/02/2022	Sheet: 3 of 3	PROPRIETARY AND CONFIDENTIAL
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