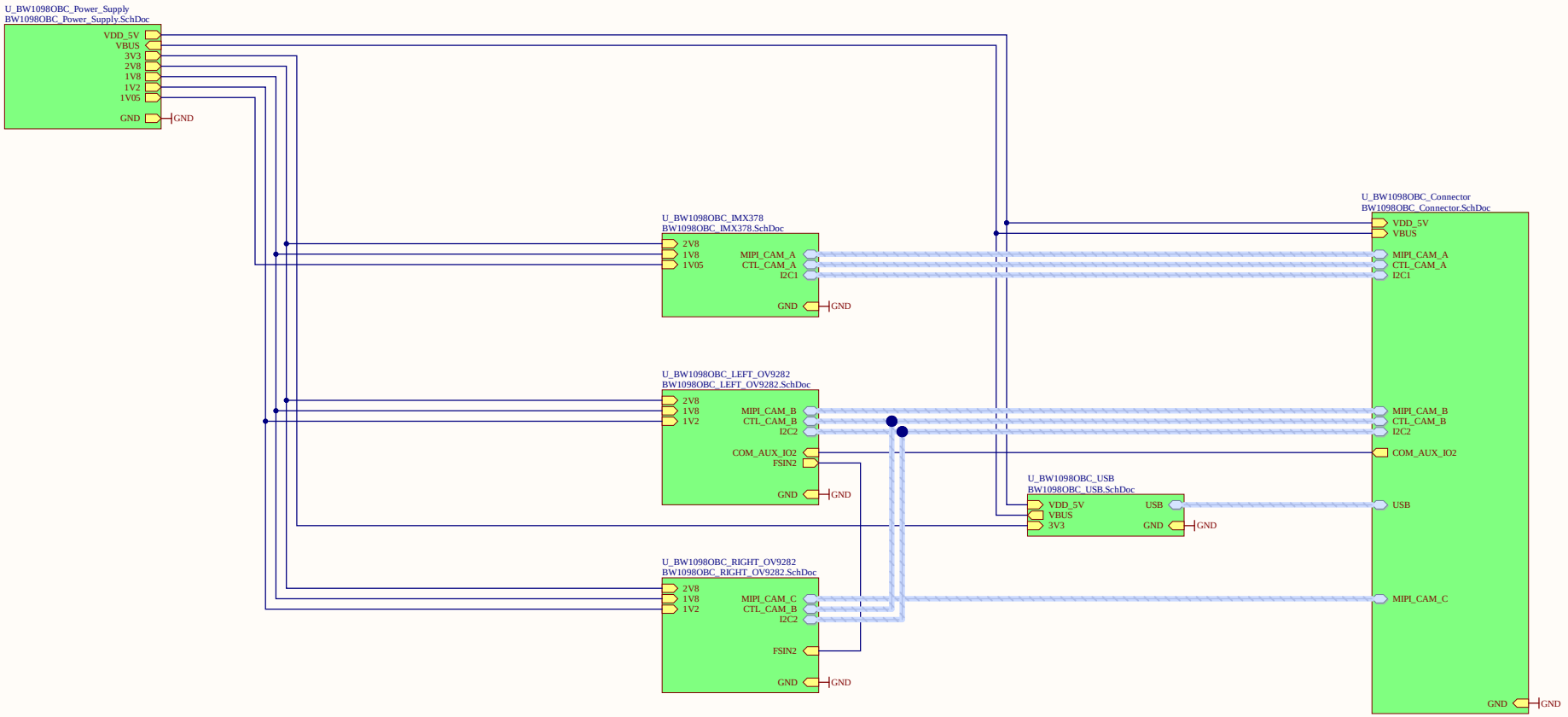
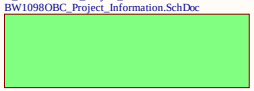
Project: ***BW1098OBC***
Current Revision: ***R2M0E2***

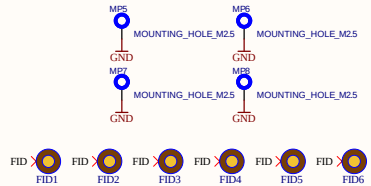
BW1098OBC Revision History:

Date	Revision	Reason for Change	Changes Implemented
10/21/2019	Initial release		
11/27/2019	R0M0E0 -> R1M0E1	1) Decoupling capacitors too close to OV9282 camera module body 2) Overlay on OV9282 camera module body too wide and should match outline of module body 3) Left/Right camera convention doens't match verbiage in schematic	1) Moved C7, C8, C9 and C12 a bit farther from the J3 (Left) camera module. Moved C23 and C25 a bit farther away from J9 (Right) camera module. 2) Updated the overlay for right and left OV9282 camera modules so that it outlined the 3D Body layer. This should match the camera module body outline and make it easier to mount and aligne the modules. 3)
04/21/2021	R1M0E1 --> R2M0E2	1) Slow plug issue with USB type-C 2) update reset and sync circuitry	1) Added 1uF capacitor to VBUS_DET updated PCB and fabrication files 2) Removed reset and updated sync circuitry

Title: ***BW1098OBC***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number: DXXXX	Revision: R2M0E2		
Date: 21/04/2021 Time: 12:26:47		Sheet 1 of 8		
Drawn by: ***Brian Weinstein***				







Title **BW1098OBC**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number:DXXXX	Revision:	
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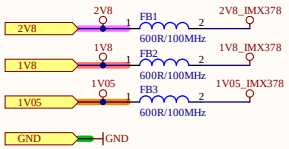
Place FBs and caps close to their associated camera connector.



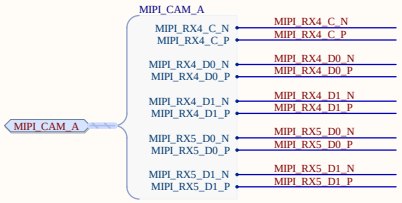
Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

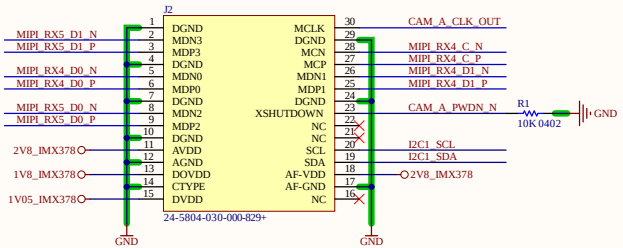
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

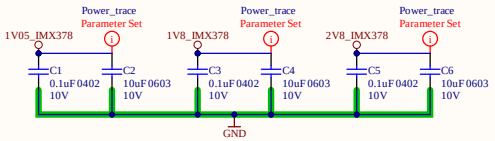
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

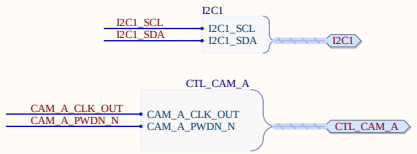


IMX378 MODULE CONNECTOR

MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz







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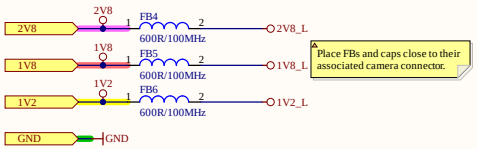
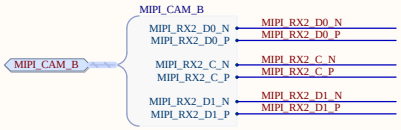


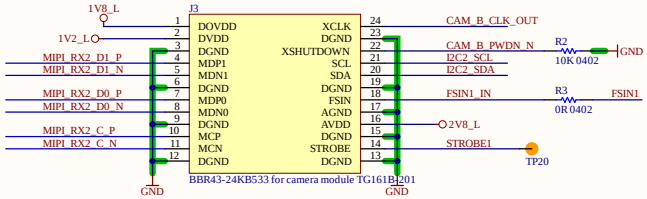
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

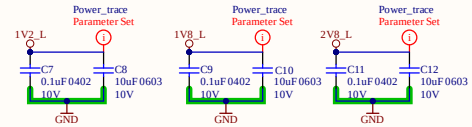
Supply Information

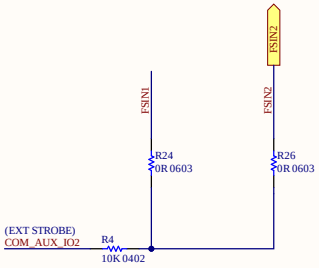
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

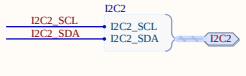


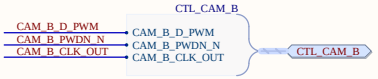
Mark "LEFT" on PCB
Place so that is the module's left camera.











Because the stereo pair of OV9282 modules hard wired to CAM_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to t sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title: BW1098OBC			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: DXXXX	Revision: R2M0E2	Cannot open file C:\Users\BrianLuxonis\
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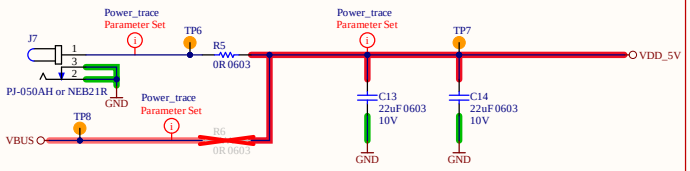
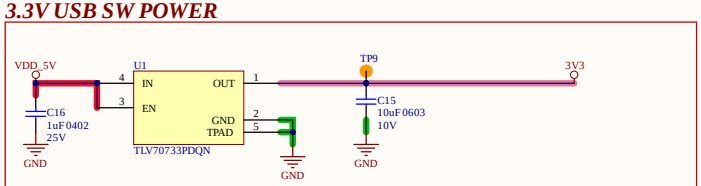
VBUS
VDD_5V
3V3
2V8
1V8
1V2
1V05
GND

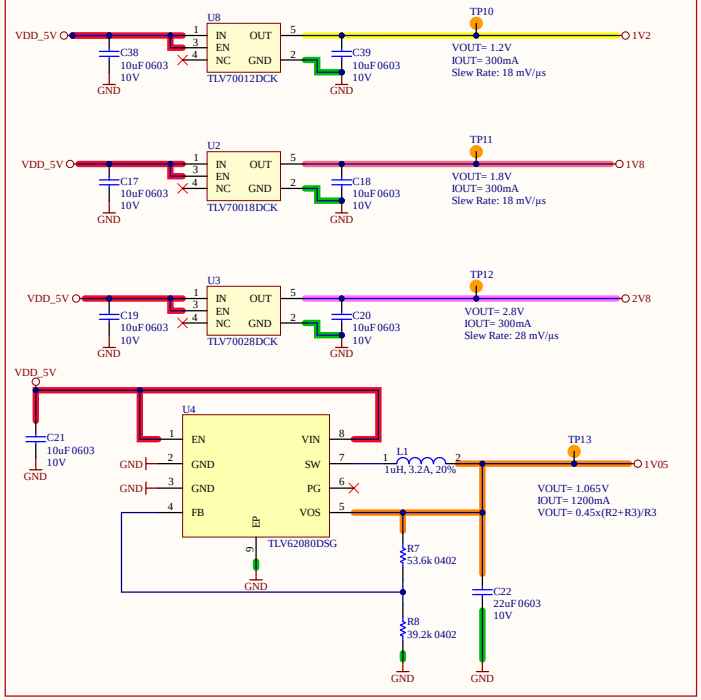
POWER INPUT



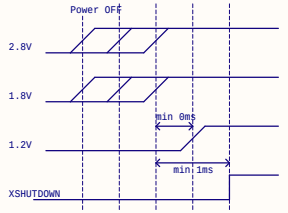
3.3V USB SW POWER



POWER SUPPLIES FOR CAMERA MODULES



OV9282 POWER REQUIREMENTS

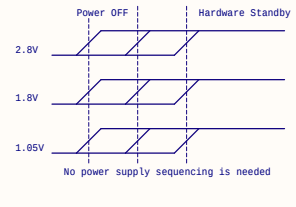


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

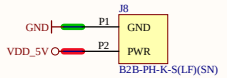
Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA

POWER SEQUENCING REQUIREMENTS:

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

FAN CONTROLLER



TP14 TP15 TP16 TP17
GND GND GND GND

Title: BW1098OBC			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
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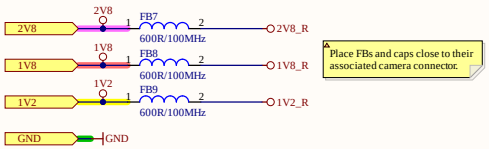
Drawn by: Brian Weinstein			



MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information

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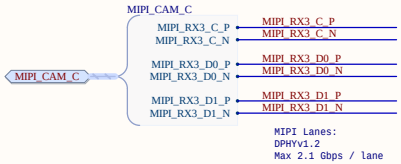
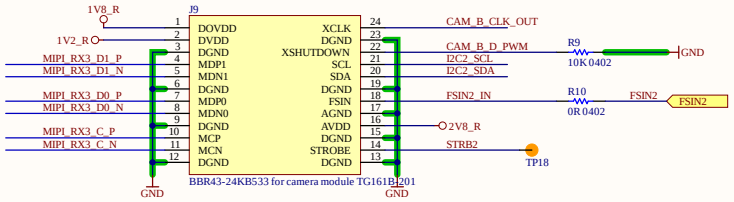
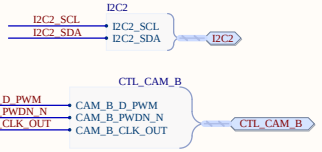
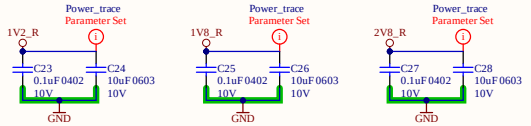


Mark "RIGHT" on PCB
Place so that this is the module's right camera.







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	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title: BW1098OBC			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
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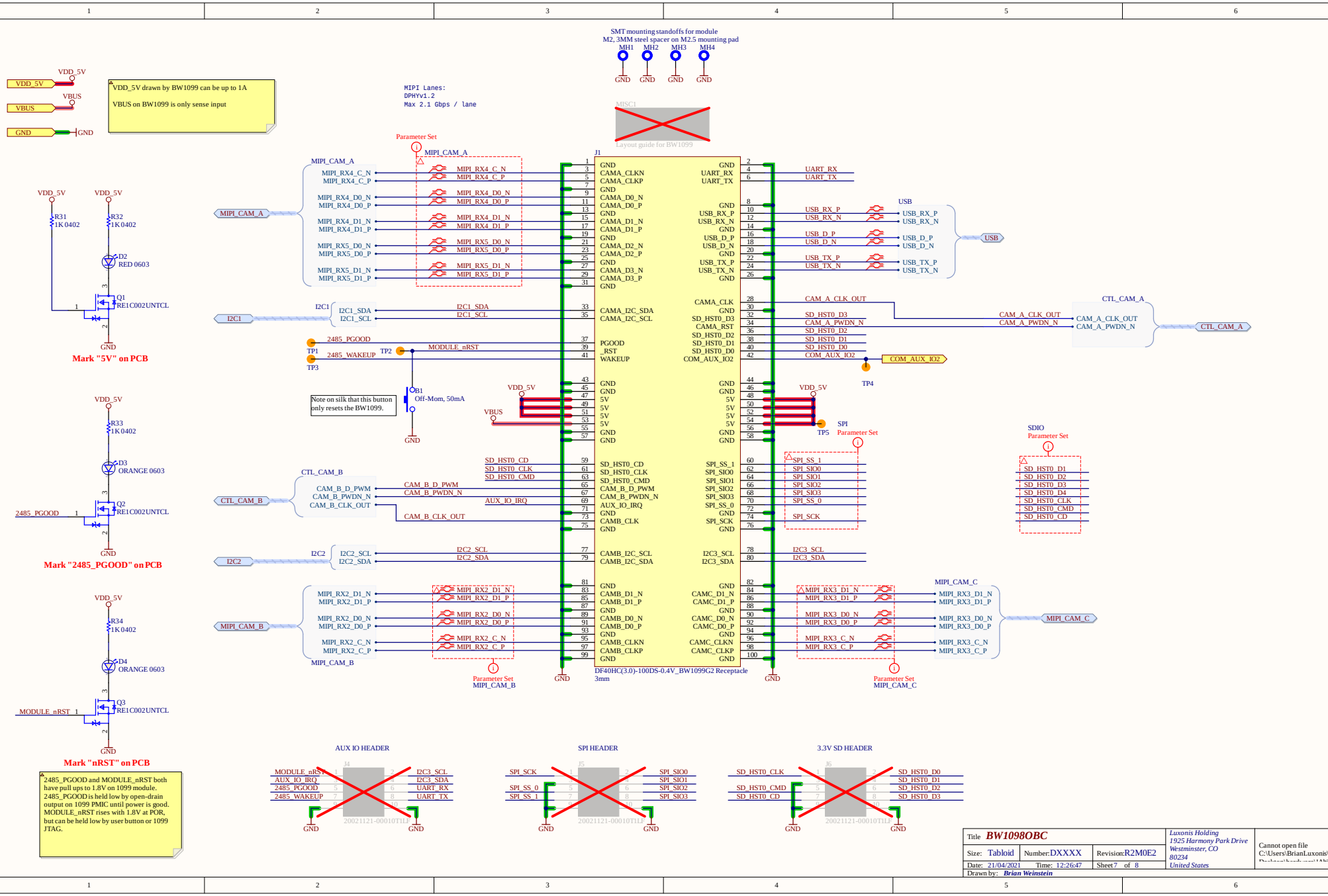
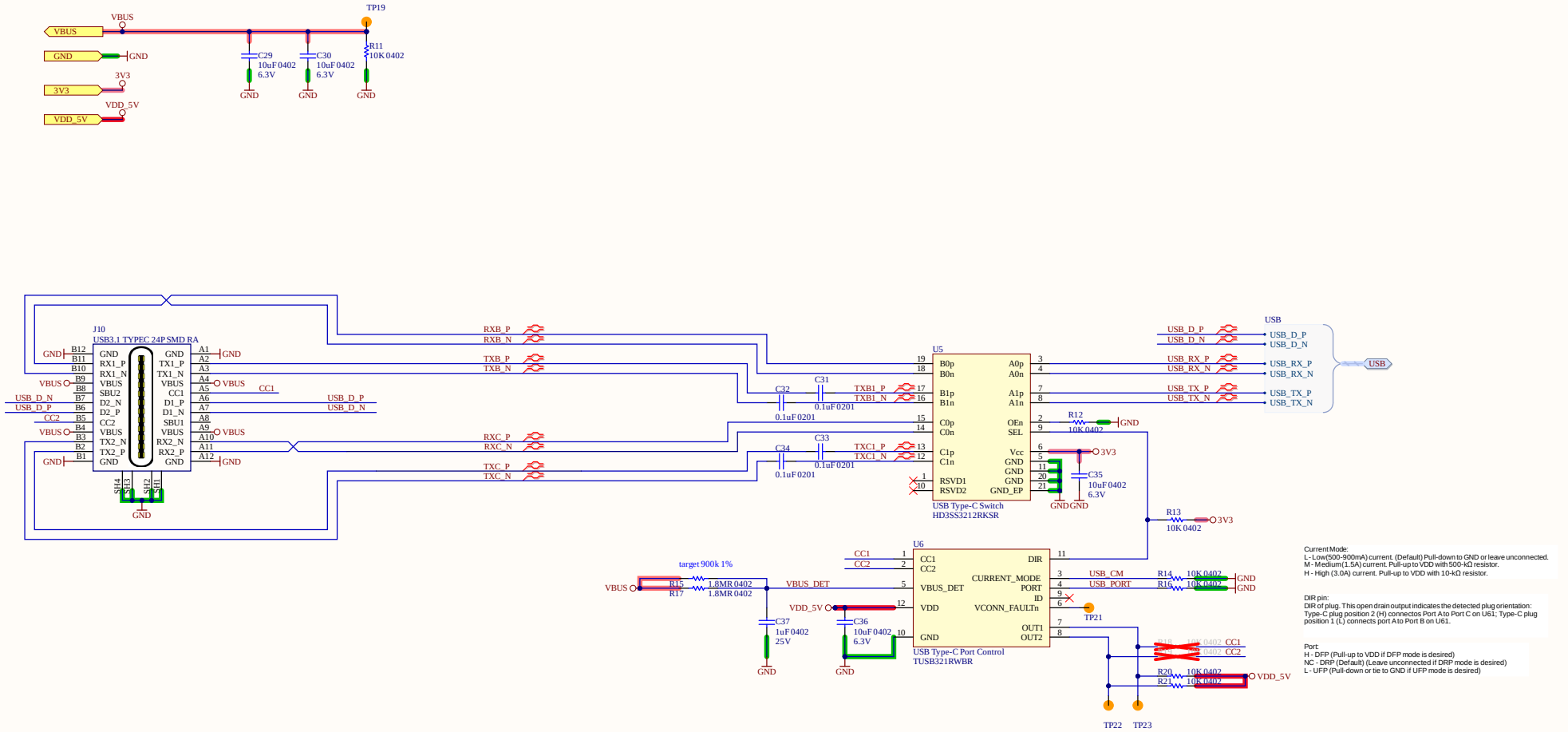

SMT mounting standoffs for module
M2, 3MM steel spacer on M2.5 mounting pad
MH1 MH2 MH3 MH4
GND GND GND GND
VDD_5V
VBUS
GND
VDD_5V drawn by BW1099 can be up to 1A
VBUS on BW1099 is only sense input
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane
MISC1
Layout guide for BW1099
Parameter Set
MIPI_CAM_A
J1
MIPI_RX4_C_N
MIPI_RX4_C_P
MIPI_RX4_D0_N
MIPI_RX4_D0_P
MIPI_RX4_D1_N
MIPI_RX4_D1_P
MIPI_RX5_D0_N
MIPI_RX5_D0_P
MIPI_RX5_D1_N
MIPI_RX5_D1_P
GND
CAMA_CLKN
CAMA_CLKP
CAMA_D0_N
CAMA_D0_P
CAMA_D1_N
CAMA_D1_P
CAMA_D2_N
CAMA_D2_P
CAMA_D3_N
CAMA_D3_P
UART_RX
UART_TX
USB_RX_P
USB_RX_N
USB_D_P
USB_D_N
USB_TX_P
USB_TX_N
USB
I2C1
I2C1_SDA
I2C1_SCL
CAMA_I2C_SDA
CAMA_I2C_SCL
CAMA_CLK
CAM_A_CLK_OUT
SD_HST0_D3
CAM_A_PWDN_N
CAMA_RST
SD_HST0_D2
SD_HST0_D1
SD_HST0_D0
COM_AUX_IO2
CTL_CAM_A
CAM_A_CLK_OUT
CAM_A_PWDN_N
2485_PGOOD
2485_WAKEUP
MODULE_nRST
PGOOD
_RST
WAKEUP
TP1
TP2
TP3
TP4
TP5
B1
Off-Mom, 50mA
Note on silk that this button only resets the BW1099.
VDD_5V
VBUS
SPI
Parameter Set
SPI_SS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3
SPI_SS_0
SPI_SCK
SDIO
Parameter Set
SD_HST0_D1
SD_HST0_D2
SD_HST0_D3
SD_HST0_D4
SD_HST0_CLK
SD_HST0_CMD
SD_HST0_CD
CTL_CAM_B
CAM_B_D_PWM
CAM_B_PWDN_N
CAM_B_CLK_OUT
AUX_IO_IRQ
CAMB_CLK
I2C2
I2C2_SCL
I2C2_SDA
CAMB_I2C_SCL
CAMB_I2C_SDA
I2C3_SCL
I2C3_SDA
MIPI_RX2_D1_N
MIPI_RX2_D1_P
MIPI_RX2_D0_N
MIPI_RX2_D0_P
MIPI_RX2_C_N
MIPI_RX2_C_P
MIPI_CAM_B
CAMB_D1_N
CAMB_D1_P
CAMB_D0_N
CAMB_D0_P
CAMB_CLKN
CAMB_CLKP
Parameter Set
MIPI_CAM_B
MIPI_CAM_C
MIPI_RX3_D1_N
MIPI_RX3_D1_P
MIPI_RX3_D0_N
MIPI_RX3_D0_P
MIPI_RX3_C_N
MIPI_RX3_C_P
CAMC_D1_N
CAMC_D1_P
CAMC_D0_N
CAMC_D0_P
CAMC_CLKN
CAMC_CLKP
DF40HC(3.0)-100DS-0.4V_BW1099G2 Receptacle
3mm
R31 1K 0402
R32 1K 0402
D2 RED 0603
Q1 RE1C002UNTCL
Mark "5V" on PCB
R33 1K 0402
D3 ORANGE 0603
Q2 RE1C002UNTCL
Mark "2485_PGOOD" on PCB
R34 1K 0402
D4 ORANGE 0603
Q3 RE1C002UNTCL
Mark "nRST" on PCB
2485_PGOOD and MODULE_nRST both have pull ups to 1.8V on 1099 module. 2485_PGOOD is held low by open-drain output on 1099 PMIC until power is good. MODULE_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.
AUX IO HEADER
J4
MODULE_nRST
AUX_IO_IRQ
2485_PGOOD
2485_WAKEUP
I2C3_SCL
I2C3_SDA
UART_RX
UART_TX
20021121-00010T1LF
SPI HEADER
J5
SPI_SCK
SPI_SS_0
SPI_SS_1
SPI_SIO0
SPI_SIO1
SPI_SIO2
SPI_SIO3
3.3V SD HEADER
J6
SD_HST0_CLK
SD_HST0_CMD
SD_HST0_CD
SD_HST0_D0
SD_HST0_D1
SD_HST0_D2
SD_HST0_D3
Title BW1098OBC
Size: Tabloid
Number:DXXXX
Revision:R2M0E2
Date: 21/04/2021
Time: 12:26:47
Sheet 7 of 8
Drawn by: Brian Weinstein
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
Cannot open file
C:\Users\BrianLuxonis\



Title: **BW1098OBC**			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: DXXXX	Revision: R2M0E2	Cannot open file C:\Users\BrianLuxonis\
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