LM016L·LM016XMBL

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (See page 79).
- +5V single power supply
- Display color: LM016L : Gray
  LM016XMBL : New-gray

MECHANICAL DATA (Nominal dimensions)

Module size . . . . 84W x 44H x 10.5T (max.) mm
Effective display area . . . . 61W x 15.8H mm
Character size (5 x 7 dots) . . . . 2.96W x 4.86H mm
Character pitch . . . . 3.55 mm
Dot size . . . . 0.56W x 0.66H mm
Weight . . . . about 35 g

ABSOLUTE MAXIMUM RATINGS   min.   max.

Power supply for logic ($V_{DD} - V_{SS}$) 0   6.5 V
Power supply for LCD drive
($V_{DD} - V_O$) 0   6.5 V
Input voltage (V_i) . . . . V_{SS} V_{DD} V
Operating temeprature (Ta) 0   50 40*°C
Storage temperature (Tstg) . . . . −20 70 60*°C
* Shows the value of type LM016XMBL.

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (V_{IH}) . . . . 2.2 V min.
Input "low" voltage (V_{IL}) . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
                                                        3.0 mA max.

POWER SUPPLY FOR LCD DRIVE (Recommended)   ($V_{DD}-V_O$)

                                                    Duty = 1/16
Range of $V_{DD} - V_O$ . . . . 1.5~5.25 V
        Ta = 0°C . . . . 4.6 V typ.
        Ta = 25°C . . . . 4.4 V typ.
        Ta = 50°C . . . . 4.2 V typ.

OPTICAL DATA . . . . See page 7

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	
2	V_{DD}	–	+5V	Power supply
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L		
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L	Data bus line Note (1), (2)	
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$, and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

Unit : mm

Fig. 1 Display pattern
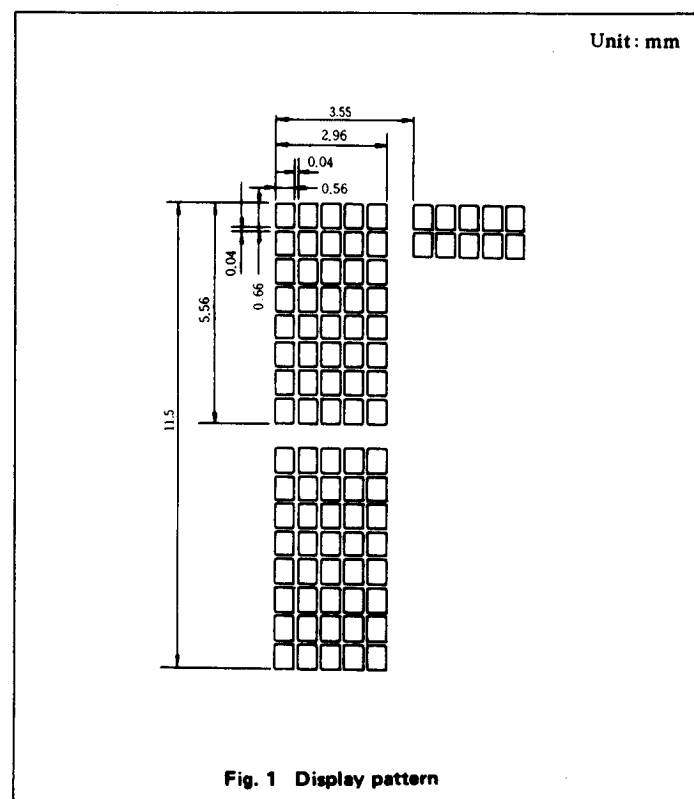
4.2 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

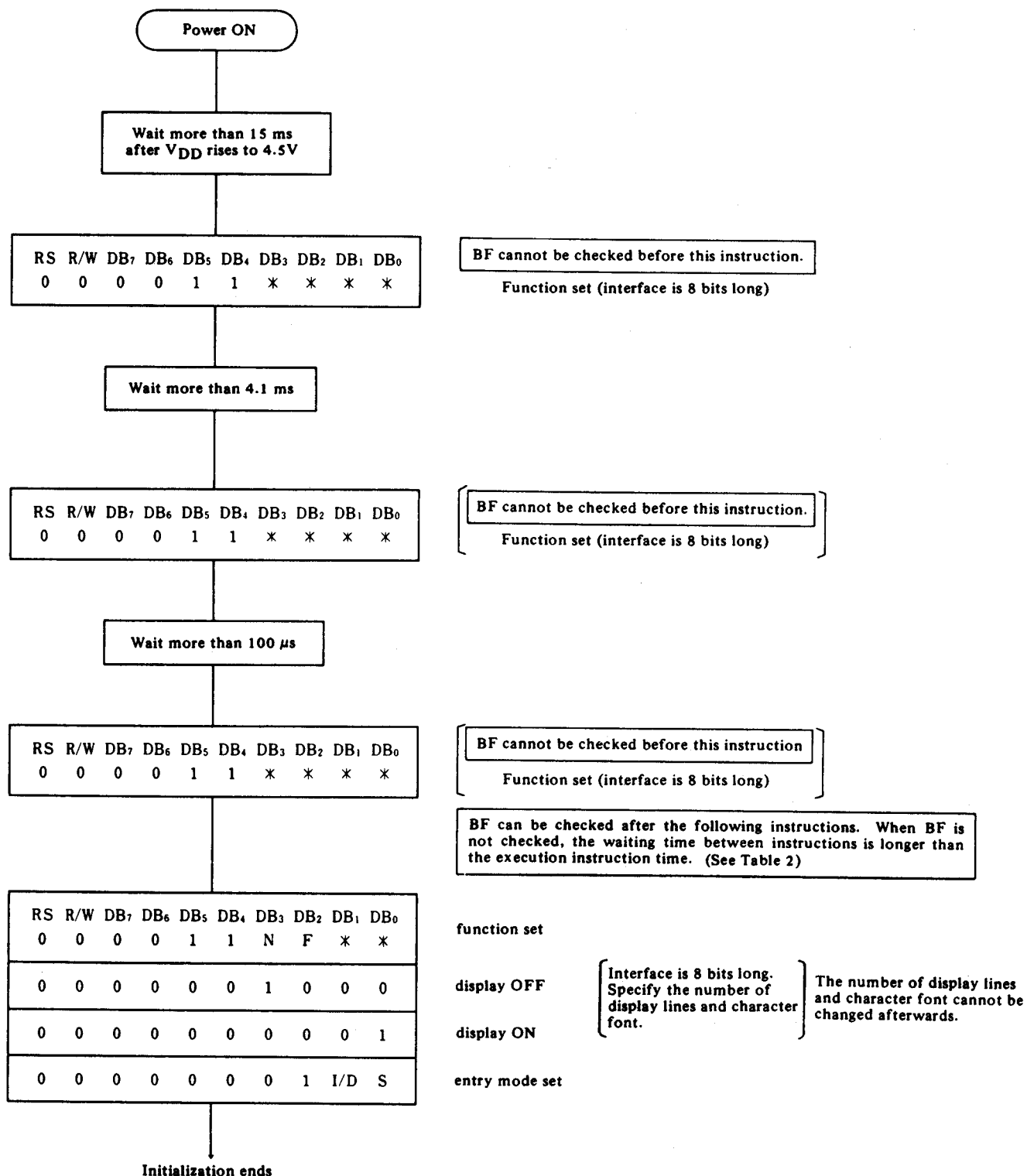(1) When interface is 8 bits long;

```
                    ┌─────────────────┐
                    │    Power ON     │
                    └────────┬────────┘
                             │
                 ┌───────────┴───────────┐
                 │  Wait more than 15 ms │
                 │  after VDD rises to 4.5V │
                 └───────────┬───────────┘
                             │
```

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (interface is 8 bits long)

```
                 ┌───────────────────────┐
                 │  Wait more than 4.1 ms │
                 └───────────┬───────────┘
```

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (interface is 8 bits long)

```
                 ┌───────────────────────┐
                 │  Wait more than 100 µs │
                 └───────────┬───────────┘
```

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction

Function set (interface is 8 bits long)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See Table 2)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	*	*
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	I/D	S

function set

display OFF

display ON

entry mode set

Interface is 8 bits long. Specify the number of display lines and character font.

The number of display lines and character font cannot be changed afterwards.

Initialization ends

Table 2 Instructions

Instruction	Code										Description	Execution time (when fosc is 250 kHz) Note 1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 μs ~ 1.64 ms	120 μs ~ 4.9 ms
Return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6 ms	120 μs ~ 4.8 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address.	0	0	0	1	A_CG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A_DD							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs
Read busy flag & address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs	1 μs
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	120 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs

I/D = 1: Increment (+1) I/D = 0: Decrement (−1) S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction	DD RAM: Display data RAM CG RAM: Character generator RAM A_CG: CG RAM address A_DD: DD RAM address Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 kHz: $40 \, \mu s \times \dfrac{250}{270} = 37 \, \mu s$

*No effect
Notes 1. Applied to models driven by 1/8 duty or 1/11 duty.
      2. Applied to models driven by 1/16 duty.

5.2 Description of details

(1) Clear display

	RS	R/W	DB$_7$							DB$_0$
Code	0	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return home

	RS	R/W	DB$_7$							DB$_0$
Code	0	0	0	0	0	0	0	0	0	*

* No effect

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

	RS	R/W	DB$_7$							DB$_0$
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S = 0.

(4) Display ON/OFF control

	RS	R/W	DB$_7$							DB$_0$
Code	0	0	0	0	0	0	1	D	C	B

D: The display is ON when D = 1 and OFF when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when f_{CP} or f_{osc} = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{CP} or f_{osc}. $409.6 \times \dfrac{250}{270} = 379.2$ ms when f_{CP} = 270 kHz.)

5 x 7 dot character font

Cursor

5 x 10 dot character font

Alternating display
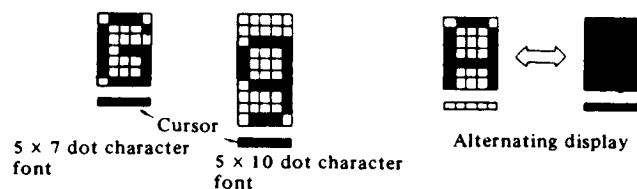
(a) Cursor Display Example   (b) Blink Display Example

(5) Cursor or display shift

	RS	R/W	DB$_7$							DB$_0$
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function set

	RS	R/W	DB7						DB0
Code	0	0	0	0	1	DL	N	F	*

              * No effect

DL: Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL = 1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL = 0.
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	No. of display lines	Character font	Duty factor	Remarks
0	0	1	5 x 7 dots	1/8	
0	1	1	5 x 10 dots	1/11	
1	*	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font.

* No effect

(7) Set CG RAM address

	RS	R/W	DB7						DB0
Code	0	0	0	1	A	A	A	A	A	A

       ← Higher Order Bits   Lower Order Bits →

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

	RS	R/W	DB7						DB0
Code	0	0	1	A	A	A	A	A	A	A

       ← Higher Order Bits   lower Order Bits →

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N = 0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal),
when N = 1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag & address

	RS	R/W	DB7						DB0
Code	0	1	BF	A	A	A	A	A	A	A

       ← Higher Order Bits   Lower Order Bits →

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.
At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write data to CG or DD RAM

	RS	R/W	DB7						DB0
Code	1	0	D	D	D	D	D	D	D	D

       ← Higher Order Bits   Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

	RS	R/W	DB₇							DB₀
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits → Lower Order Bits →
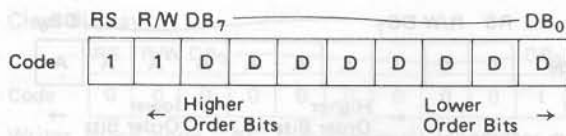
Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

5.3 Instruction and display correspondence

(1) 8-bit operation, 8-digit × 1-line display (using internal reset)

Following table shows an example of 8-bit × 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	—	—	μs
Enable pulse width	PW_{EH}	Fig. 5, Fig. 6	450	—	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	—	—	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	—	—	ns
Data delay time	t_{DDR}	Fig. 6	—	—	320	ns
Data set up time	t_{DSW}	Fig. 5	195	—	—	ns
Hold time	t_H	Fig. 5, Fig. 6	20	—	—	ns
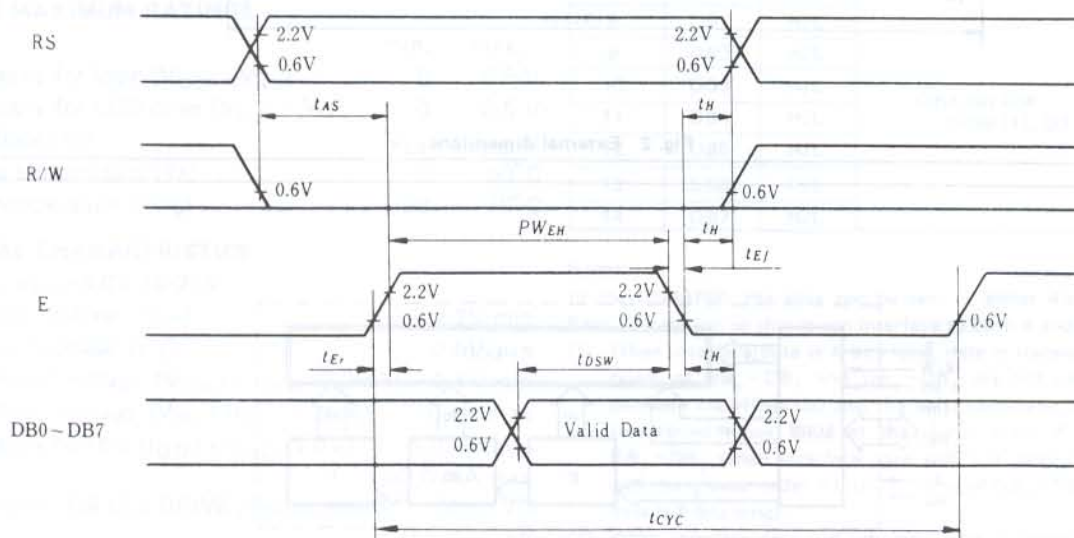
Fig. 5   Interface timing (data write)
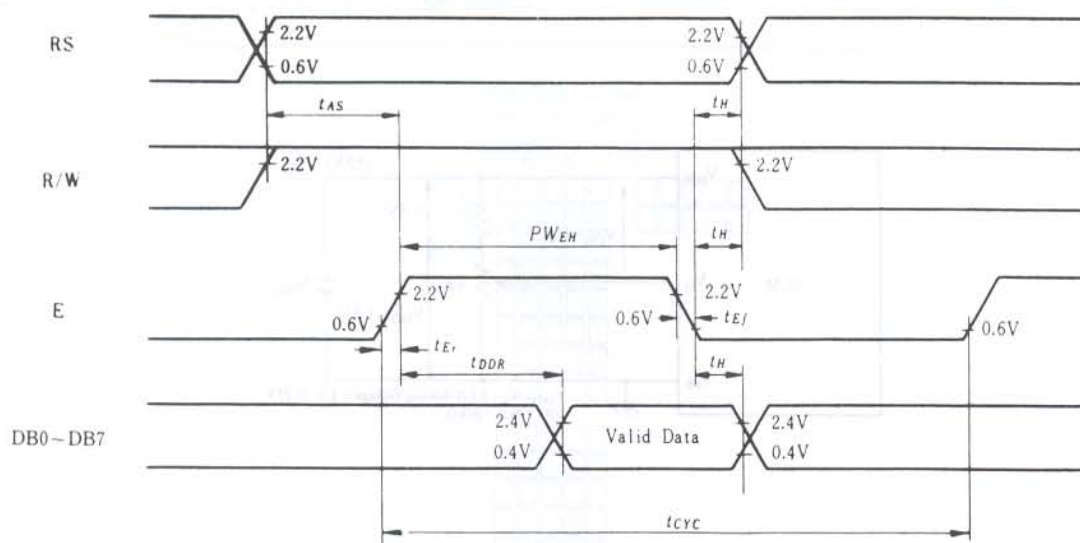
Fig. 6   Interface timing (data read)

(3) 8-bit operation, 8-digit x 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See the following table) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second display will only move within each line many times.

8 bit operation, 8-digit x 2-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB$_7$ ———— DB$_0$ 0 0 0 0 1 1 1 0 • •		Sets to 8-bit operation and selects 2-line display and 5 x 7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	—	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	—	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H _	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6			
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	H I T A C H I _	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	H I T A C H I _ _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	H I T A C H I M _	Writes "M".
10			
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	H I T A C H I M I C R O C O _	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	H I T A C H I M I C R O C O _	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	I T A C H I I C R O C O M _	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14			
15	Return Home 0 0 0 0 0 0 0 0 1 0	H I T A C H I M I C R O C O M	Returns both display and cursor to the original position (Address 0).