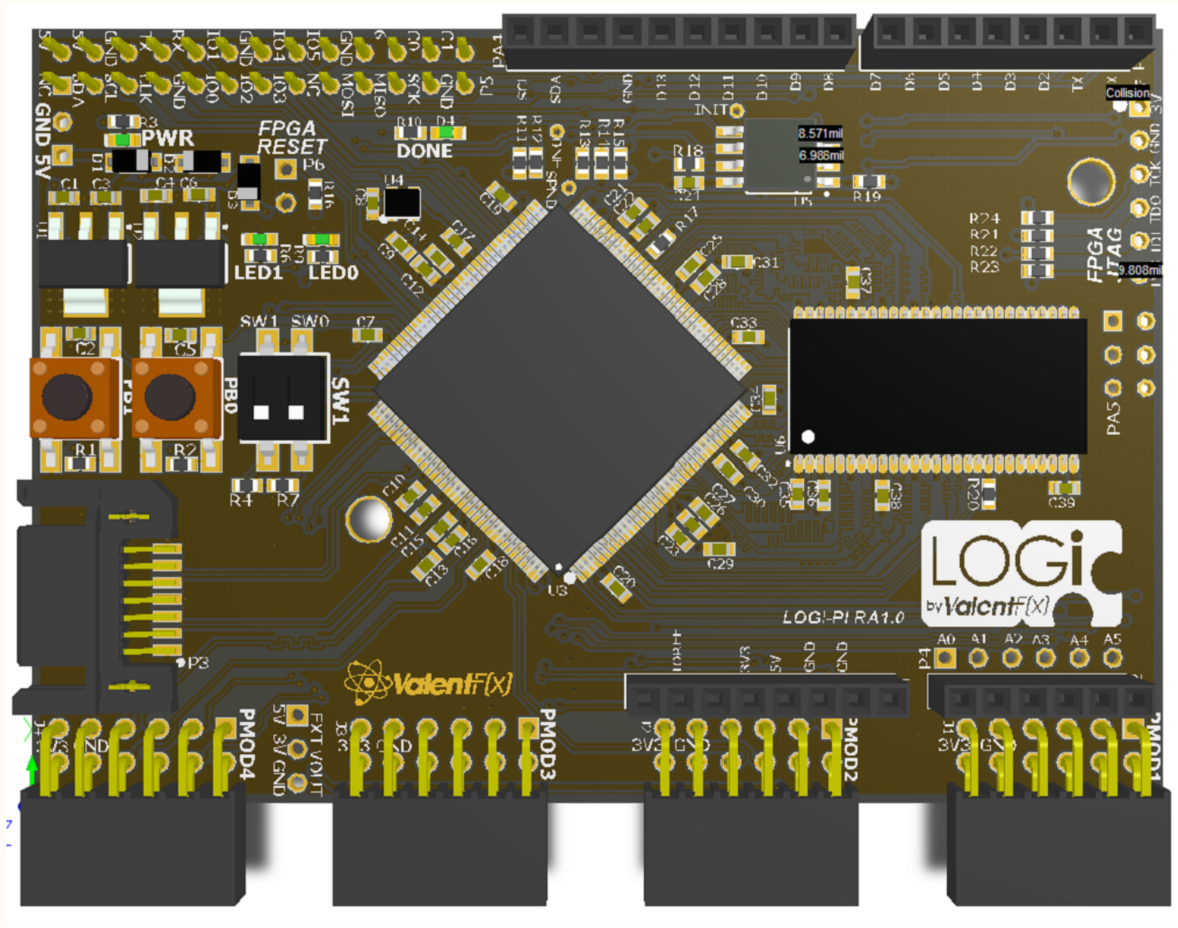
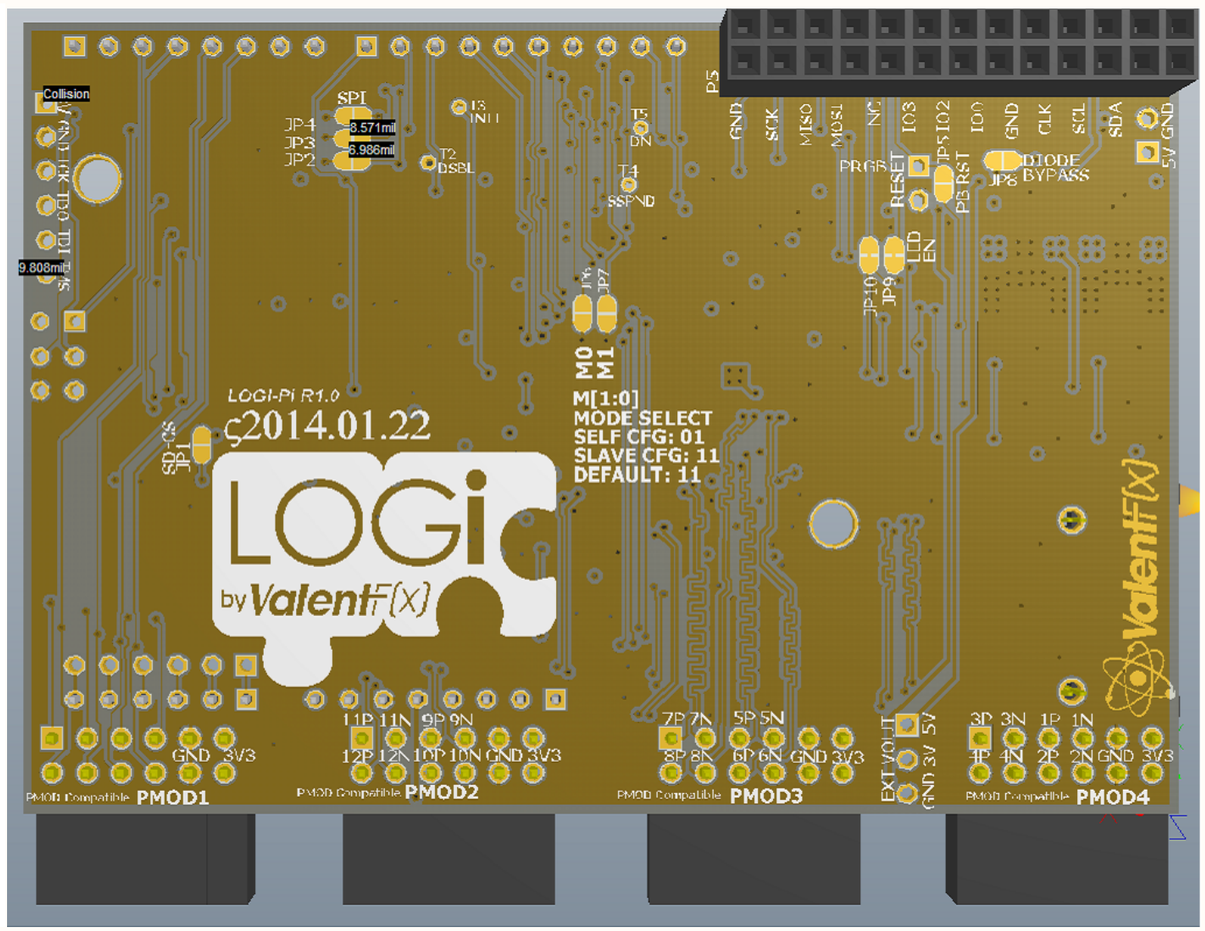




U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

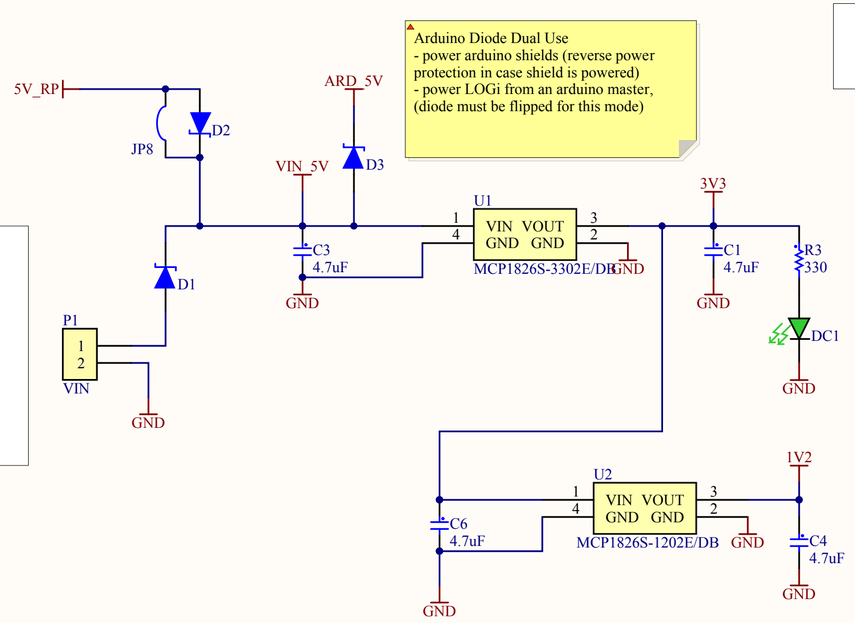
U_RAM
RAM.SchDoc

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

Title	LOGi-Pi Top Level		
Revision:	R1.0	Sheet	1 of 7
Date:	1/27/2014	Engineer:	Michael Jones

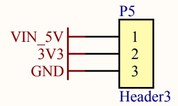
ValentF(X) ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the .
Raspberry Pi
Optionally power can be supplied through FPGA VIN header.



Arduino Diode Dual Use
- power arduino shields (reverse power protection in case shield is powered)
- power LOGi from an arduino master, (diode must be flipped for this mode)

1 x Auxillary Power output Header



VALENTFX-LOGO-500
Logo2

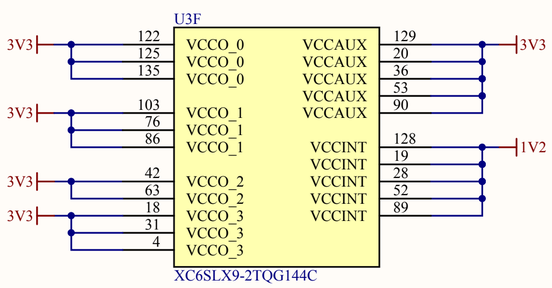
VALENTFX-LOGO-750
Logo3

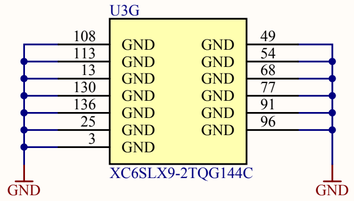
LOGI-LOGO-600
LOGO4

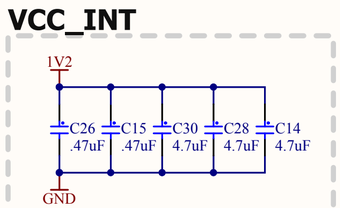
LOGI-LOGO-1000
LOGO1

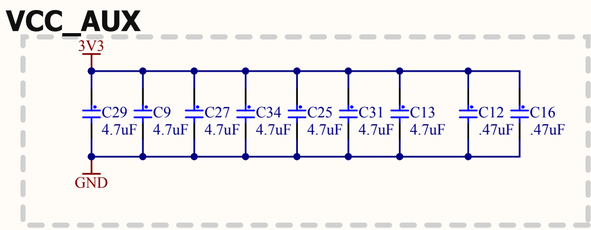
Title	Power Supply		
Revision:	R1.0	Sheet	2 of 7
Date:	1/27/2014	Engineer:	Michael Jones

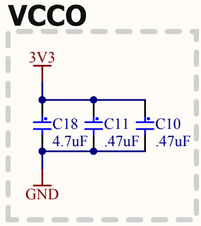
ValentF(X) ELECTRONICS INNOVATION

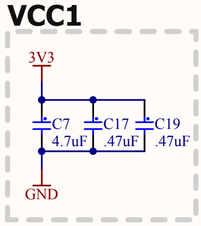


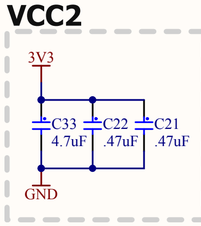


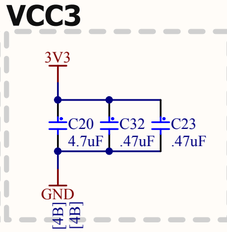






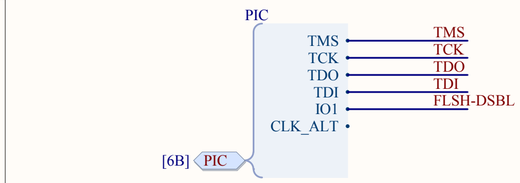


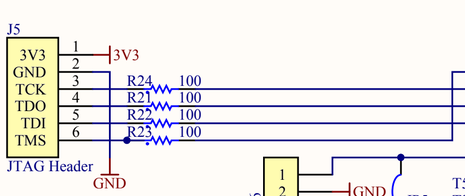


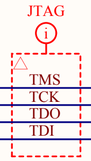


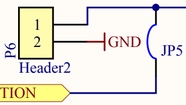
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

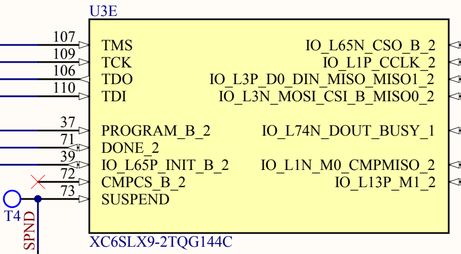
[2C], [3B], [4B]
[2C], [3A], [4B]

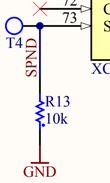


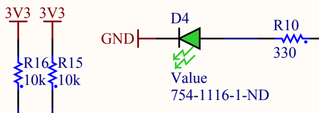


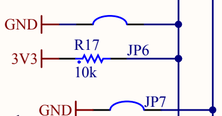




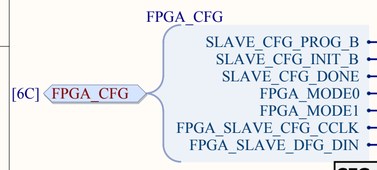








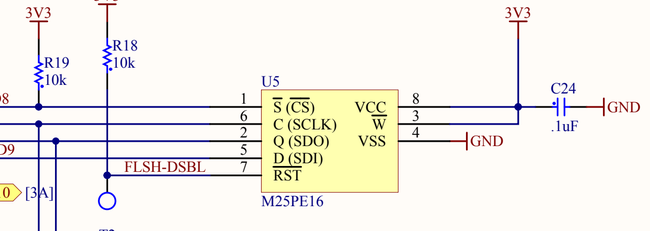
M1 default 1
M0 default 1



CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

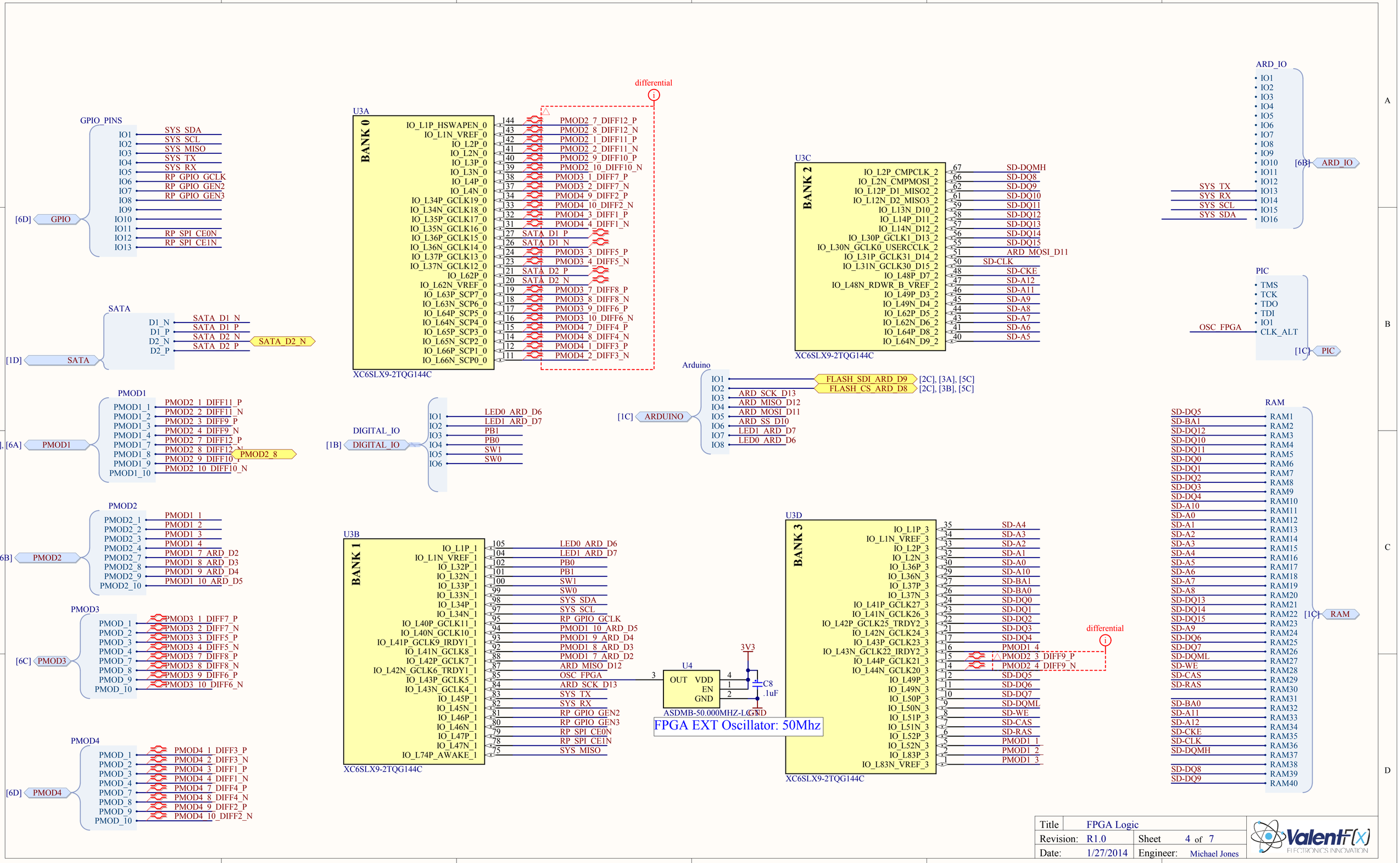
M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

FLASH_CS_ARD_D8
FLASH_SDI_ARD_D9

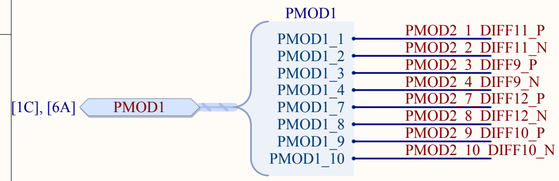


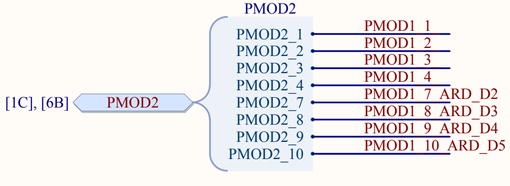
Title	FPGA Configuration		
Revision:	R1.0	Sheet	3 of 7
Date:	1/27/2014	Engineer:	Michael Jones

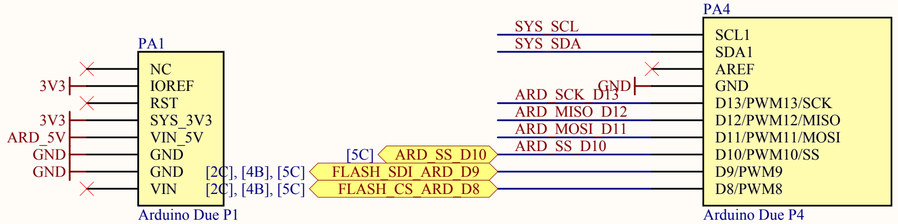
ValentF(X) ELECTRONICS INNOVATION

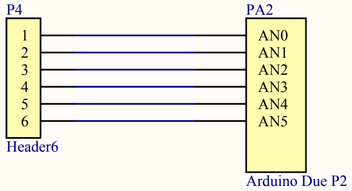

GPIO_PINS
IO1 SYS_SDA
IO2 SYS_SCL
IO3 SYS_MISO
IO4 SYS_TX
IO5 SYS_RX
IO6 RP_GPIO_GCLK
IO7 RP_GPIO_GEN2
IO8 RP_GPIO_GEN3
IO9
IO10
IO11 RP_SPI_CE0N
IO12 RP_SPI_CE1N
IO13
[6D] GPIO
SATA
D1_N SATA_D1_N
D1_P SATA_D1_P
D2_N SATA_D2_N
D2_P SATA_D2_P
SATA_D2_N
[1D] SATA
PMOD1
PMOD1_1 PMOD2_1_DIFF11_P
PMOD1_2 PMOD2_2_DIFF11_N
PMOD1_3 PMOD2_3_DIFF9_P
PMOD1_4 PMOD2_4_DIFF9_N
PMOD1_7 PMOD2_7_DIFF12_P
PMOD1_8 PMOD2_8_DIFF12_N
PMOD1_9 PMOD2_9_DIFF10_P
PMOD1_10 PMOD2_10_DIFF10_N
PMOD2_8
[1B], [6A] PMOD1
PMOD2
PMOD2_1 PMOD1_1
PMOD2_2 PMOD1_2
PMOD2_3 PMOD1_3
PMOD2_4 PMOD1_4
PMOD2_7 PMOD1_7_ARD_D2
PMOD2_8 PMOD1_8_ARD_D3
PMOD2_9 PMOD1_9_ARD_D4
PMOD2_10 PMOD1_10_ARD_D5
[B], [6B] PMOD2
PMOD3
PMOD_1 PMOD3_1_DIFF7_P
PMOD_2 PMOD3_2_DIFF7_N
PMOD_3 PMOD3_3_DIFF5_P
PMOD_4 PMOD3_4_DIFF5_N
PMOD_7 PMOD3_7_DIFF8_P
PMOD_8 PMOD3_8_DIFF8_N
PMOD_9 PMOD3_9_DIFF6_P
PMOD_10 PMOD3_10_DIFF6_N
[6C] PMOD3
PMOD4
PMOD_1 PMOD4_1_DIFF3_P
PMOD_2 PMOD4_2_DIFF3_N
PMOD_3 PMOD4_3_DIFF1_P
PMOD_4 PMOD4_4_DIFF1_N
PMOD_7 PMOD4_7_DIFF4_P
PMOD_8 PMOD4_8_DIFF4_N
PMOD_9 PMOD4_9_DIFF2_P
PMOD_10 PMOD4_10_DIFF2_N
[6D] PMOD4
U3A
differential
BANK 0
IO_L1P_HSWAPEN_0 144 PMOD2_7_DIFF12_P
IO_L1N_VREF_0 143 PMOD2_8_DIFF12_N
IO_L2P_0 142 PMOD2_1_DIFF11_P
IO_L2N_0 141 PMOD2_2_DIFF11_N
IO_L3P_0 140 PMOD2_9_DIFF10_P
IO_L3N_0 139 PMOD2_10_DIFF10_N
IO_L4P_0 138 PMOD3_1_DIFF7_P
IO_L4N_0 137 PMOD3_2_DIFF7_N
IO_L34P_GCLK19_0 134 PMOD4_9_DIFF2_P
IO_L34N_GCLK18_0 133 PMOD4_10_DIFF2_N
IO_L35P_GCLK17_0 132 PMOD4_3_DIFF1_P
IO_L35N_GCLK16_0 131 PMOD4_4_DIFF1_N
IO_L36P_GCLK15_0 127 SATA_D1_P
IO_L36N_GCLK14_0 126 SATA_D1_N
IO_L37P_GCLK13_0 124 PMOD3_3_DIFF5_P
IO_L37N_GCLK12_0 123 PMOD3_4_DIFF5_N
IO_L62P_0 121 SATA_D2_P
IO_L62N_VREF_0 120 SATA_D2_N
IO_L63P_SCP7_0 119 PMOD3_7_DIFF8_P
IO_L63N_SCP6_0 118 PMOD3_8_DIFF8_N
IO_L64P_SCP5_0 117 PMOD3_9_DIFF6_P
IO_L64N_SCP4_0 116 PMOD3_10_DIFF6_N
IO_L65P_SCP3_0 115 PMOD4_7_DIFF4_P
IO_L65N_SCP2_0 114 PMOD4_8_DIFF4_N
IO_L66P_SCP1_0 112 PMOD4_1_DIFF3_P
IO_L66N_SCP0_0 111 PMOD4_2_DIFF3_N
XC6SLX9-2TQG144C
DIGITAL_IO
IO1 LED0_ARD_D6
IO2 LED1_ARD_D7
IO3 PB1
IO4 PB0
IO5 SW1
IO6 SW0
[1B] DIGITAL_IO
U3C
BANK 2
IO_L2P_CMPCLK_2 67 SD-DQMH
IO_L2N_CMPMOSI_2 66 SD-DQ8
IO_L12P_D1_MISO2_2 62 SD-DQ9
IO_L12N_D2_MISO3_2 61 SD-DQ10
IO_L13N_D10_2 59 SD-DQ11
IO_L14P_D11_2 58 SD-DQ12
IO_L14N_D12_2 57 SD-DQ13
IO_L30P_GCLK1_D13_2 56 SD-DQ14
IO_L30N_GCLK0_USERCCLK_2 55 SD-DQ15
IO_L31P_GCLK31_D14_2 51 ARD_MOSI_D11
IO_L31N_GCLK30_D15_2 50 SD-CLK
IO_L48P_D7_2 48 SD-CKE
IO_L48N_RDWR_B_VREF_2 47 SD-A12
IO_L49P_D3_2 46 SD-A11
IO_L49N_D4_2 45 SD-A9
IO_L62P_D5_2 44 SD-A8
IO_L62N_D6_2 43 SD-A7
IO_L64P_D8_2 41 SD-A6
IO_L64N_D9_2 40 SD-A5
XC6SLX9-2TQG144C
Arduino
IO1 FLASH_SDI_ARD_D9 [2C], [3A], [5C]
IO2 FLASH_CS_ARD_D8 [2C], [3B], [5C]
IO3 ARD_SCK_D13
IO4 ARD_MISO_D12
IO5 ARD_MOSI_D11
IO6 ARD_SS_D10
IO7 LED1_ARD_D7
IO8 LED0_ARD_D6
[1C] ARDUINO
ARD_IO
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
SYS_TX
SYS_RX
SYS_SCL
SYS_SDA
[6B] ARD_IO
PIC
TMS
TCK
TDO
TDI
IO1
CLK_ALT
OSC_FPGA
[1C] PIC
RAM
SD-DQ5 RAM1
SD-BA1 RAM2
SD-DQ12 RAM3
SD-DQ10 RAM4
SD-DQ11 RAM5
SD-DQ0 RAM6
SD-DQ1 RAM7
SD-DQ2 RAM8
SD-DQ3 RAM9
SD-DQ4 RAM10
SD-A10 RAM11
SD-A0 RAM12
SD-A1 RAM13
SD-A2 RAM14
SD-A3 RAM15
SD-A4 RAM16
SD-A5 RAM17
SD-A6 RAM18
SD-A7 RAM19
SD-A8 RAM20
SD-DQ13 RAM21
SD-DQ14 RAM22
SD-DQ15 RAM23
SD-A9 RAM24
SD-DQ6 RAM25
SD-DQ7 RAM26
SD-DQML RAM27
SD-WE RAM28
SD-CAS RAM29
SD-RAS RAM30
RAM31
SD-BA0 RAM32
SD-A11 RAM33
SD-A12 RAM34
SD-CKE RAM35
SD-CLK RAM36
SD-DQMH RAM37
RAM38
SD-DQ8 RAM39
SD-DQ9 RAM40
[1C] RAM
U3B
BANK 1
IO_L1P_1 105 LED0_ARD_D6
IO_L1N_VREF_1 104 LED1_ARD_D7
IO_L32P_1 102 PB0
IO_L32N_1 101 PB1
IO_L33P_1 100 SW1
IO_L33N_1 99 SW0
IO_L34P_1 98 SYS_SDA
IO_L34N_1 97 SYS_SCL
IO_L40P_GCLK11_1 95 RP_GPIO_GCLK
IO_L40N_GCLK10_1 94 PMOD1_10_ARD_D5
IO_L41P_GCLK9_IRDY1_1 93 PMOD1_9_ARD_D4
IO_L41N_GCLK8_1 92 PMOD1_8_ARD_D3
IO_L42P_GCLK7_1 88 PMOD1_7_ARD_D2
IO_L42N_GCLK6_TRDY1_1 87 ARD_MISO_D12
IO_L43P_GCLK5_1 85 OSC_FPGA
IO_L43N_GCLK4_1 84 ARD_SCK_D13
IO_L45P_1 83 SYS_TX
IO_L45N_1 82 SYS_RX
IO_L46P_1 81 RP_GPIO_GEN2
IO_L46N_1 80 RP_GPIO_GEN3
IO_L47P_1 79 RP_SPI_CE0N
IO_L47N_1 78 RP_SPI_CE1N
IO_L74P_AWAKE_1 75 SYS_MISO
XC6SLX9-2TQG144C
3
U4
OUT VDD 4
EN 1
GND 2
ASDMB-50.000MHZ-LC-T
3V3
C8
.1uF
GND
FPGA EXT Oscillator: 50Mhz
U3D
BANK 3
IO_L1P_3 35 SD-A4
IO_L1N_VREF_3 34 SD-A3
IO_L2P_3 33 SD-A2
IO_L2N_3 32 SD-A1
IO_L36P_3 30 SD-A0
IO_L36N_3 29 SD-A10
IO_L37P_3 27 SD-BA1
IO_L37N_3 26 SD-BA0
IO_L41P_GCLK27_3 24 SD-DQ0
IO_L41N_GCLK26_3 23 SD-DQ1
IO_L42P_GCLK25_TRDY2_3 22 SD-DQ2
IO_L42N_GCLK24_3 21 SD-DQ3
IO_L43P_GCLK23_3 17 SD-DQ4
IO_L43N_GCLK22_IRDY2_3 16 PMOD1_4
IO_L44P_GCLK21_3 15 PMOD2_3_DIFF9_P
IO_L44N_GCLK20_3 14 PMOD2_4_DIFF9_N
IO_L49P_3 12 SD-DQ5
IO_L49N_3 11 SD-DQ6
IO_L50P_3 10 SD-DQ7
IO_L50N_3 9 SD-DQML
IO_L51P_3 8 SD-WE
IO_L51N_3 7 SD-CAS
IO_L52P_3 6 SD-RAS
IO_L52N_3 5 PMOD1_1
IO_L83P_3 3 PMOD1_2
IO_L83N_VREF_3 1 PMOD1_3
XC6SLX9-2TQG144C
differential
Title FPGA Logic
Revision: R1.0
Sheet 4 of 7
Date: 1/27/2014
Engineer: Michael Jones
ValentF(X)
ELECTRONICS INNOVATION

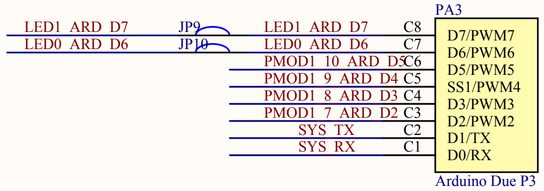
Arduino IO

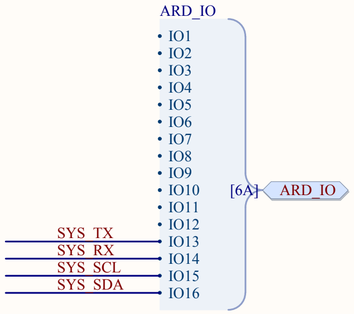


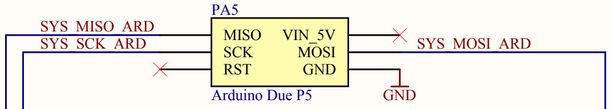


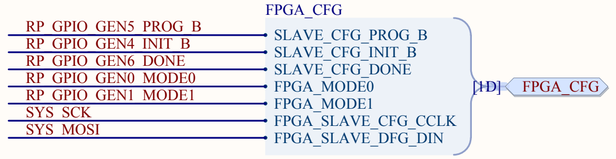


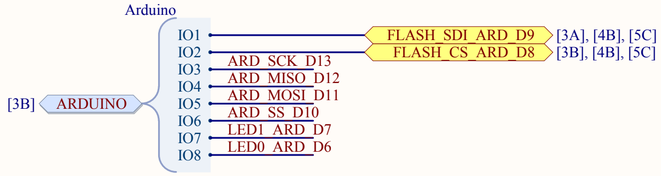






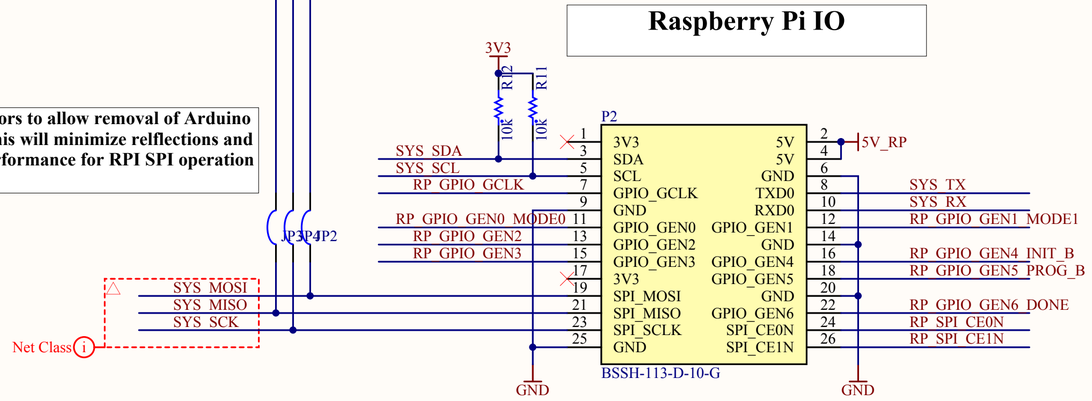


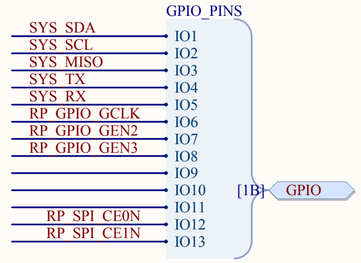




0 ohm resistors to allow removal of Arduino SPI pins. This will minimize relflections and optimize performance for RPI SPI operation

Raspberry Pi IO





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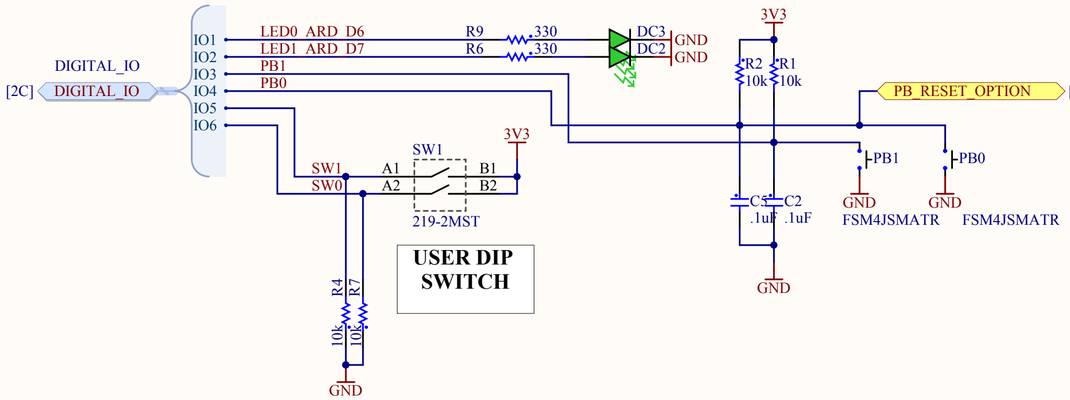
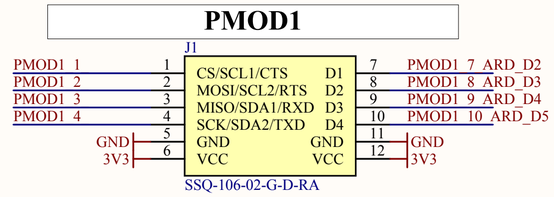
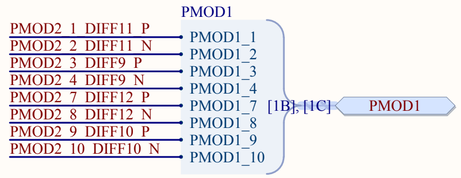
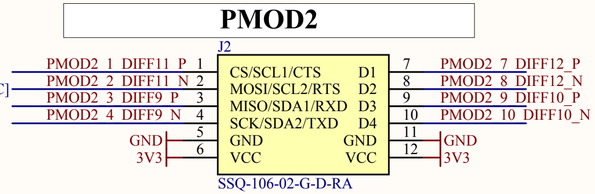
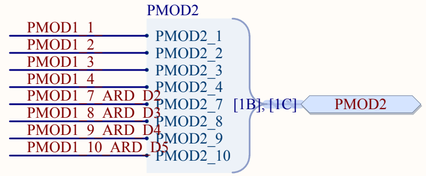
DIGITAL IO

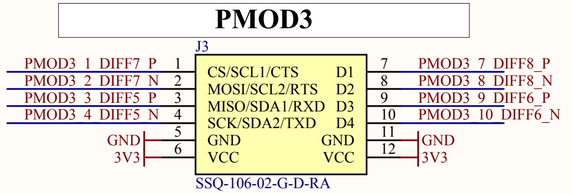


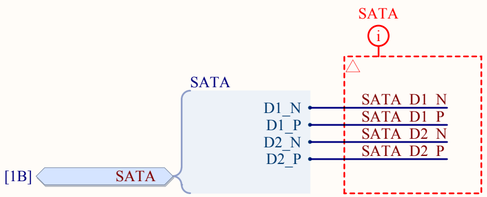


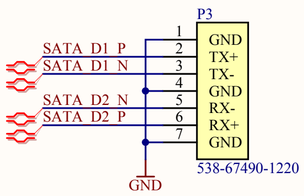


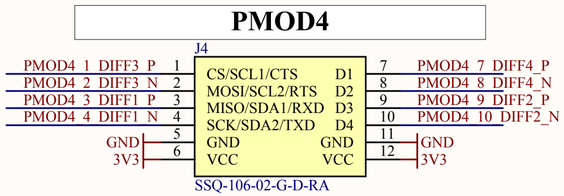


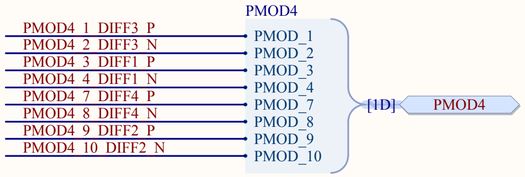












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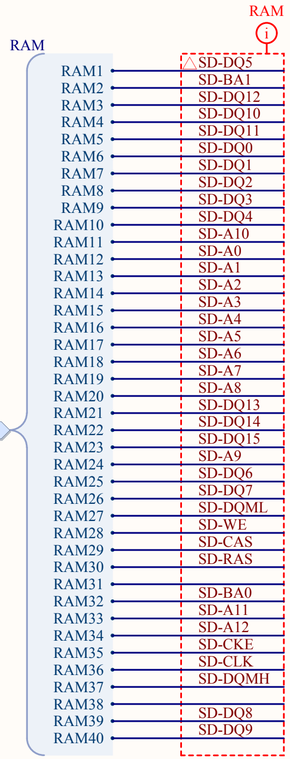
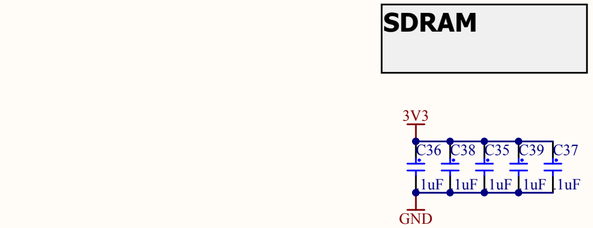
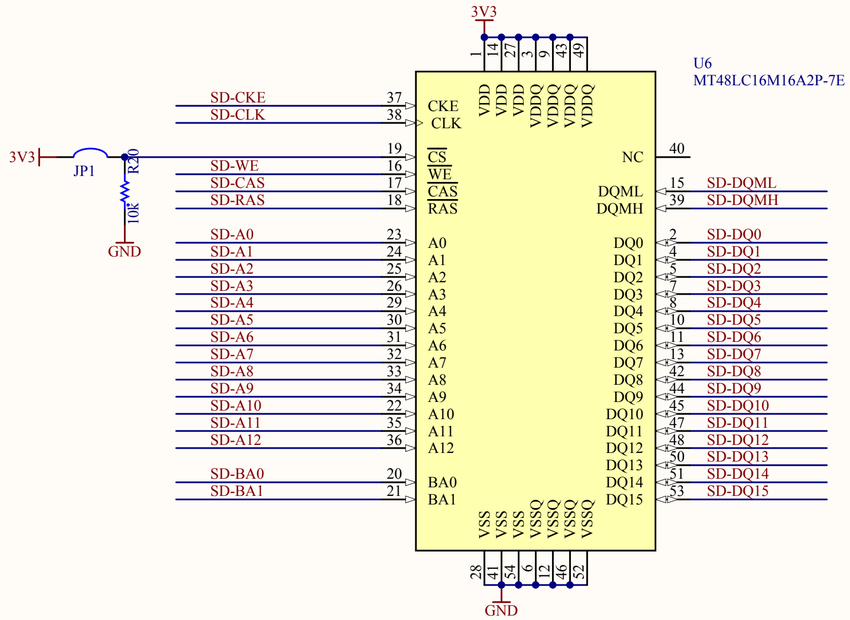
SDRAM







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