
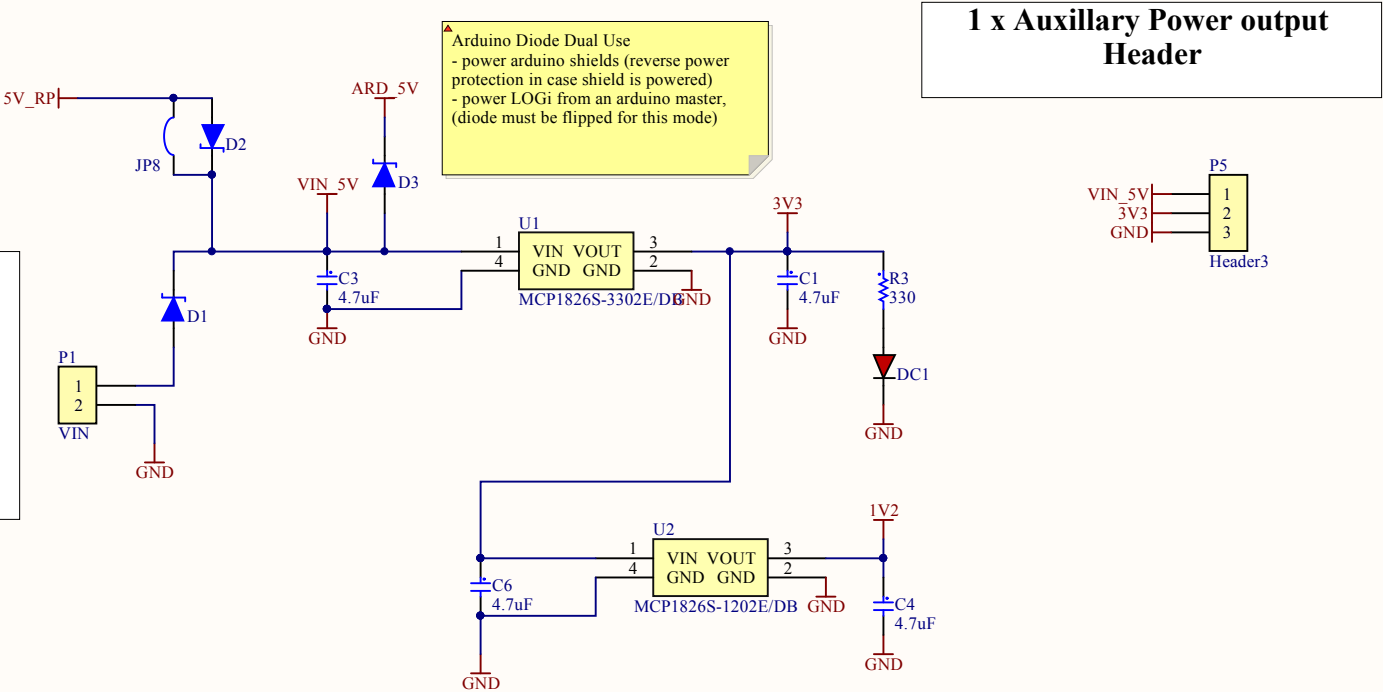


<p>U_POWER_SUPPLY POWER_SUPPLY.SchDoc</p> <p>U_FPGA_POWER_AND_CONFIGURATION FPGA_POWER_AND_CONFIGURATION.SchDoc</p>	<p>U_LOGIC_FPGA LOGIC_FPGA.SchDoc</p>	<p>U_DIGITAL_IO DIGITAL_IO.SchDoc</p>													
<p>U_RAM RAM.SchDoc</p>		<p>U_PERIPHERAL_PORT_IO PERIPHERAL_PORT_IO.SchDoc</p>	<table border="1"> <tr> <td>Title</td><td colspan="3">LOGi-Pi Top Level</td></tr> <tr> <td>Revision:</td><td>R1.1</td><td>Sheet</td><td>1 of 7</td></tr> <tr> <td>Date:</td><td>12/15/2014</td><td>Engineer:</td><td>Michael Jones</td></tr> </table> 	Title	LOGi-Pi Top Level			Revision:	R1.1	Sheet	1 of 7	Date:	12/15/2014	Engineer:	Michael Jones
Title	LOGi-Pi Top Level														
Revision:	R1.1	Sheet	1 of 7												
Date:	12/15/2014	Engineer:	Michael Jones												

Power: By Default Power will be supplied by the .
Raspberry Pi
Optionally power can be supplied through
FPGA VIN header.

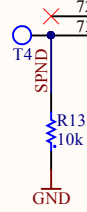
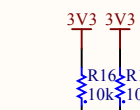
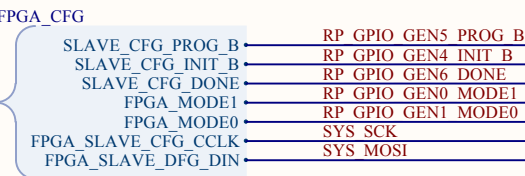
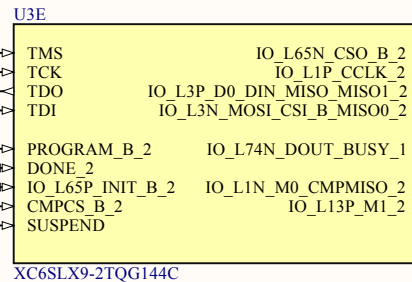
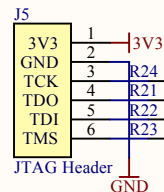
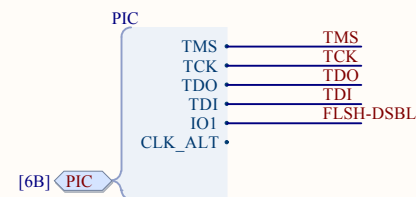
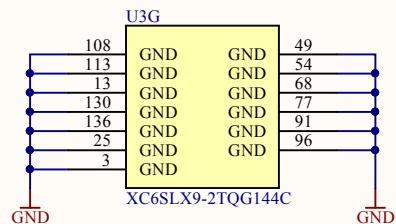
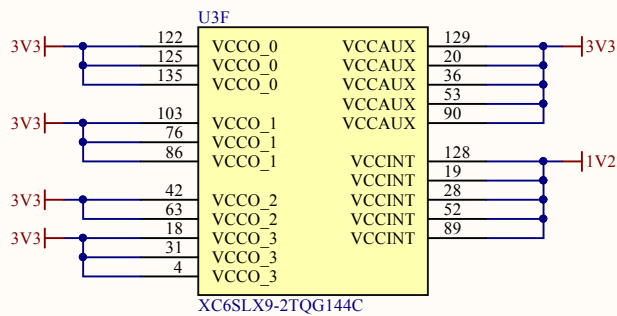


VALENTFX-LOGO-500
Logo2

VALENTFX-LOGO-750
Logo3

LOGI-LOGO-600
LOGO4

LOGI-LOGO-1000
LOGO1

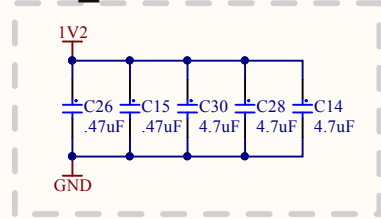


M1 default 1

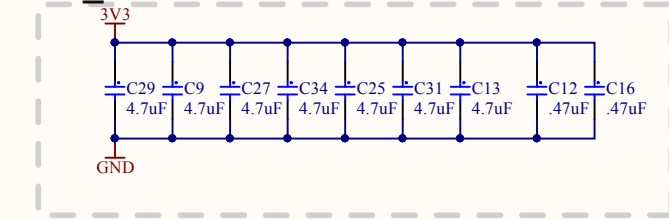
M0 default 1

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

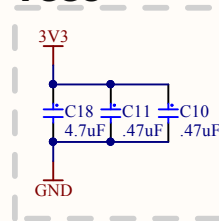
VCC_INT



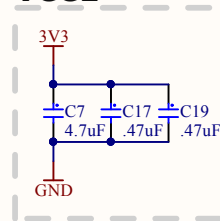
VCC_AUX



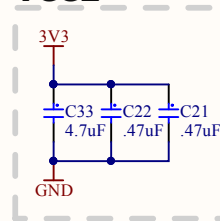
VCCO



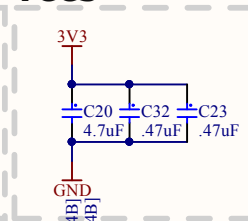
VCC1



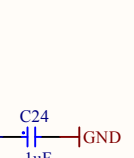
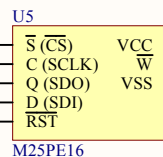
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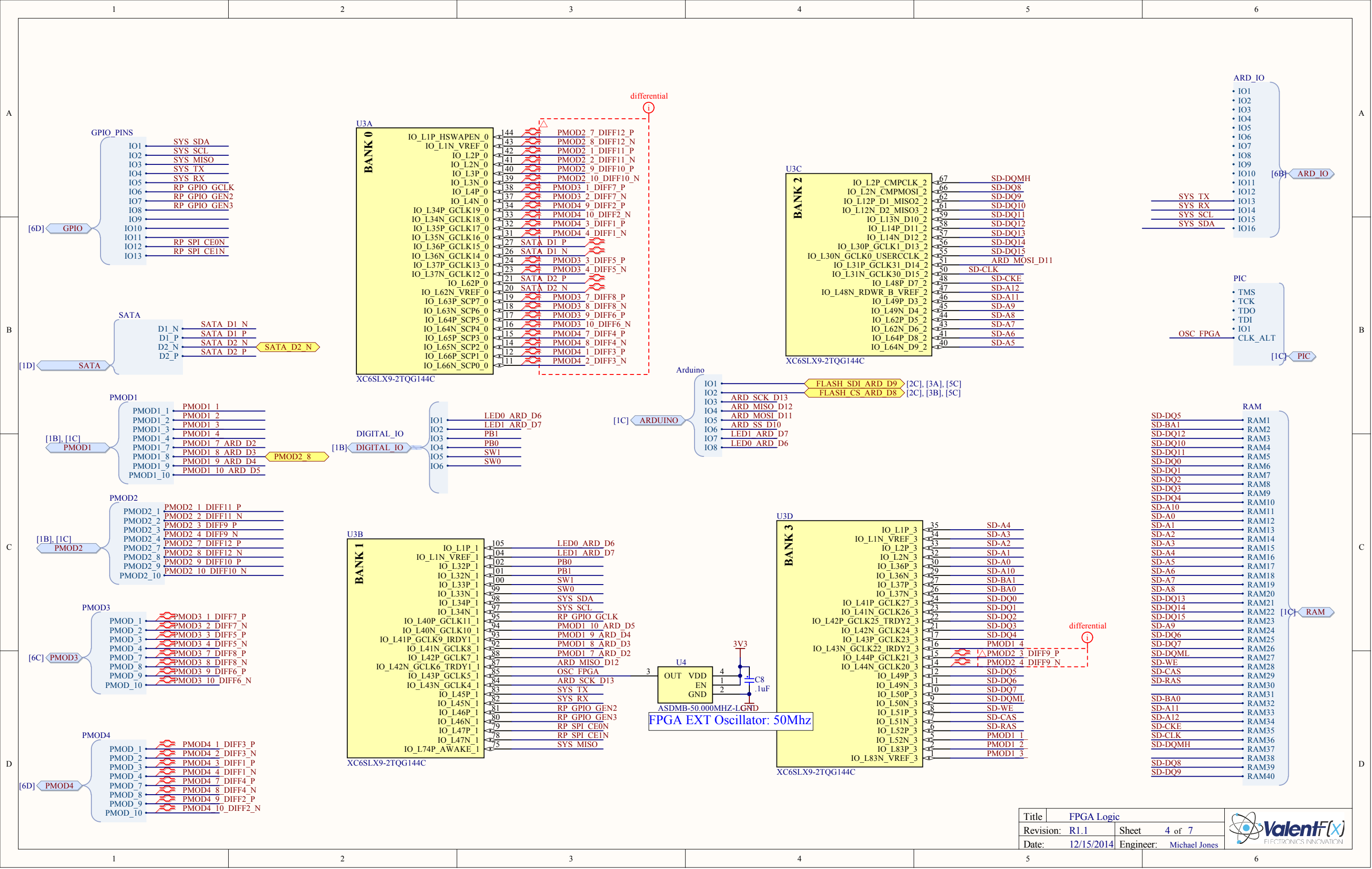


VCC3

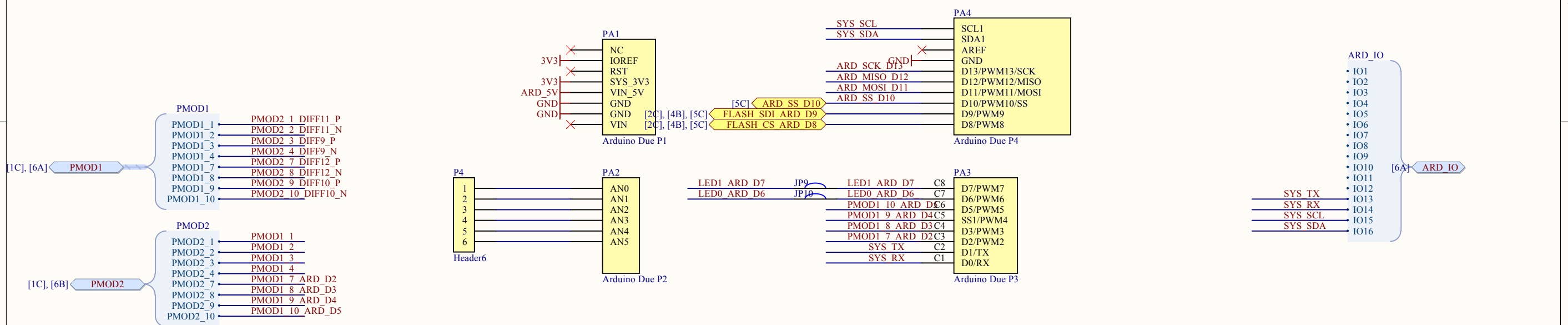


Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

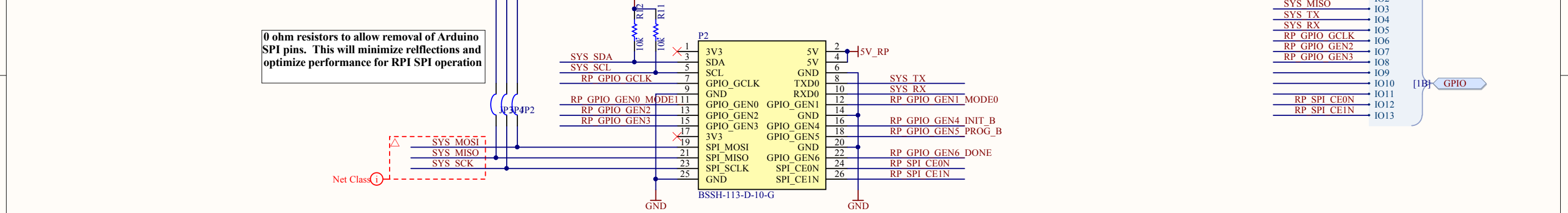




Arduino IO



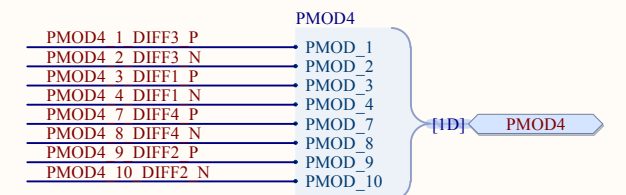
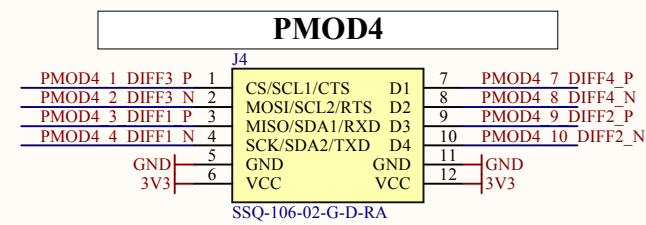
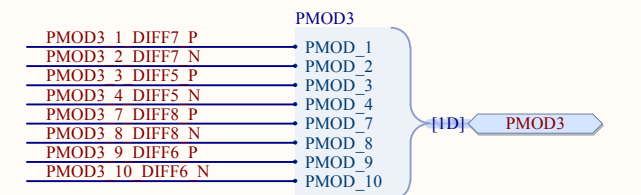
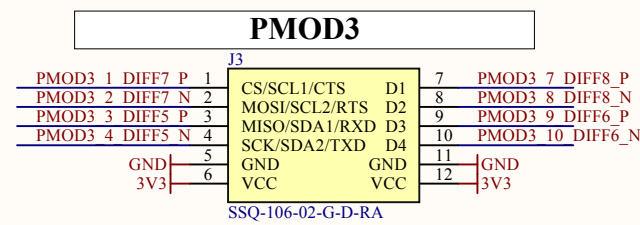
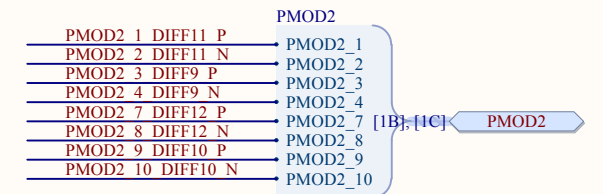
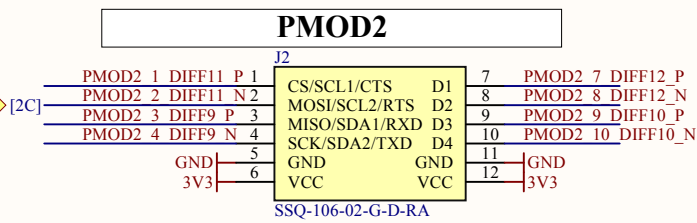
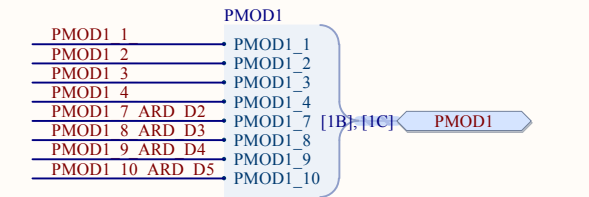
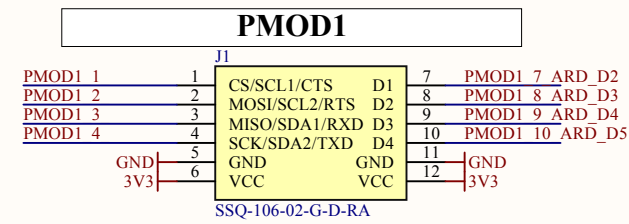
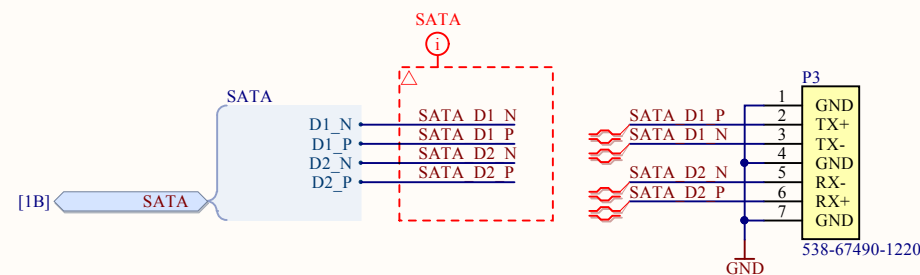
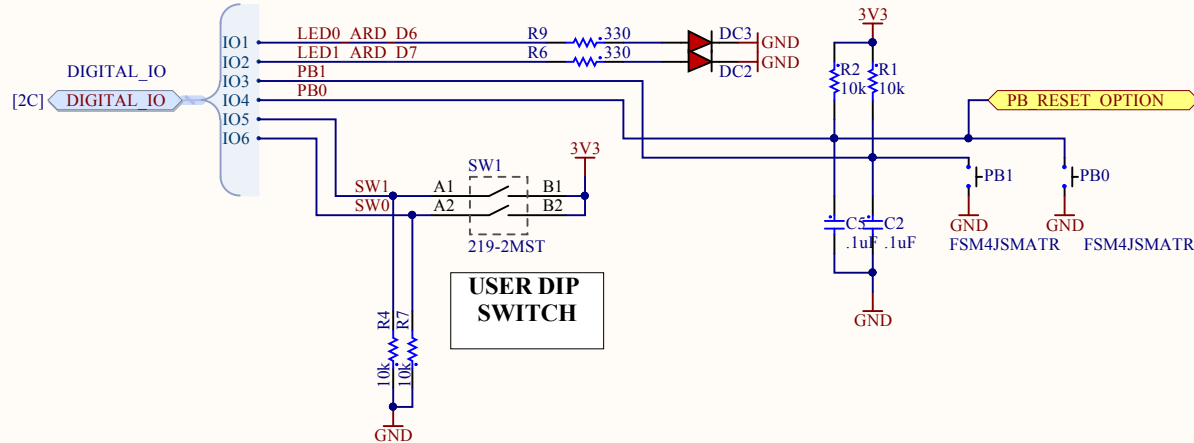
Raspberry Pi IO



0 ohm resistors to allow removal of Arduino SPI pins. This will minimize reflections and optimize performance for RPI SPI operation

Net Class 1

DIGITAL IO	
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A

B

C

D

A

B

C

D

