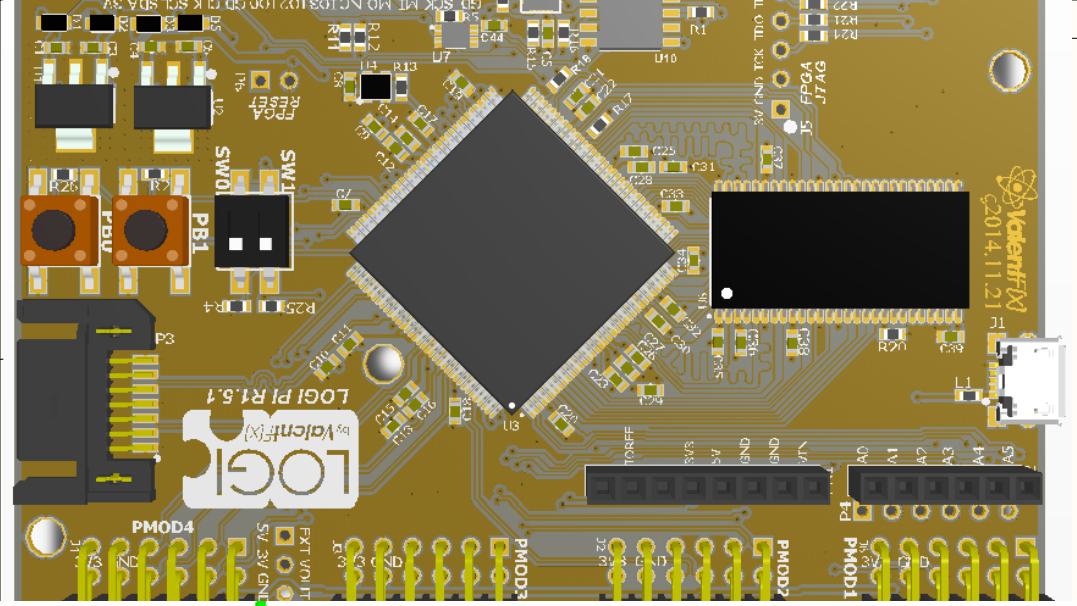
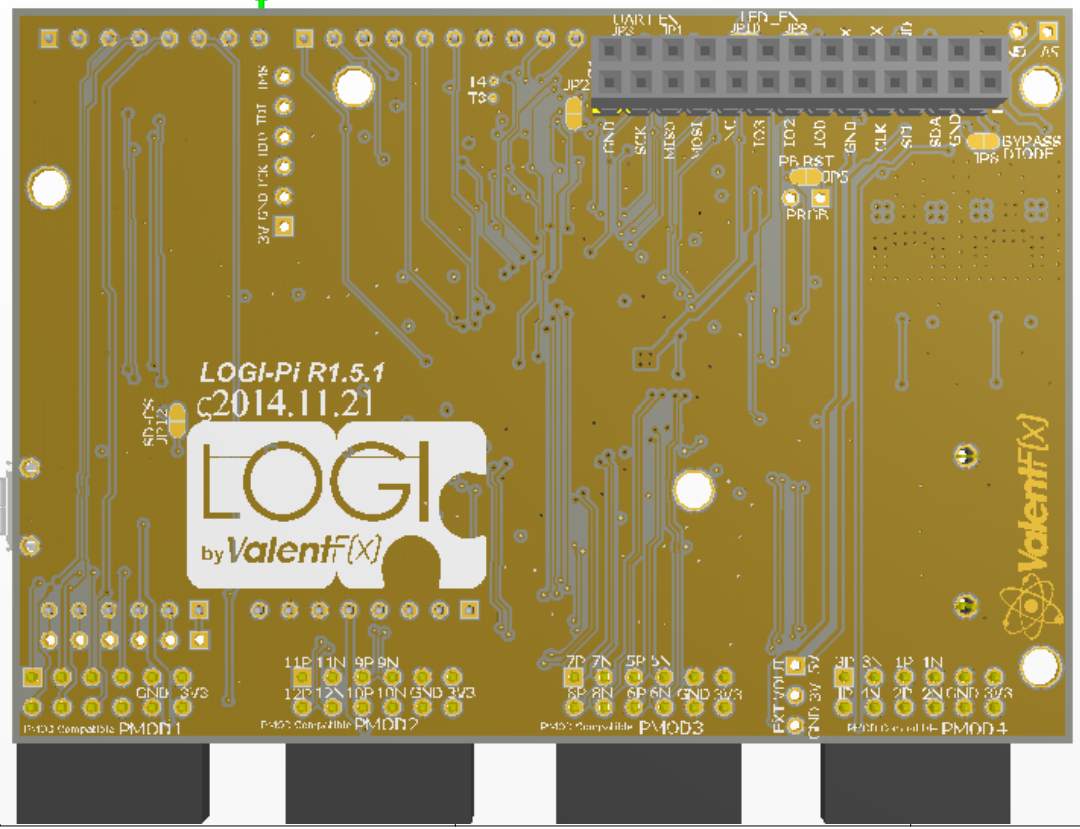




3	4

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

SCRW1
SCRW - 4-40x1/4-Nylon
SCRW2
SCRW - 4-40x1/4-Nylon
SCRW3
SCRW - 4-40x1/4-Nylon
SCRW4
SCRW - 4-40x1/4-Nylon

STDOFF1
STDOFF - 4-40-5/8"
STDOFF2
STDOFF - 4-40-5/8"

M1
Rubber Bumper
Rubber Bumper Standoff

Title	LOGi-Pi Top Level		
Revision:	R1.5	Sheet	1 of 7
Date:	1/22/2015	Engineer:	Michael Jones

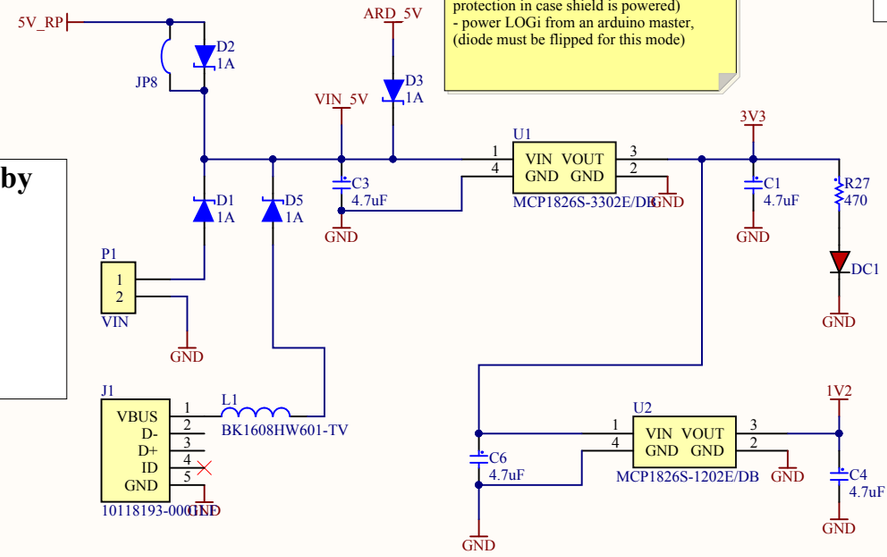
ValentF(x) ELECTRONICS INNOVATION

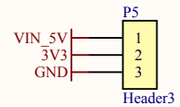
3	4

Power: By Default Power will be supplied by the .
Raspberry Pi
Optionally power can be supplied through FPGA VIN header.

Arduino Diode Dual Use
- power arduino shields (reverse power protection in case shield is powered)
- power LOGi from an arduino master, (diode must be flipped for this mode)

1 x Auxillary Power output Header





LOGI-LOGO
LOGO1

VALENTFX-LOGO-500
Logo2

VALENTFX-LOGO-750
Logo3

Title	Power Supply		
Revision:	R1.5	Sheet	2 of 7
Date:	1/22/2015	Engineer:	Michael Jones

ValentF(X) ELECTRONICS INNOVATION

Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

U3F — XC6SLX9-2TQG144C

VCCO_0 (122, 125, 135) ← 3V3
VCCO_1 (103, 76, 86) ← 3V3
VCCO_2 (42, 63, 18) ← 3V3
VCCO_3 (31, 4) ← 3V3
VCCAUX (129, 20, 36, 53, 90) → 3V3
VCCINT (128, 19, 28, 52, 89) → 1V2

U3G — XC6SLX9-2TQG144C

GND (108, 113, 13, 130, 136, 25, 3, 49, 54, 68, 77, 91, 96) → GND

GPIO Expander - Handling of General Config/Control Pins

VCC_INT

1V2 — C26 .47uF, C15 .47uF, C30 4.7uF, C28 4.7uF, C14 4.7uF — GND

VCC_AUX

3V3 — C29 4.7uF, C9 4.7uF, C27 4.7uF, C34 4.7uF, C25 4.7uF, C31 4.7uF, C13 4.7uF, C12 .47uF, C16 .47uF — GND

VCCO

3V3 — C18 4.7uF, C11 .47uF, C10 .47uF — GND

VCC1

3V3 — C7 4.7uF, C17 .47uF, C19 .47uF — GND

VCC2

3V3 — C33 4.7uF, C22 .47uF, C21 .47uF — GND

VCC3

3V3 — C20 4.7uF, C32 .47uF, C23 .47uF — GND

JTAG Header

J5 — JTAG Header
3V3 (1), GND (2), TCK (3), TDO (4), TDI (5), TMS (6) → 3V3
R24 220, R23 220, R22 220, R21 220, R20 220
GND

U5 — SX1505I087TRT

ADDR (12), VDDM (14), VCC1 (7), VCC2 (17)
RST# (1), INT# (11), SCL (4), SDA (2)
GND (8), GND (18)
IO0 (5) CFG_PRGB
IO1 (6) CFG_INITB
IO2 (9) CFG_DONE
IO3 (10) CFG_M1
IO4 (15) CFG_BUF_OE#
IO5 (16) FLSH_RST
IO6 (19) → T3
IO7 (20) → T4

3V3 — JP2 — R3 10k — GND
C5 .1uF
4[3C], 5[2C] SYS_SCL
4[3C], 5[2C] SYS_SDA

U7 — NC7WZ125K8X

3V3 — R5 10k — CFG_BUF_OE#
C44 1uF
OE1# (1), OE2# (7), A1 (2), A2 (5), VCC (8), GND (4), Y1 (6), Y2 (3)
4[3D], 5[2D] SYS_MOSI
4[3D], 5[2D] SYS_SCK
CFG_CLK

Push Button Reset option

6[3B] PB_RESET_OPTION — JP5 — P6 Header2 (1, 2) — GND
R10 470 — DC4 — GND

CFG_DIN
CFG_PRGB
CFG_INITB
R16 10k, R15 10k — 3V3

JTAG

U3E — XC6SLX9-2TQG144C

TMS (107), TCK (109), TDO (106), TDI (110)
PROGRAM_B_2, DONE_2, IO_L6P_INIT_B_2, CMPCS_B_2, SUSPEND (37, 71, 39, 72, 73) → GND
CFG_DONE
IO_L65N_CSO_B_2, IO_L1P_CCLK_2, IO_L3P_D0_DIN_MISO_MISO1_2, IO_L3N_MOSI_CSI_B_MISO0_2, IO_L74N_DOUT_BUSY_1, IO_L1N_M0_CMPMISO_2, IO_L13P_M1_2

FLASH_CS_ARD_D8 (38, 70) 4[4B], 5[2C], 5[3B]
CFG_CLK (65)
CFG_DIN (64)
FLASH_SDI_ARD_D9 (74) 4[4B], 5[2C], 5[3A]
ARD_SS_D10 (69) 5[3A]
CFG_M1 (60)

JP4 — R17 — 3V3 GND
R18 10k — 3V3

Flash for Configuration or FPGA usage

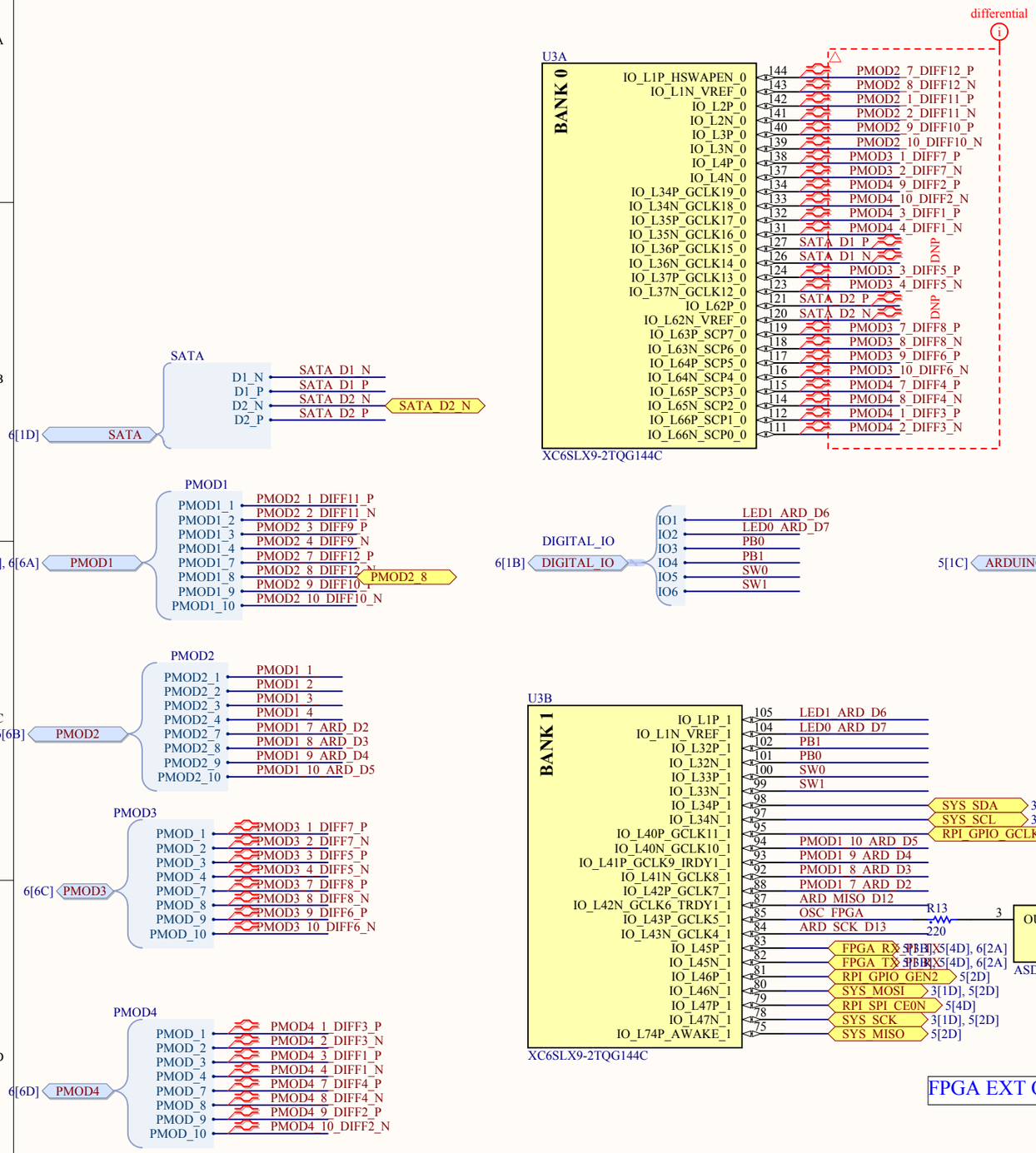
3V3 — R19 10k
U10 — S25FL032P0XMFI011
S (CS) (1), C (SCLK) (6), Q (SDO) (2), D (SDI) (5), RST (7), VCC (8), W (3), VSS (4)
FLSH_RST
R1 10k — 3V3
3V3 — C24 .1uF — GND

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

Hard wire Mode pin 0.
Mode1 controlled from GPIO EXP, default (0) self config for standalone mode. User can solder jumper to hard wire to self config

Title	FPGA Configuration		
Revision:	R1.5	Sheet	3 of 7
Date:	1/22/2015	Engineer:	Michael Jones

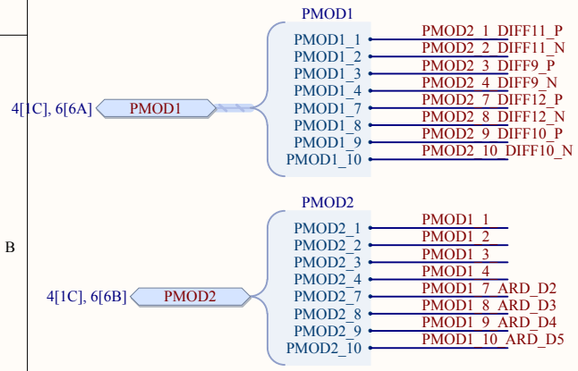
ValentF(x) ELECTRONICS INNOVATION

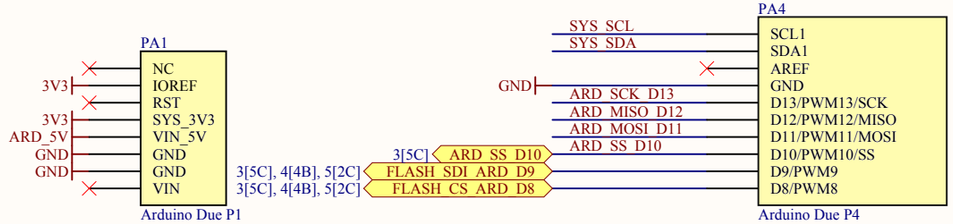


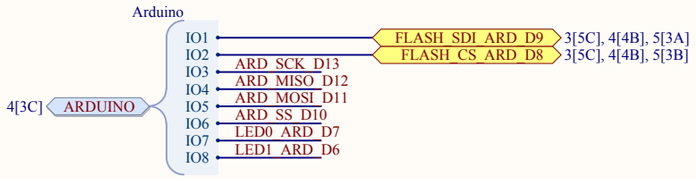
Title	FPGA Logic		
Revision:	R1.5	Sheet	4 of 7
Date:	1/22/2015	Engineer:	Michael Jones

ValentF(x) ELECTRONICS INNOVATION

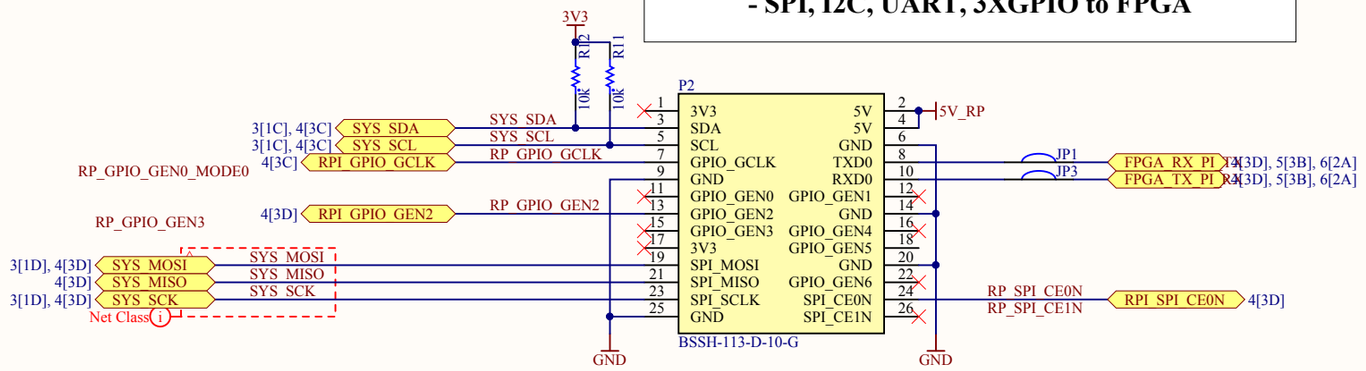
Arduino IO







Raspberry Pi IO
- SPI, I2C, UART, 3XGPIO to FPGA

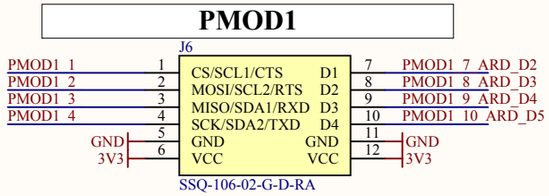


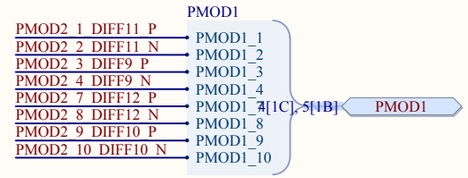
Title	Peripheral Port IO		
Revision:	R1.5	Sheet	5 of 7
Date:	1/22/2015	Engineer:	Michael Jones

ValentF(x) ELECTRONICS INNOVATION

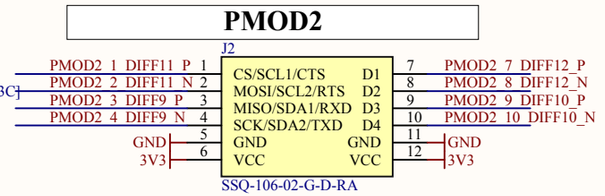
DIGITAL IO

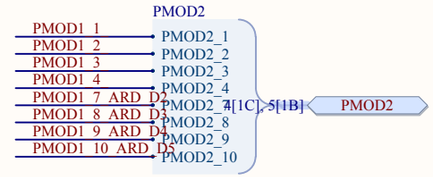
PMOD1

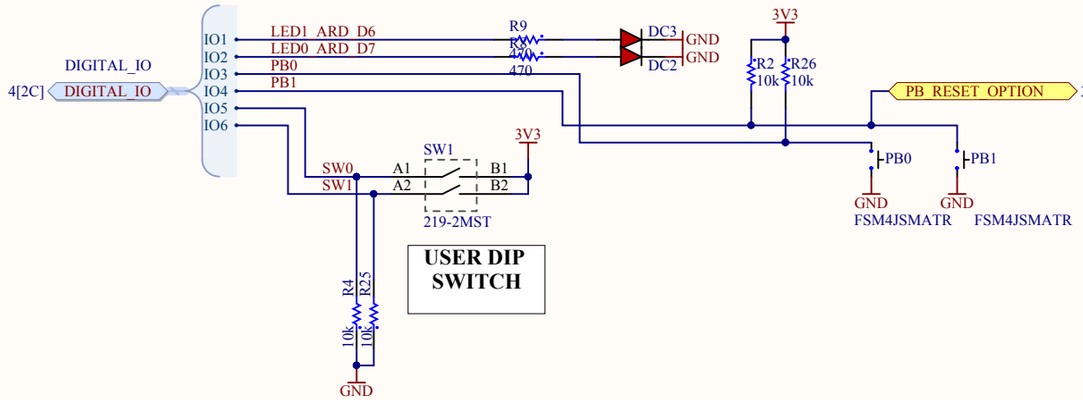




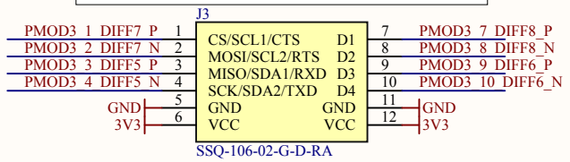
PMOD2

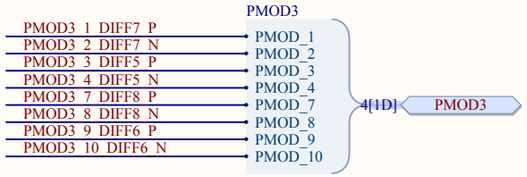


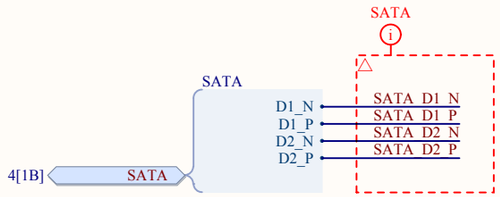


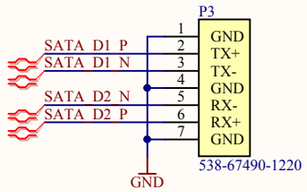


PMOD3

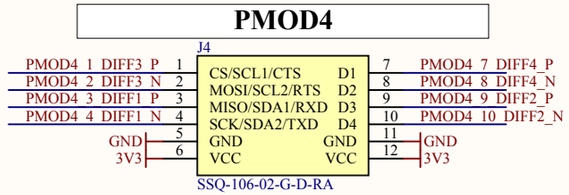


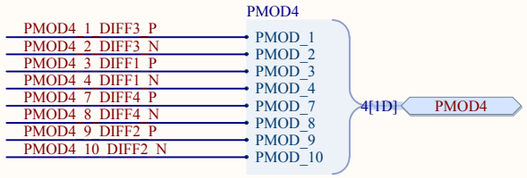






PMOD4

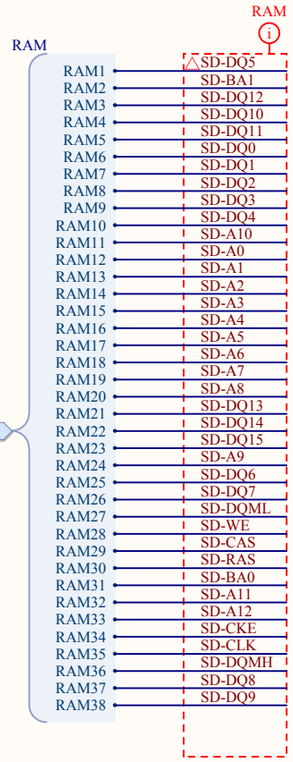


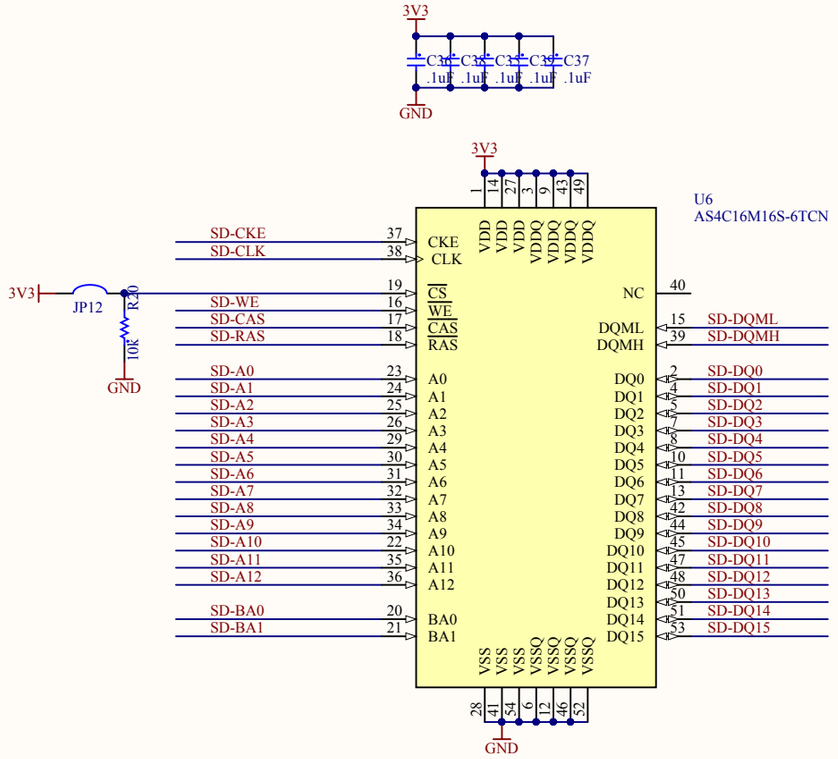


Title	Digital IO		
Revision:	R1.5	Sheet	6 of 7
Date:	1/22/2015	Engineer:	Michael Jones

ValentF(x) ELECTRONICS INNOVATION

SDRAM





Title	SDRAM		
Revision:	R1.5	Sheet	7 of 7
Date:	1/22/2015	Engineer:	Michael Jones

ValentF(x) ELECTRONICS INNOVATION