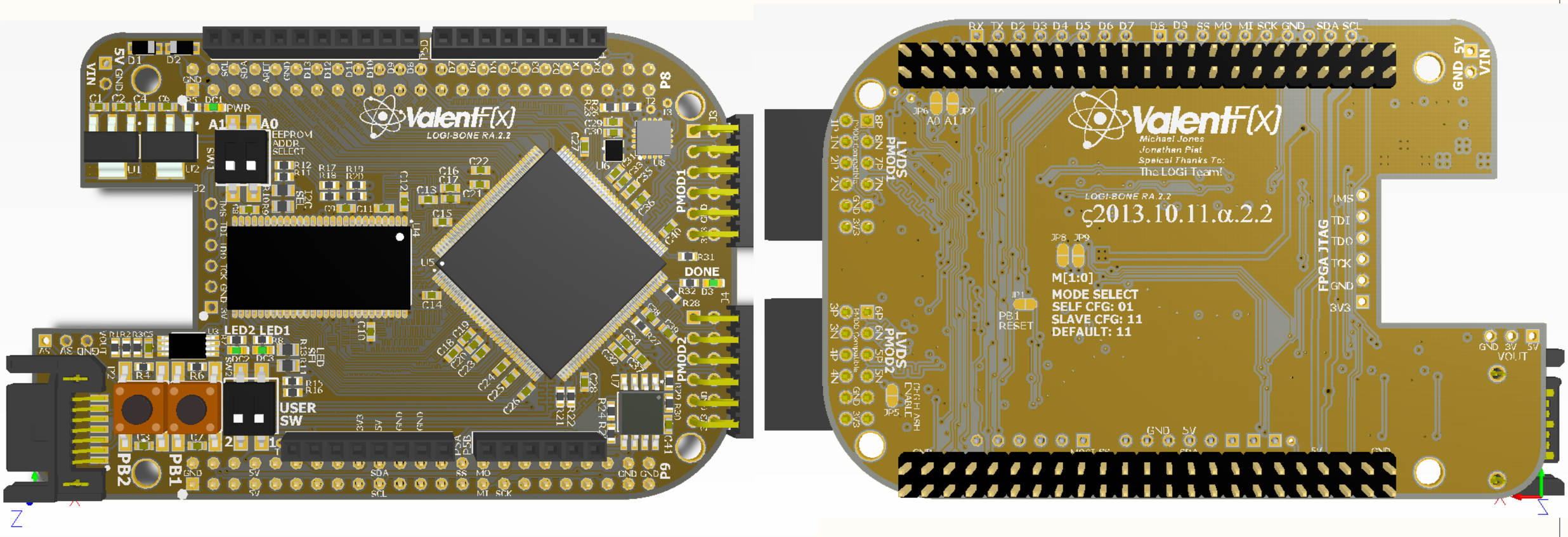


U_RAM
RAM.SchDoc

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

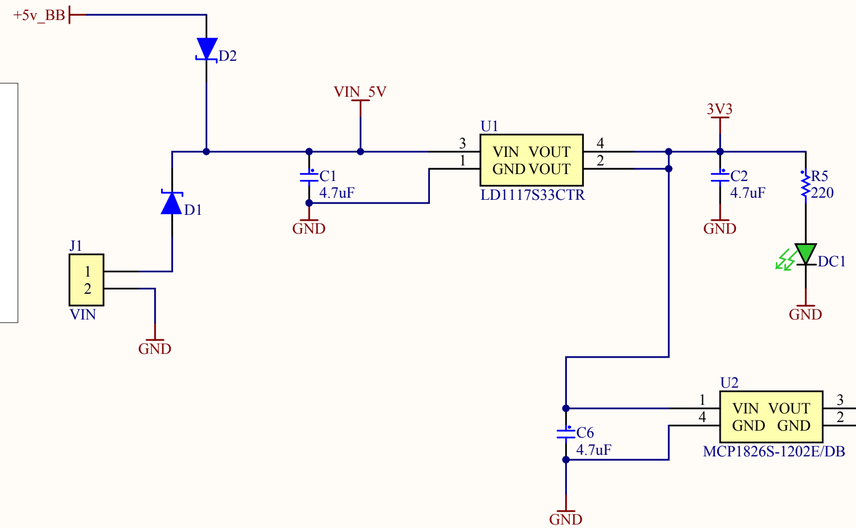
U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

Title	LOGi-Bone Top Level		
Revision:	RA2.2	Sheet	1 of 7
Date:	1/27/2014	Engineer:	MJones

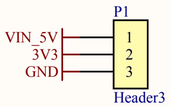
ValentF(X) ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



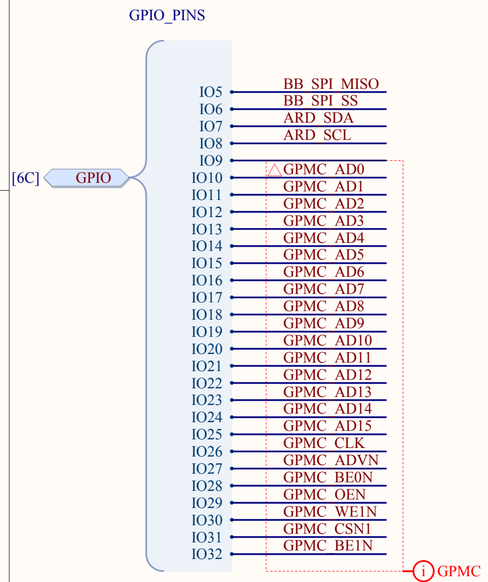
1 x Auxillary Power output Headers

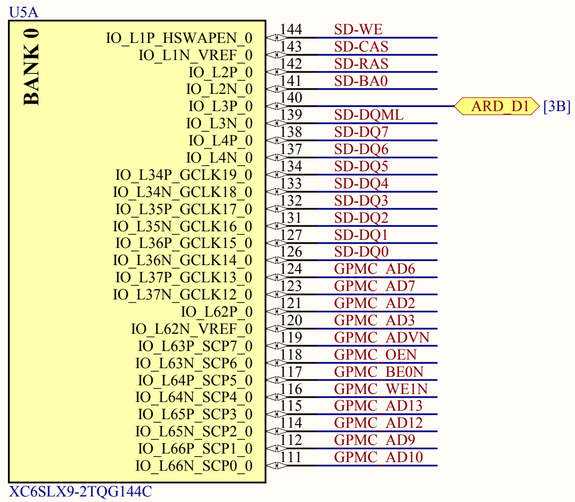


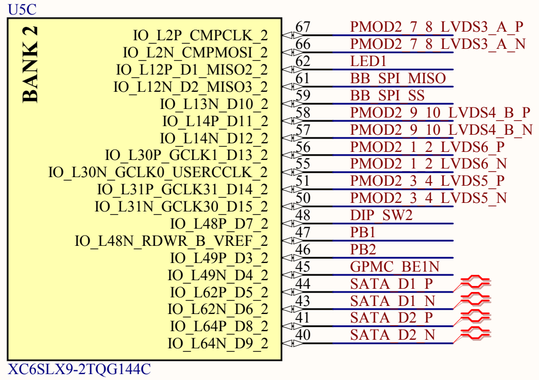
Logo1
Valent Logo 750
Logo2
Valent Logo 1000

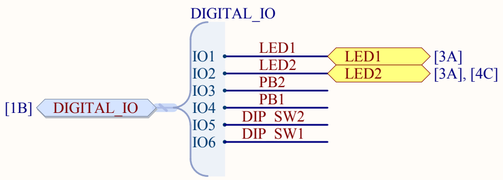
Title	Power Supply		
Revision:	RA2.2	Sheet	1 of 6
Date:	1/27/2014	Engineer:	MJones

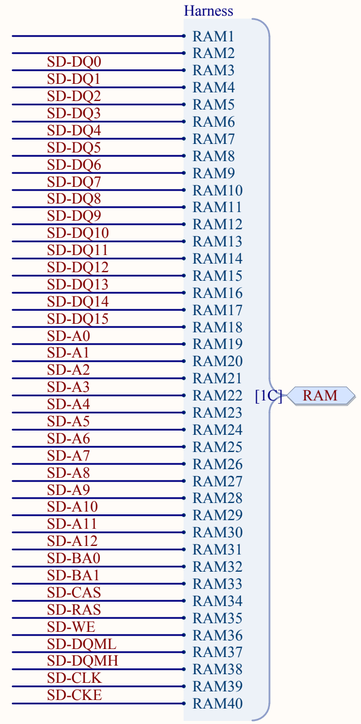
ValentF(X) ELECTRONICS INNOVATION

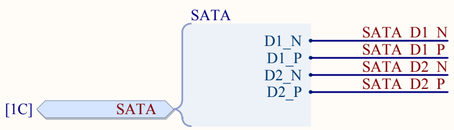


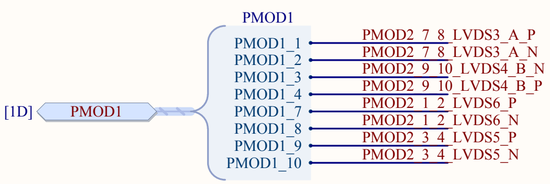


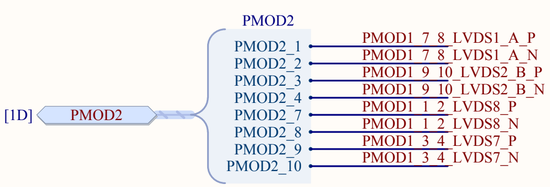


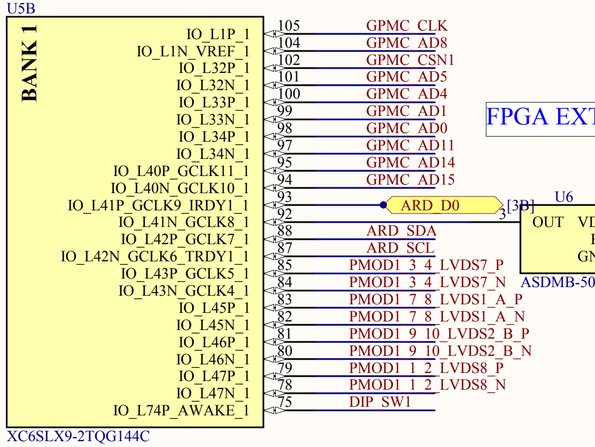




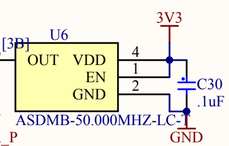


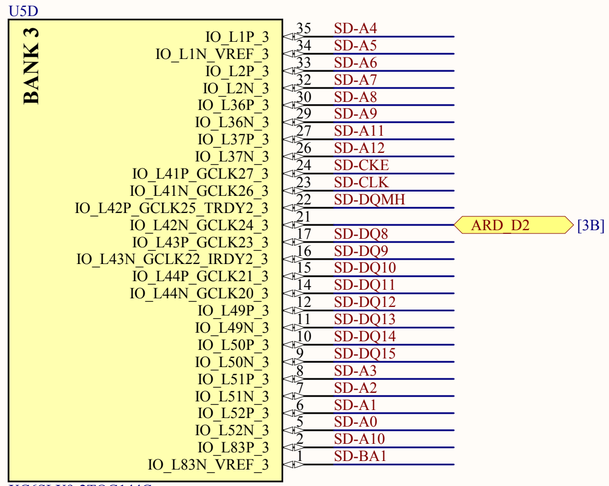






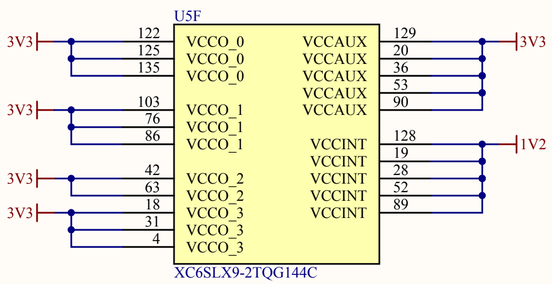
FPGA EXT Oscillator: 50Mhz

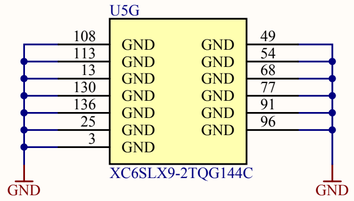


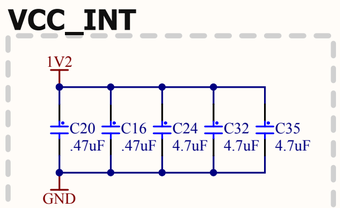


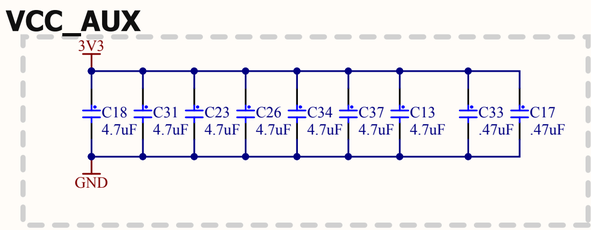
Title	FPGA Logic		
Revision:	RA2.2	Sheet	2 of 6
Date:	1/27/2014	Engineer:	MJones

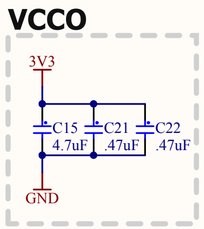
ValentF(x) ELECTRONICS INNOVATION

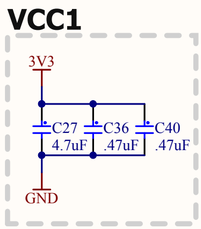


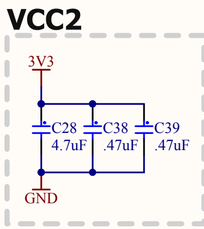


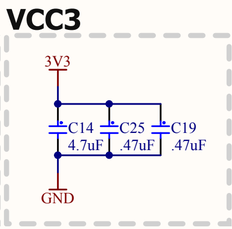




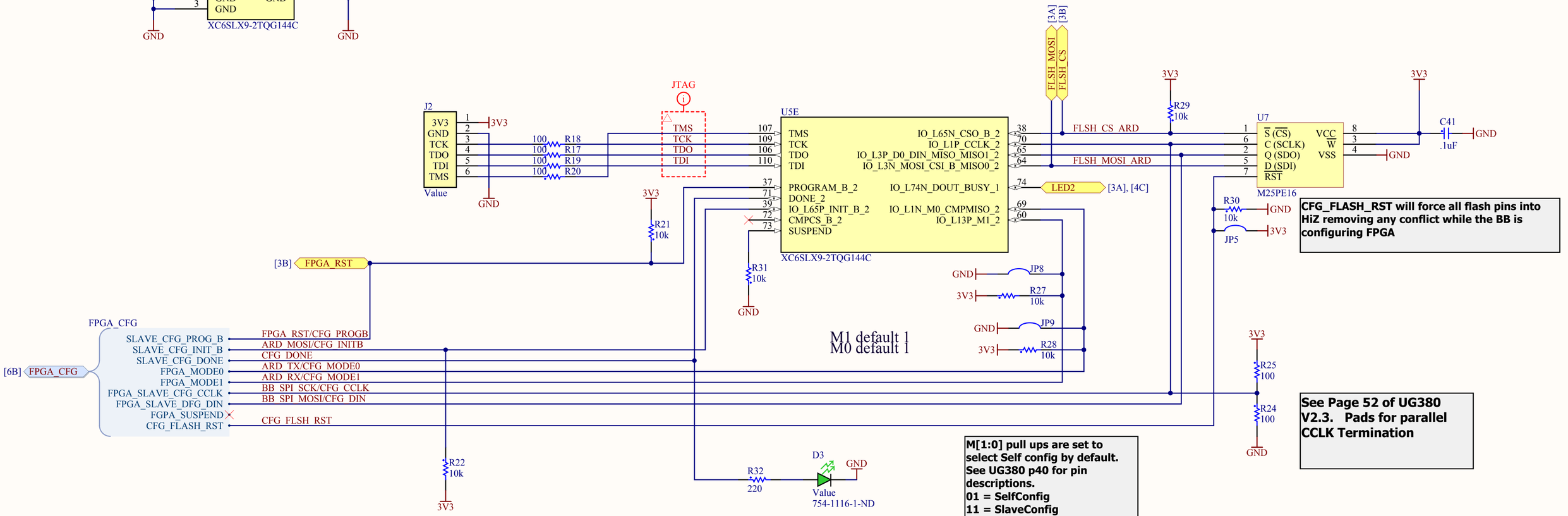








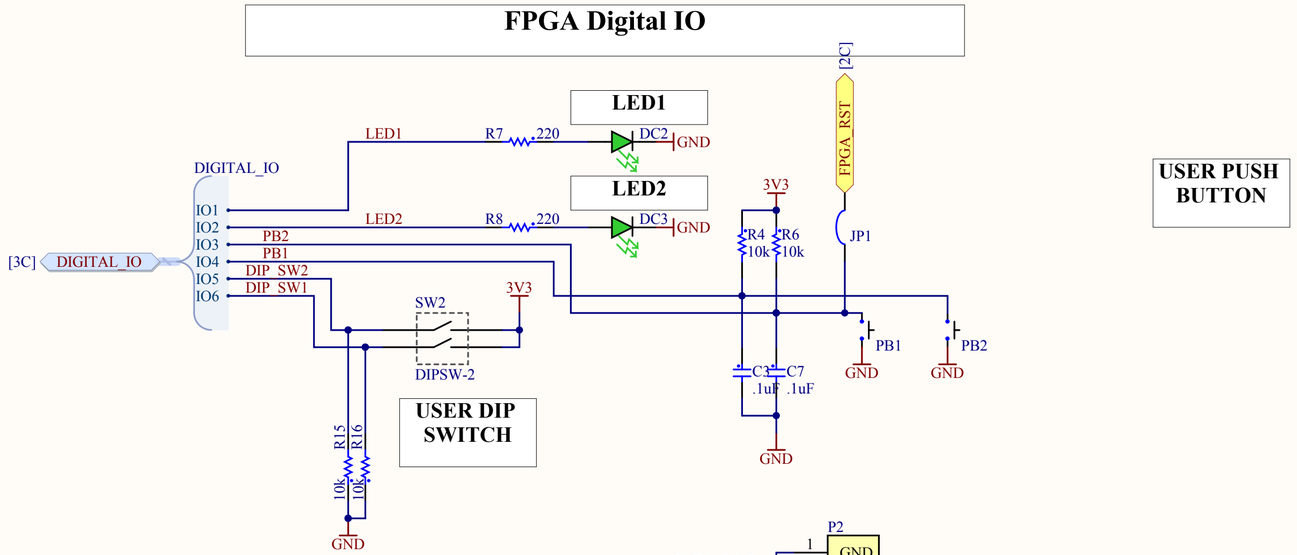
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

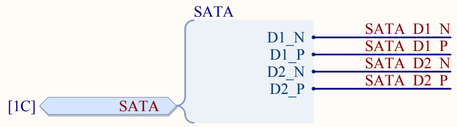


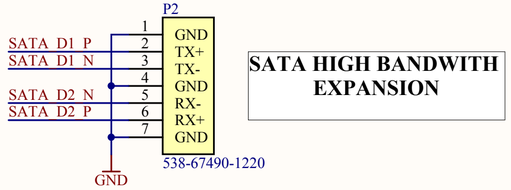
Title	FPGA Configuration		
Revision:	RA2.2	Sheet	3 of 6
Date:	1/27/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

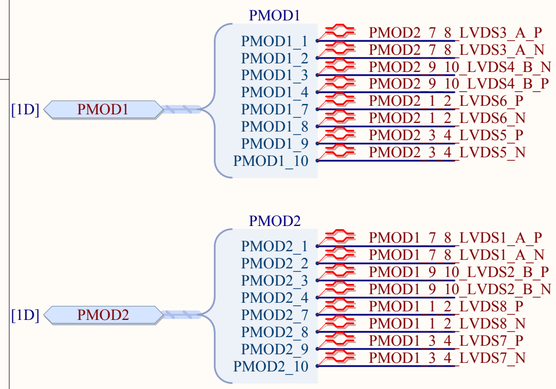
FPGA Digital IO



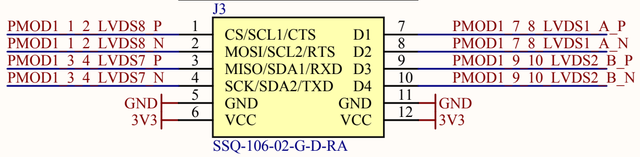




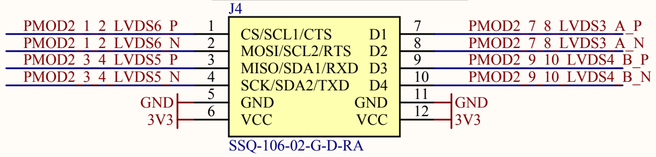
SATA HIGH BANDWITH EXPANSION



PMOD1 PORT



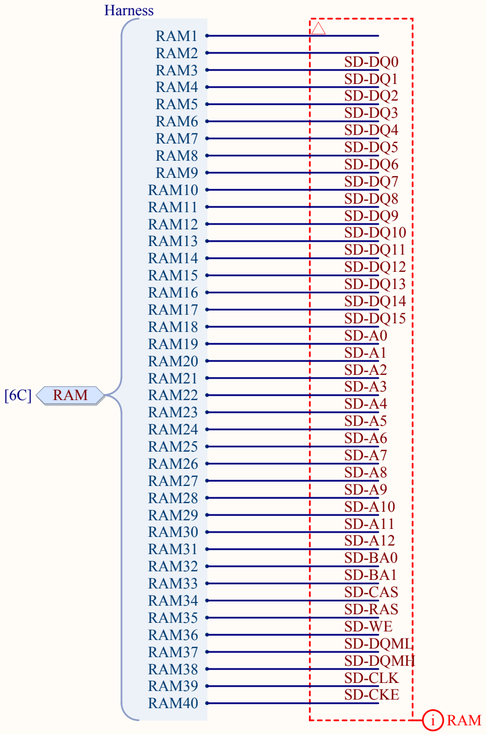
PMOD2 PORT

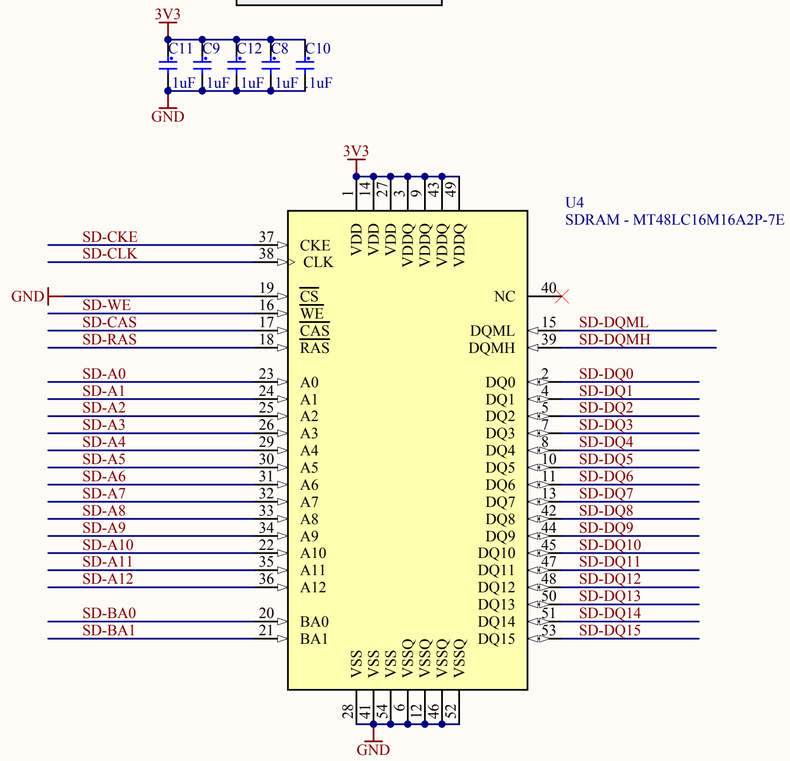


Title	Digital IO		
Revision:	RA2.2	Sheet	4 of 6
Date:	1/27/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

SDRAM

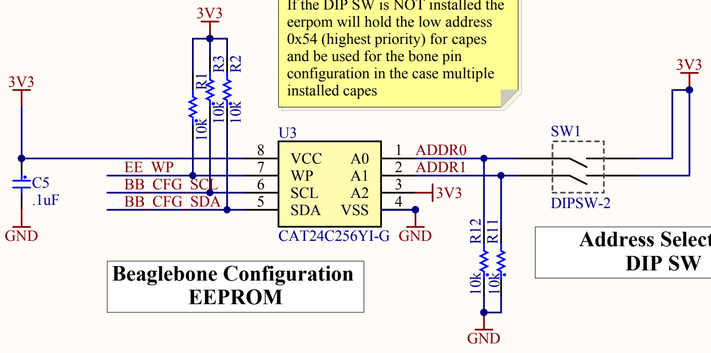




Title	RAM		
Revision:	RA2.2	Sheet	5 of 6
Date:	1/27/2014	Engineer:	MJones

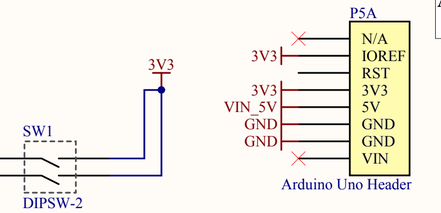
ValentF(X) ELECTRONICS INNOVATION

Beaglebone Configuration EEPROM

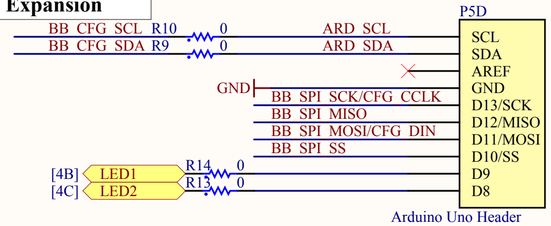


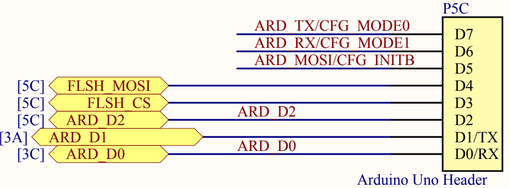
If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed capes

Address Selection DIP SW

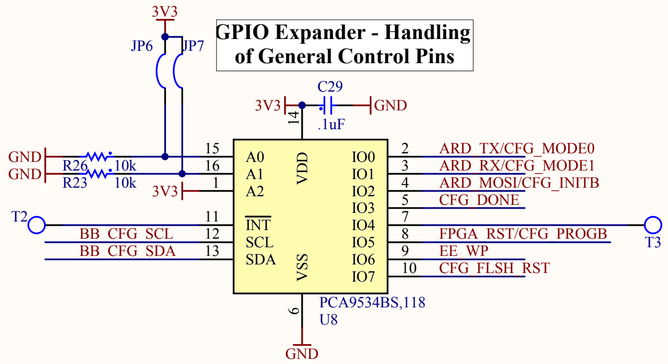


Arduino Header - Arduino Shield Expansion

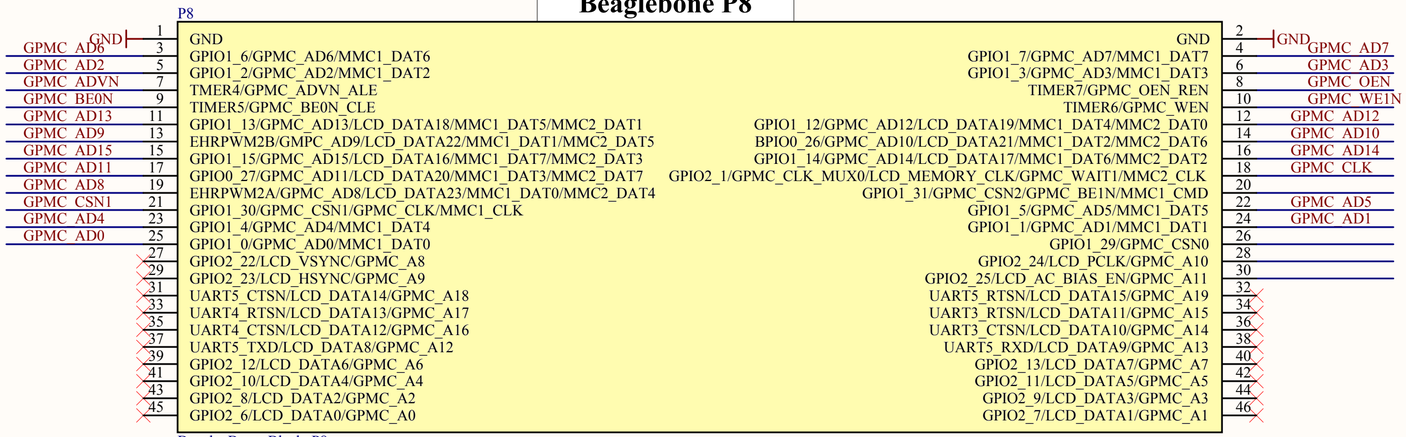




GPIO Expander - Handling of General Control Pins

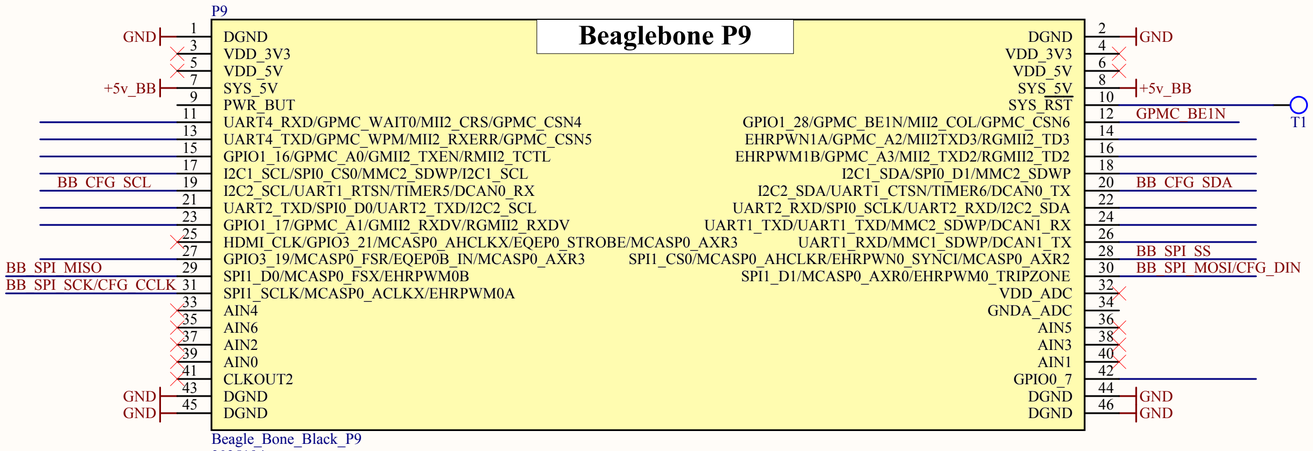


Beaglebone P8

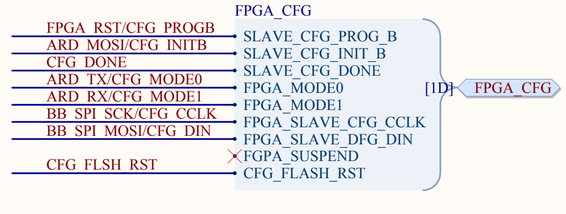


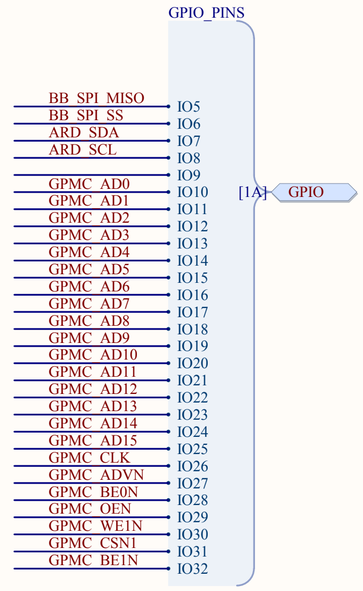
Beagle_Bone_Black_P8
2025194

Beaglebone P9



Beagle_Bone_Black_P9
2025194





Title	Peripheral Port IO		
Revision:	RA2.2	Sheet	6 of 6
Date:	1/27/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION