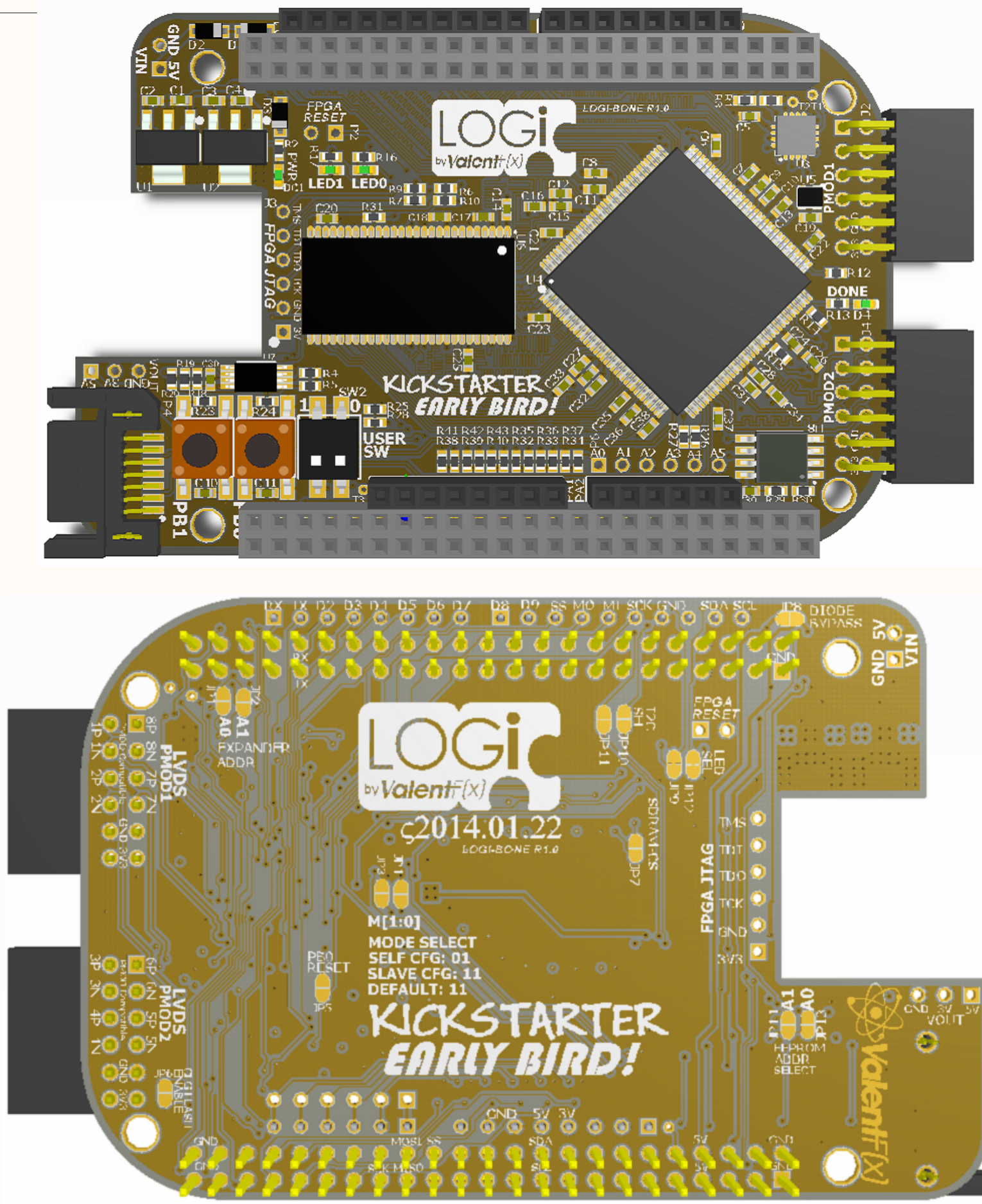


U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

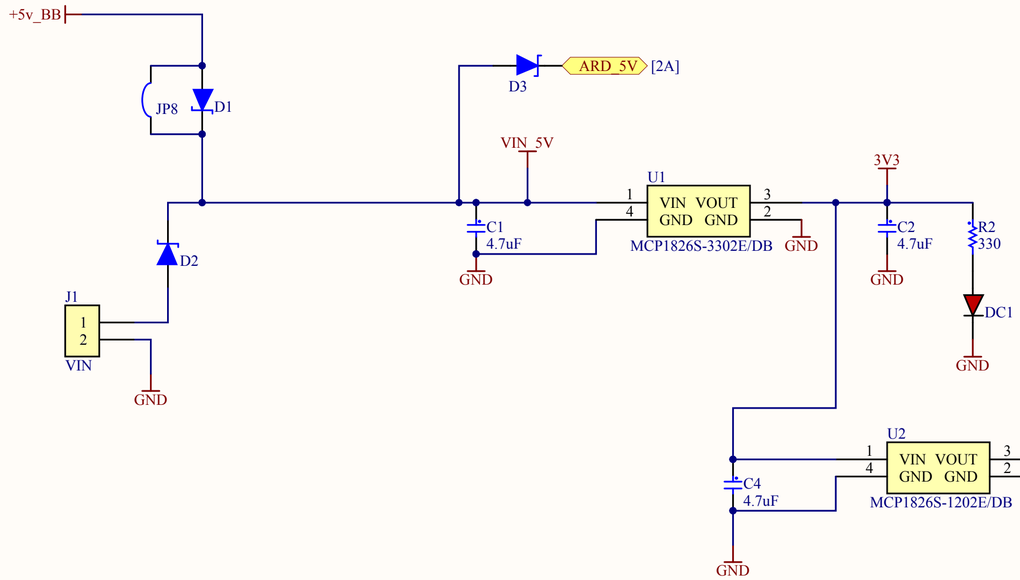
U_DIGITAL_IO
DIGITAL_IO.SchDoc

LOGi-Bone Top Level			
Revision:	R1.0	Sheet	1 of 7
Date:	4/23/2014	Engineer:	MJones

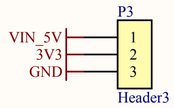
ValentF(X) ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



1 x Auxillary Power output Headers

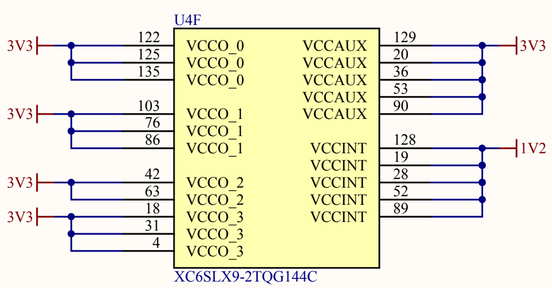


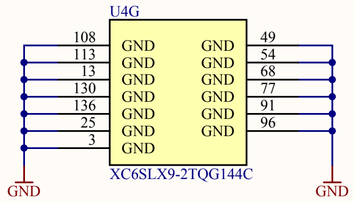
LOGI-LOGO-600
LOGO3

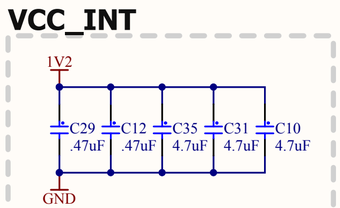
VALENTFX-LOGO-750
Logo5

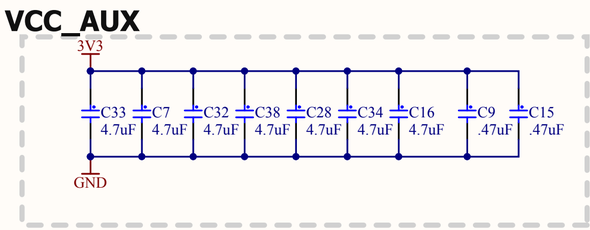
LOGI-LOGO-750
LOGO4

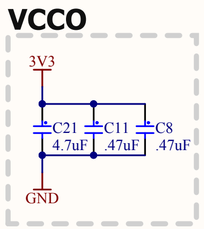
Title	Power Supply		
Revision:	R1.0	Sheet	2 of 7
Date:	4/23/2014	Engineer:	MJones

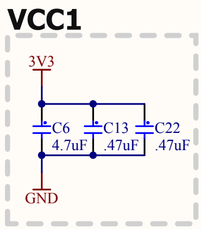


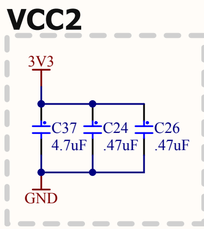


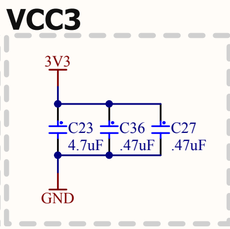




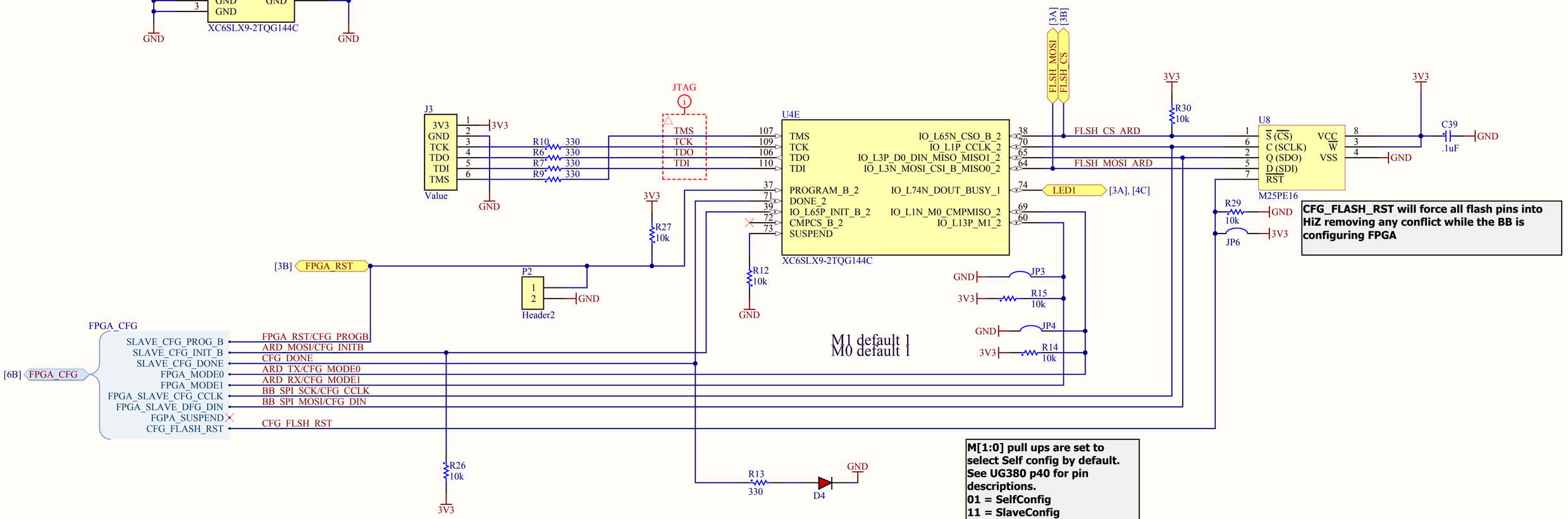






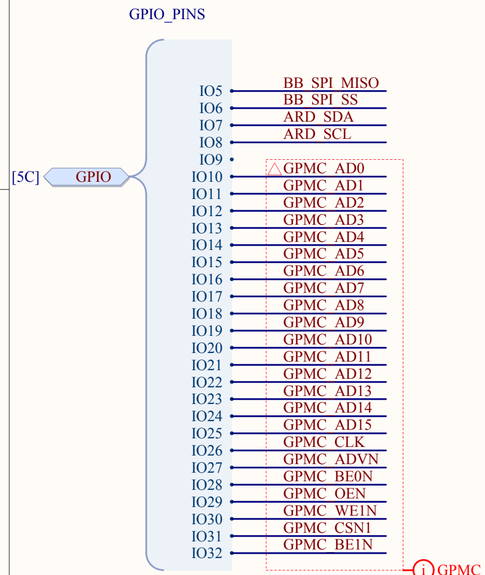


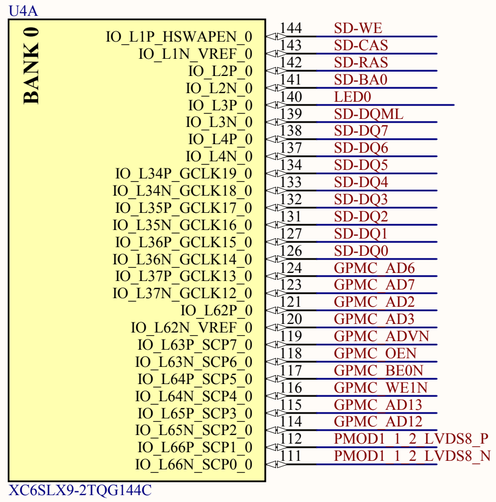
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

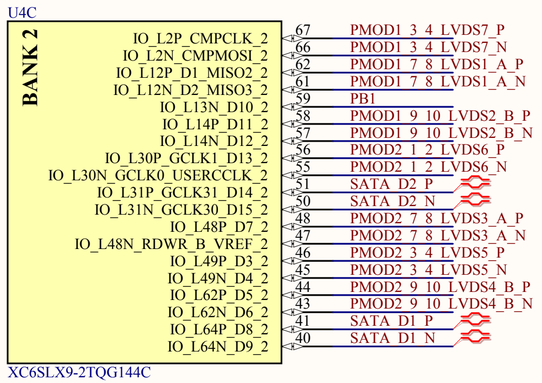


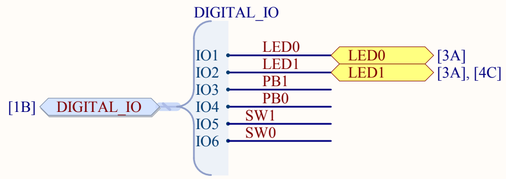
Title	FPGA Configuration		
Revision:	R1.0	Sheet	3 of 7
Date:	4/23/2014	Engineer:	MJones

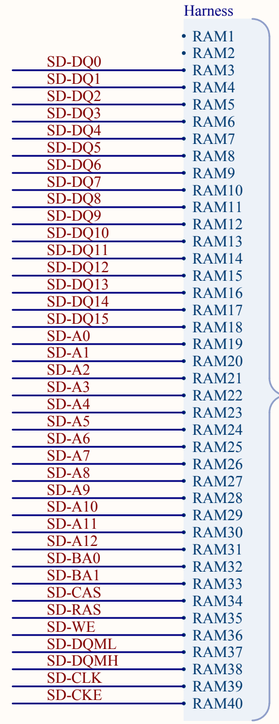
ValentF(X) ELECTRONICS INNOVATION

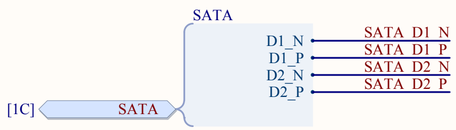


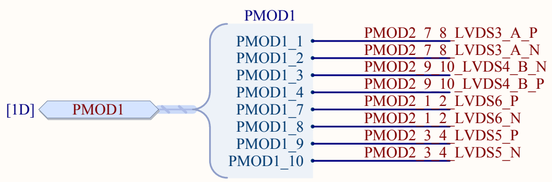


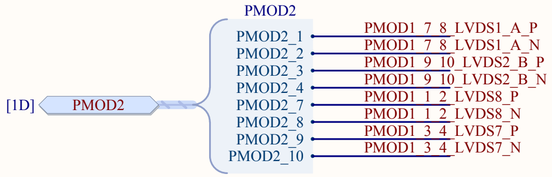


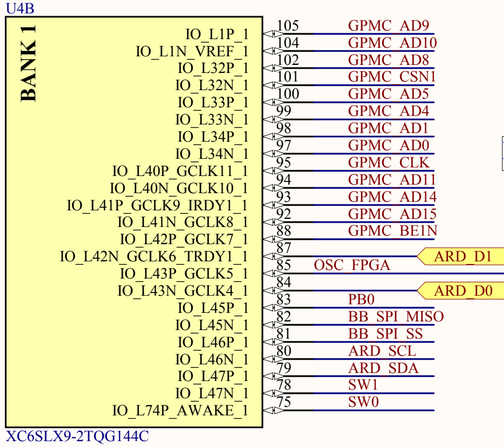




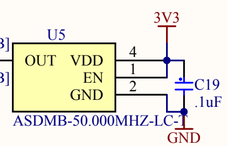


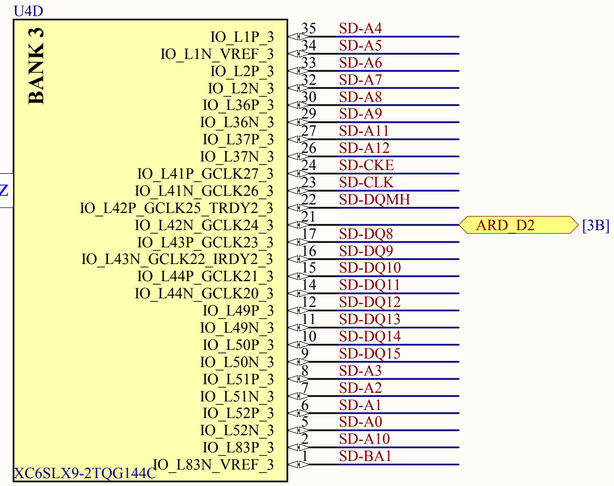






FPGA EXT Oscillator: 50Mhz

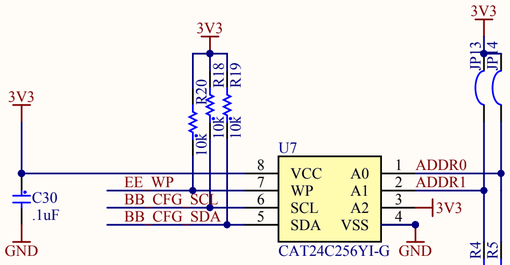




Title	FPGA Logic		
Revision:	R1.0	Sheet	4 of 7
Date:	4/23/2014	Engineer:	MJones

ValentF(x) ELECTRONICS INNOVATION

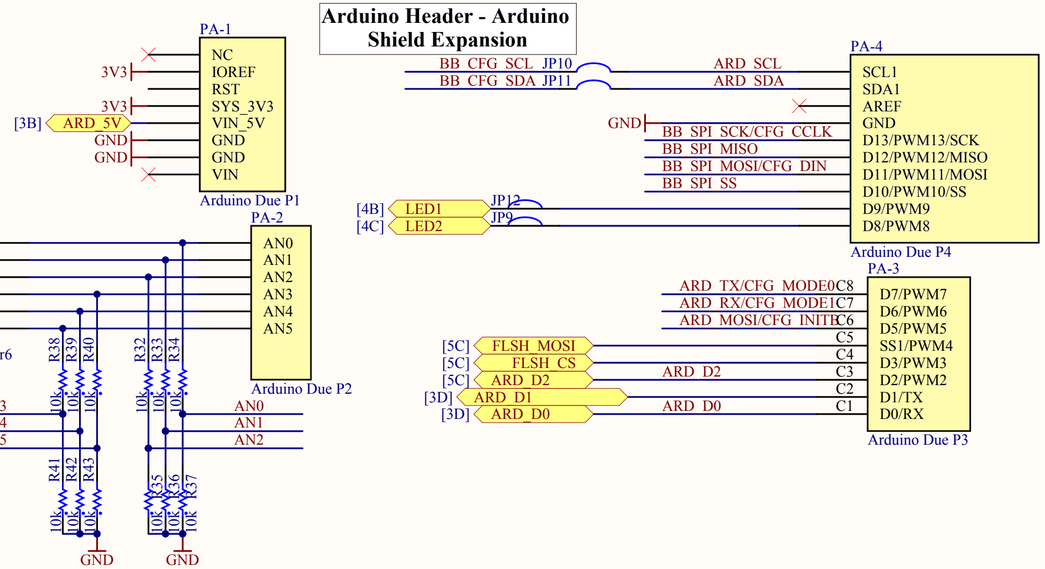
Beaglebone Configuration EEPROM



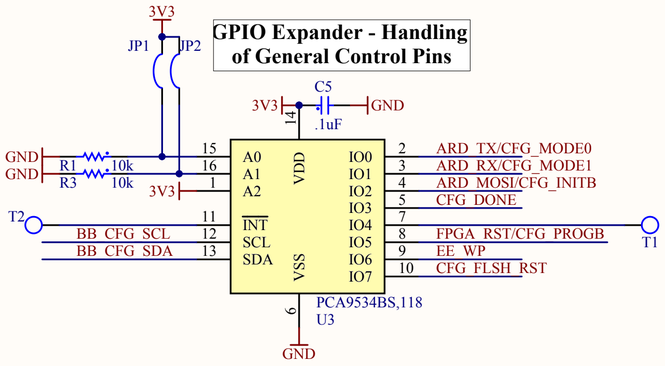
Address Selection DIP SW

If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed of capes

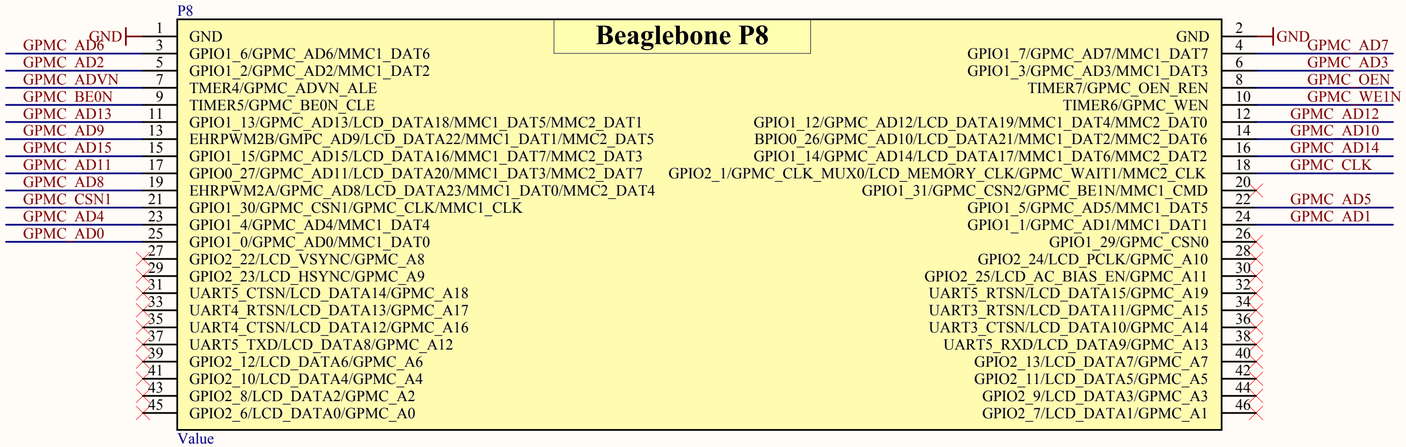
Arduino Header - Arduino Shield Expansion



GPIO Expander - Handling of General Control Pins

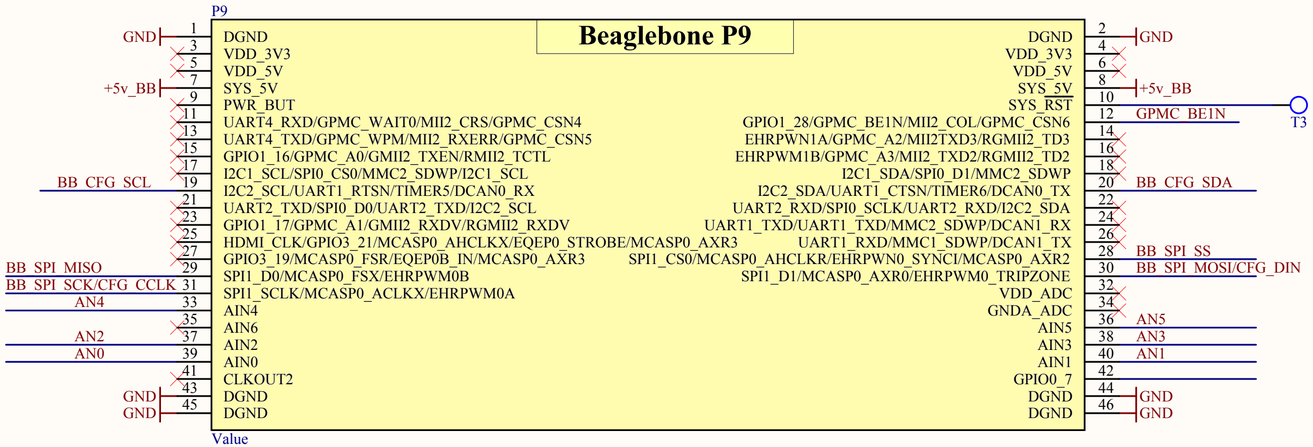


Beaglebone P8

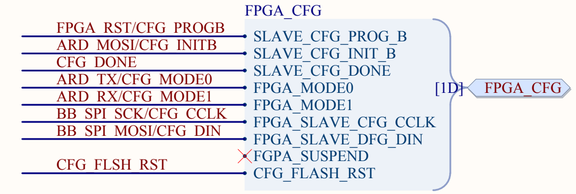


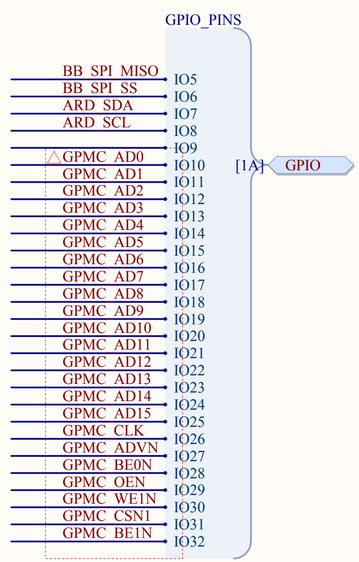
Value
SAM1197-23-ND

Beaglebone P9



Value

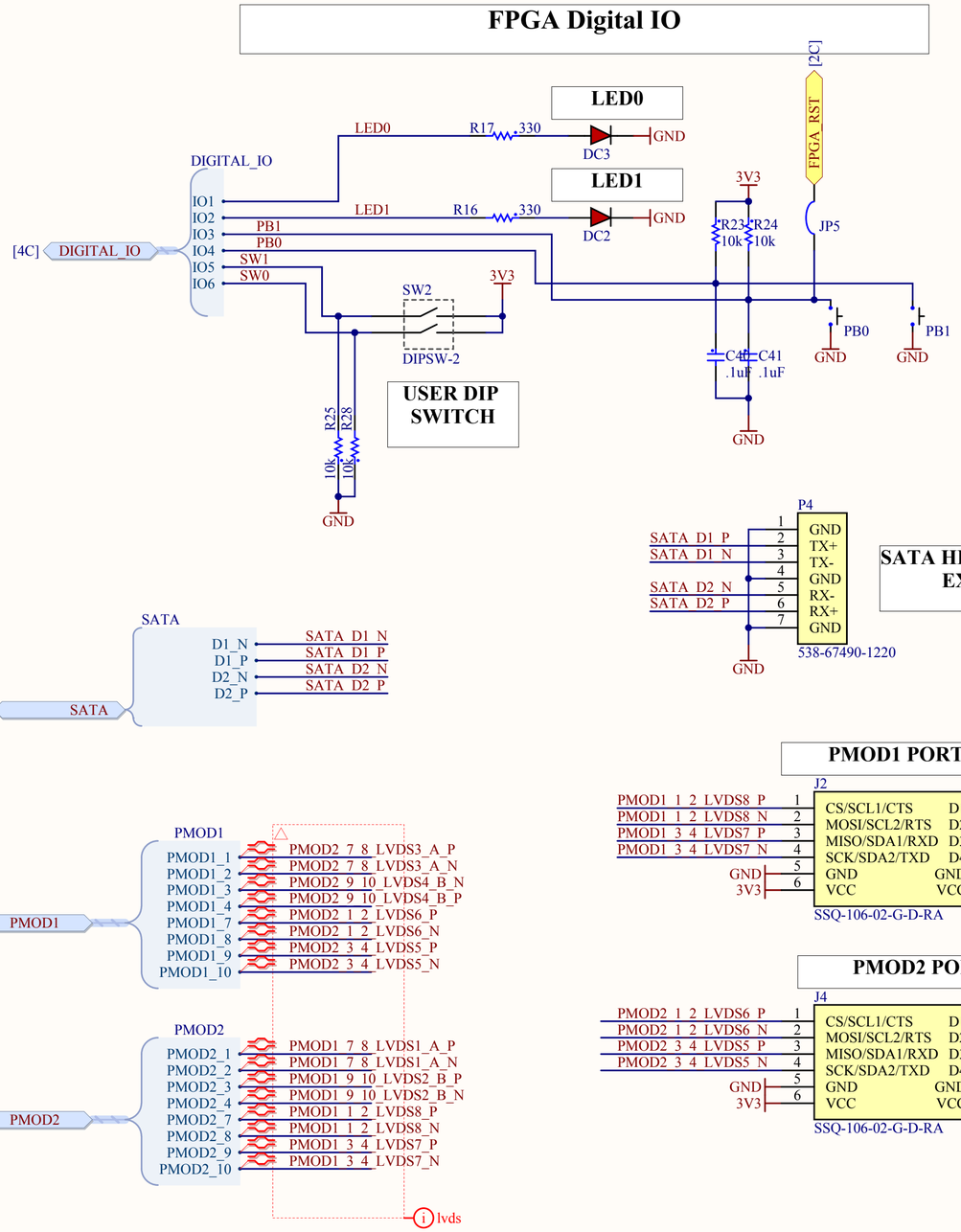




Title	Peripheral Port IO		
Revision:	R1.0	Sheet	5 of 7
Date:	4/23/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

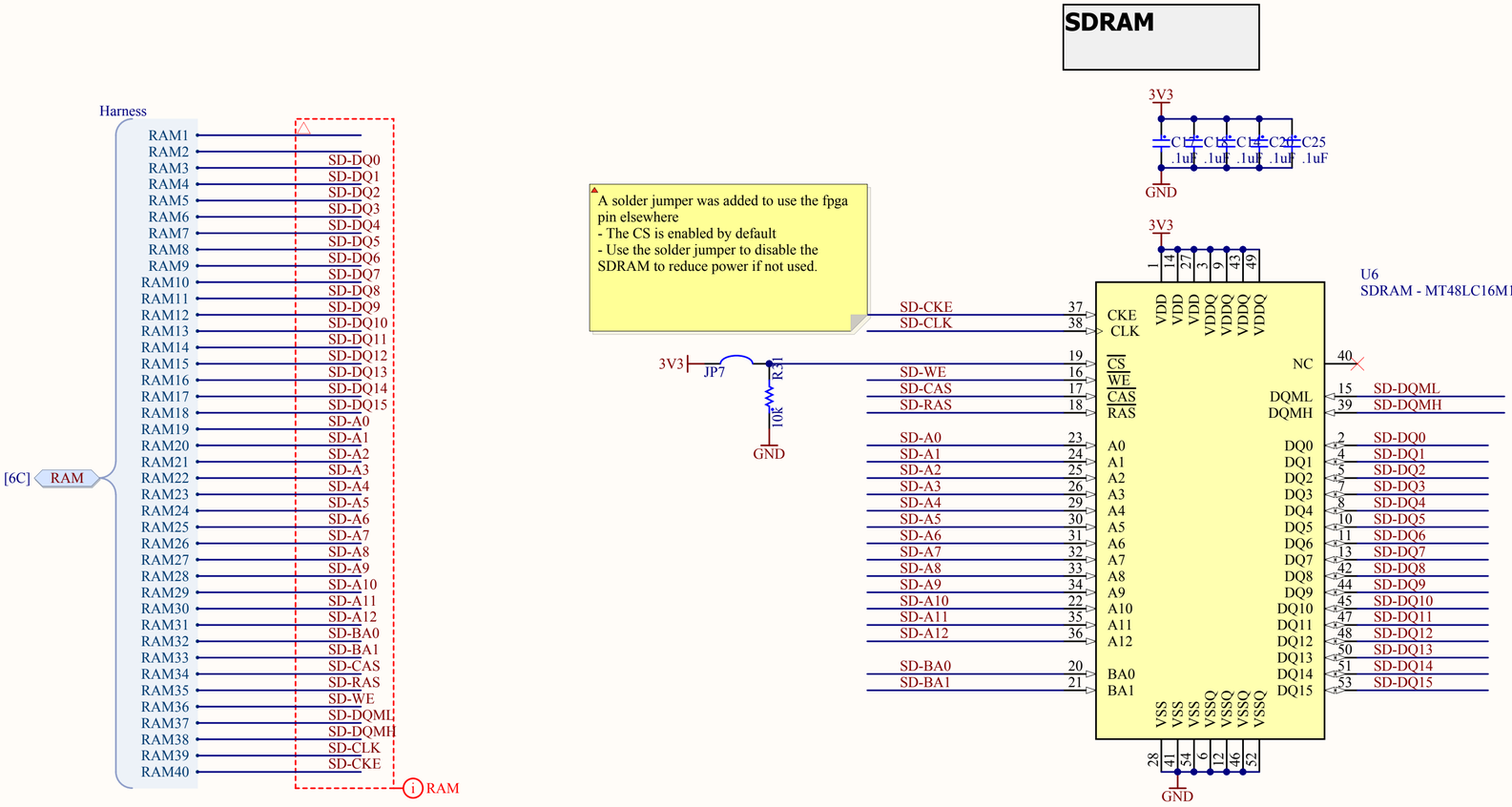
FPGA Digital IO



Title	Digital IO		
Revision:	R1.0	Sheet	6 of 7
Date:	4/23/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

SDRAM



Title	RAM		
Revision:	R1.0	Sheet	7 of 7
Date:	4/23/2014	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION