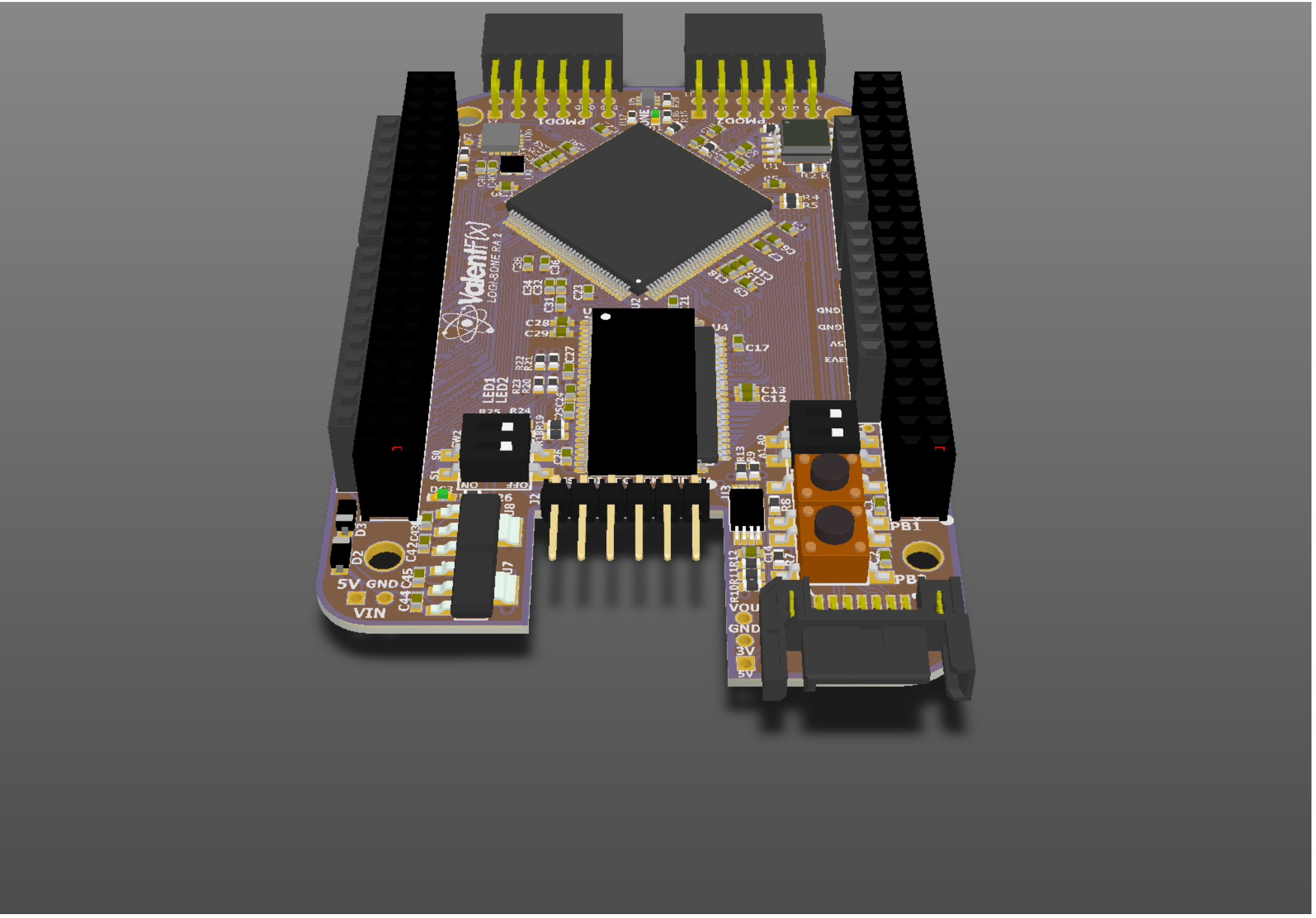
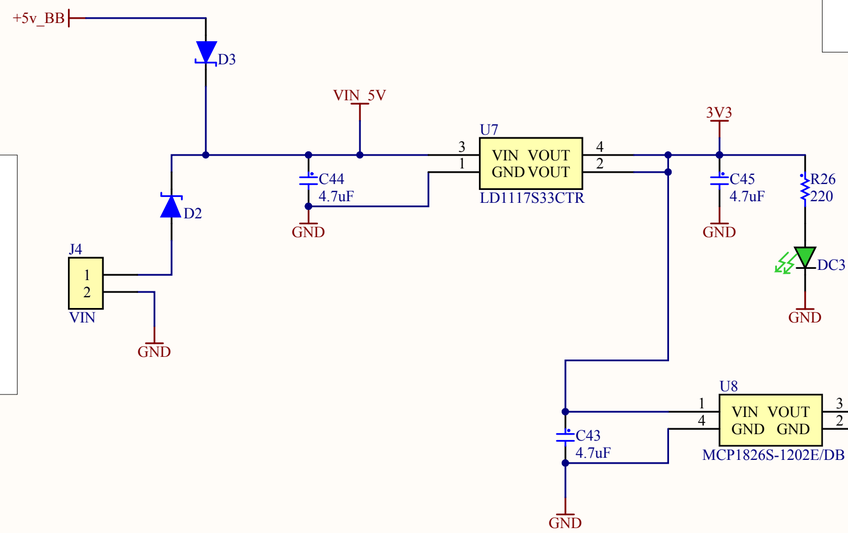
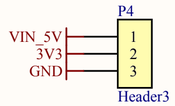

PMOD1
PMOD2
LOGI-BONE RA 2
LED1
LED2
SW2
PB1
5V GND
VIN
GND
3V
5V

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header.



1 x Auxillary Power output Headers

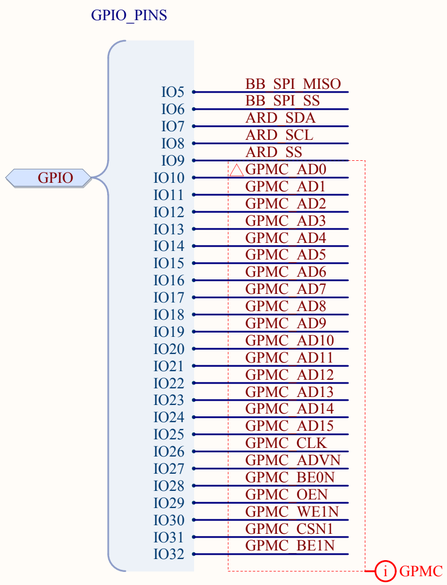


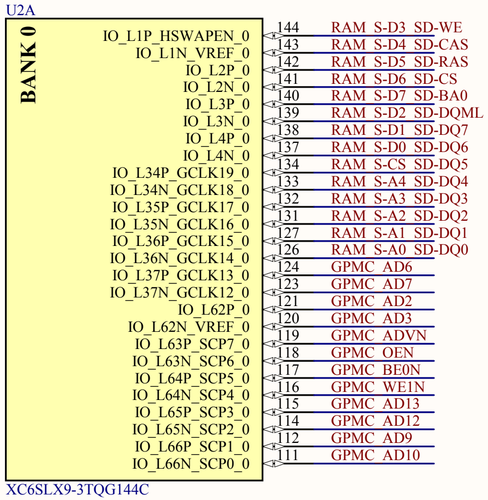
Logo1
Valent Logo 750

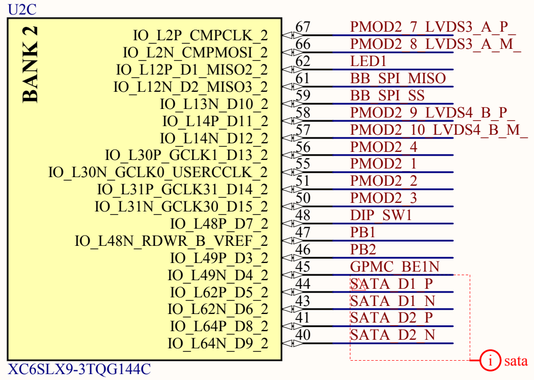
Logo2
Valent Logo 1000

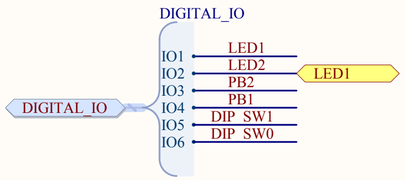
Title	Power Supply		
Revision:	RA.1	Sheet	1 of 6
Date:	7/25/2013	Engineer:	M. Jones

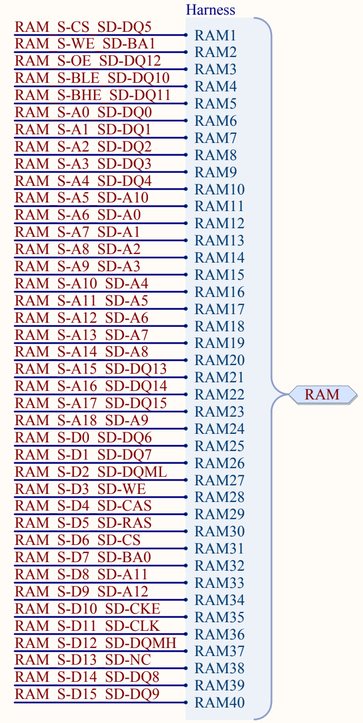
ValentF(X)
FLECTRONICS INNOVATION

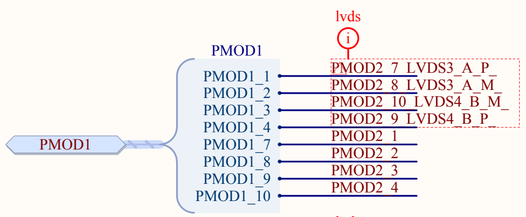


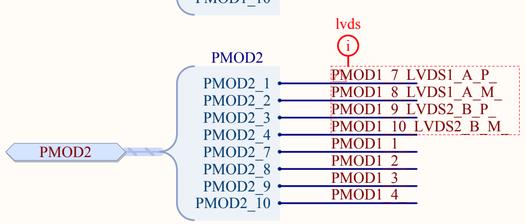


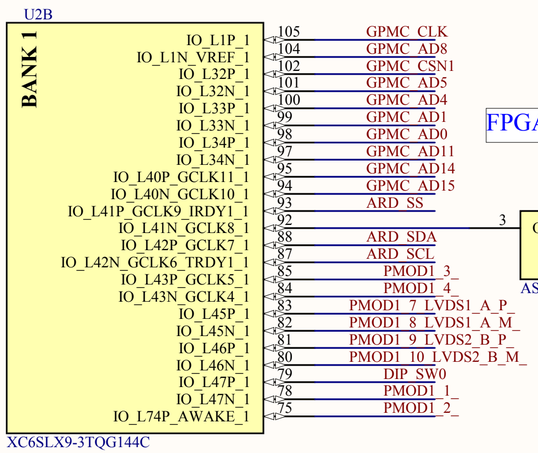




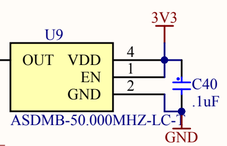


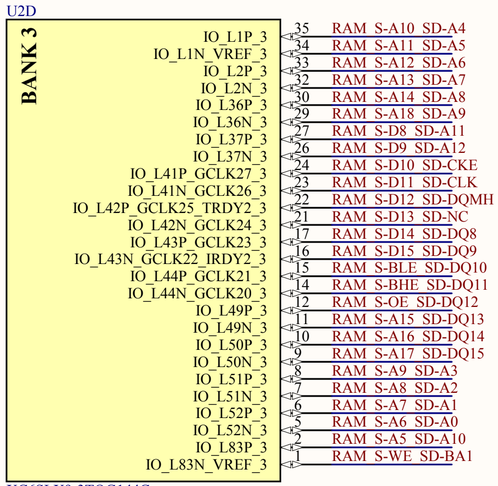






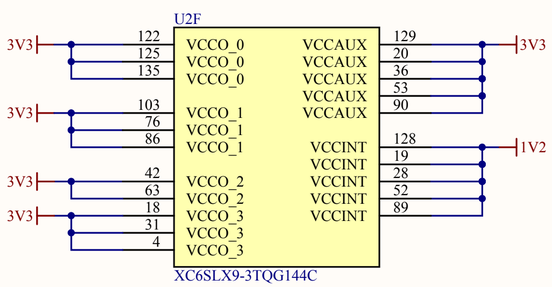
FPGA EXT Oscillator: 50Mhz

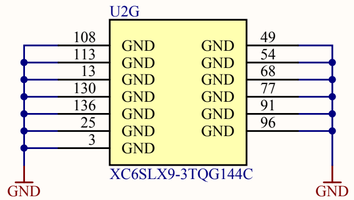


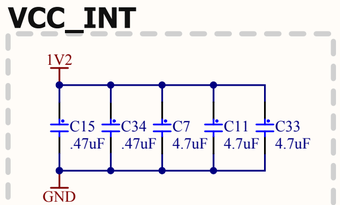


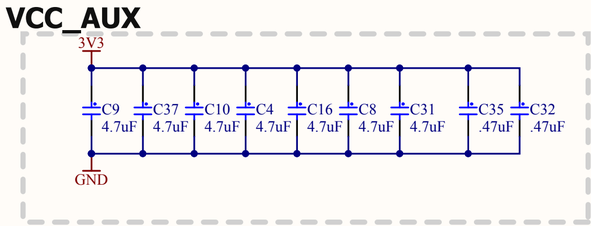
Title	FPGA Logic		
Revision:	RA.1	Sheet	2 of 6
Date:	7/25/2013	Engineer:	M. Jones

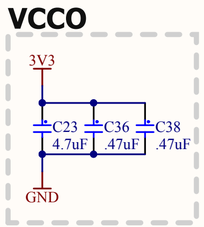
ValentF(X) ELECTRONICS INNOVATION

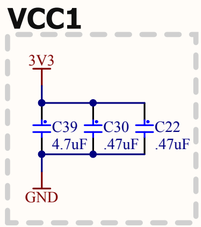


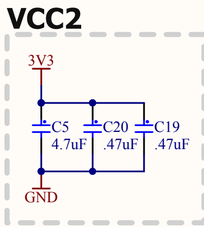


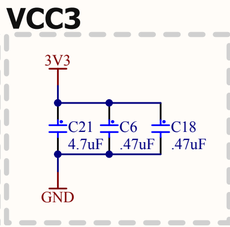




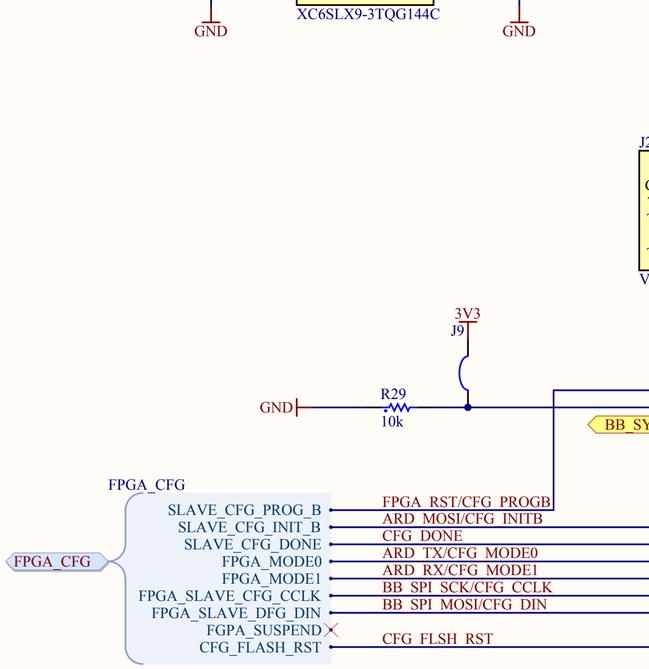








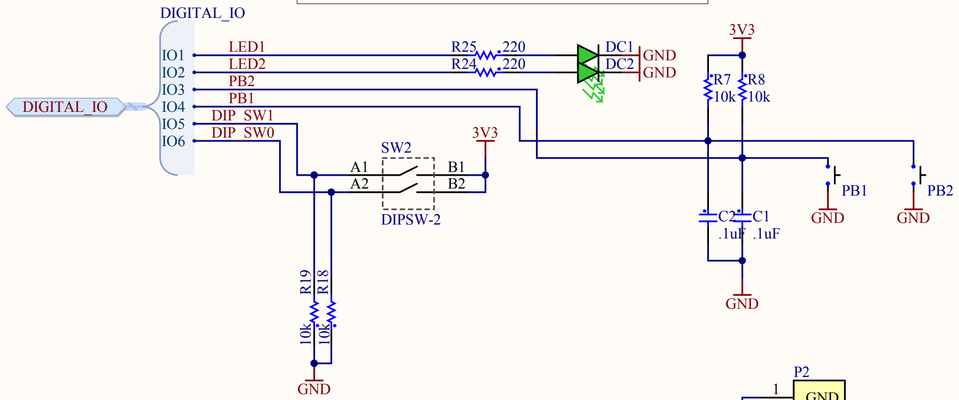
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

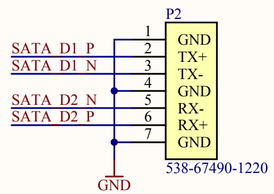


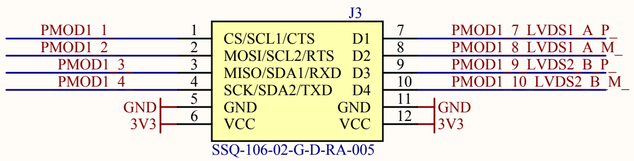
Title	FPGA Configuration		
Revision:	RA.1	Sheet	3 of 6
Date:	7/25/2013	Engineer:	M. Jones

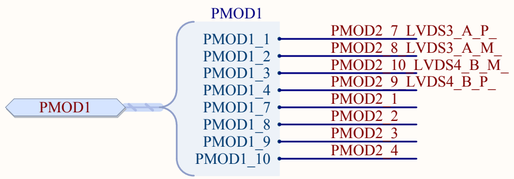
ValentF(x) ELECTRONICS INNOVATION

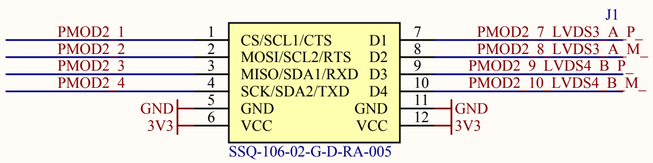
FPGA IO

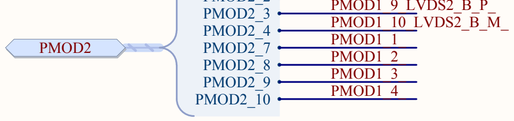






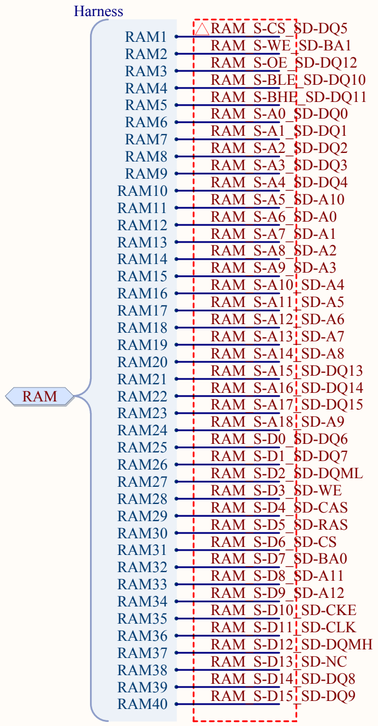




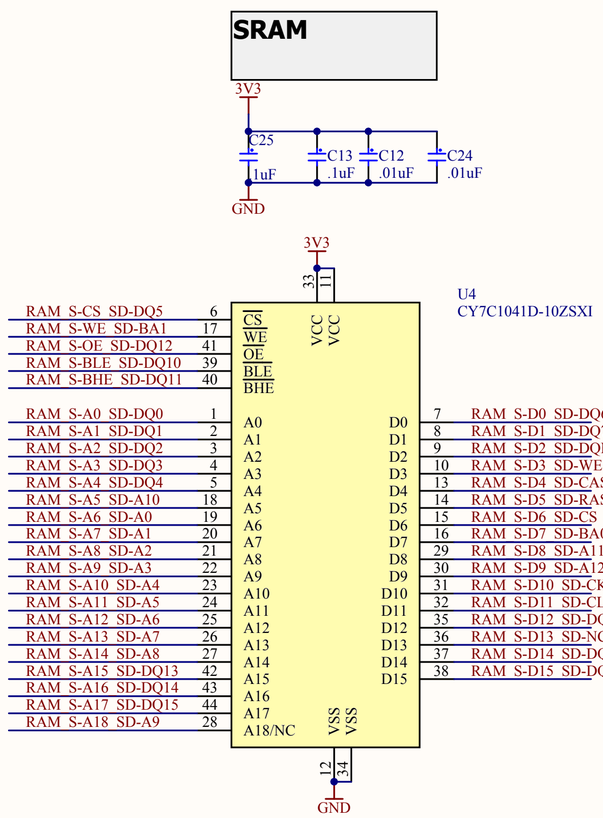


Title	Digital IO		
Revision:	RA.1	Sheet	4 of 6
Date:	7/25/2013	Engineer:	M. Jones

ValentF(X) ELECTRONICS INNOVATION



SRAM



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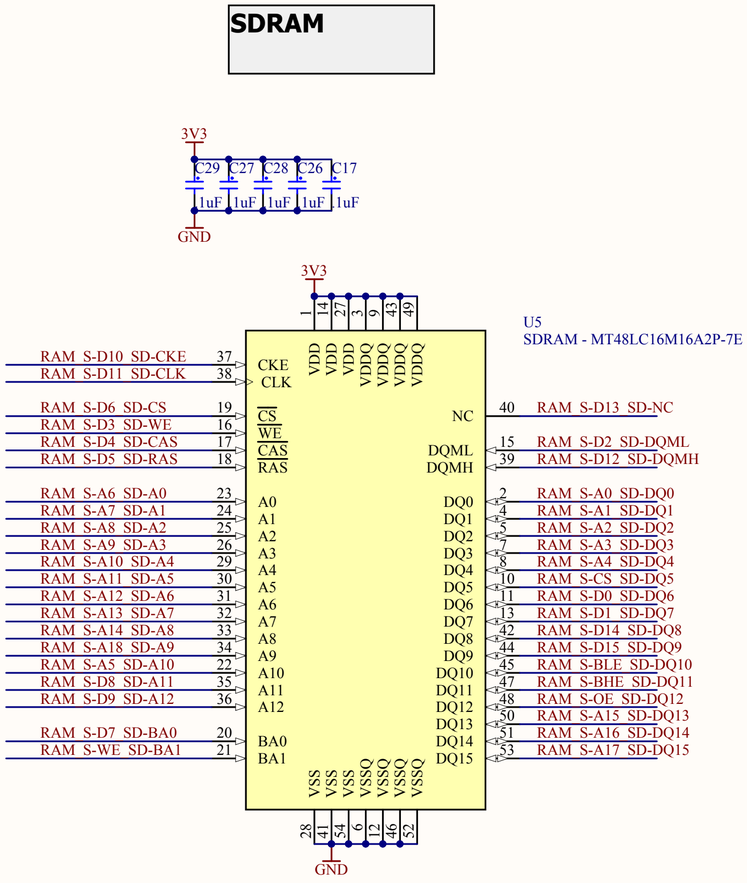
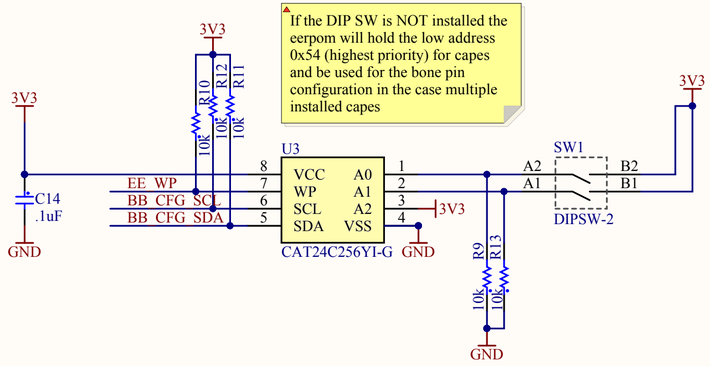
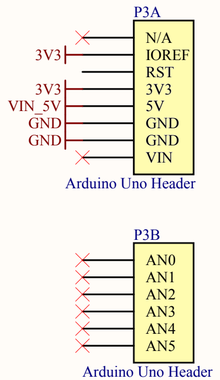


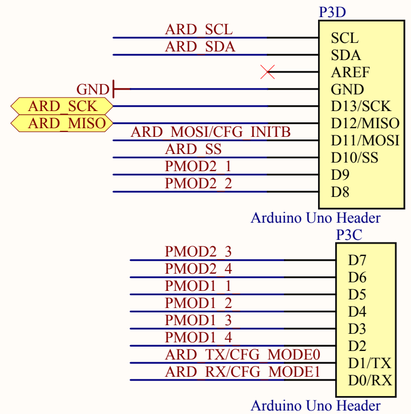
Title	RAM		
Revision:	*	Sheet	5 of 6
Date:	7/25/2013	Engineer:	MJones

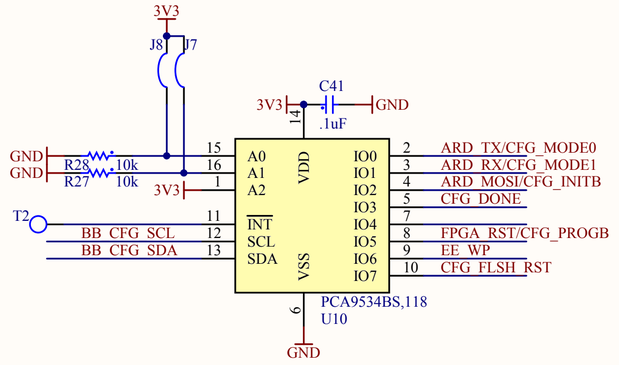
ValentF(X) ELECTRONICS INNOVATION

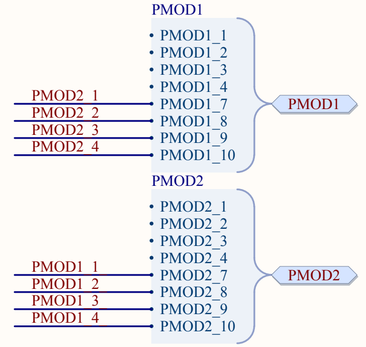
If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed capes



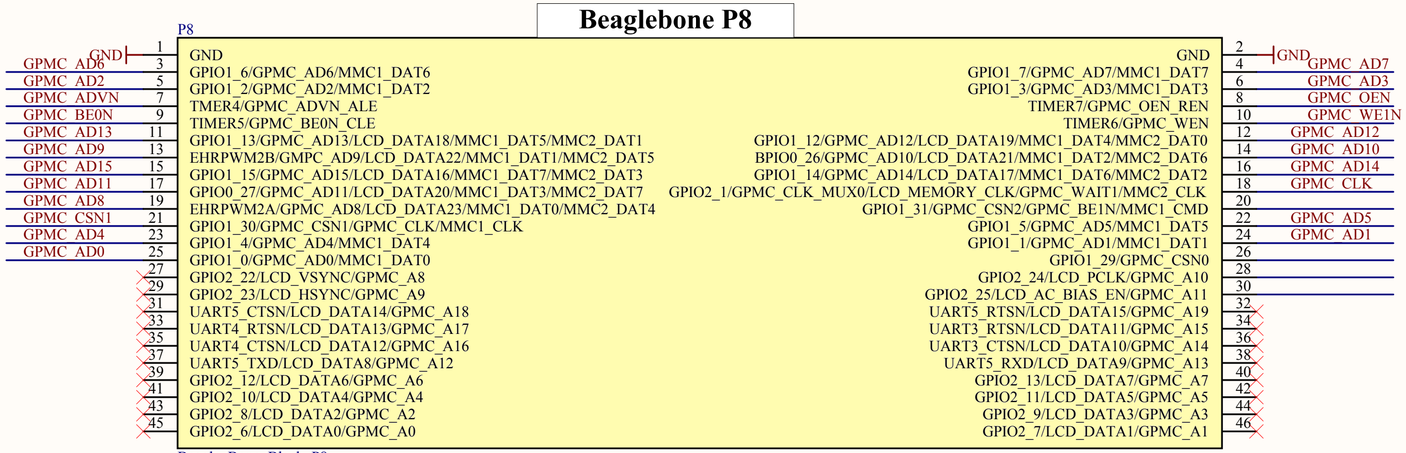




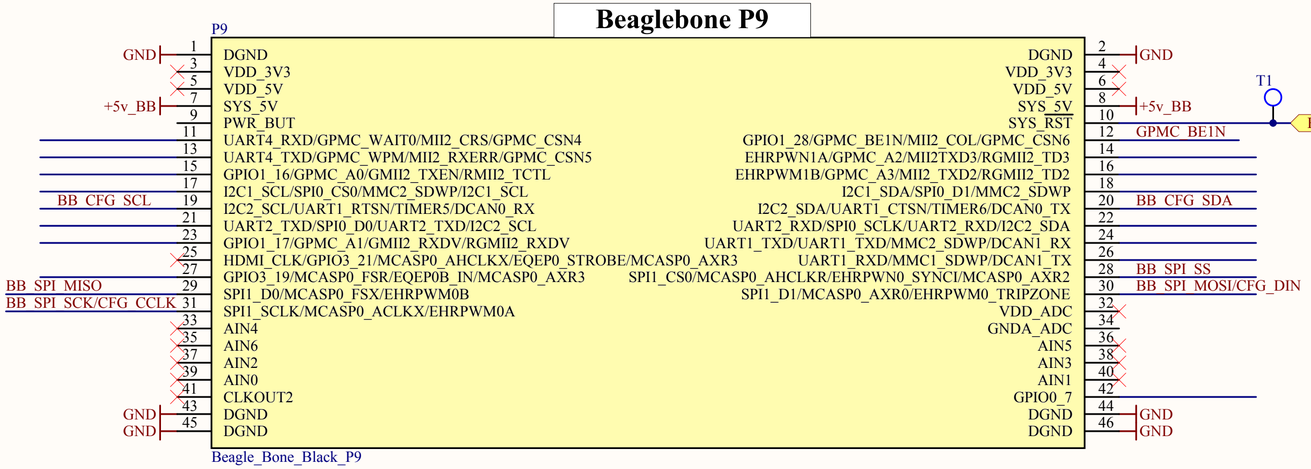


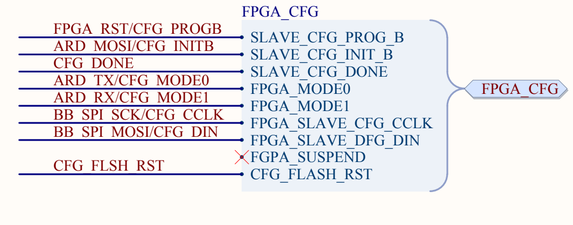


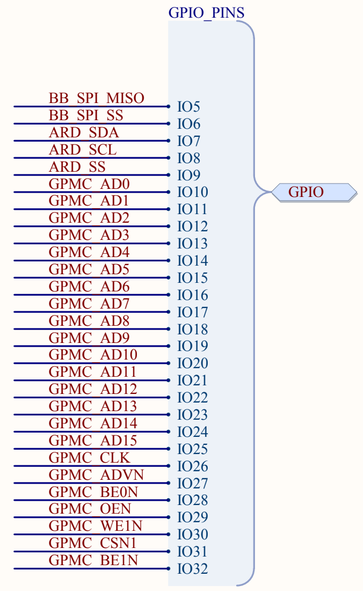
Beaglebone P8



Beaglebone P9







Title	Peripheral Port IO		
Revision:	RA.1	Sheet	6 of 6
Date:	7/25/2013	Engineer:	M. Jones

ValentF(X) ELECTRONICS INNOVATION