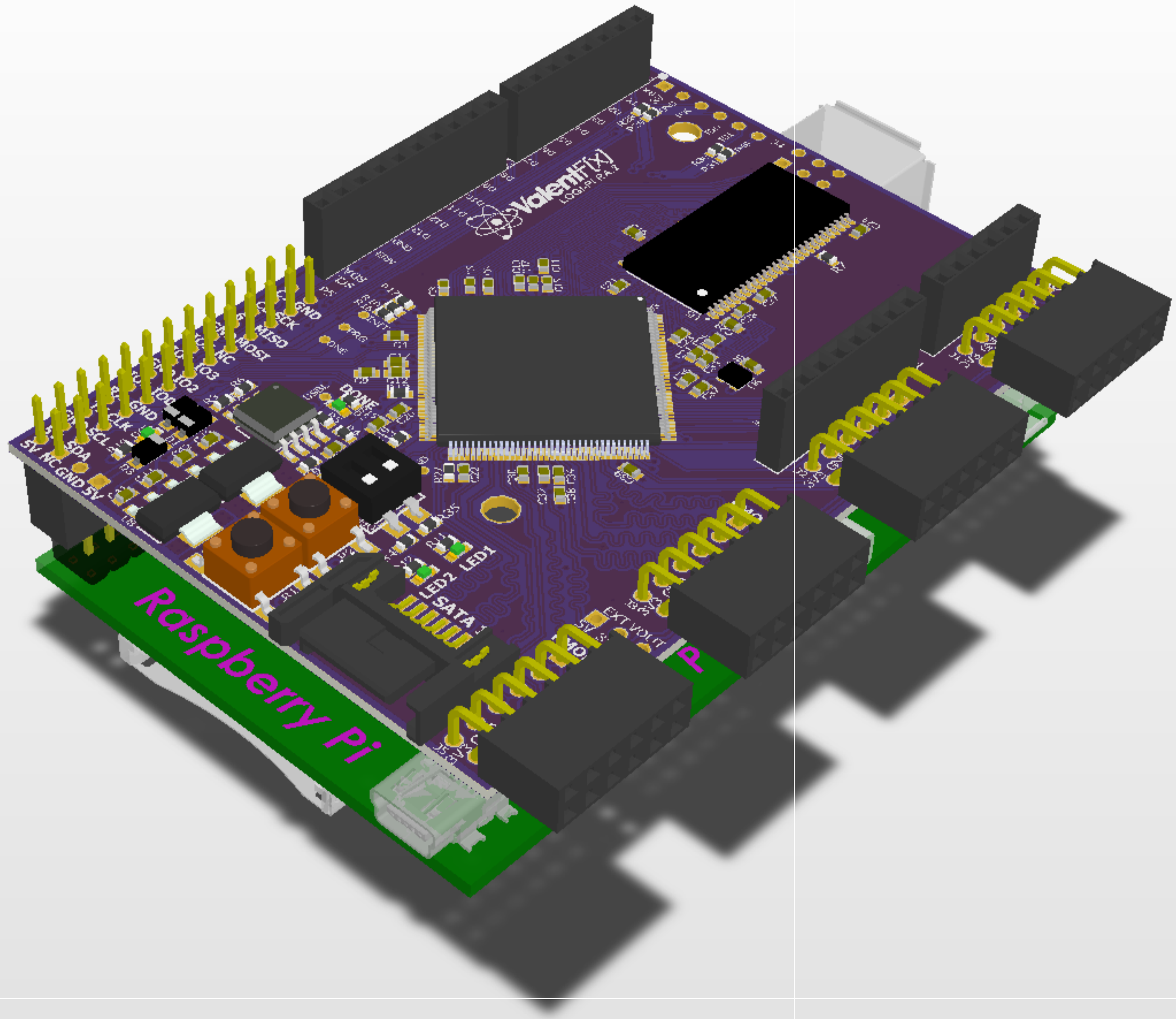
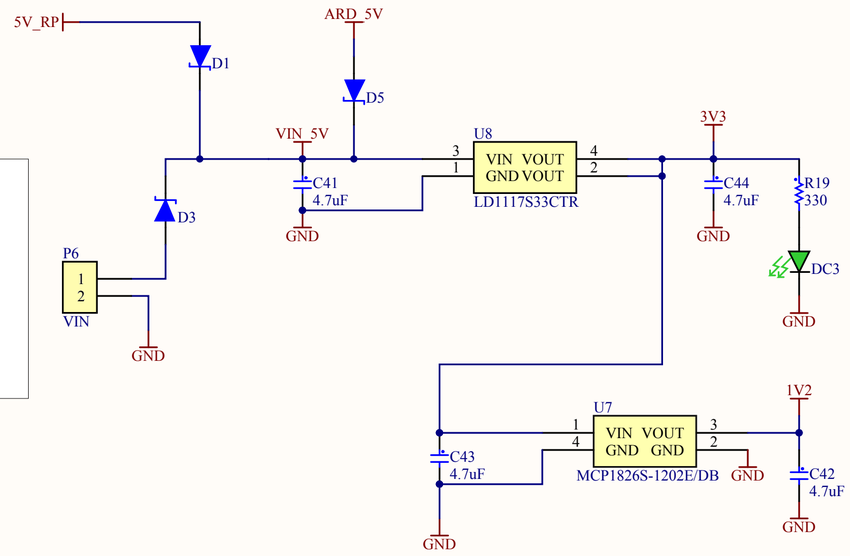
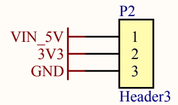

ValentF(x)
Raspberry Pi
LED1
LED2
SATA_1
DONE

Power: By Default Power will be supplied by the .
Raspberry Pi
Optionally power can be supplied through FPGA VIN header.



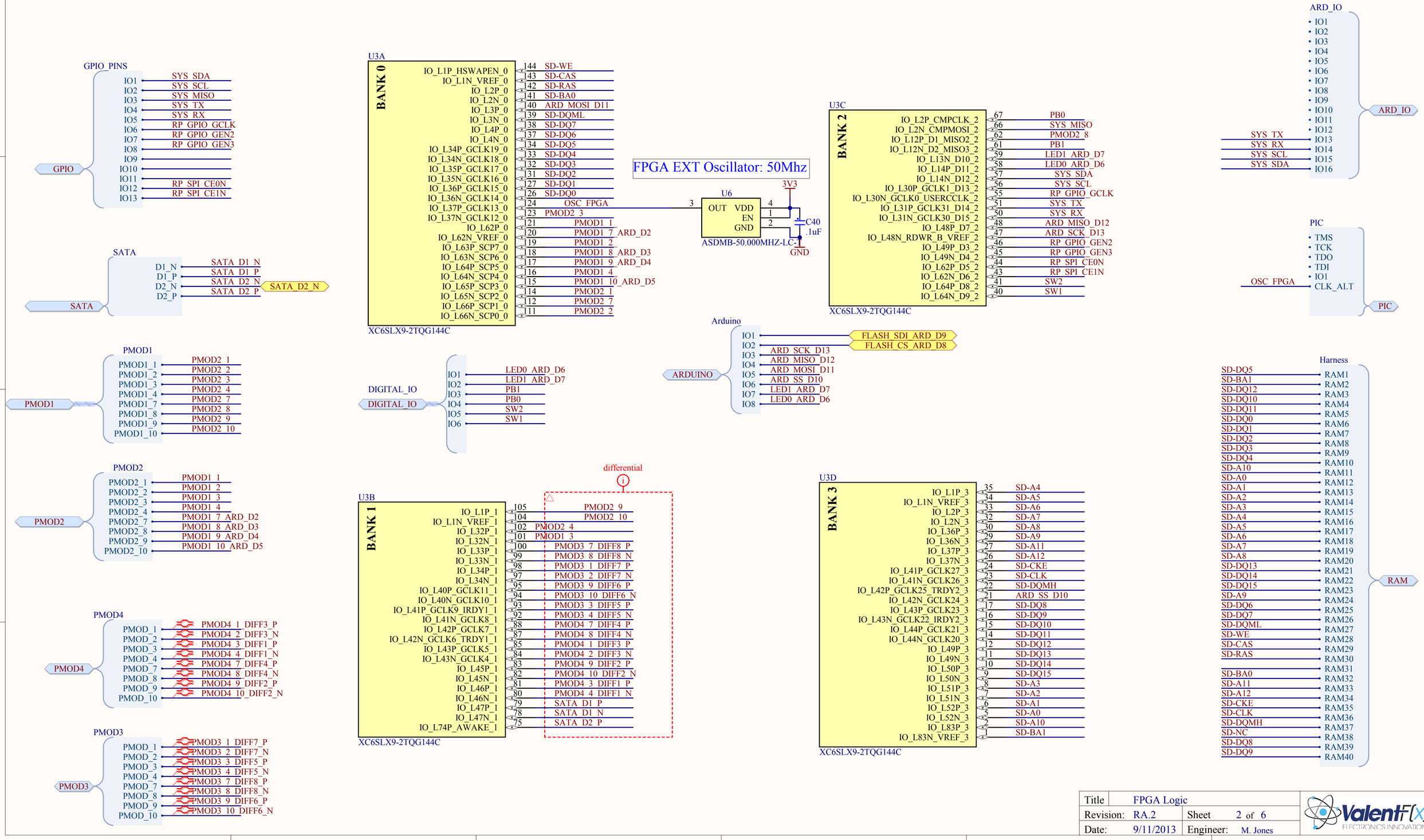
1 x Auxillary Power output Header



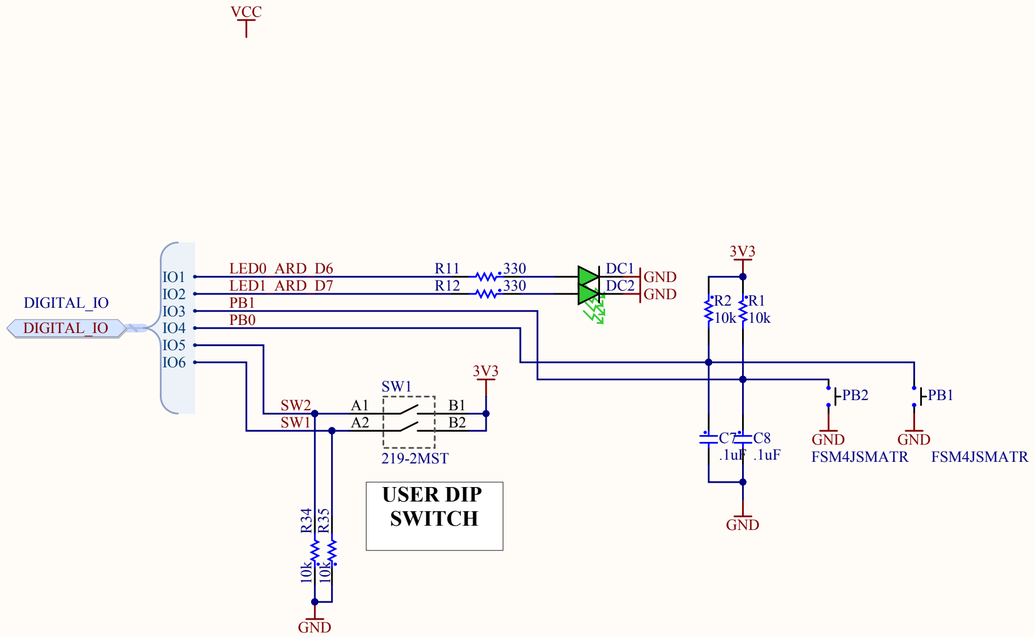
Logo1
Valent Logo 750

Logo2
Valent Logo 1000

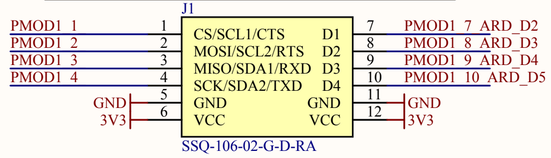
Title	Power Supply		
Revision:	RA.2	Sheet	1 of 6
Date:	9/11/2013	Engineer:	M. Jones

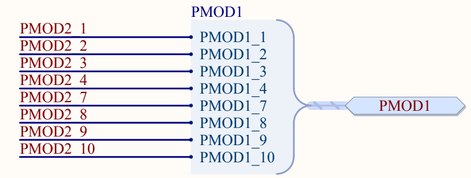

GPIO_PINS
IO1 SYS_SDA
IO2 SYS_SCL
IO3 SYS_MISO
IO4 SYS_TX
IO5 SYS_RX
IO6 RP_GPIO_GCLK
IO7 RP_GPIO_GEN2
IO8 RP_GPIO_GEN3
IO9
IO10
IO11
IO12 RP_SPI_CE0N
IO13 RP_SPI_CE1N
GPIO
SATA
D1_N SATA_D1_N
D1_P SATA_D1_P
D2_N SATA_D2_N
D2_P SATA_D2_P
SATA_D2_N
SATA
PMOD1
PMOD1_1 PMOD2_1
PMOD1_2 PMOD2_2
PMOD1_3 PMOD2_3
PMOD1_4 PMOD2_4
PMOD1_7 PMOD2_7
PMOD1_8 PMOD2_8
PMOD1_9 PMOD2_9
PMOD1_10 PMOD2_10
PMOD1
PMOD2
PMOD2_1 PMOD1_1
PMOD2_2 PMOD1_2
PMOD2_3 PMOD1_3
PMOD2_4 PMOD1_4
PMOD2_7 PMOD1_7_ARD_D2
PMOD2_8 PMOD1_8_ARD_D3
PMOD2_9 PMOD1_9_ARD_D4
PMOD2_10 PMOD1_10_ARD_D5
PMOD4
PMOD_1 PMOD4_1_DIFF3_P
PMOD_2 PMOD4_2_DIFF3_N
PMOD_3 PMOD4_3_DIFF1_P
PMOD_4 PMOD4_4_DIFF1_N
PMOD_7 PMOD4_7_DIFF4_P
PMOD_8 PMOD4_8_DIFF4_N
PMOD_9 PMOD4_9_DIFF2_P
PMOD_10 PMOD4_10_DIFF2_N
PMOD4
PMOD3
PMOD_1 PMOD3_1_DIFF7_P
PMOD_2 PMOD3_2_DIFF7_N
PMOD_3 PMOD3_3_DIFF5_P
PMOD_4 PMOD3_4_DIFF5_N
PMOD_7 PMOD3_7_DIFF8_P
PMOD_8 PMOD3_8_DIFF8_N
PMOD_9 PMOD3_9_DIFF6_P
PMOD_10 PMOD3_10_DIFF6_N
PMOD3
U3A
BANK 0
IO_L1P_HSWAPEN_0 144 SD-WE
IO_L1N_VREF_0 143 SD-CAS
IO_L2P_0 142 SD-RAS
IO_L2N_0 141 SD-BA0
IO_L3P_0 140 ARD_MOSI_D11
IO_L3N_0 139 SD-DQML
IO_L4P_0 138 SD-DQ7
IO_L4N_0 137 SD-DQ6
IO_L34P_GCLK19_0 134 SD-DQ5
IO_L34N_GCLK18_0 133 SD-DQ4
IO_L35P_GCLK17_0 132 SD-DQ3
IO_L35N_GCLK16_0 131 SD-DQ2
IO_L36P_GCLK15_0 127 SD-DQ1
IO_L36N_GCLK14_0 126 SD-DQ0
IO_L37P_GCLK13_0 124 OSC_FPGA
IO_L37N_GCLK12_0 123 PMOD2_3
IO_L62P_0 121 PMOD1_1
IO_L62N_VREF_0 120 PMOD1_7_ARD_D2
IO_L63P_SCP7_0 119 PMOD1_2
IO_L63N_SCP6_0 118 PMOD1_8_ARD_D3
IO_L64P_SCP5_0 117 PMOD1_9_ARD_D4
IO_L64N_SCP4_0 116 PMOD1_4
IO_L65P_SCP3_0 115 PMOD1_10_ARD_D5
IO_L65N_SCP2_0 114 PMOD2_1
IO_L66P_SCP1_0 112 PMOD2_7
IO_L66N_SCP0_0 111 PMOD2_2
XC6SLX9-2TQG144C
FPGA EXT Oscillator: 50Mhz
U6
OUT VDD
EN
GND
ASDMB-50.000MHZ-LC-T
3V3
C40
.1uF
GND
U3C
BANK 2
IO_L2P_CMPCLK_2 67 PB0
IO_L2N_CMPMOSI_2 66 SYS_MISO
IO_L12P_D1_MISO2_2 62 PMOD2_8
IO_L12N_D2_MISO3_2 61 PB1
IO_L13N_D10_2 59 LED1_ARD_D7
IO_L14P_D11_2 58 LED0_ARD_D6
IO_L14N_D12_2 57 SYS_SDA
IO_L30P_GCLK1_D13_2 56 SYS_SCL
IO_L30N_GCLK0_USERCCLK_2 55 RP_GPIO_GCLK
IO_L31P_GCLK31_D14_2 51 SYS_TX
IO_L31N_GCLK30_D15_2 50 SYS_RX
IO_L48P_D7_2 48 ARD_MISO_D12
IO_L48N_RDWR_B_VREF_2 47 ARD_SCK_D13
IO_L49P_D3_2 46 RP_GPIO_GEN2
IO_L49N_D4_2 45 RP_GPIO_GEN3
IO_L62P_D5_2 44 RP_SPI_CE0N
IO_L62N_D6_2 43 RP_SPI_CE1N
IO_L64P_D8_2 41 SW2
IO_L64N_D9_2 40 SW1
XC6SLX9-2TQG144C
ARD_IO
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
SYS_TX IO13
SYS_RX IO14
SYS_SCL IO15
SYS_SDA IO16
ARD_IO
PIC
TMS
TCK
TDO
TDI
IO1
OSC_FPGA CLK_ALT
PIC
Arduino
IO1 FLASH_SDI_ARD_D9
IO2 FLASH_CS_ARD_D8
IO3 ARD_SCK_D13
IO4 ARD_MISO_D12
IO5 ARD_MOSI_D11
IO6 ARD_SS_D10
IO7 LED1_ARD_D7
IO8 LED0_ARD_D6
ARDUINO
DIGITAL_IO
IO1 LED0_ARD_D6
IO2 LED1_ARD_D7
IO3 PB1
IO4 PB0
IO5 SW2
IO6 SW1
DIGITAL_IO
differential
U3B
BANK 1
IO_L1P_1 105 PMOD2_9
IO_L1N_VREF_1 104 PMOD2_10
IO_L32P_1 102 PMOD2_4
IO_L32N_1 101 PMOD1_3
IO_L33P_1 100 PMOD3_7_DIFF8_P
IO_L33N_1 99 PMOD3_8_DIFF8_N
IO_L34P_1 98 PMOD3_1_DIFF7_P
IO_L34N_1 97 PMOD3_2_DIFF7_N
IO_L40P_GCLK11_1 95 PMOD3_9_DIFF6_P
IO_L40N_GCLK10_1 94 PMOD3_10_DIFF6_N
IO_L41P_GCLK9_IRDY1_1 93 PMOD3_3_DIFF5_P
IO_L41N_GCLK8_1 92 PMOD3_4_DIFF5_N
IO_L42P_GCLK7_1 88 PMOD4_7_DIFF4_P
IO_L42N_GCLK6_TRDY1_1 87 PMOD4_8_DIFF4_N
IO_L43P_GCLK5_1 85 PMOD4_1_DIFF3_P
IO_L43N_GCLK4_1 84 PMOD4_2_DIFF3_N
IO_L45P_1 83 PMOD4_9_DIFF2_P
IO_L45N_1 82 PMOD4_10_DIFF2_N
IO_L46P_1 81 PMOD4_3_DIFF1_P
IO_L46N_1 80 PMOD4_4_DIFF1_N
IO_L47P_1 79 SATA_D1_P
IO_L47N_1 78 SATA_D1_N
IO_L74P_AWAKE_1 75 SATA_D2_P
XC6SLX9-2TQG144C
U3D
BANK 3
IO_L1P_3 35 SD-A4
IO_L1N_VREF_3 34 SD-A5
IO_L2P_3 33 SD-A6
IO_L2N_3 32 SD-A7
IO_L36P_3 30 SD-A8
IO_L36N_3 29 SD-A9
IO_L37P_3 27 SD-A11
IO_L37N_3 26 SD-A12
IO_L41P_GCLK27_3 24 SD-CKE
IO_L41N_GCLK26_3 23 SD-CLK
IO_L42P_GCLK25_TRDY2_3 22 SD-DQMH
IO_L42N_GCLK24_3 21 ARD_SS_D10
IO_L43P_GCLK23_3 17 SD-DQ8
IO_L43N_GCLK22_IRDY2_3 16 SD-DQ9
IO_L44P_GCLK21_3 15 SD-DQ10
IO_L44N_GCLK20_3 14 SD-DQ11
IO_L49P_3 12 SD-DQ12
IO_L49N_3 11 SD-DQ13
IO_L50P_3 10 SD-DQ14
IO_L50N_3 9 SD-DQ15
IO_L51P_3 8 SD-A3
IO_L51N_3 7 SD-A2
IO_L52P_3 6 SD-A1
IO_L52N_3 5 SD-A0
IO_L83P_3 3 SD-A10
IO_L83N_VREF_3 1 SD-BA1
XC6SLX9-2TQG144C
Harness
SD-DQ5 RAM1
SD-BA1 RAM2
SD-DQ12 RAM3
SD-DQ10 RAM4
SD-DQ11 RAM5
SD-DQ0 RAM6
SD-DQ1 RAM7
SD-DQ2 RAM8
SD-DQ3 RAM9
SD-DQ4 RAM10
SD-A10 RAM11
SD-A0 RAM12
SD-A1 RAM13
SD-A2 RAM14
SD-A3 RAM15
SD-A4 RAM16
SD-A5 RAM17
SD-A6 RAM18
SD-A7 RAM19
SD-A8 RAM20
SD-DQ13 RAM21
SD-DQ14 RAM22
SD-DQ15 RAM23
SD-A9 RAM24
SD-DQ6 RAM25
SD-DQ7 RAM26
SD-DQML RAM27
SD-WE RAM28
SD-CAS RAM29
SD-RAS RAM30
RAM31
SD-BA0 RAM32
SD-A11 RAM33
SD-A12 RAM34
SD-CKE RAM35
SD-CLK RAM36
SD-DQMH RAM37
SD-NC RAM38
SD-DQ8 RAM39
SD-DQ9 RAM40
RAM
Title FPGA Logic
Revision: RA.2
Sheet 2 of 6
Date: 9/11/2013
Engineer: M. Jones
ValentF(X)
FLECTRONICS INNOVATION

DIGITAL IO



PMOD1





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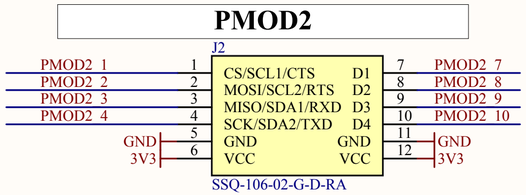

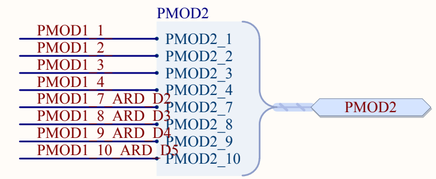

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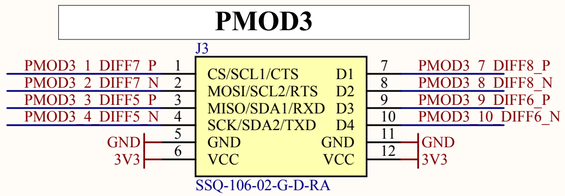
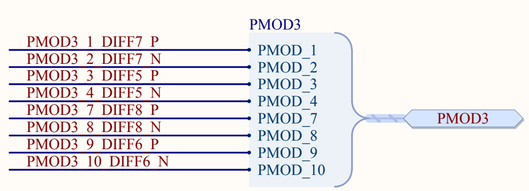
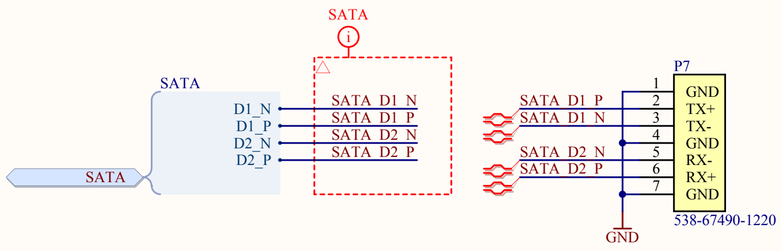
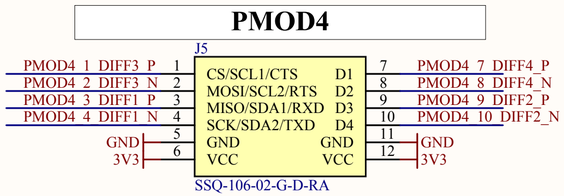
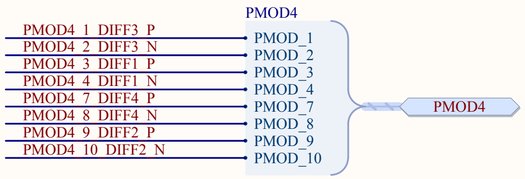






PMOD4

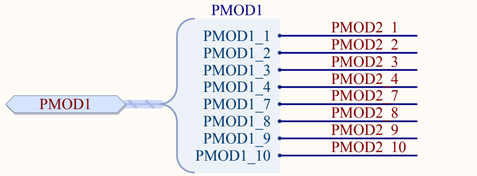


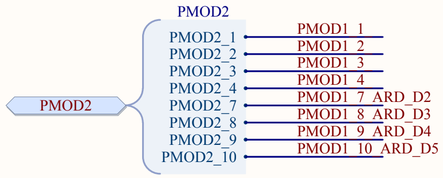


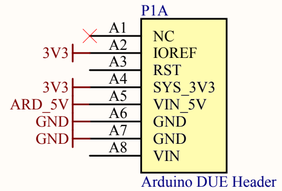
Title	Digital IO		
Revision:	RA.2	Sheet	3 of 6
Date:	9/11/2013	Engineer:	M. Jones

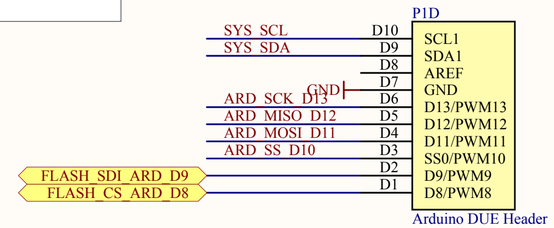
ValentF(X) ELECTRONICS INNOVATION

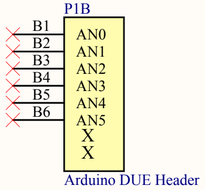
Arduino IO

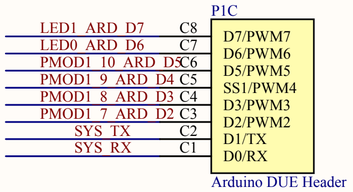


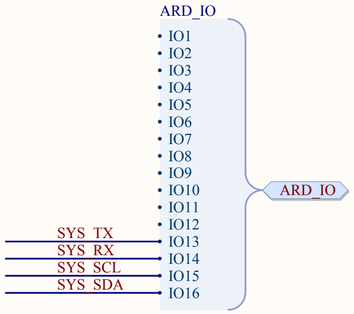


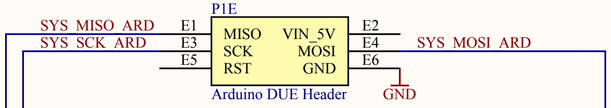


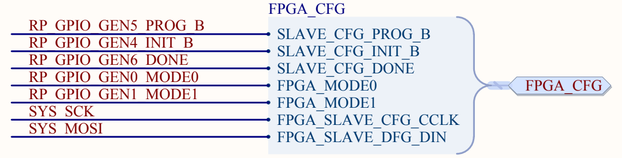


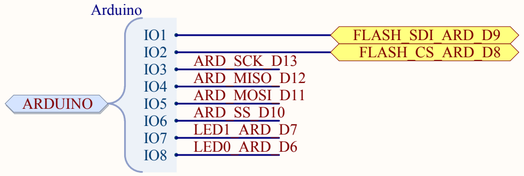






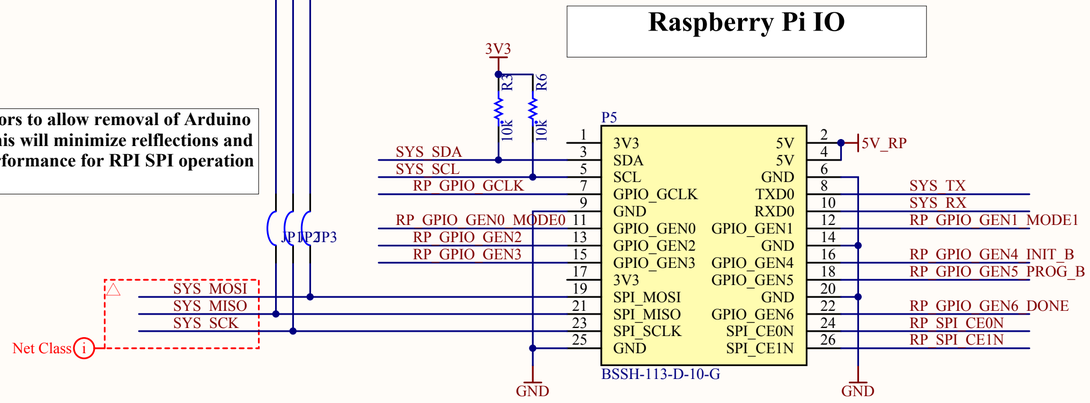


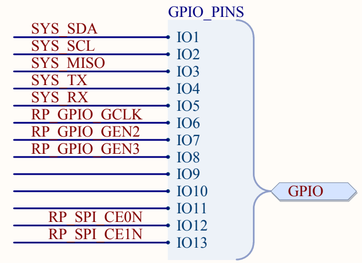




0 ohm resistors to allow removal of Arduino SPI pins. This will minimize relflections and optimize performance for RPI SPI operation

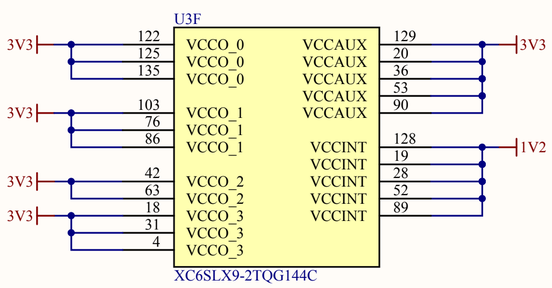
Raspberry Pi IO

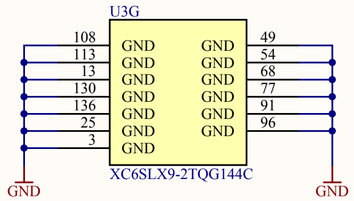


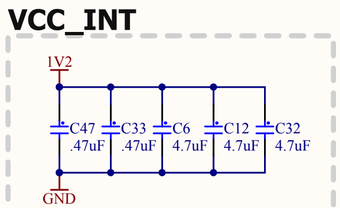


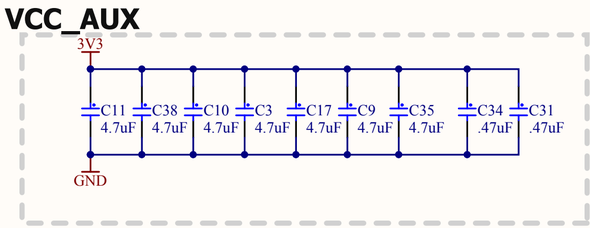
Title	Peripheral Port IO		
Revision:	RA.2	Sheet	4 of 6
Date:	9/11/2013	Engineer:	M. Jones

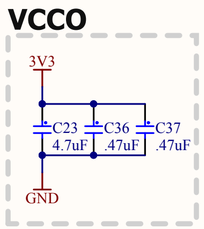
ValentF(X) ELECTRONICS INNOVATION

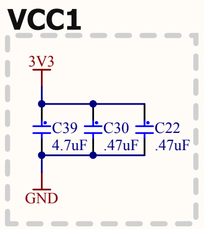


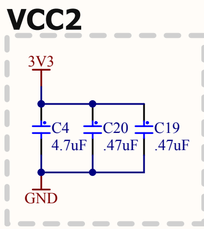


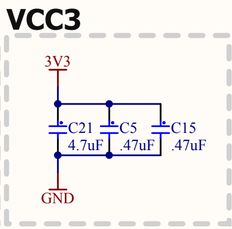




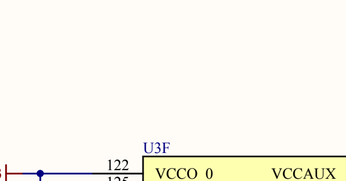


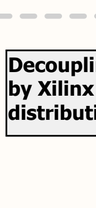






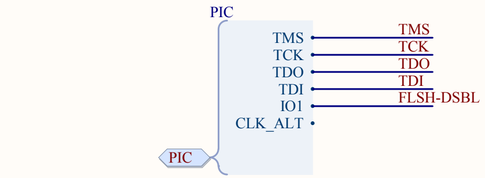
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

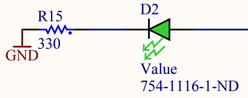


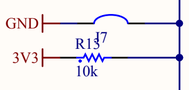


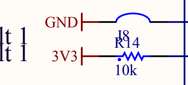
See Page 52 of UG380 V2.3. Pads for parallel CCLK Termination

Loads the Signal to 32mA! But keeps clean. Does not appear to be required by measurements.









M1 default 1
M0 default 1

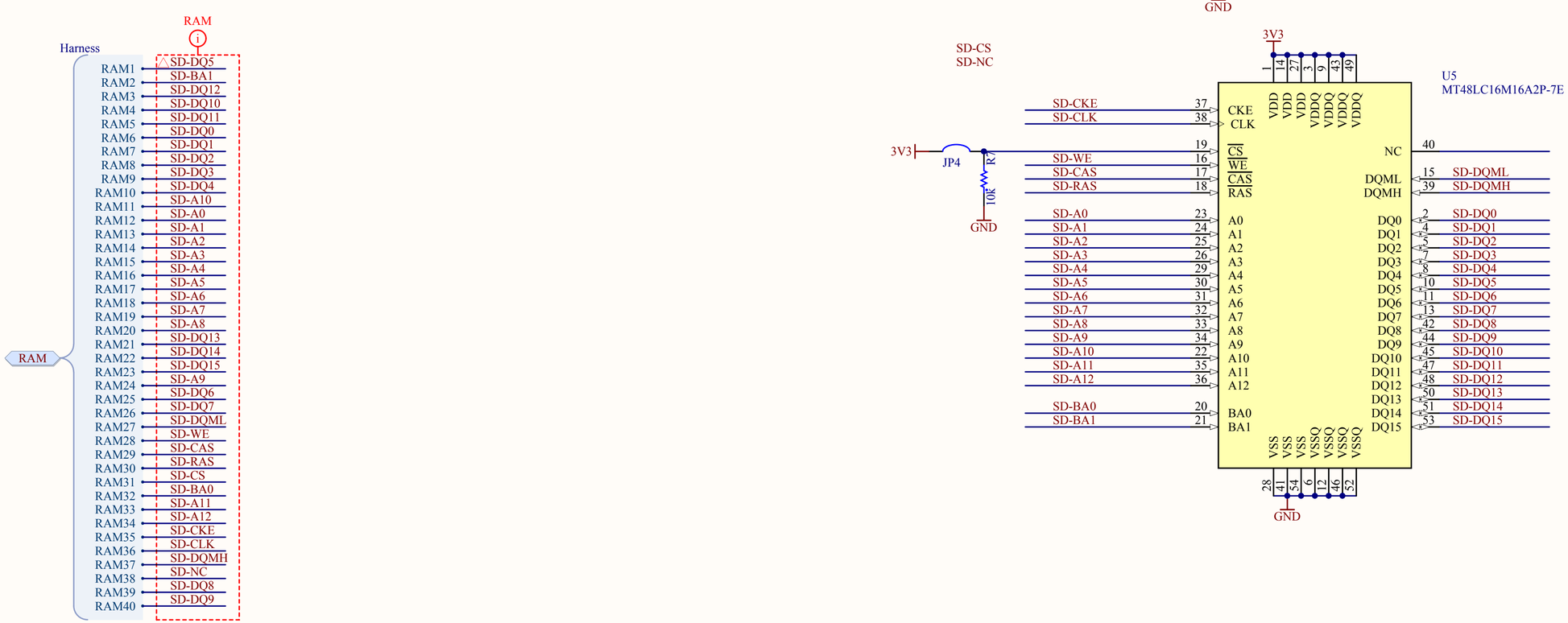
CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

Title	FPGA Configuration		
Revision:	RA.2	Sheet	5 of 6
Date:	9/11/2013	Engineer:	M. Jones

ValentF(X) ELECTRONICS INNOVATION

SDRAM



Title	SDRAM		
Revision:	RA.2	Sheet	6 of 6
Date:	9/11/2013	Engineer:	M. Jones

ValentF(X) ELECTRONICS INNOVATION