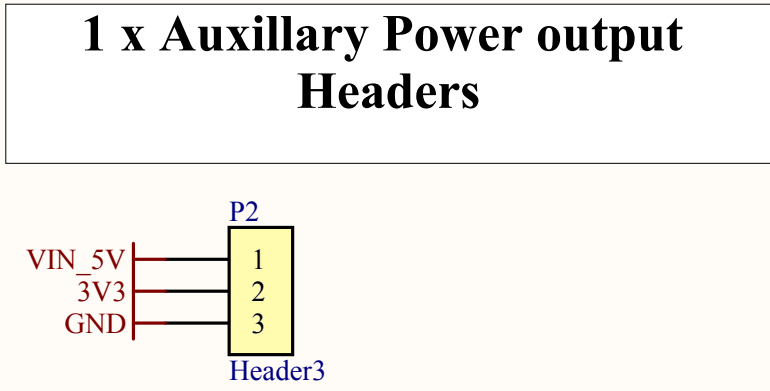
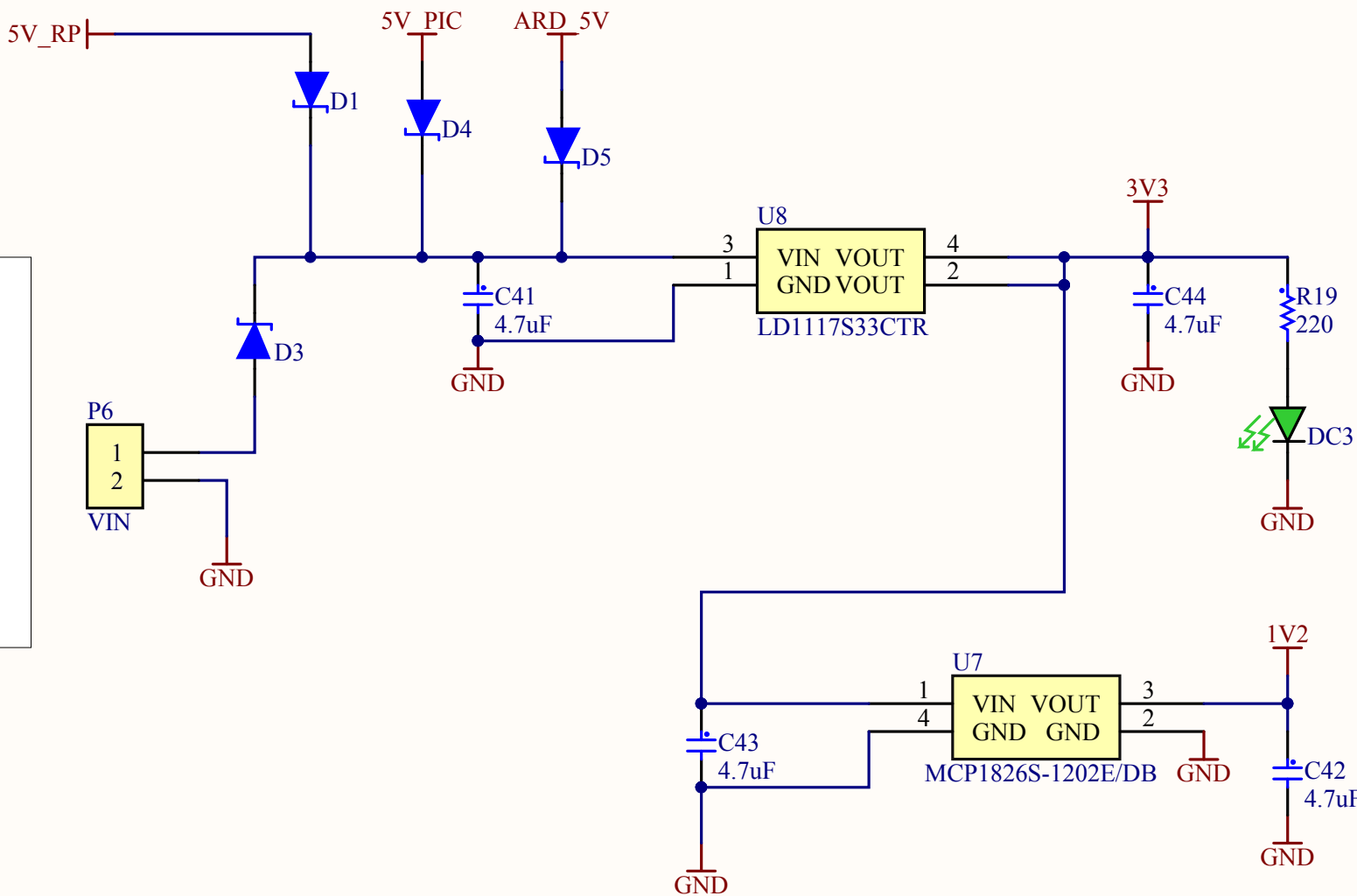
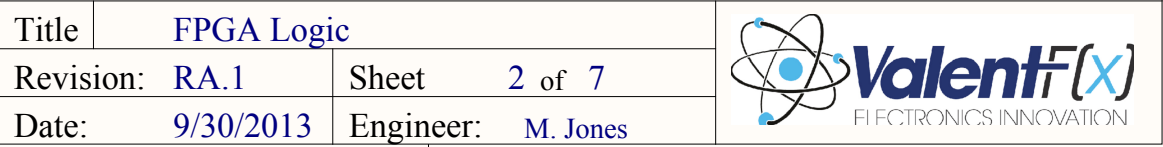
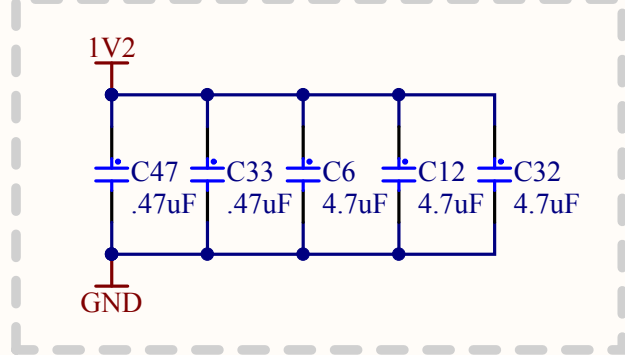


Power: By Default Power will be supplied by the .  
Raspberry Pi  
Optionally power can be supplied through  
FPGA VIN header.

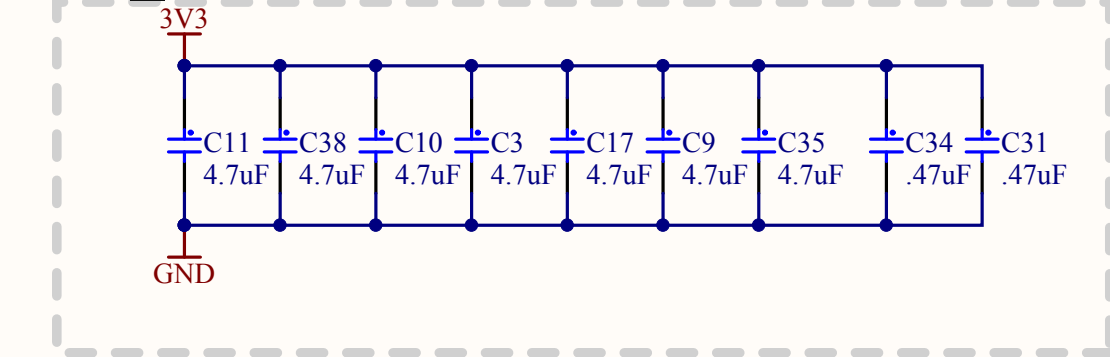




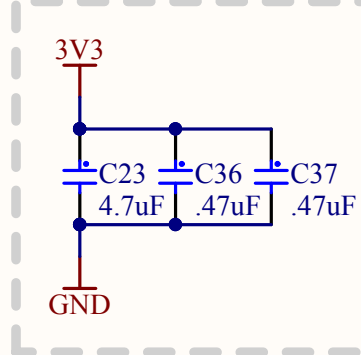
## VCC\_INT



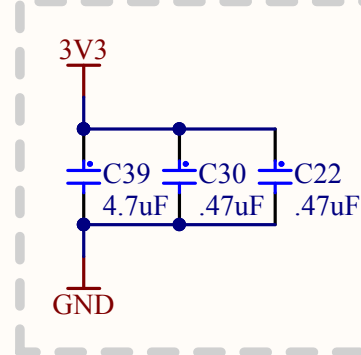
## VCC\_AUX



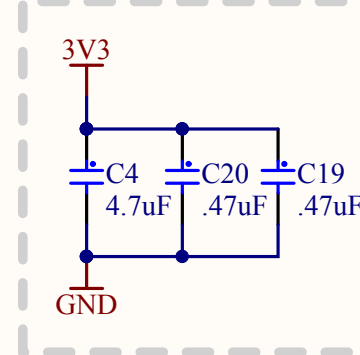
## VCCO



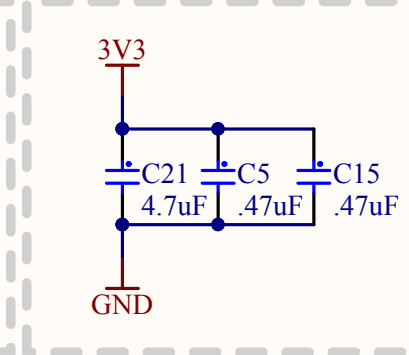
## VCC1



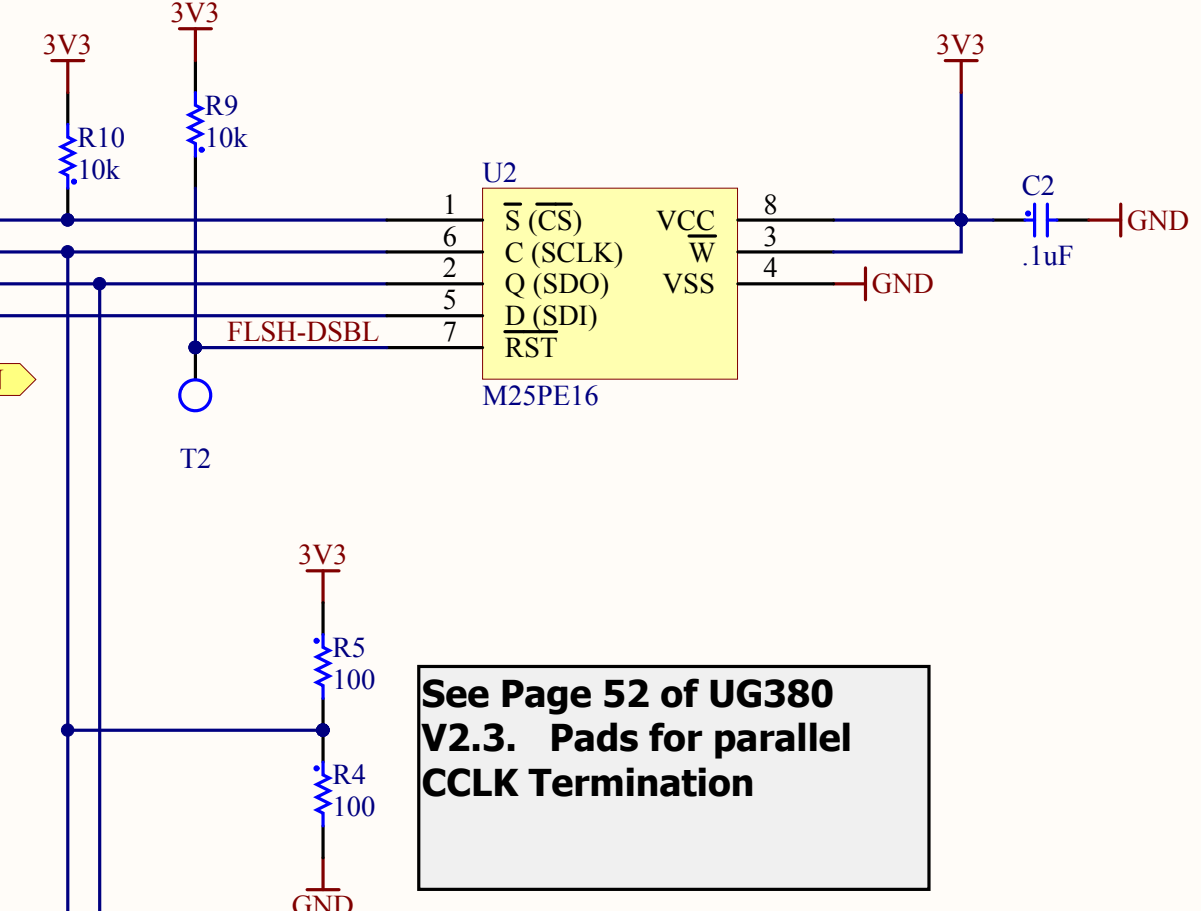
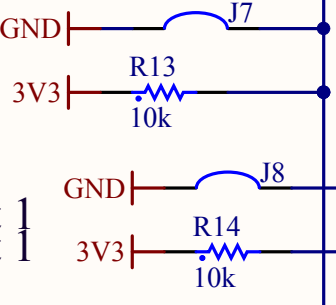
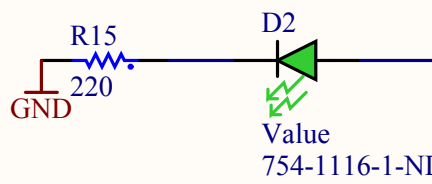
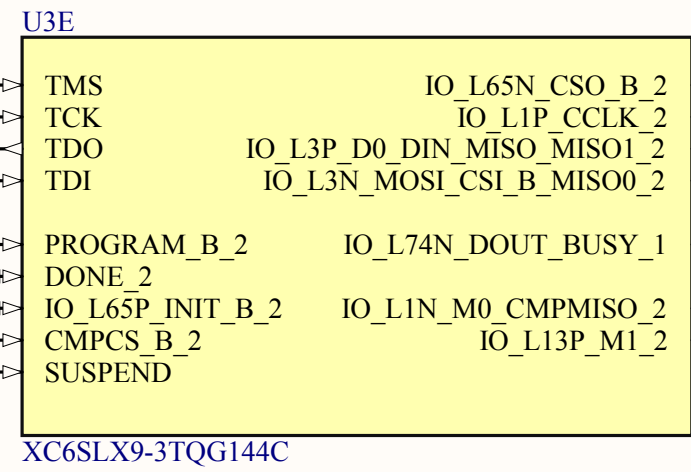
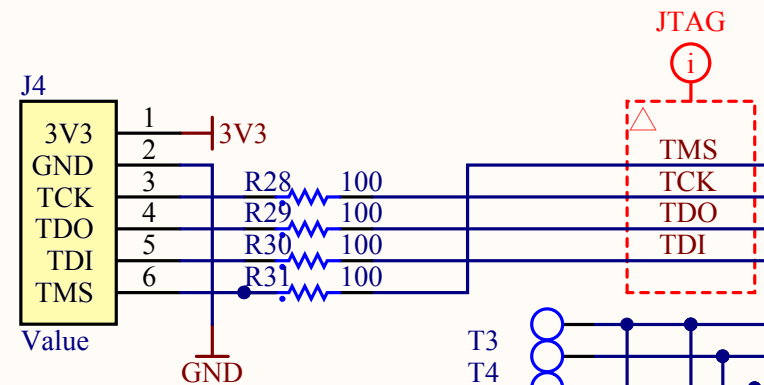
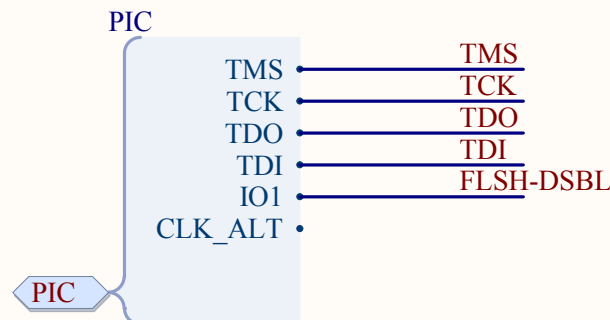
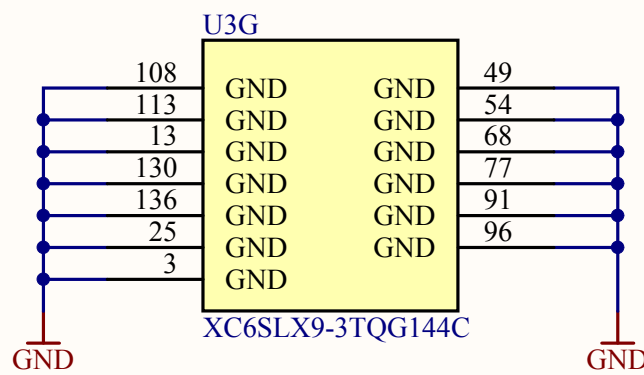
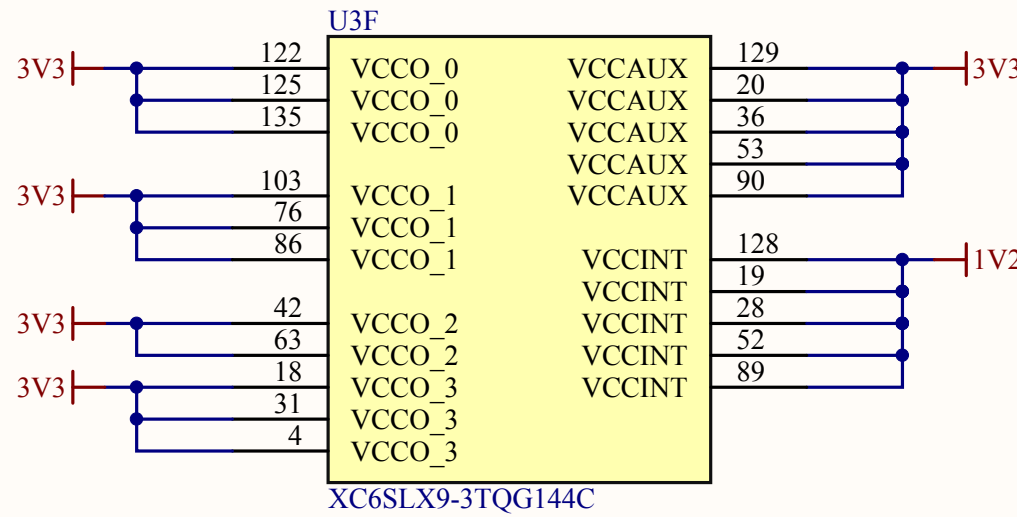
## VCC2



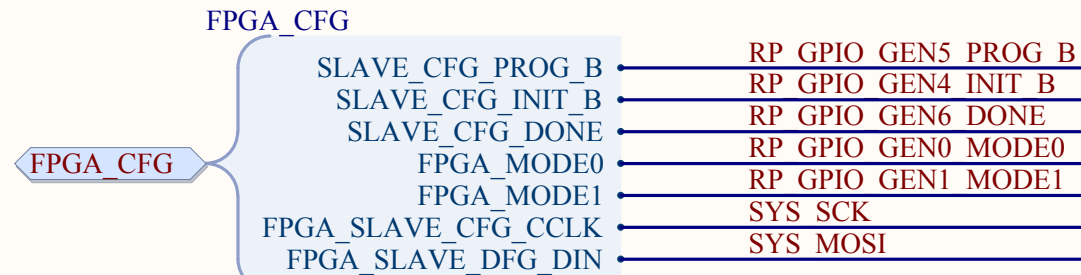
## VCC3



Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution



See Page 52 of UG380 V2.3. Pads for parallel CCLK Termination



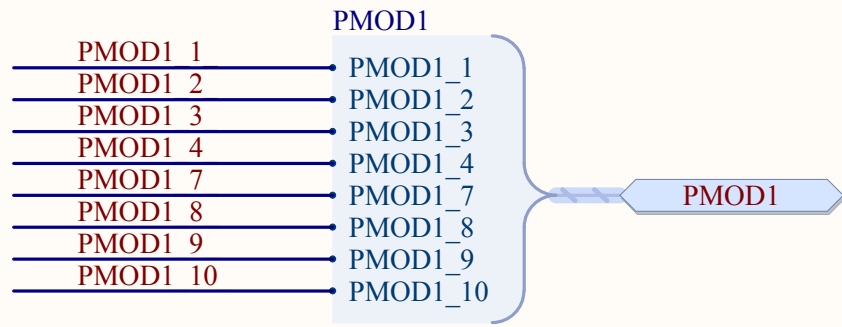
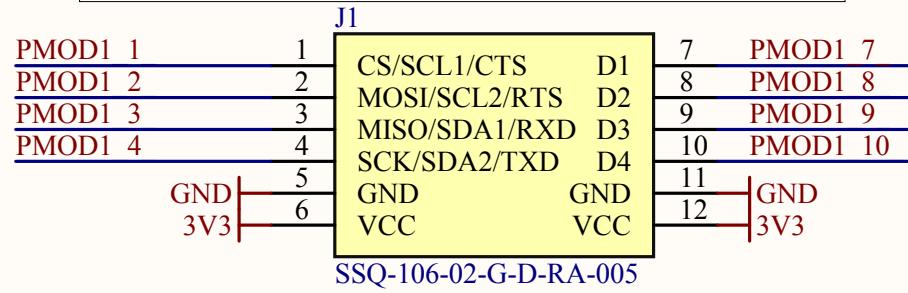
CFG\_FLASH\_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.  
01 = SelfConfig  
11 = SlaveConfig

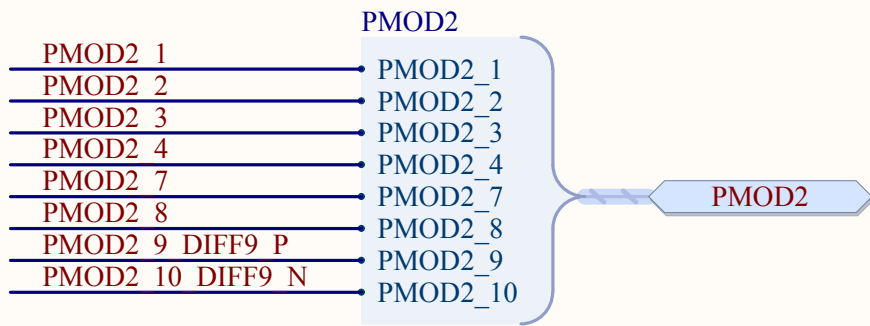
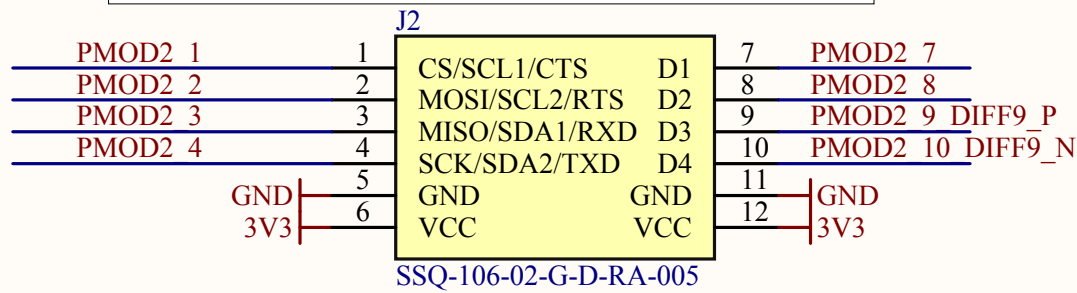


DIGITAL IO

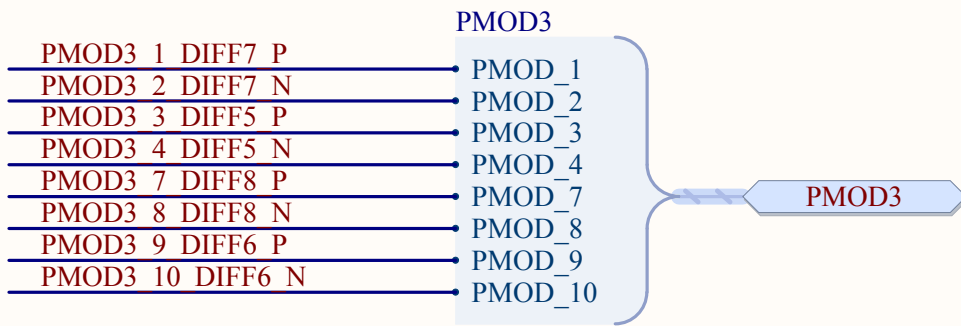
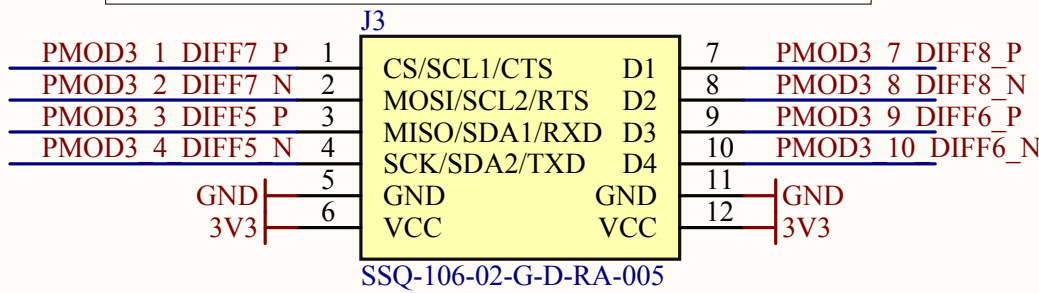
PMOD1



PMOD2



PMOD3



PMOD4

