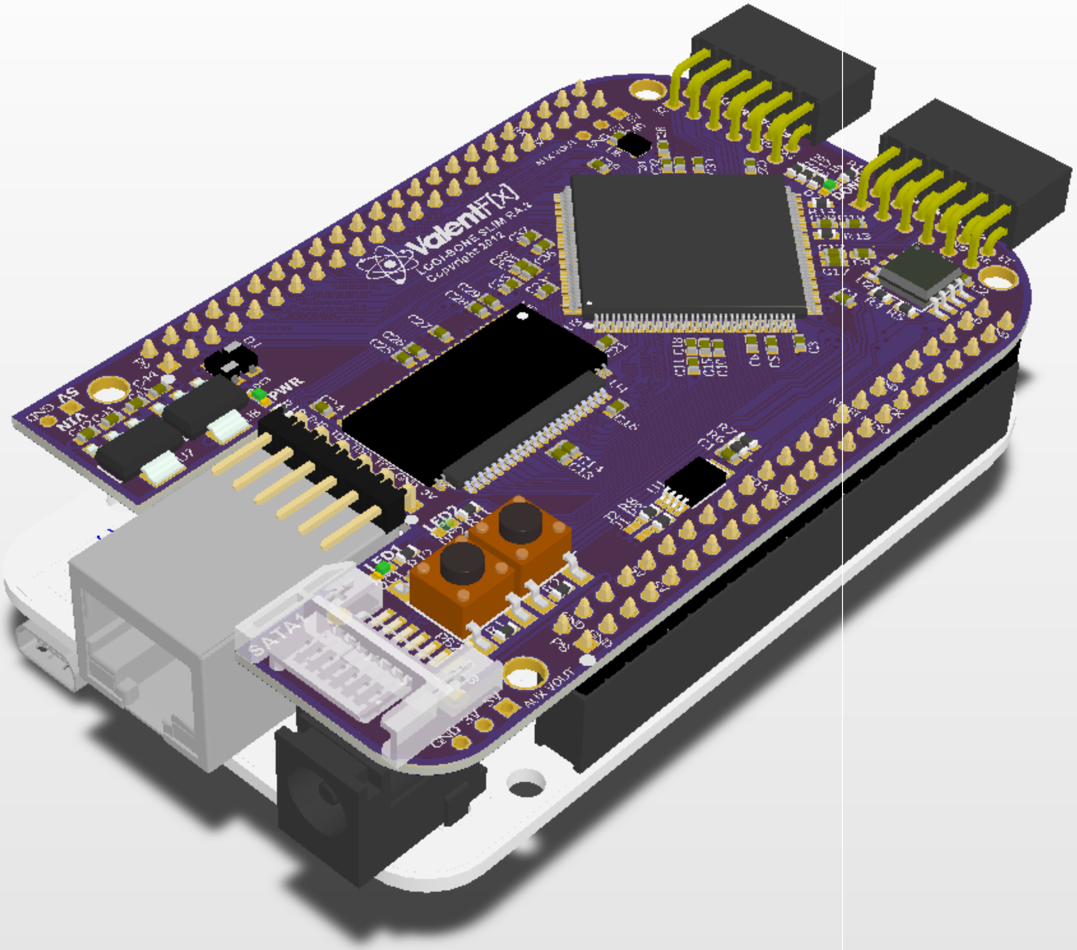
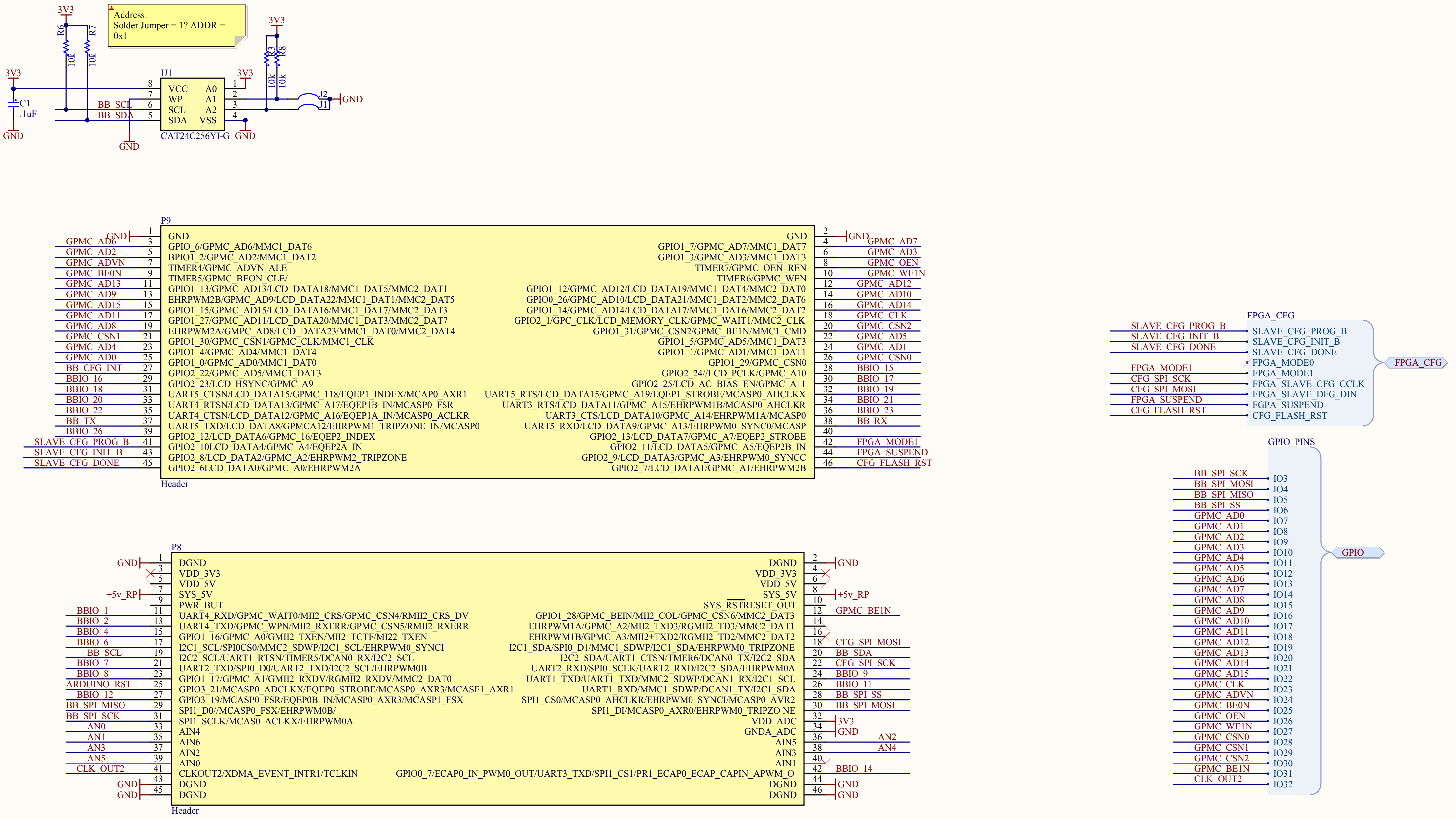

ValentF[X]
LOGI-BONE SLIM R4.2
Copyright 2012
PWR
LED1
LED2
SATA1
AUX VOUT
GND

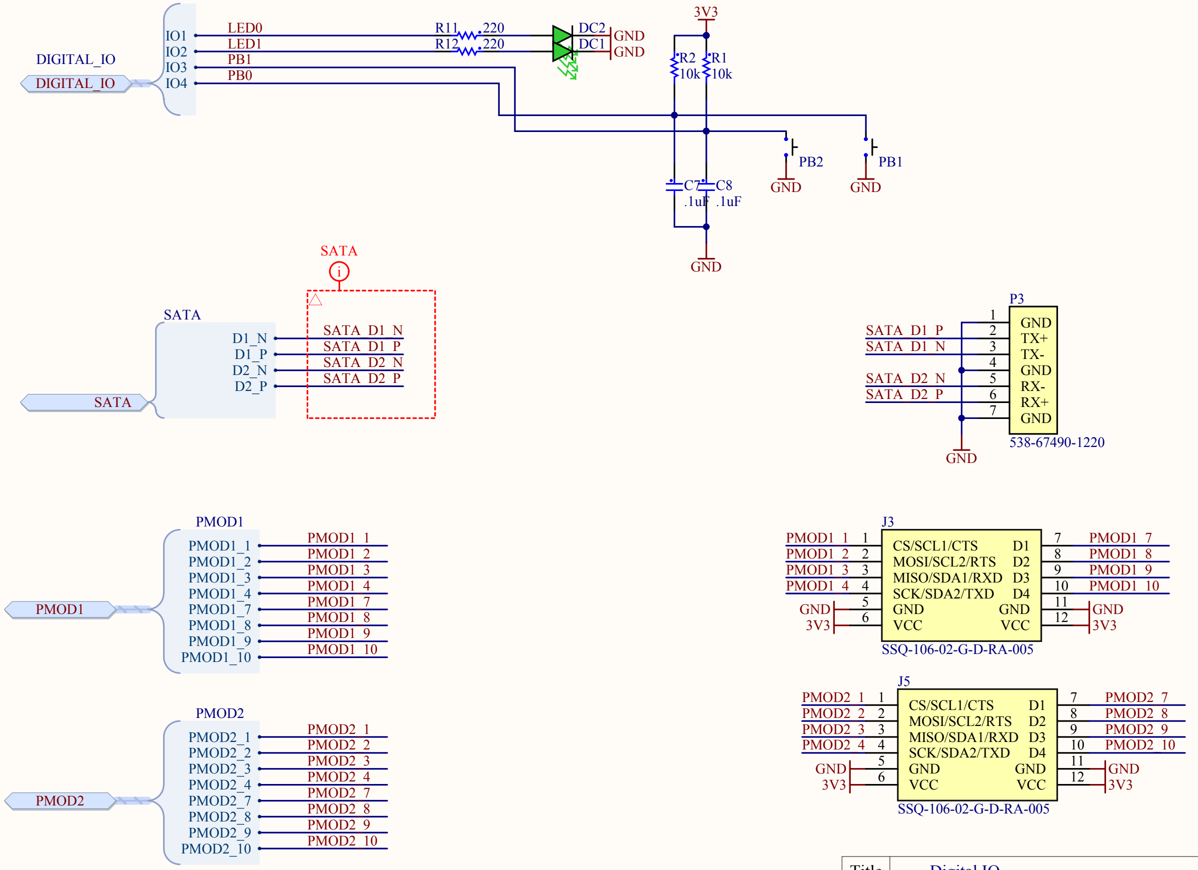
Beaglebone IO



Title	Peripheral Port IO		
Revision:	RA.1	Sheet	1 of 1
Date:	12/31/2012	Engineer:	M. Jones

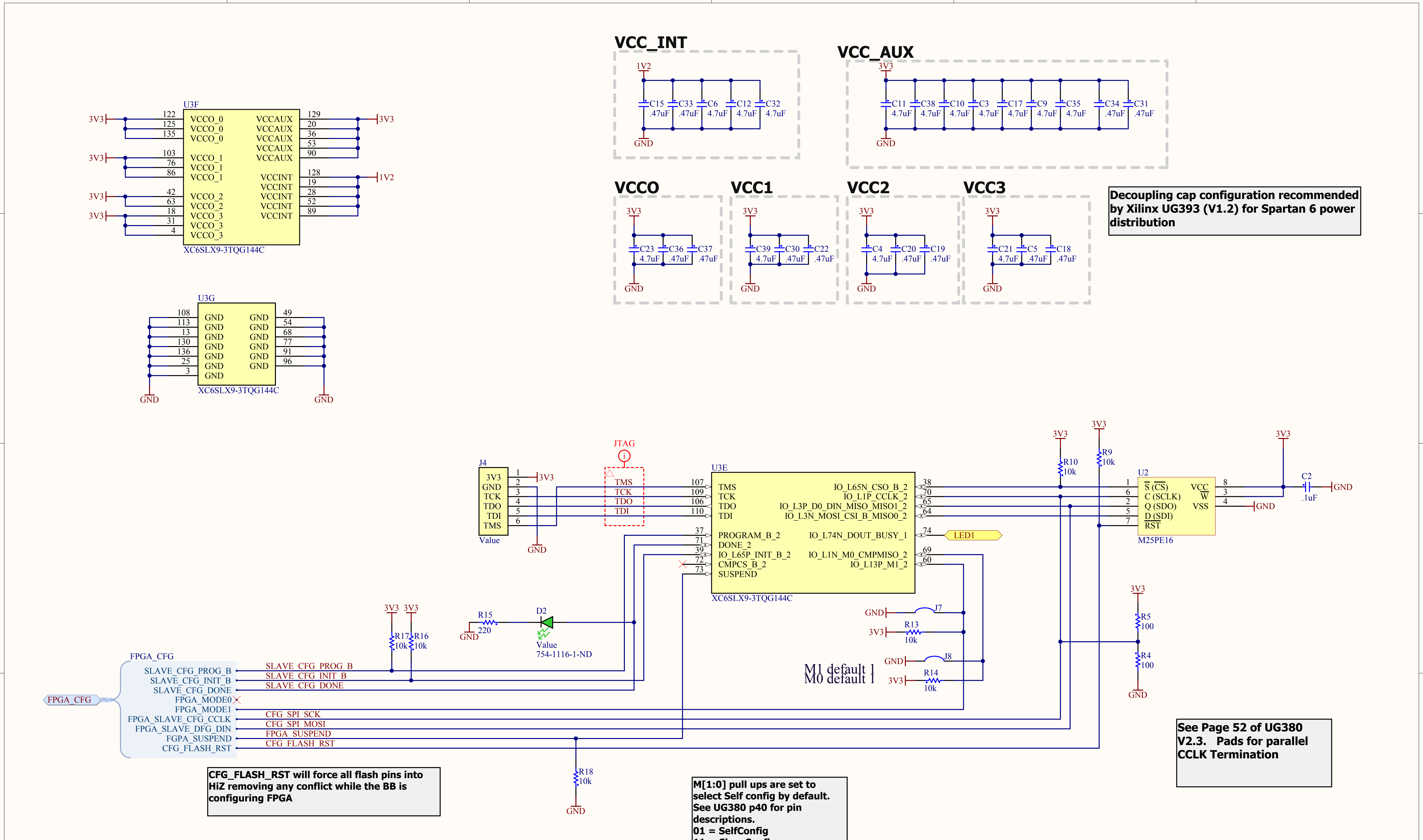
ValentF(x)
ELECTRONICS INNOVATION

FPGA IO



Title	Digital IO		
Revision:	RA.1	Sheet	1 of 1
Date:	12/31/2012	Engineer:	M. Jones

ValentF(X)
ELECTRONICS INNOVATION



Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

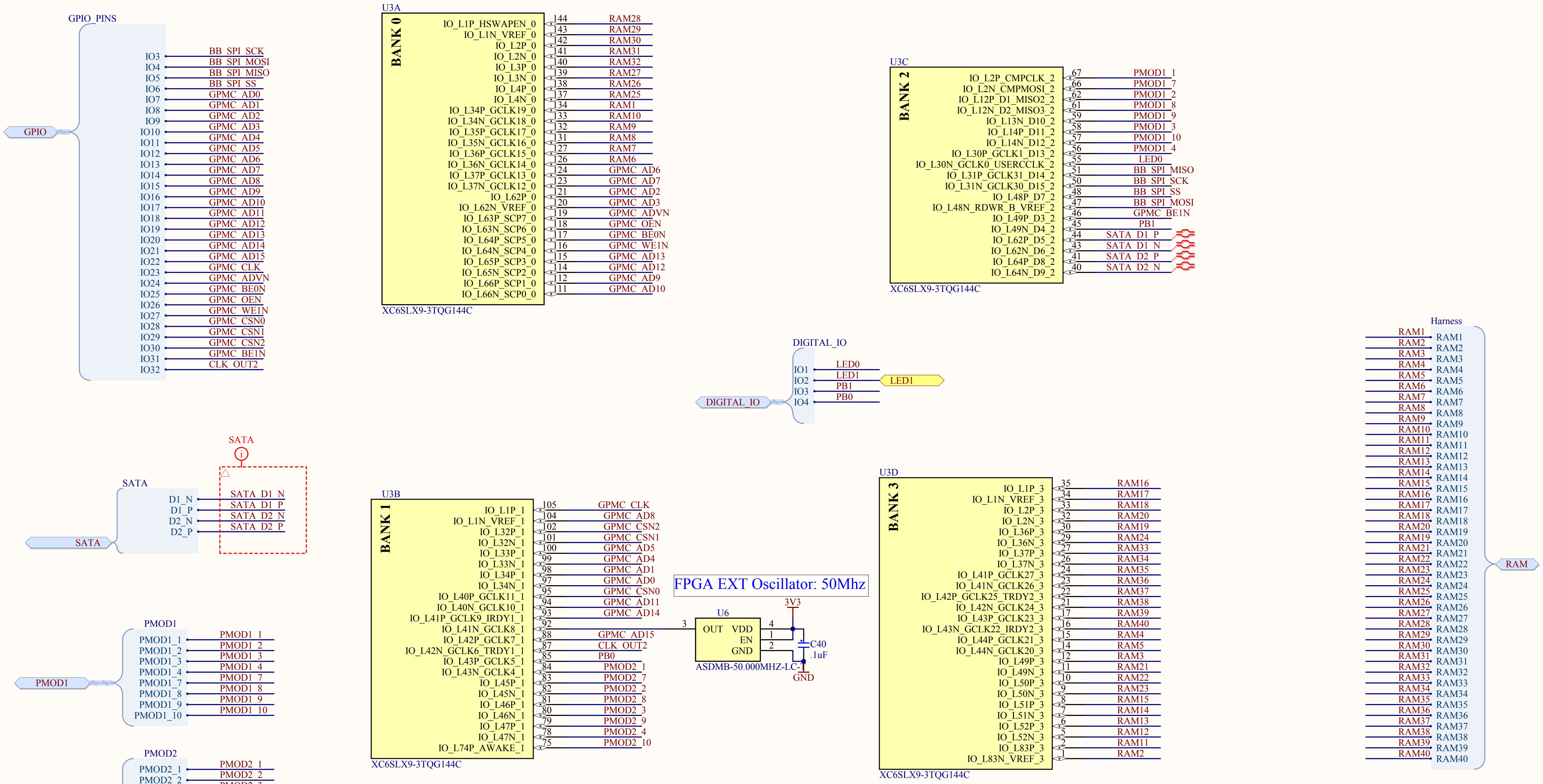
See Page 52 of UG380 V2.3. Pads for parallel CCLK Termination

CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

Title	FPGA Configuration		
Revision:	RA.1	Sheet	1 of 1
Date:	12/31/2012	Engineer:	M. Jones

ValentF(x)
ELECTRONICS INNOVATION



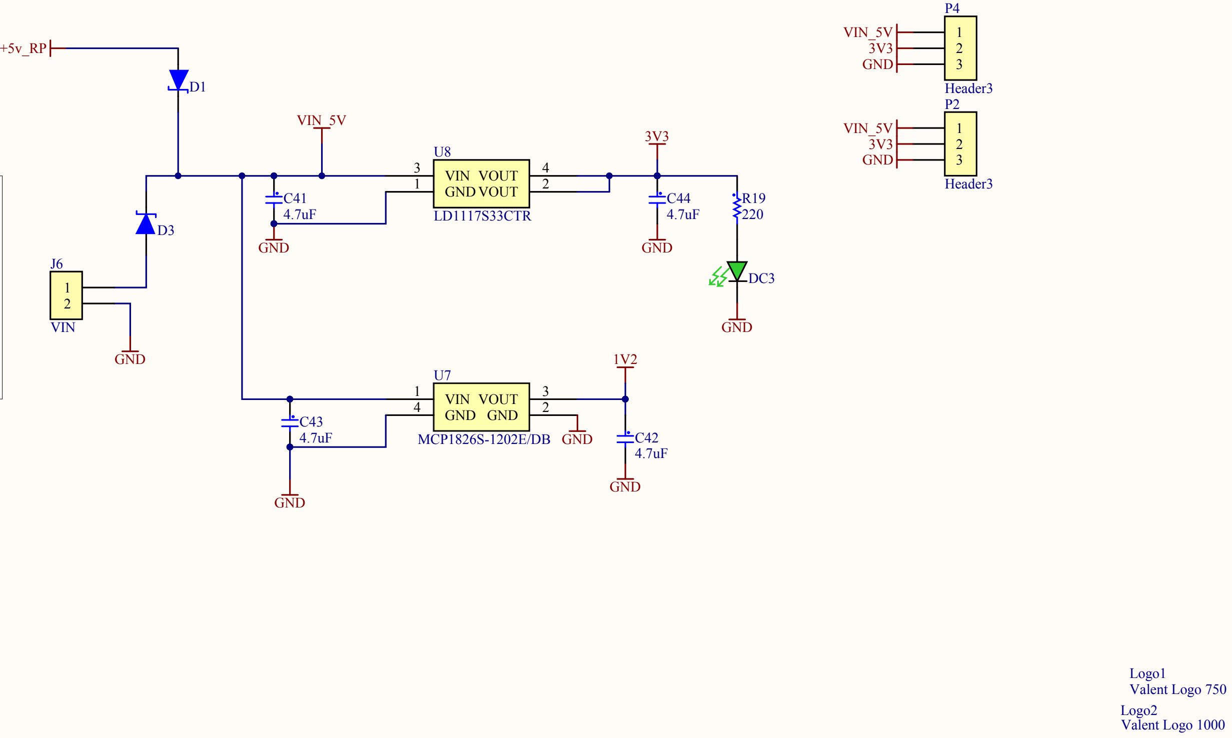
Title	FPGA Logic		
Revision:	RA.1	Sheet	1 of 1
Date:	12/31/2012	Engineer:	M. Jones

ValentF(x)
ELECTRONICS INNOVATION

2 x Auxillary Power output Headers

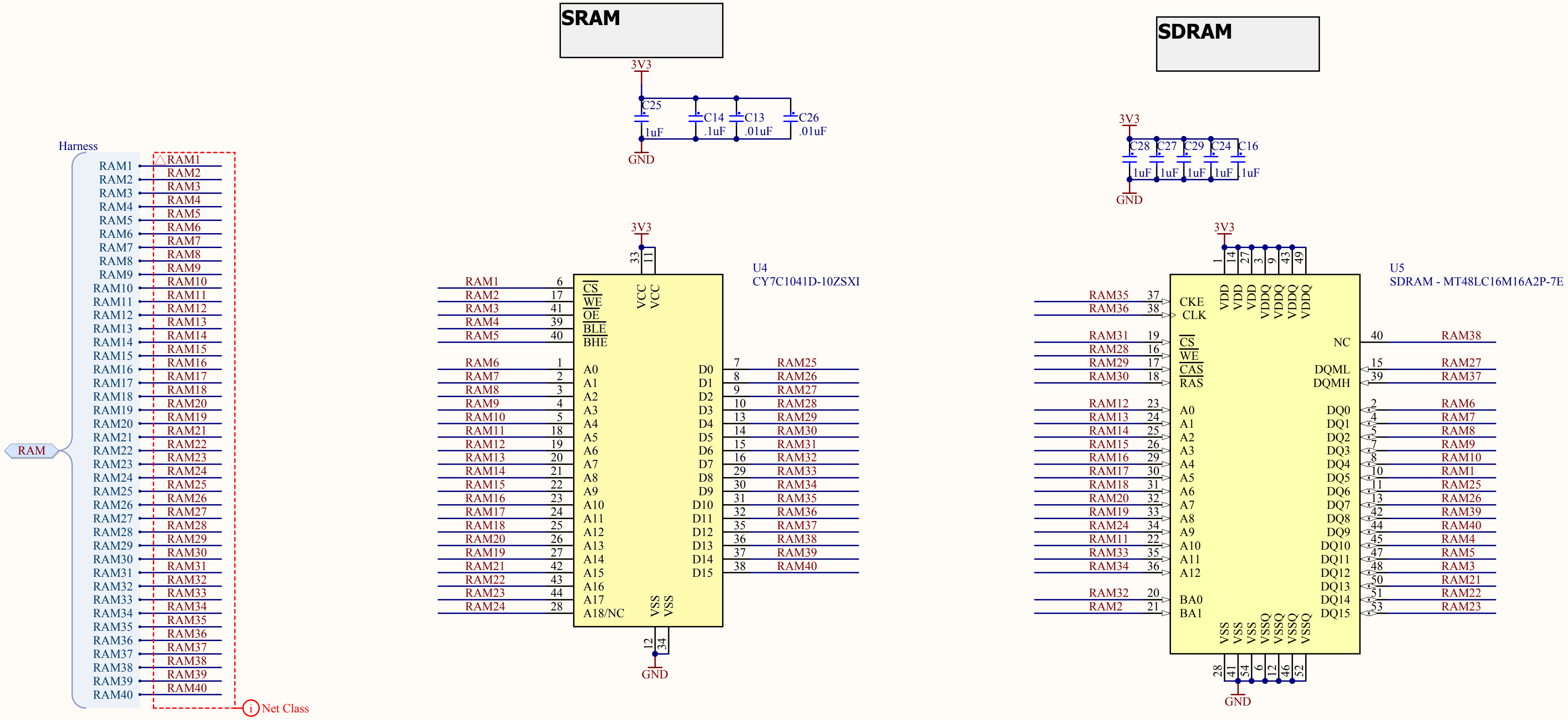
Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header.



Title	Power Supply		
Revision:	RA.1	Sheet	1 of 1
Date:	12/31/2012	Engineer:	M. Jones

ValentF(x)
ELECTRONICS INNOVATION



Title	*		
Revision:	*	Sheet	* of *
Date:	12/31/2012	Engineer:	*

ValentF(x)
ELECTRONICS INNOVATION