

A

B

C

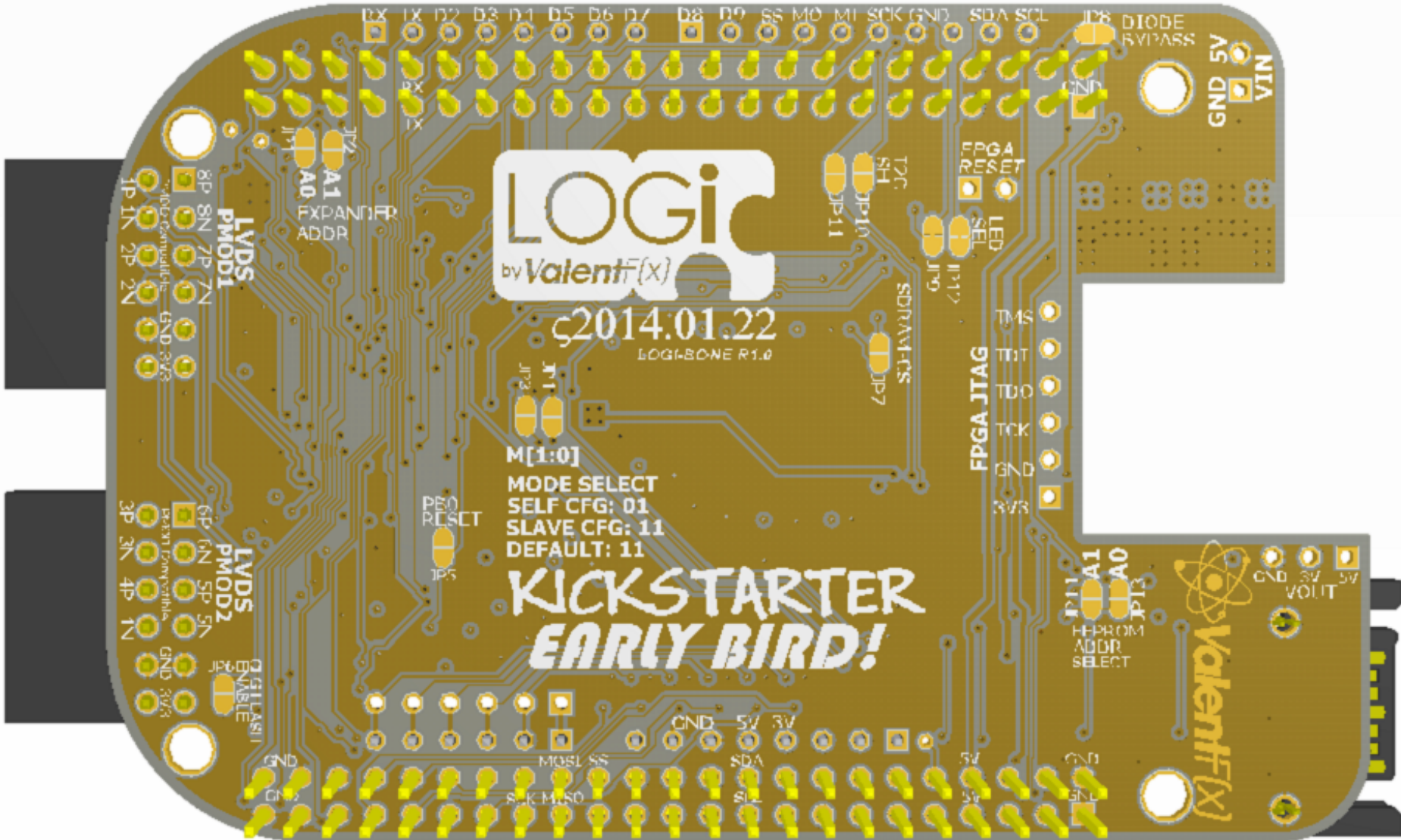
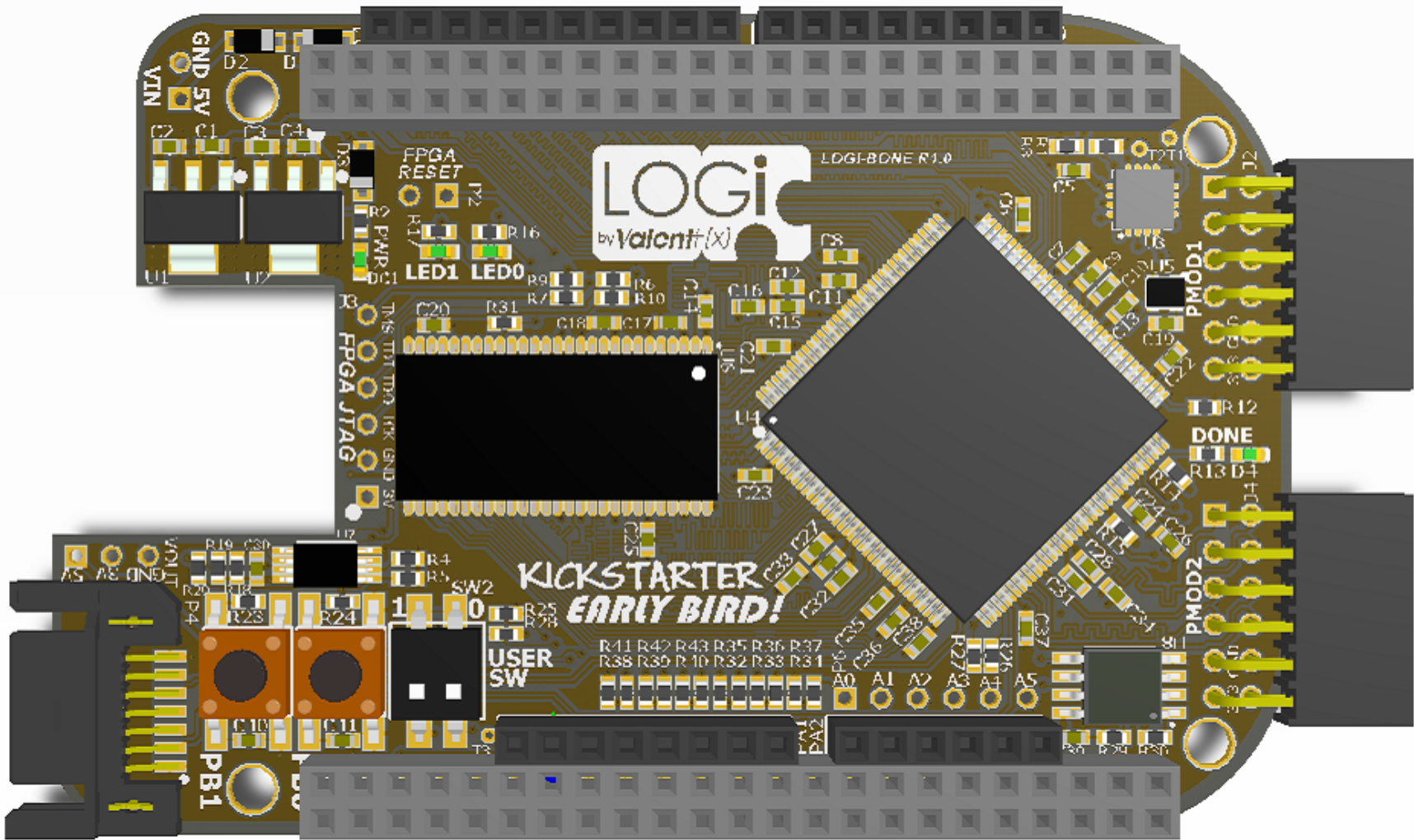
D

A

B

C

D



U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

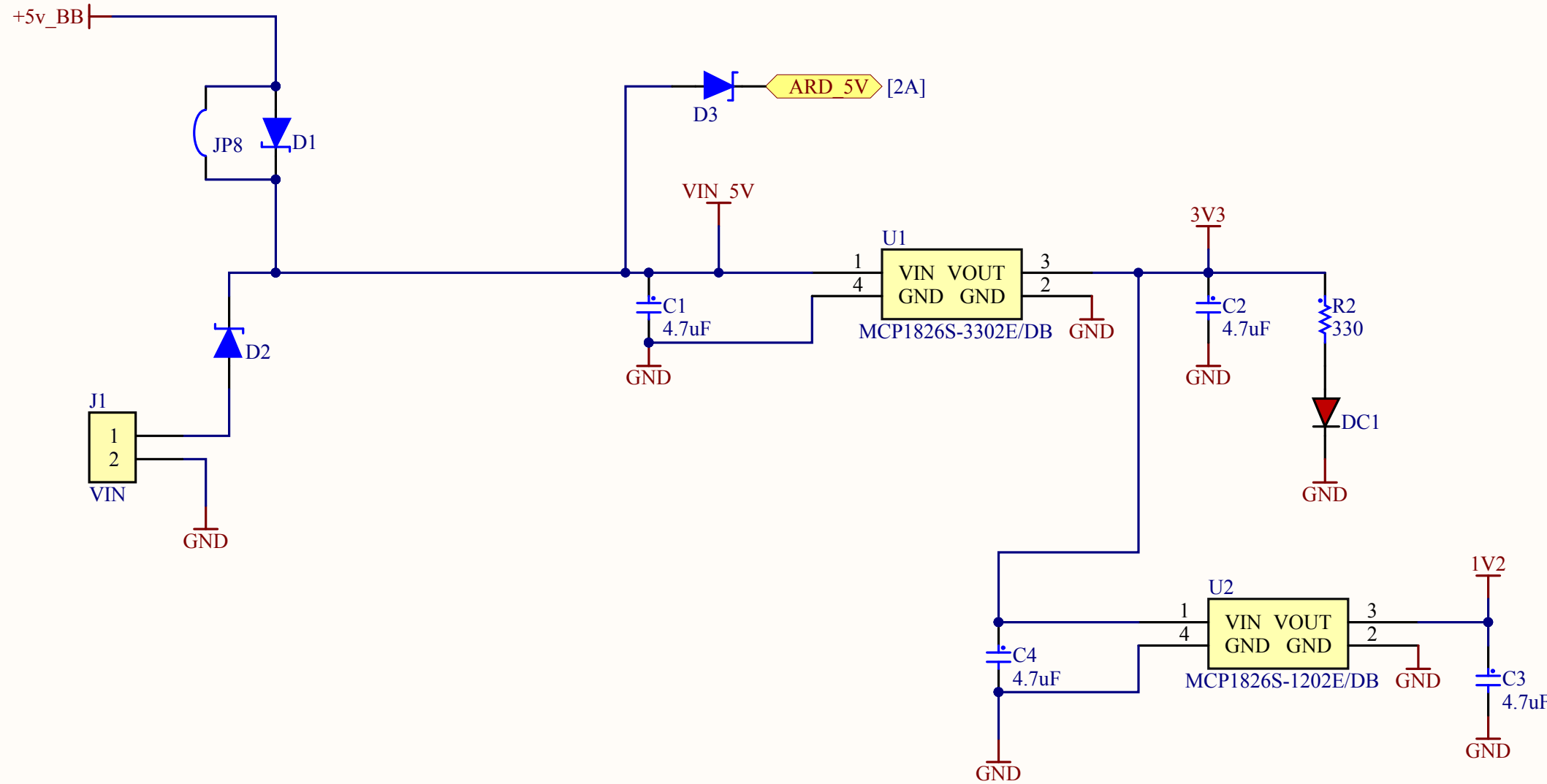
LOGi-Bone Top Level

Revision:	R1.0	Sheet	1 of 7
Date:	5/27/2014	Engineer:	MJones

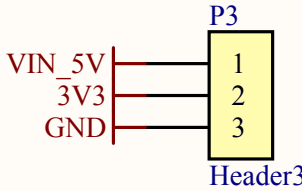


Power: By Default Power will be supplied by the Beaglebone.

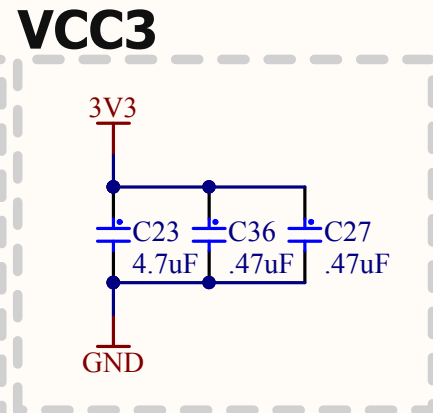
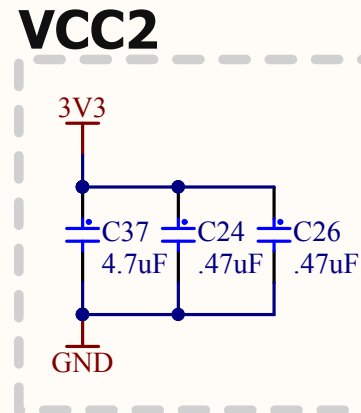
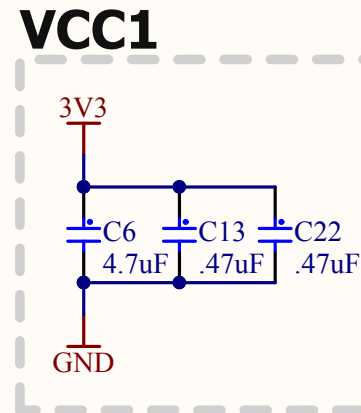
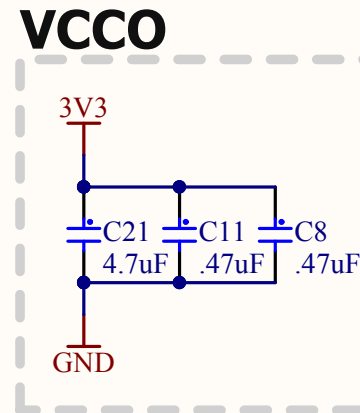
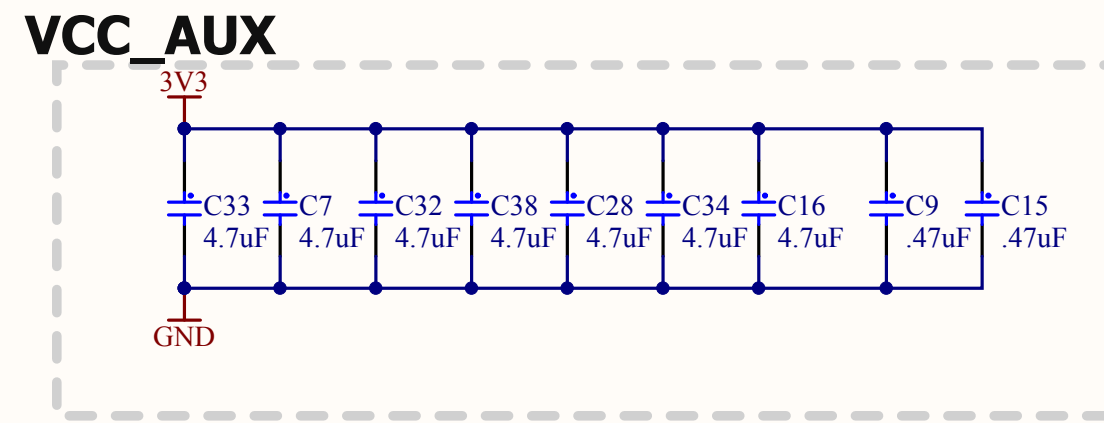
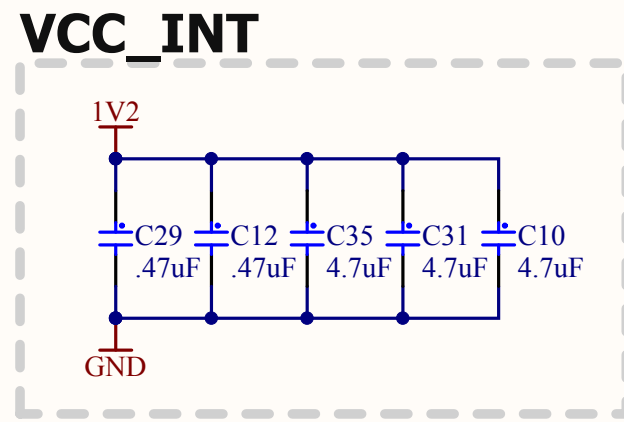
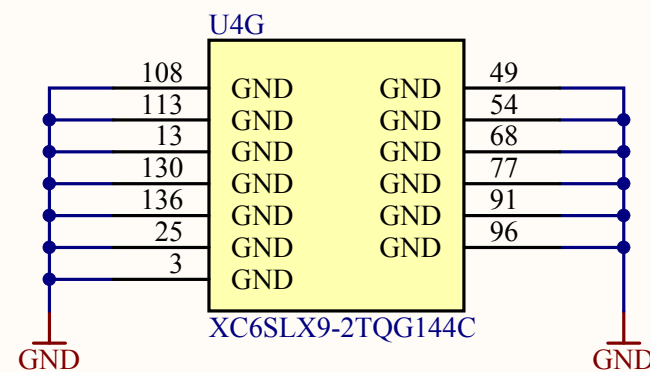
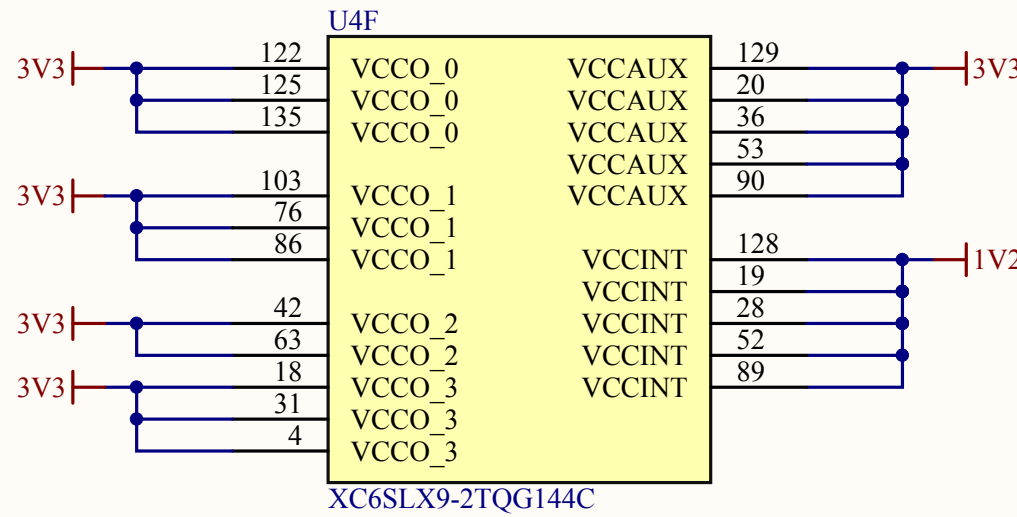
Optionally power can be supplied through FPGA VIN header J1.



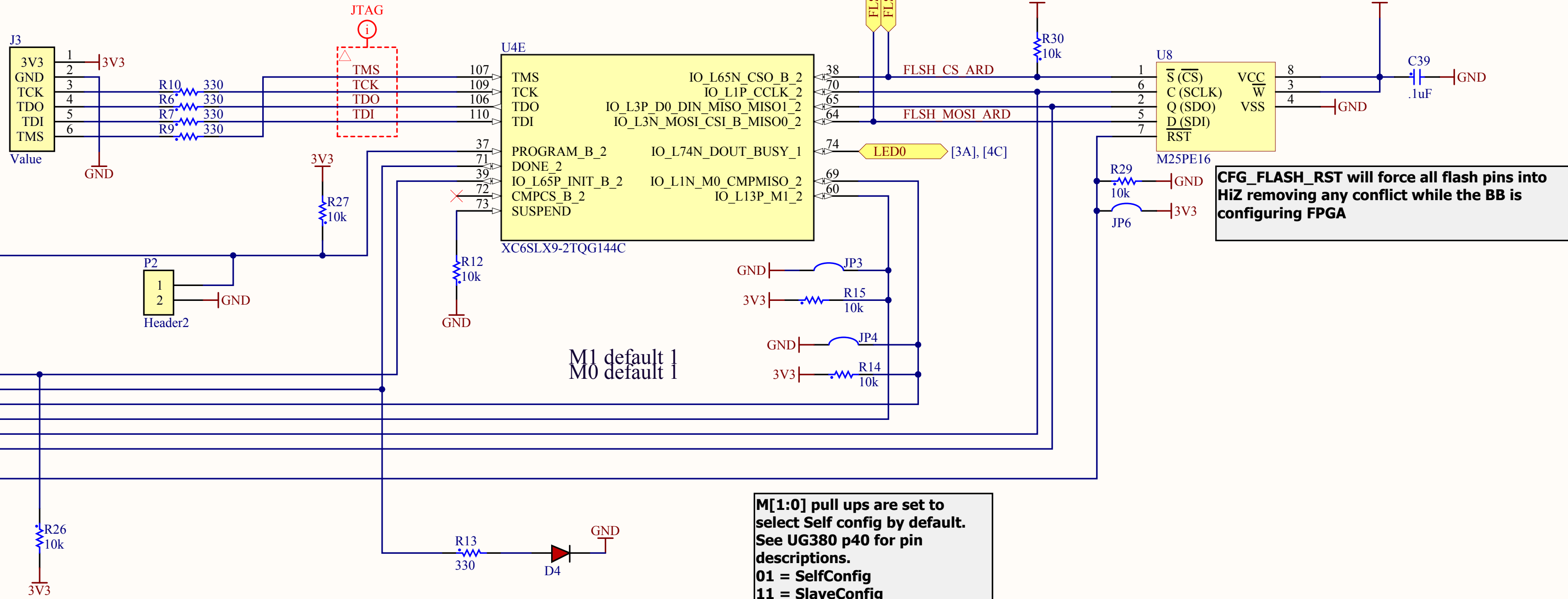
1 x Auxillary Power output Headers



LOGI-LOGO-600
LOGO3
VALENTFX-LOGO-750
Logo5
LOGI-LOGO-750
LOGO4



Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution



CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

