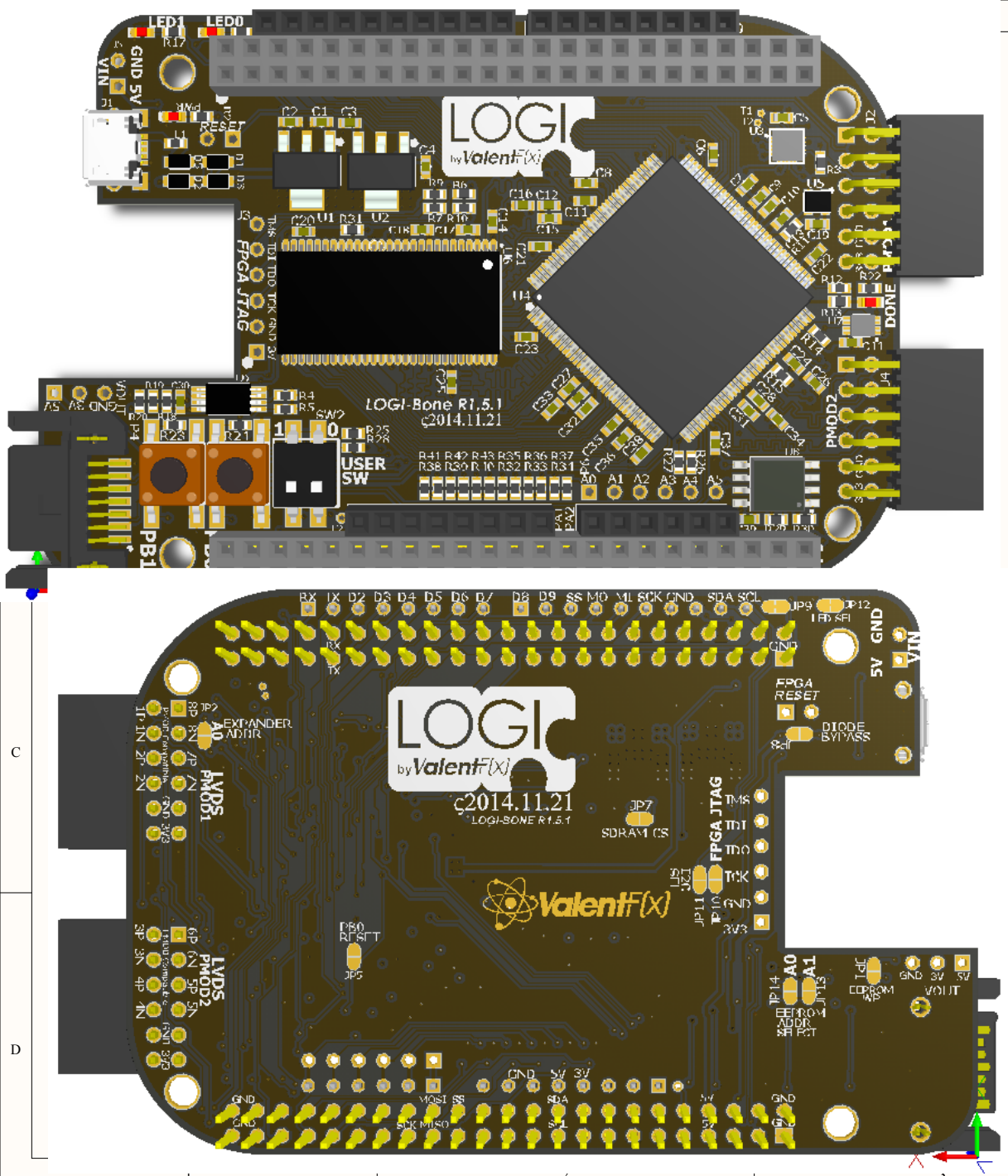


U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

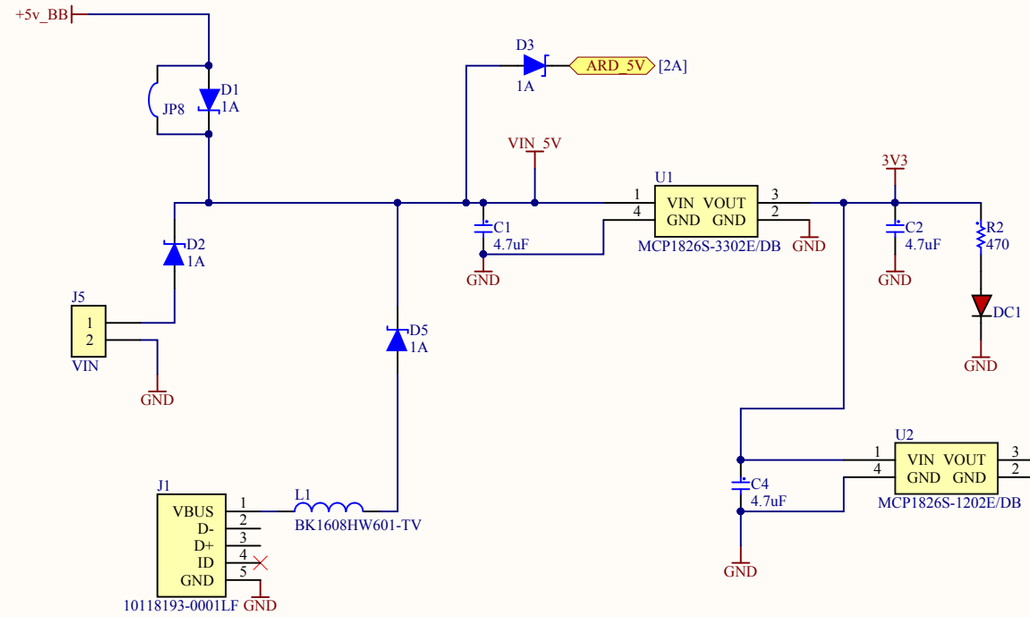
U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

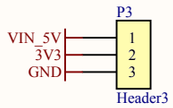
i-Bone Top Level		
	Sheet 1 of 7	ValentF(x) ELECTRONICS INNOVATION
2015	Engineer: MJones	

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



1 x Auxillary Power output Headers



VALENTFX-LOGO-500
Logo1

VALENTFX-LOGO-750
Logo5

LOGI-LOGO
LOGO4

Title	Power Supply		
Revision:	R1.0	Sheet	2 of 7
Date:	1/22/2015	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

U4G
XC6SLX9-2TQG144C
GND

U4F
XC6SLX9-2TQG144C
3V3
1V2

VCC_INT
1V2
C29 .47uF, C12 .47uF, C35 4.7uF, C31 4.7uF, C10 4.7uF
GND

VCC_AUX
3V3
C33 4.7uF, C7 4.7uF, C32 4.7uF, C38 4.7uF, C28 4.7uF, C34 4.7uF, C16 4.7uF, C9 .47uF, C15 .47uF
GND

VCCO
3V3
C21 4.7uF, C11 .47uF, C8 .47uF
GND

VCC1
3V3
C6 4.7uF, C13 .47uF, C22 .47uF
GND

VCC2
3V3
C37 4.7uF, C24 .47uF, C26 .47uF
GND

VCC3
3V3
C23 4.7uF, C36 .47uF, C27 .47uF
GND

Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

GPIO Expander - Handling of General Control Pins

U3 SX1505I087TRT
3V3, GND, C5 .1uF, JP2, R3 10k
ADDR, VDDM, VCC1, VCC2, RST#, INT#, SCL, SDA, GND, GND
IO0 CFG_PRGB
IO1 CFG_INITB
IO2 CFG_DONE
IO3 CFG_M1
IO4 CFG_BUF_OE#
IO5 FLSH_RST
IO6 T1
IO7 T2
4[3C], 5[2C] SYS_SCL
4[3C], 5[2C] SYS_SDA

J3
3V3, GND, TCK, TDO, TDI, TMS
Value
R10, R11, R8, R9 220

JTAG
TMS, TCK, TDO, TDI

U4E
XC6SLX9-2TQG144C
TMS, TCK, TDO, TDI
IO_L65N_CSO_B_2
IO_L1P_CCLK_2
IO_L3P_D0_DIN_MISO_MISO1_2
IO_L3N_MOSI_CSI_B_MISO0_2
PROGRAM_B_2
DONE_2
IO_L65P_INIT_B_2
CMPCS_B_2
SUSPEND
IO_L74N_DOUT_BUSY_1
IO_L1N_M0_CMPMISO_2
IO_L13P_M1_2

FLSH_MOSI [3A] [3B]
FLSH_CS
CFG_CLK_ARD13
CFG_DIN_ARD11
FLSH_CS_ARD
FLSH_MOSI_ARD
LED0 [3A], [4C]

U8
S25FL032P0XMFI011
S (CS), C (SCLK), Q (SDO), D (SDI), RST, VCC, W, VSS
C39 .1uF
R30 10k
R29 10k
FLSH_RST_7

CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

FPGA_RST
CFG_PRGB
P2 Header2
R26 10k, R27 10k
R12 10k

M1 Strong pull down needed when expander is in reset

3V3, JP3, R15 470
R14 10k

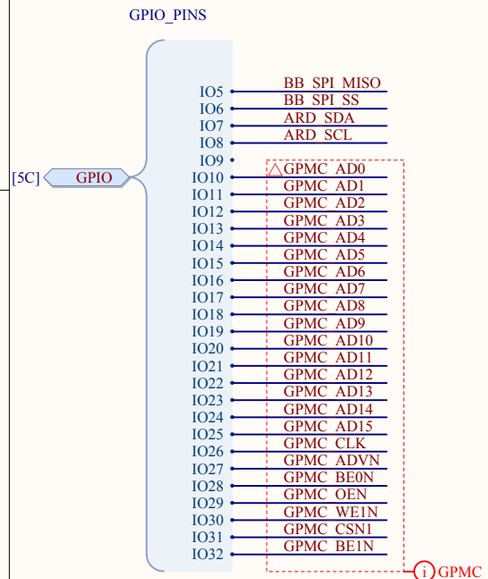
Self Config by default.
- When host is use, it will pull M1 high to force slave config using GPIO expander.
- Even though self config is default, the FPGA will not configure if a bistream is not stored in flash.

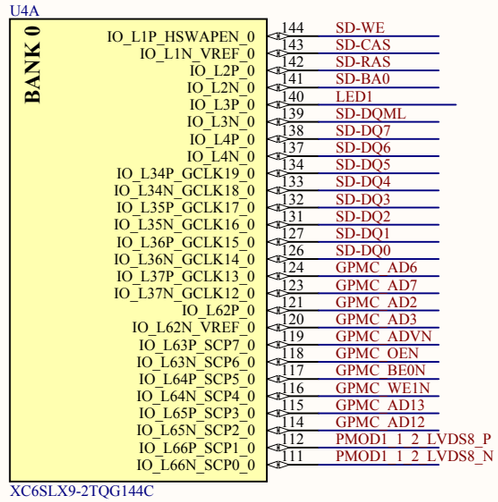
U7 NC7WZ125K8X
C44 .1uF, R22 10k
CFG_BUF_OE#
BB_SPI_MOSI_DIN
BB_SPI_SCK_CCLK
[5C] ARD_MOSI/CFG_INITB → CFG_INITB
CFG_DONE
[5C] ARD_TX_CFG_MODE0 → CFG_M0
[5C] ARD_RX/CFG_MODE1 → CFG_M1
CFG_SCK
R13 470, D4

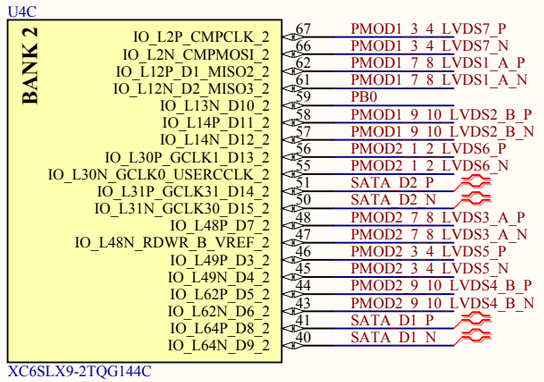
M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

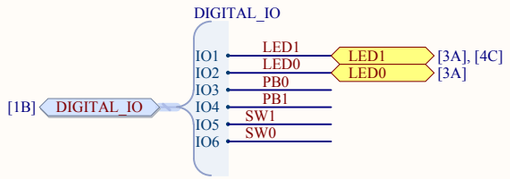
Title	FPGA Configuration		
Revision:	R1.0	Sheet	3 of 7
Date:	1/22/2015	Engineer:	MJones

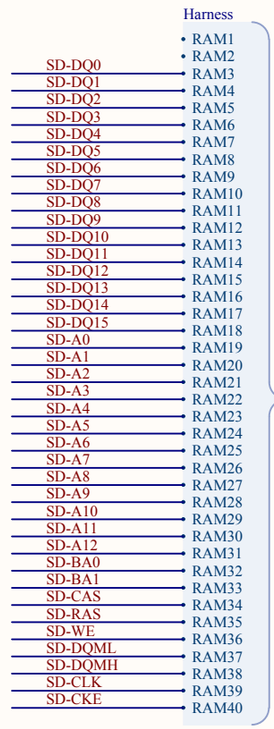
ValentF(X) ELECTRONICS INNOVATION

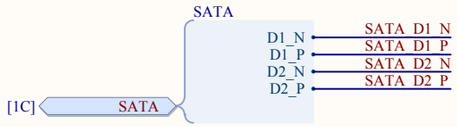


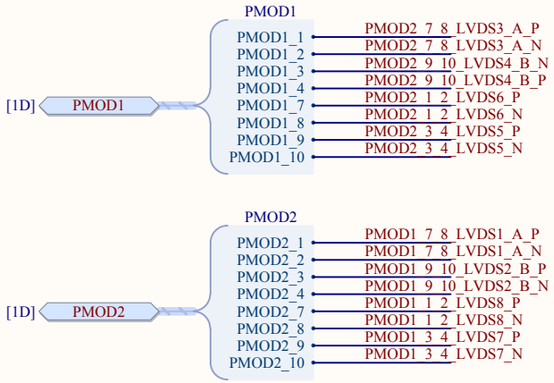


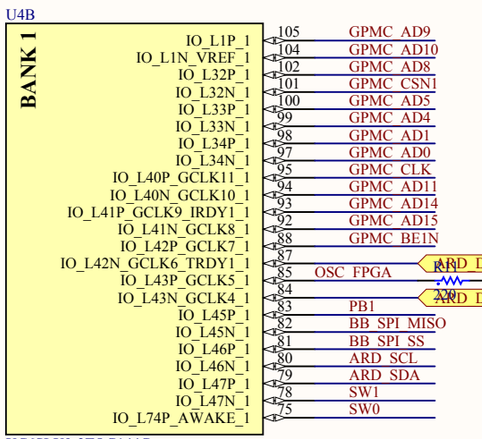




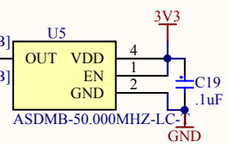


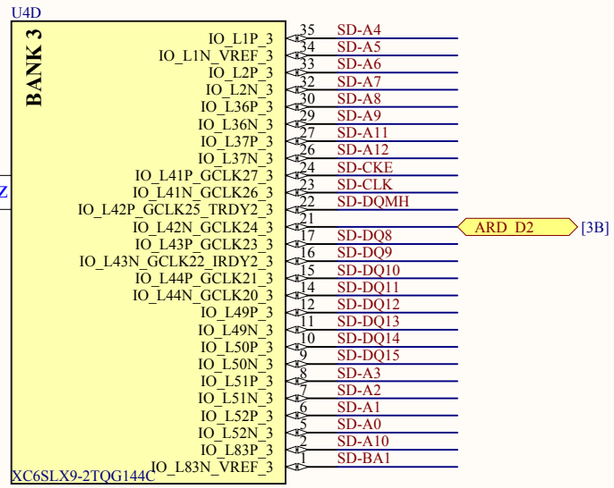






FPGA EXT Oscillator: 50Mhz

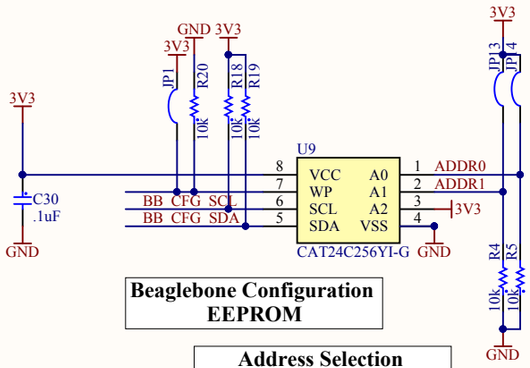




Title	FPGA Logic		
Revision:	R1.0	Sheet	4 of 7
Date:	1/22/2015	Engineer:	MJones

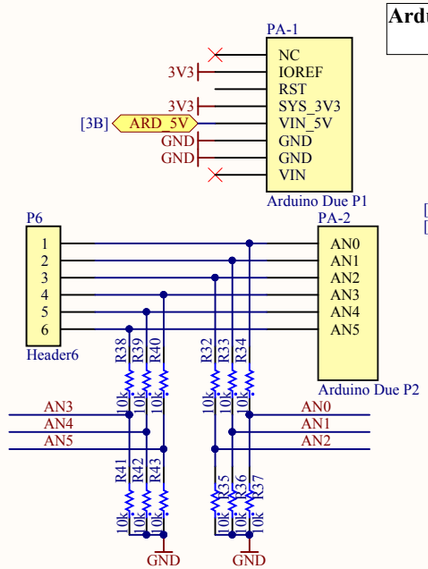
ValentF(x) ELECTRONICS INNOVATION

Beaglebone Configuration EEPROM

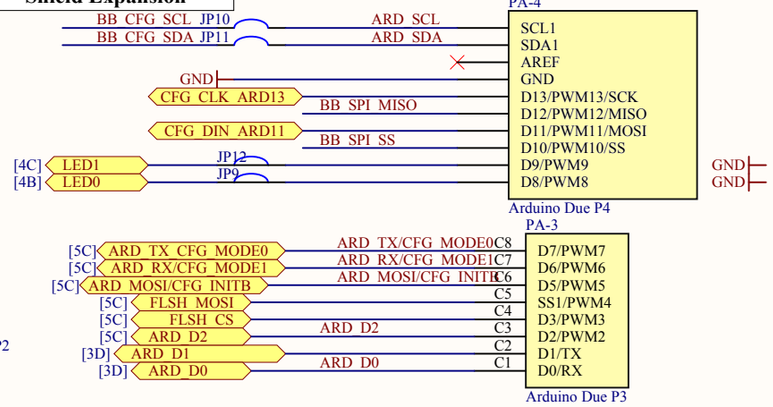


Address Selection DIP SW

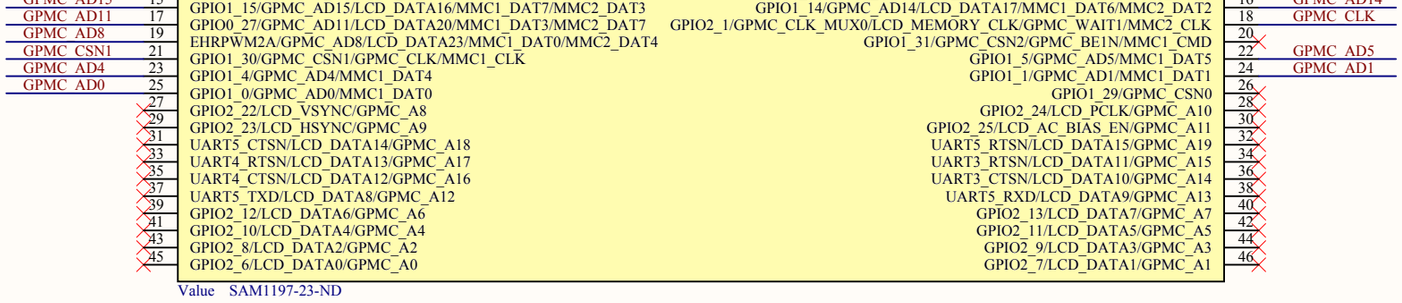
If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed of capes



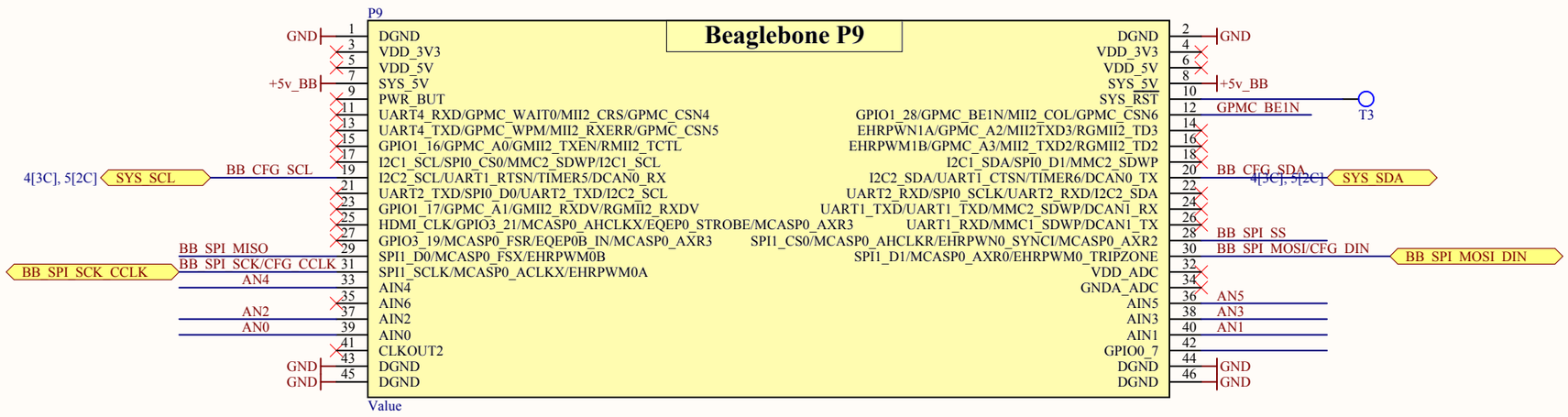
Arduino Header - Arduino Shield Expansion

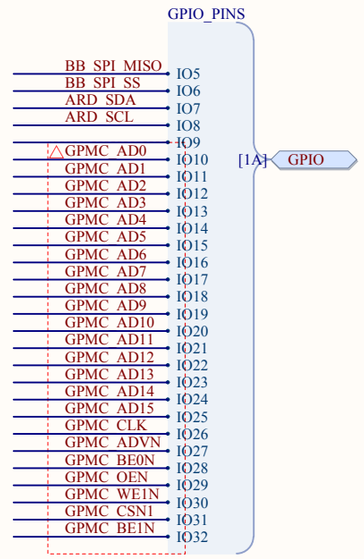


Beaglebone P8



Beaglebone P9

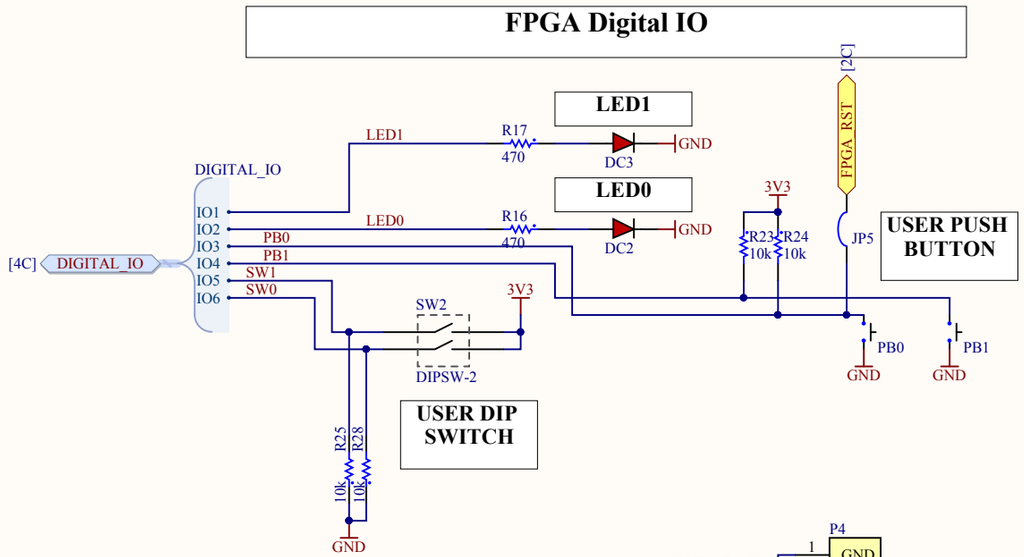


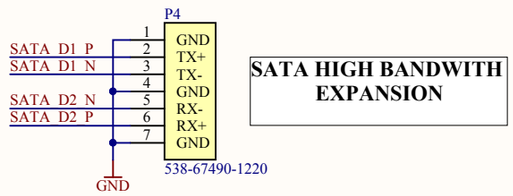


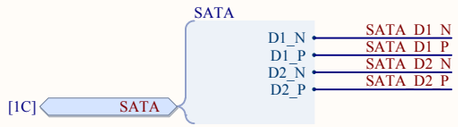
Title	Peripheral Port IO		
Revision:	R1.0	Sheet	5 of 7
Date:	1/22/2015	Engineer:	MJones

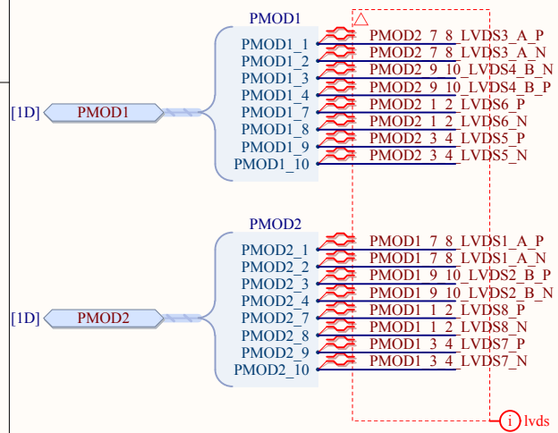
ValentF(x) ELECTRONICS INNOVATION

FPGA Digital IO

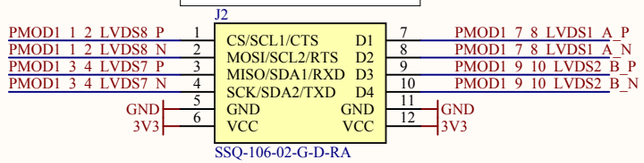




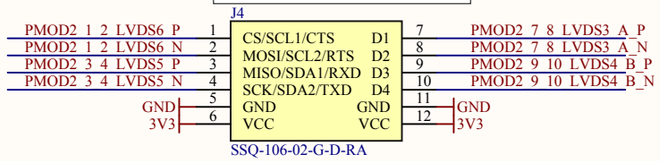




PMOD1 PORT



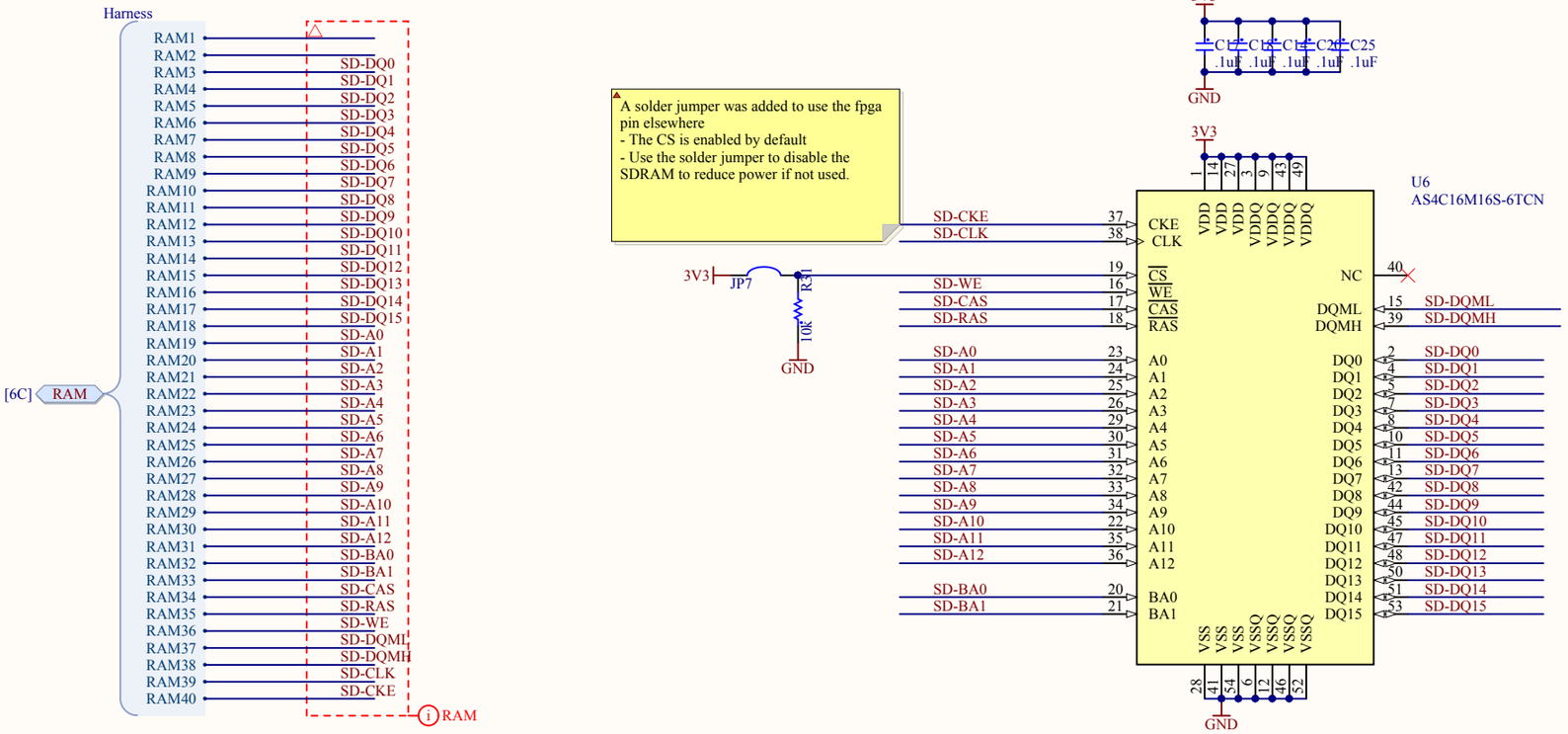
PMOD2 PORT



Title	Digital IO		
Revision:	R1.0	Sheet	6 of 7
Date:	1/22/2015	Engineer:	MJones

ValentF(X) FLECTRONICS INNOVATION

SDRAM



Title	RAM		
Revision:	R1.0	Sheet	7 of 7
Date:	1/22/2015	Engineer:	MJones

ValentF(x) ELECTRONICS INNOVATION