

# Course Overview

## Computer Organization

Adapted from Ricardo Chaves



**TÉCNICO** LISBOA

# The Computer Revolution

- Progress in computer technology
  - Reinforced by Moore's Law
- Makes novel applications feasible
  - Computers in automobiles
  - Cell phones
  - Human genome project
  - World Wide Web
  - Search Engines
- Computers are pervasive

# Classes of Computers

- Desktop
    - single user, general purpose, with a typical set up of display, keyboard, and mouse
- Critical: cost, performance

# Desktop Computer



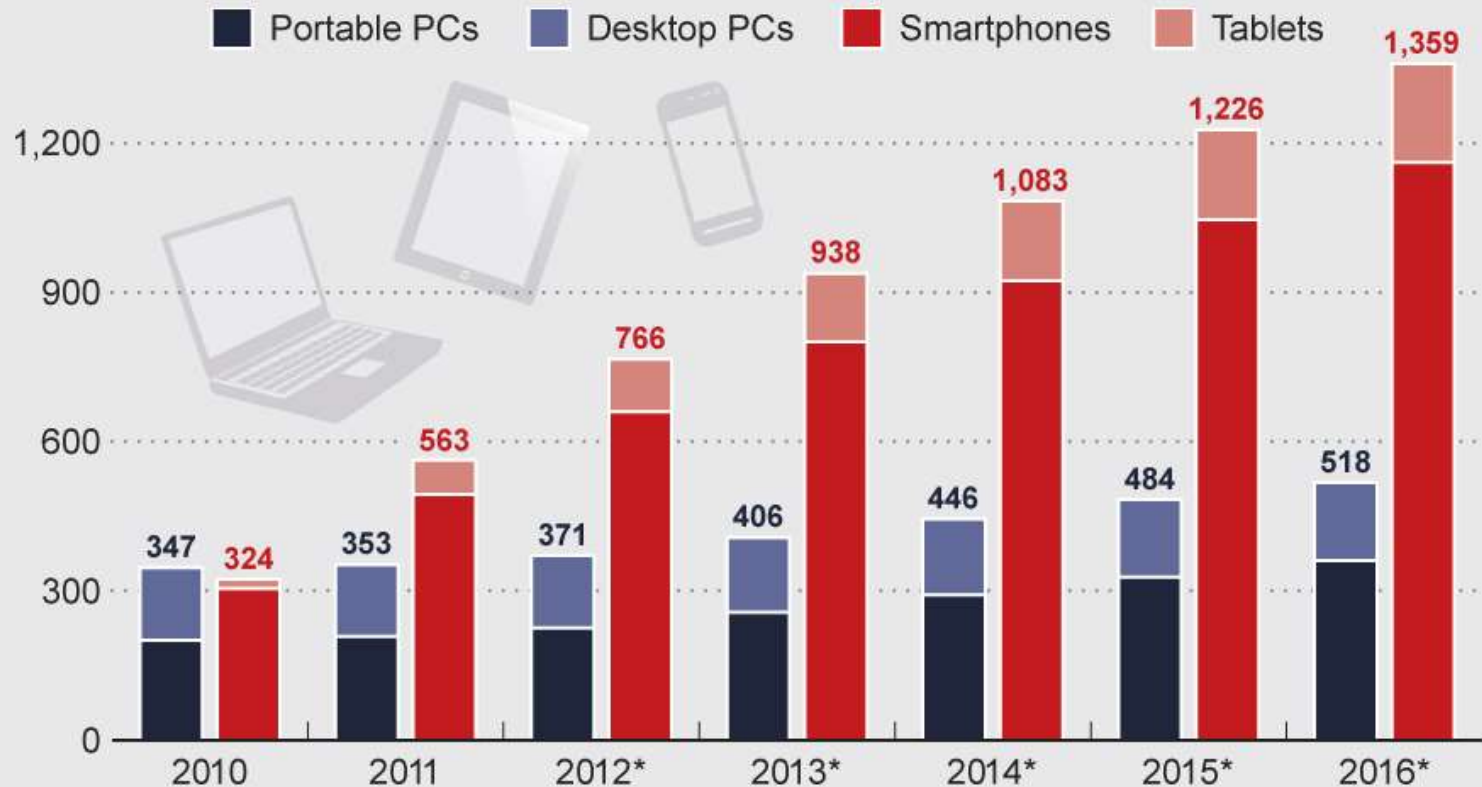
# Classes of Computers

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  - Critical: **cost, performance**
- Personal Mobile Device (PMD)
  - single user, general purpose, small-size touchscreen
  - Critical: **power, cost**

# The Post-PC Era

## The Post-PC Era Has Arrived

Global smartphone, tablet and PC shipments (in millions)



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- Servers
  - run larger programs in parallel for multiple users, typically accessed remotely
  - Critical: performance, capacity, security, reliability

# Server



Server

Rack





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- Supercomputers
  - clusters with hundreds to thousands of processors, terabytes of memory and petabytes of storage
  - Critical: performance, capacity, expandability

# Supercomputer



**Summit**, an IBM-built supercomputer  
running at the Department of Energy's (DOE)

Currently the world most powerful supercomputer  
(4,356 nodes each with 22-core Power9 and 6 NVIDIA Tesla V100 GPUs)  
with a performance of **122.3 petaflops**

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- Embedded
  - hidden component of a system, running a predefined program
  - Critical: **cost, power, performance**

# Embedded Computers



Over 99% of processor sales are for embedded systems!

# Issues in Embedded Systems

Specific issues when programming embedded systems:

- Real-time requirements
  - Often worst-case is more important than average-case
- Resource constraints
  - Power and memory
- Reliability
  - Safety critical systems
  - Difficult access
- Diversity
  - Heterogeneity of computing architectures
  - Diverse set of input/output devices

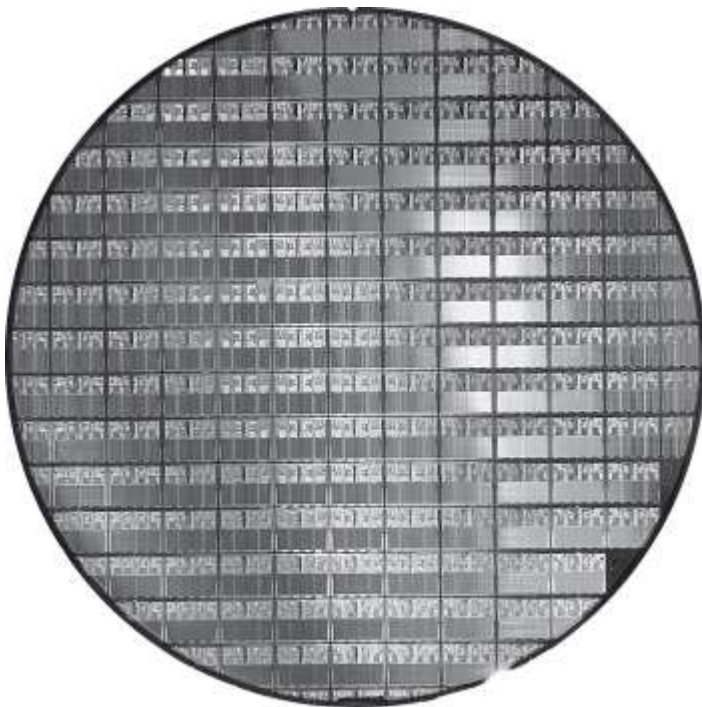
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# Technology Trends

- The transistor density increases about 35% per year.
- The circuits area increases about 10% to 20% per year.
- The number of transistors per circuit increases about 55% per year.

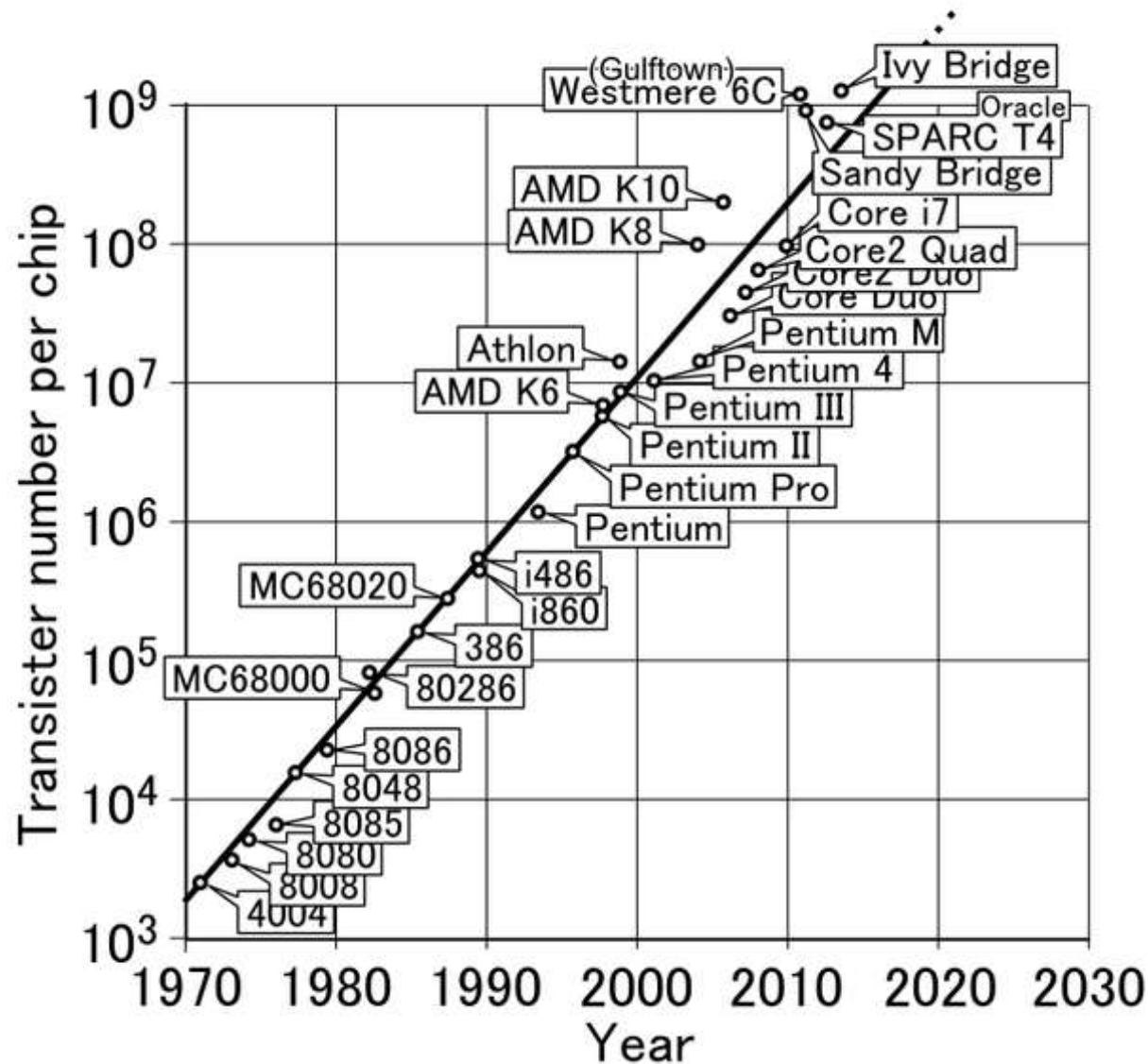


## Moore's Law (1965):

“The number of transistors per square-centimeter of integrated circuit doubles every 18 months.”

- In practice, the density increased about 1,000,000x in the last 45 years!

# Moore's Law in Practice

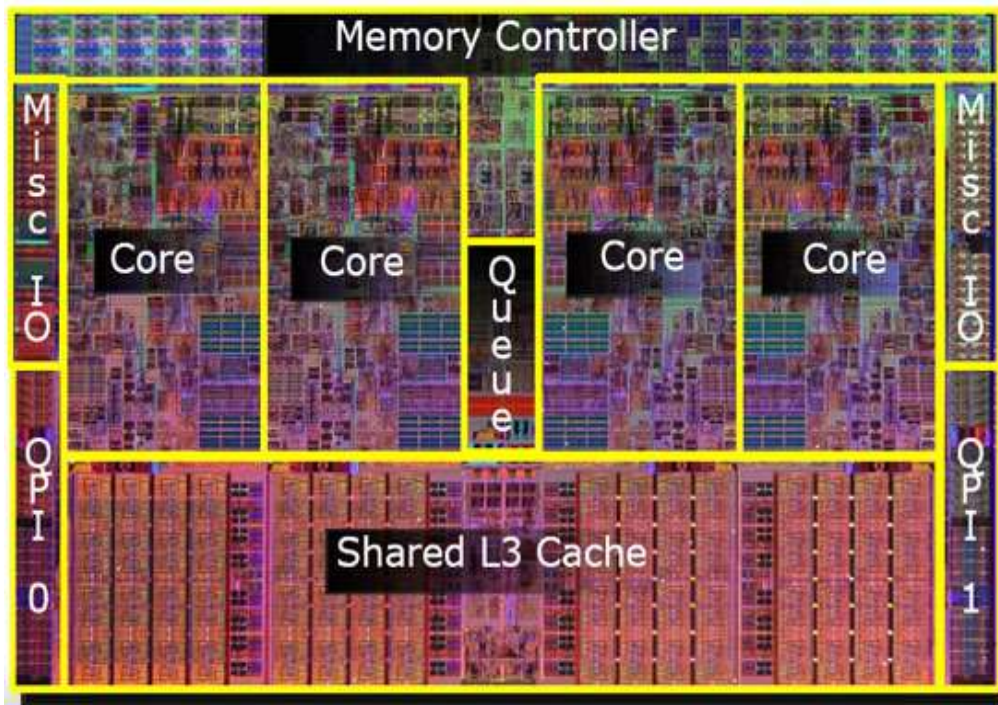




# Inside the Processor

Intel Core i7:

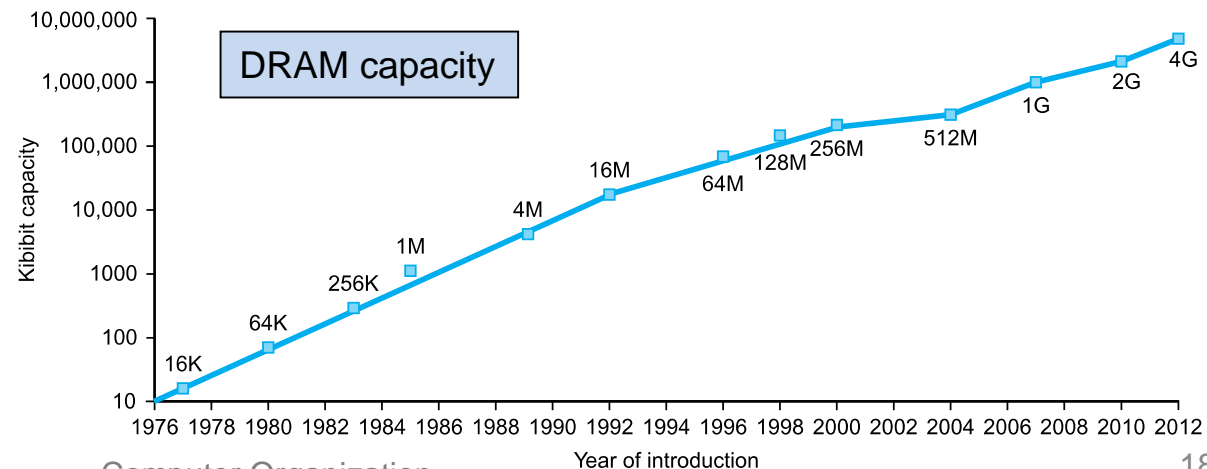
4 processor cores,  $1.3 \times 10^9$  transistors



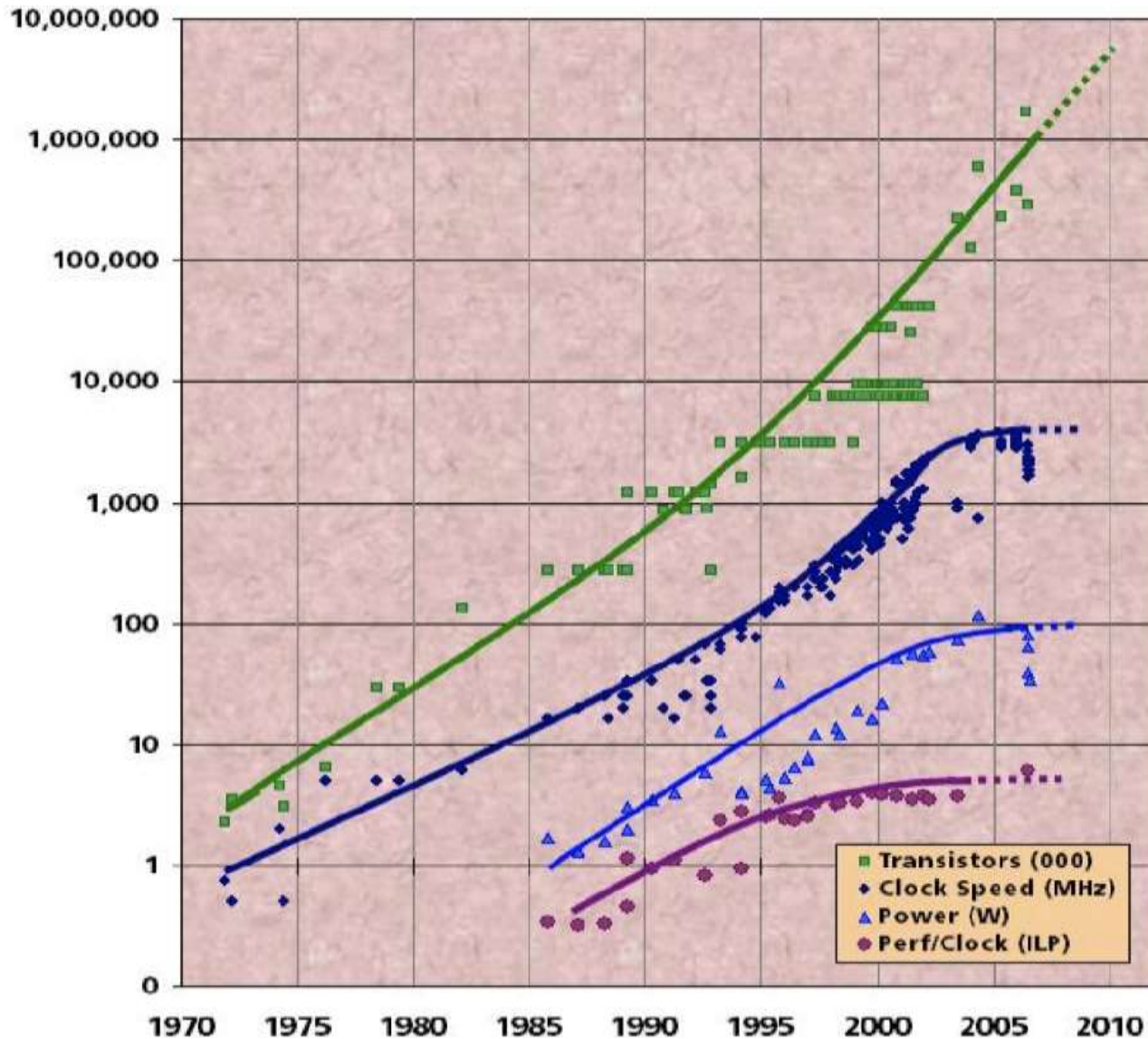
# Technology Trends

Year	Technology	Relative performance/cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit (IC)	900
1995	Very large scale IC (VLSI)	2,400,000
2013	Ultra large scale IC	250,000,000,000

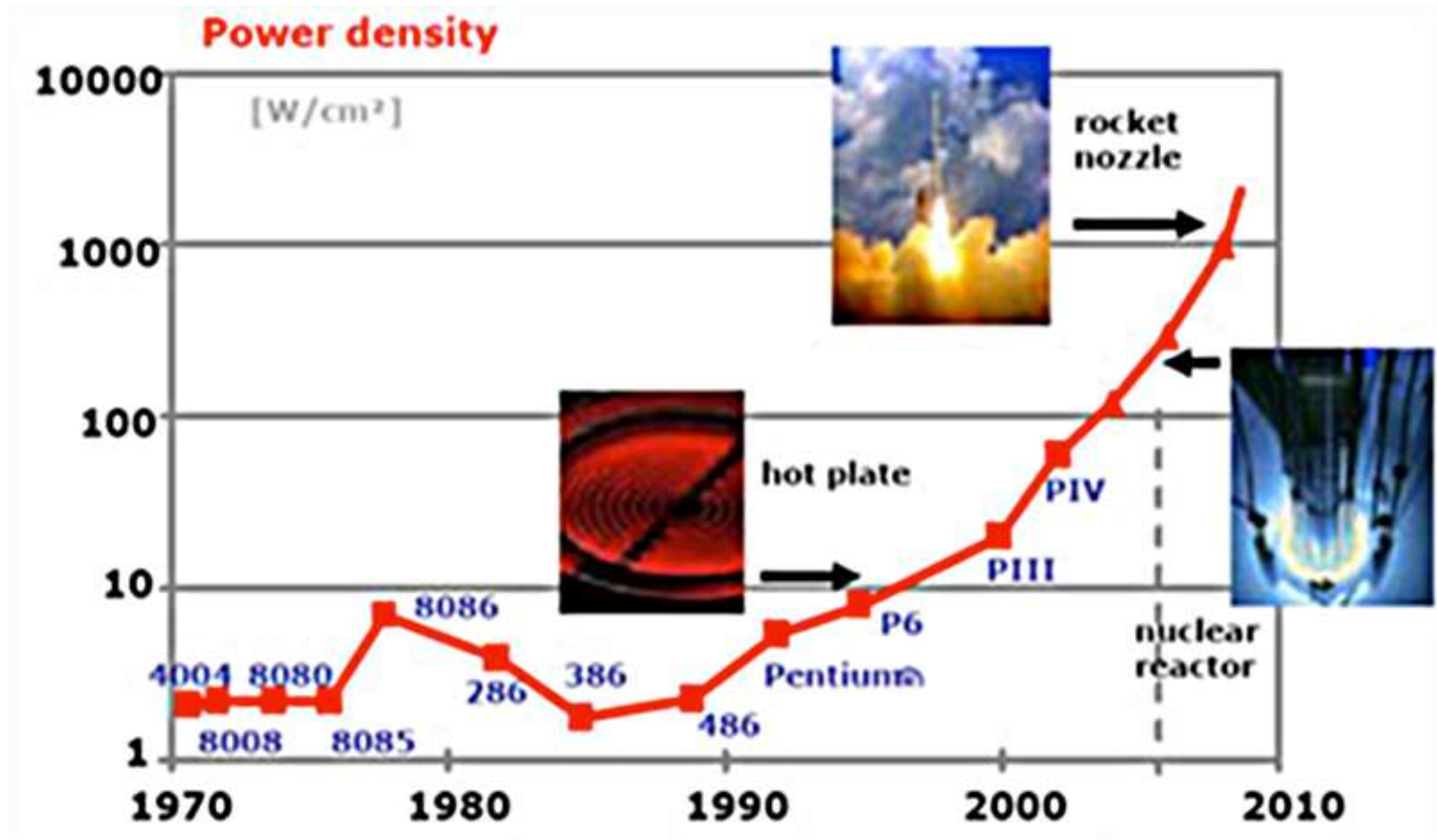
- Electronics technology continues to evolve
  - Increased capacity and performance
  - Reduced cost



# Technology Trends



# Power Density



# Power Trends

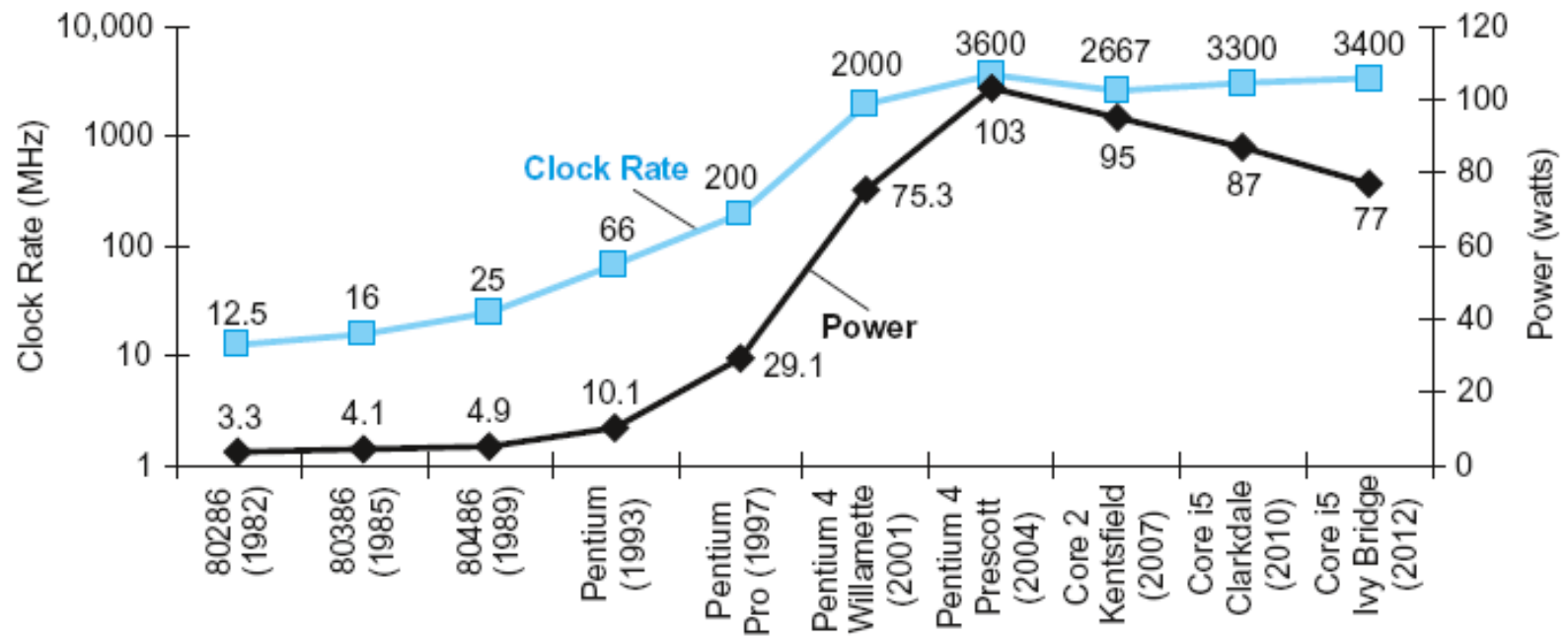
In CMOS IC technology

$$\text{Power} = \text{Capacitive load} \cdot \text{Voltage}^2 \cdot \text{Frequency}$$

×30

5V → 1V

×1000



The power wall!



# Multiprocessors

The power wall:

- can't reduce voltage further
- can't remove more heat

How else can we improve performance?

➔ **Multicore microprocessors**

- More than one processor per chip

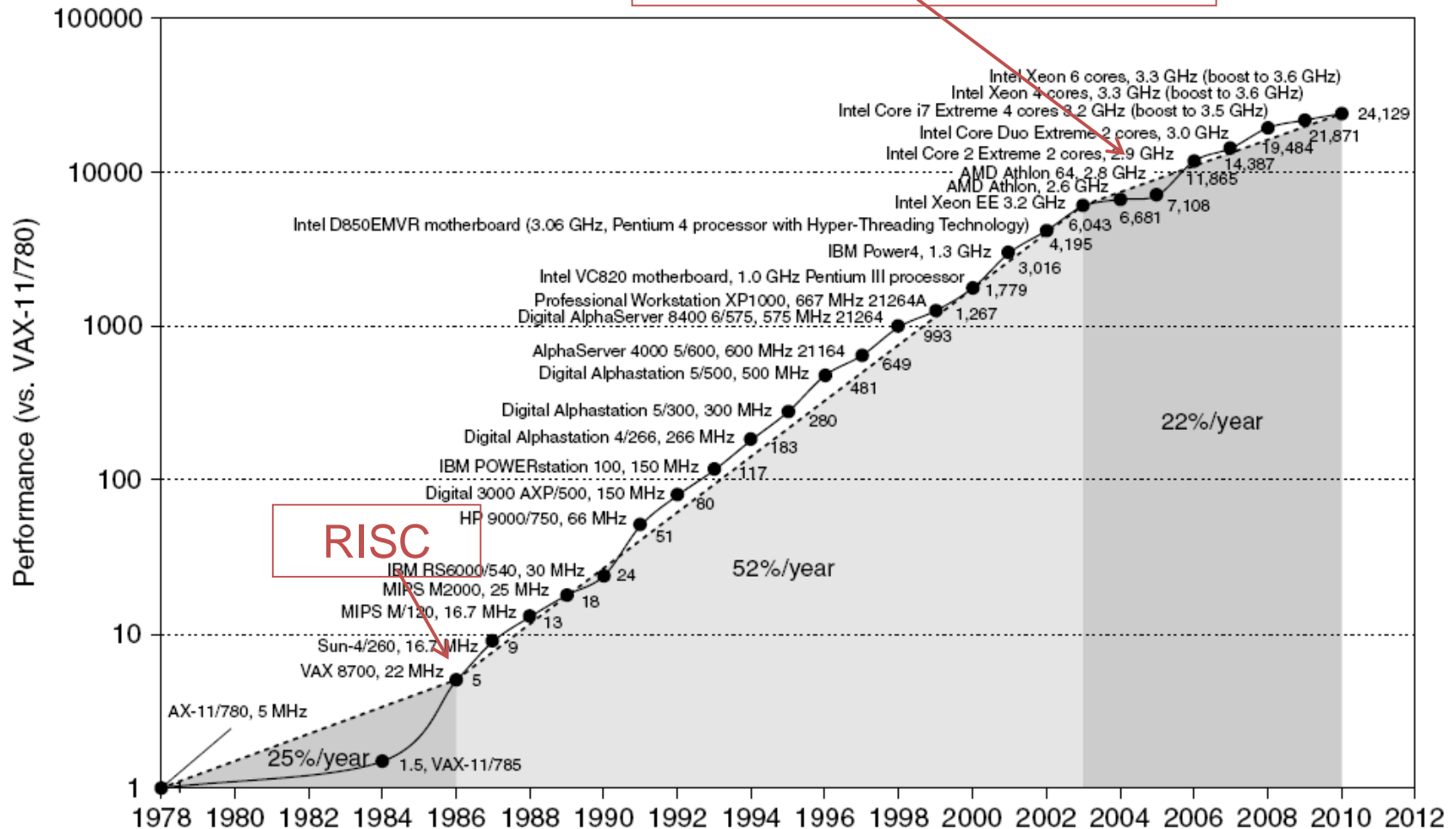
New paradigm!

Requires explicitly parallel programming:

- Compare with instruction level parallelism
  - Hardware executes multiple instructions at once
  - Hidden from the programmer
- Hard to do
  - Programming for performance
  - Load balancing
  - Optimizing communication and synchronization

# Processor Performance

Move to multi-processor



# Trends in Technology

- Integrated circuit technology
  - Transistor density: 35%/year
  - Die size: 10-20%/year
  - Integration overall: 40-55%/year
- DRAM capacity: 25-40%/year (slowing)
- Flash capacity: 50-60%/year
  - 15-20X cheaper/bit than DRAM
- Magnetic disk technology: 40%/year
  - 15-25X cheaper/bit than Flash
  - 300-500X cheaper/bit than DRAM



# Bandwidth and Latency

- Bandwidth or throughput
  - Total work done in a given time
  - 10,000-25,000X improvement for processors
  - 300-1200X improvement for memory and disks
- Latency or response time
  - Time between start and completion of an event
  - 30-80X improvement for processors
  - 6-8X improvement for memory and disks

# What You Will Learn

- Architecture of current processors
  - Performance metrics
- Integrated view of the computer system
  - Memory hierarchy
  - Input/Output system
- How to improve program performance
- Features related to embedded systems
- What is parallel processing
- Future trends

# Teaching Staff

## Theoretical lectures:

Alberto Cunha

`alberto.cunha@tecnico.ulisboa.pt`

Sub:[OC] ...

## Practice/Lab classes:

David Martins

## Course email:

[oc-a-leic@tecnico.ulisboa.pt](mailto:oc-a-leic@tecnico.ulisboa.pt)

Sub:[OC] ...

# Class Schedule

	Seg 9/21	Ter 9/22	Qua 9/23	Qui 9/24	Sex 9/25	Sáb 9/26	Dom 9/27
07:00							
08:00							
09:00							
10:00			10:00 - 11:30 T A4				
11:00							
12:00	11:30 - 13:00 T A4						
13:00							
14:00	14:00 - 15:30 L 1 - 15			14:00 - 15:30 L 1 - 15			
15:00							
16:00	15:30 - 17:00 L 1 - 15	15:30 - 17:00 L 1 - 15					
17:00							
18:00							

- L shifts are currently almost full.
- We are waiting for indications from the Taguspark management (more capacity and, possibly, other rooms → [check OC page](#)).

# Grade assessment

Final grade = 50% x Exam + 24% x Labs + 26% x Exercises

- Exam =  $\max(\text{Ex\_1}, \text{Ex\_2})$  , Min. grade = 7
- Labs =  $(L1 + L2 + L3) / 3$  , Min. grade = 9
- Exercises =  $(\sum 5 \text{ best } P\_i) / 5$  , Min. grade = 9

## Exam (50%):

- 1<sup>st</sup> Exam: January 11, 9h30
- 2<sup>nd</sup> Exam: February 3, 15h00
- minimum grade in the exam  $\geq 7$
- recovery exam can be used to improve grade (best grade used).

# Grade assessment: Labs

## Labs (25%)

- 3 lab works, 8% each
  - groups of 3 elements (odd or even)
  - lab grade defined individually at the oral discussions
  - minimum grade of 9
  - can be reused from the last 2 years (2018/2019 and 2019/2020)
- 
- Important dates (weeks):
    - Publication Lab1 & 2 : 12 Oct
    - Delivery of Lab 1 : 19 Oct
    - Publication Lab3 : 2 Nov
    - Delivery of Lab 2 : 9 Nov
    - Defense of Labs 1 & 2 : 16 Nov
    - Delivery of Lab 3 : 30 Nov
    - Defense of Lab 3 : 7 Dec

# Grade assessment: Exercises

## Exercises (25%)

- 6 exercises, counting the best 5
  - Starting from the 3<sup>rd</sup> practical class
  - Handwritten, 2 submissions by each student in the group
- groups of 3 elements (odd or even)
  - Does not have to be the same group as the one for the labs (but highly recommended)
    - Can be separate groups. especially for those that already have the grade for the labs (from the previous 2 years)
- the grade is defined individually at the oral discussions
  - 3 during the semester (each discussion will consider 2 exercises)
  - Zoom authenticated via IST, and with camera ON
  - Can be in-person, rather than remote
- minimum grade of 9
- All students must do it. (NEW. Exercises are not TPCs of 2019/20.)

# Lectures

## Theoretical lectures:

- Remote lectures via Zoom
  - Do use your cameras...
  - Lectures are interactive
- First 3 weeks
  - 1h30 lecture
- Following weeks
  - 1h00 lecture
  - 30 min exercise solving



# Teaching logistics

## Theoretical lectures

- Remote via zoom
  - With camera on, please!!
  - We need some visual feedback

## Practice/Lab lectures

- Hybrid (in-person + zoom + discord)
- David Martins

# Bibliography

## Main book:

*Computer Organization and Design: The Hardware/Software Interface*

D. Patterson, J. Hennessy

Morgan Kaufmann, 5<sup>th</sup> Edition, 2014, ISBN: 978-0-12-407726-3

## Secondary Bibliography:

- *Structured Computer Organization*  
A. Tanenbaum, T. Austin  
Prentice-Hall, 6<sup>th</sup> Edition, 2013, ISBN: 978-0273769248
- *Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools*  
J. Fisher, P. Faraboschi, C. Young  
Morgan Kaufmann, 4<sup>th</sup> Edition, 2005, ISBN: 978-1558607668
- *Computer Architecture: A Quantitative Approach*  
J. Hennessy, D. Patterson  
Morgan Kaufmann, 5<sup>th</sup> Edition, 2011, ISBN: 978-0123838728

# Next Class

- Review of basic concepts on computer architecture
- Performance metrics

# Course Overview

Computer Organization



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