INSTITUTO SUPERIOR TÉCNICO

DEPARTAMENTO DE ENGENHARIA INFORMÁTICA

ORGANIZAÇÃO DE COMPUTADORES

LEIC

Conjunto de Exercícios II

Métricas de Desempenho

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Exercise 1

A design optimization was applied to a computer system in order to increase the performance of a given execution mode by a factor of 10. The optimized mode is used 50% of the time, measured as a percentage of the execution time *after* the optimization has been applied.

(a) What is the global speedup value that is achieved with this optimization?

Remind: Amdahl's law defines the global speedup as a function of the optimized fraction *before* the optimization is applied. As a consequence, the 50% ratio cannot be directly used to evaluate this speedup value.

(b) What is the percentage of the original execution time that is affected by this optimization?

(c) How much should such execution mode be optimized in order to achieve a global speedup of 11?

Exercise 2 *

Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	3 GHz	1.5
P2	2.5 GHz	1.0
P3	4 GHz	2.2

(a) Which processor has the highest performance expressed in instructions per second?

(b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

(c) We are trying to reduce the execution time of the program by increasing the clock speed but this leads to an increase of 20% in the CPI. What clock rate is necessary to get a time reduction of 30%?

Exercise 3 †

The following table shows the number of instructions for a program.

Arith	Store	Load	Branch	Total
650	100	600	50	1400

(a) Assuming that arithmetic instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?

(b) Find the CPI for the program.

(c) If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

*Exercises 1.3.1—1.3.3 from [1].
†Exercises 1.4.4—1.4.6 from [1].

Exercise 4 [‡]

Consider two different implementations of the same instruction set architecture. There are four classes of instructions: A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

Processor	Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	2.5 GHz	2	1.5	2	1
P2	3 GHz	1	2	1	1

(a) Consider a program executing 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D. Determine which implementation is faster.

(b) What is the global CPI for each implementation?

(c) Find the clock cycles required in both cases.

References

[1] David Patterson and John Hennessy. *Computer Organization and Design: The Hardware/Software Interface*. Morgan Kaufmann, 4^{th} edition, 2011.

[‡]Exercises 1.4.1—1.4.3 from [1].