YUEPENG FAN

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RESEARCH INTERESTS

VLSI, machine learning accelerators, efficient and flexible hardware, design methodology

EDUCATION

KAIST, Daejeon, Korea *Aug. 2016 – Aug. 2018*

- M.S. in Electrical Engineering (GPA 3.91/4.3)
- Advisor: Prof. Youngsoo Shin
- Thesis: Accurate Wirelength Prediction for Placement Driven Synthesis through Machine Learning

Seoul National University, Seoul, Korea *Aug. 2015 – Jan. 2016*

- Non-Degree exchange program in Electrical and Computer Engineering

Harbin Institute of Technology, Harbin, China *Aug. 2012 - Jul. 2016*

- B.S. in Electrical Engineering and Automation

RESEARCH AND PROJECTS

Display driver integrated circuit(DDIC) design
Associate Researcher, MS R&D Center, Silicon Works, Korea *Sep. 2018 - present*

- Optimized a corner notch IP size and power by merging similar sub-blocks and adding clock gating logic, reducing the size from 900,000 to 100,000 gates and the power consumption from 5 mW to 2 mW.
- Designed a new IP that aimed to compensate for the image in corner, notch, or hole area by adding a flexible memory controller and color compensation logic to eliminate jaggedness and color fringe and match or exceed the image quality of competitor companies.
- Optimized serial peripheral interface(SPI) by modifying the finite state machine and memory controller to make it compatible with Flash from various vendors and interconnect it with specific memory and registers under users' control, not fixed as past.
- Wrote scripts in Bash and Python for verification to enable designers to efficiently check simulation results and work on different tasks simultaneously to accelerate the design process.
- Attended numerous mass production projects that have been assembled in mobile phone models, such as the Samsung M51, LG Wing, and LG Velvet.

Machine learning-based path length estimation
Research Assistant, uComputing Lab, KAIST, Korea *Sep. 2017 - Aug. 2018*

- Proposed an algorithm to predict the path length of critical paths based on virtual placement generated by the Synopsys Design Compiler Graphical and constraint information from designers using machine learning techniques.
- Proposed an algorithm to select and combine different regressors, including neural network, support vector machine, and random forest techniques.

Automatic synthesis of clock gating through detection of cyclic paths
Research Assistant, uComputing Lab, KAIST, Korea *Jul. 2017 - Feb. 2018*

- Designed an algorithm to automatically implement clock-gating synthesis on cyclic paths by extracting gating logic, simplifying combinational logic, and grouping registers. Achieved a 18% and 22% greater power reduction compared with RTL clock gating and conventional gate-level clock gating, respectively.

Gate level power estimation
Research Assistant, uComputing Lab, KAIST, Korea *Dec. 2016 - May 2017*

- Designed an algorithm to calculate leakage power, internal power, and switching power according to the gate netlist and other technique information, which also worked in multiple voltage mode.

FPGA-based timing control system design
Graduate Thesis, Harbin Institute of Technology, China *Feb. 2016 - Jul. 2016*

- Designed graphical user interface with LabVIEW and a serial communication model to transfer users' control information, as well as a signal processing model aimed to generate delayed signals.

PUBLICATIONS

International Conferences

[1] Daijoon Hyun, *Yuepeng Fan*, and Youngsoo Shin, "Accurate wirelength prediction for placement-aware synthesis through machine learning," Proc. Design, Automation & Test in Europe (DATE), Mar. 2019

Domestic Journals and Conferences

[1] *Yuepeng Fan*, Daijoon Hyun, and Youngsoo Shin, "Wirelength Prediction of Pre-Placement Netlist Using Machine Learning," 2018 System on Chip Conference, May. 2018 **(Best Paper Award)**

[2] *Yuepeng Fan*, Inhak Han, and Youngsoo Shin, "Automatic Clock Gating Synthesis through Detection of Cyclic Paths," The 25th Korean Conference on Semiconductors, Feb. 2018

AWARDS AND SCHOLARSHIPS

- **Best Paper Award**, 2018 Korean System on Chip Conference *May 2018*
- **China Scholarship Council(CSC) Scholarship** *Aug. 2015 - Jan. 2016*
  Scholarship from the State Scholarship Fund to support study in Seoul National University.
- **First prize in HIT Scientific and Technological Innovation Project** *May 2015*
  Awarded to the winning group for the best-designed products out of 30 teams.
- **First-Class Students Scholarship** (three times) *2012 - 2015*
  Awarded for being among the top 10% students according to GPA.

SKILLS

Computer languages	Verilog HDL, C/C++, Python, and Matlab
Protocols and APIs	Scipy/Numpy, Scikit-learn, and Tensorflow
CAD Tools	NC-Verilog, Design Compiler, IC-Compiler, PrimeTime, and SpyGlass

LANGUAGES

- Chinese: native
- English: fluent (GRE 161(V)+169(Q)+3.5 TOEFL 103)
- Korean: intermediate (TOPIK level 4)