TAG
Variant: [No Variations]

3/1/2018
D1

RELEASED

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .
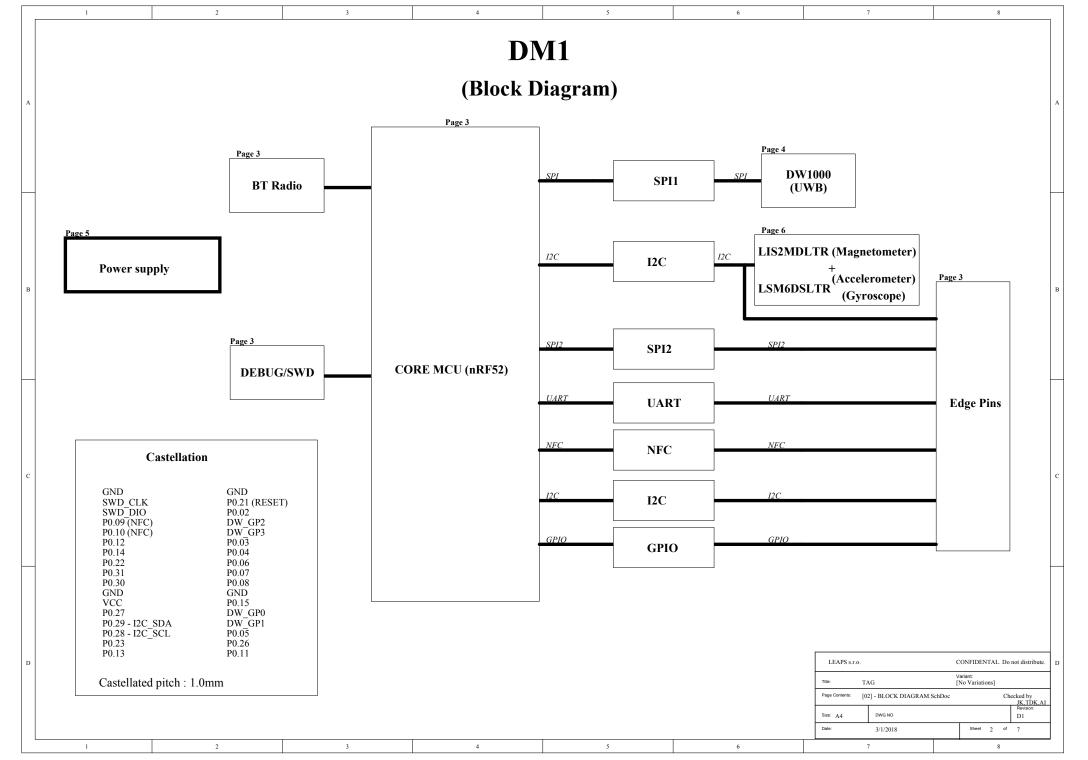
DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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Title: TAG

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[No Variations]

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Checked by
JK,TDK,AI

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DWG NO

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DM1

(Block Diagram)

Page 3

Page 3
BT Radio

Page 5
Power supply

Page 3
DEBUG/SWD

CORE MCU (nRF52)

SPI — **SPI1** — SPI — Page 4 **DW1000 (UWB)**

I2C — **I2C** — I2C — Page 6 **LIS2MDLTR (Magnetometer) + LSM6DSLTR (Accelerometer) (Gyroscope)**

Page 3
Edge Pins

SPI2 — **SPI2** — SPI2

UART — **UART** — UART

NFC — **NFC** — NFC

I2C — **I2C** — I2C

GPIO — **GPIO** — GPIO

Castellation

GND	GND
SWD_CLK	P0.21 (RESET)
SWD_DIO	P0.02
P0.09 (NFC)	DW_GP2
P0.10 (NFC)	DW_GP3
P0.12	P0.03
P0.14	P0.04
P0.22	P0.06
P0.31	P0.07
P0.30	P0.08
GND	GND
VCC	P0.15
P0.27	DW_GP0
P0.29 - I2C_SDA	DW_GP1
P0.28 - I2C_SCL	P0.05
P0.23	P0.26
P0.13	P0.11

Castellated pitch : 1.0mm

Core MCU

L7 15nH
C44 1uF
GND

VCC_DEV
C36 10uF
C46 12pF
GND
GND

L8 10uH

J1
J2

I2C SDA → I2C SDA 6
I2C SCL → I2C SCL 6

IRQ MAG → IRQ MAG 6

P0.27 → J3

P0.26 → J33

32.768KHZ-KCBB
X3
DEC1
C47 100nF
GND

C3 12pF
C6 12pF
GND

U6
NRF52832-CIAA

X1
32.00 MHz - 2CAS

C48 12pF
C49 12pF
GND
GND 100pF C50
C51 100pF
GND

A2 AT3216-B2R7HAAT
2.4GHz

U6 — nRF52832

Pin	Signal
A7	VDD
B6	DCC
A6	DEC4
C5	VSS
C4	VSS
B5	P0.31/AIN7
A5	P0.30/AIN6
A4	P0.29/AIN5
A3	P0.28/AIN4
B4	P0.27
D3	P0.26
B3	P0.25

B7	DEC1
D7	P0.00/XL1
C7	P0.01/XL2
C6	P0.02/AIN0
D6	P0.03/AIN1
E6	P0.04/AIN2
E7	P0.05/AIN3
F7	P0.06
F6	P0.07
G7	P0.08
G6	P0.09
G5	P0.10
C3	N.C.
E3	VSS
F5	VSS

XC2 A1 XC2
XC1 B2 XC1
DEC3 C2 DEC3
DEC2 A2 DEC2
VSS_PA D2
ANT D1 BT RADIO ANT
P0.24 E1
P0.23 E2
P0.22 F2
SWDIO G1 SWDIO
SWDCLK F1 SWDCLK

L9 3.3nH
C52 1pF
GND
BT ANT
NFC53 TBD
GND

DW RST → DW RST 4
IRQ1 → IRQ1 4
IRQ DRDY → IRQ DRDY 4

DESIGN NOTE:
Use for antenna matching.

J6 P0.02
J7 P0.03
J8 P0.04
J34 P0.05
J9 P0.06
J10 P0.07
J11 P0.08
J12 NFC1
J13 NFC2

VDD
P0.11
P0.12
P0.13
P0.14
P0.15
P0.16
P0.17
P0.18
P0.19
P0.20
P0.21/RESET

H7 F4 H6 G4 H5 H4 H3 G3 H2 F3 G2 H1

VCC_DEV
C54 100nF
C55 12pF
GNDGND GND

IRQ1 → J14
P0.22 → J15
SWDIO → J16
SWDCLK → J17
P0.21 → J18
P0.15 → J19
IRQ DRDY → J20
IRQ2 → J21
P0.12 → J22
P0.11 → J32

SH1
RF SHIELD
BMI-S-102
GND

J27
F1 F2
FIDUCIAL FIDUCIAL
GND

SPI1 MISO → SPI1 MISO 4
DW IRQ → DW IRQ 4
SPI1 MOSI → SPI1 MOSI 4
DW CS → DW CS 4
SPI1 CLK → SPI1 CLK 4
IRQ2 → 4

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Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - CORE MCU.SchDoc

Designator
[04] - DW radio.SchDoc

Designator
[05] - Power supply.SchDoc

Designator
[06] - SPI I2C devices.SchDoc

Designator
[07] - DOC REVISION HISTORY.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example

Net Class
ClassName: PCIE

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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DW1000

DESIGN NOTE:
Use test point for high voltage OTP programming
Vmin 3.7V Vmax 3.9V

U1

DW1000

GND
VDDLDO
VBAT
TestMode
IRQn
VDDDIG
VSSIO
VDDIO
SPIclk
SPIMISO
SPIMOSI
GPIO_0
GPIO_1

XTAL1
XTAL2
VREF1
VDDMS
VDDIF
CLKTUNE
VDDCLK
VDDSYN
VDDVCO
VCOTUNE

GPIO_2
GPIO_3
GPIO_4
GPIO_5
VSSIO_1
VDDIO
GPIO_6
SYNC
VDDIOA_1
RSTn
VDDLDO2
VDD_AON

VDDLNA
RF_P
RF_N
VDDPA2
VDDPA1
VDDREG
ExtOn
ForceOn
WakeUp
SPICSn

DW_IRQ
SPI1_CLK
SPI1_MISO
SPI1_MOSI

DW_GP0
DW_GP1

J30
J31

DW_GP2
DW_GP3

J23
J24

GPIO5 — T2

GPIO6 — T3

DW_RST

DW_RST

VCC_DEV

DW_CS
DW_EXTON

DW_CS
DW_EXTON

VDDIO

X2
38.4000MHz-2CAT

GND

C22
12pF

C38
12pF

GND   GND

C7
100nF

C8
100nF

R1
11k

GND   GND

R2
16k

C11
27pF

C12
1.2pF

GND

GND   C10   100nF

C15
100nF

C16
100nF

C13
820pF

R3
270R

C19
18pF

GND   GND

GND

C20
10nF

+3V0

C21
12pF

C23
12pF

BALUN_RF_P   DW_RF_P
DIFF100   DIFF100

BALUN_RF_N   DW_RF_N
DIFF100   DIFF100

U2
HHM1595A1

J35

UWB_ANT

SMA/FLANGE

GND

GND

+1V8

+3V0

C4
100nF

C5
100nF

GND   GND

C1
100nF

GND

C2
100nF

GND

C9
100nF

GND

+3V0

+1V8

C14
100nF

C17
100nF

C18
100nF

GND   GND   GND

VDDDIG

GND

C24
100nF

GND

+3V0

C25
47uF

GND

+3V0
L2
BLM15AG601SN1D

C26
22uF

C27
100nF

C28
330pF

C29
12pF

C30
12pF

C31
330pF

C32
100nF

+3V0
L3
BLM15AG601SN1D

GND

GND

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Power supply

DCDC 1.8V

+1V8

VCC

J25

D2
5V0 ESD

GND

J26

J28

J29

GND

4, 5 DW_EXTON

C37
10uF

GND

U3
6	Vin	Lx	1
5	Vss	Vss	2
4	CE	Vout	3

GND

0   XC9257/8

GND

L4
CKP20162R2M-T

C58
22pF

GND

C34
10uF

GND

L5
15nH

C35
4.7uF

GND

DESIGN NOTE:
F=2.25Mhz, VconvRipple=60mV,
VmaxRipple=5mV
http://www.aimtec.com/site/Aimtec/files/doc
uments/ApplicationNotes/a016e%20-%20red
uction%20of%20output%20ripple%20&%20
noise.pdf

Power supply selection

VCC

R10
0R

VCC_DEV

+3V0

R11
0R

I2C/SPI devices
LIS2MDLTR + LSM6DSLTR

3-Axes Magnetometer

U4
LIS2MDLTR

- 12 NC
- 11 NC
- 1 SCL/SPC
- 2 NC
- 3 CS
- 4 SDA/SDI/SDO
- 10 VDD_IO
- 9 VDD
- 8 GND
- 7 INT/DRDY
- 5 C1
- 6 GND

I2C_SCL

VCC_DEV

I2C_SDA

VCC_DEV — C43 100nF — GND

VCC_DEV — C41 100nF — GND

IRQ_MAG → 3

C57 220nF — GND

LAYOUT NOTE:
Sharing C36 with nRF.

DESIGN NOTE:
I2C address 0011110b = 0x1E

6-Axes Accelerometer and Gyroscope

VCC_DEV

I2C_SCL
I2C_SDA

U7
LSM6DSLTR

- 14 SDA
- 13 SCL
- 12 CS
- 1 SDO/SA0
- 2 SDx
- 3 SCx
- 4 INT1
- 11 NC
- 10 NC
- 9 INT2
- 8 VDD
- 5 VDDIO
- 6 GND
- 7 GND

VCC_DEV

IRQ2 → 3

VCC_DEV — C39 100nF — GND

VCC_DEV — C45 100nF — GND

GND

IRQ1 → 3

DESIGN NOTE:
I2C address 1101011b = 0x6B

Barometer

VCC_DEV — C33 100nF — GND

GND

U5
LPS22HB

- 10 VDD
- 9 GND
- 8 GND
- 1 Vdd_IO
- 2 SCL/SPC
- 7 INT_DRDY
- 6 CS
- 3 GND
- 4 SDA/SDI/SDO
- 5 SDO/SA0

I2C_SCL

IRQ_DRDY → 3

I2C_SDA

GND GND

DESIGN NOTE:
I2C address 1011100b = 0x5C

DOC: REVISION HISTORY

A1

- Inital version

B1

- DW_CS path corrcted

- NetC30_2 - Via connection fixed

- P0.5 path corrected

- Chnaged 32MHz, 38.4MHz xtals to ABM10 footprint (2.0 x 2.5 mm)

C1

- Changed BT antenna A2 to ACX AT3216-B2R7HAA

- Changed all 0.1UF capacitor to Murata GRM033C81E0104KE14D

- Changed C56 to 10uF

- Changed C40 to 10pF

- Changed R7 to 340K 1%

- Changed R9 to 68.1K 1%

- Changed Balun U2 to TDK HHM1595A1

- Changed U5 to TI TPS63036YFGR

- Changed L4 to Taiyo Yuden CKP20162R2M-T

- Changed L6 to Taiyo Yuden CKP2012N2R2M-T

- Changed 32 MHz crystal X1 to Commutek 2CAS (2520-size)

- Changed 38.4MHz crystal X2 to Commutek 2CAT (2520-size)

- Changed 32.768KHz crystal X3 to Commutek KCBB (3215-size)

- Changed C35 and C37 to 4.7uF 6.3V X5R 0603

- Del C33 and C57

D1

- Disconnect U5 (TPS63036) pin B2 (PS/Sync) from ground and tie to VIN by adding pull-up resistor R4

CLOCKS (CPU & PCIE)

- Changed C42 from 10uF to 47uF (0603)

- Changed C25 from 22uF to 47uF (0603)

- Changed R7 from to 340K to 287 K 1%

- Changed R9 from 68.1K to 51.1K 1%

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