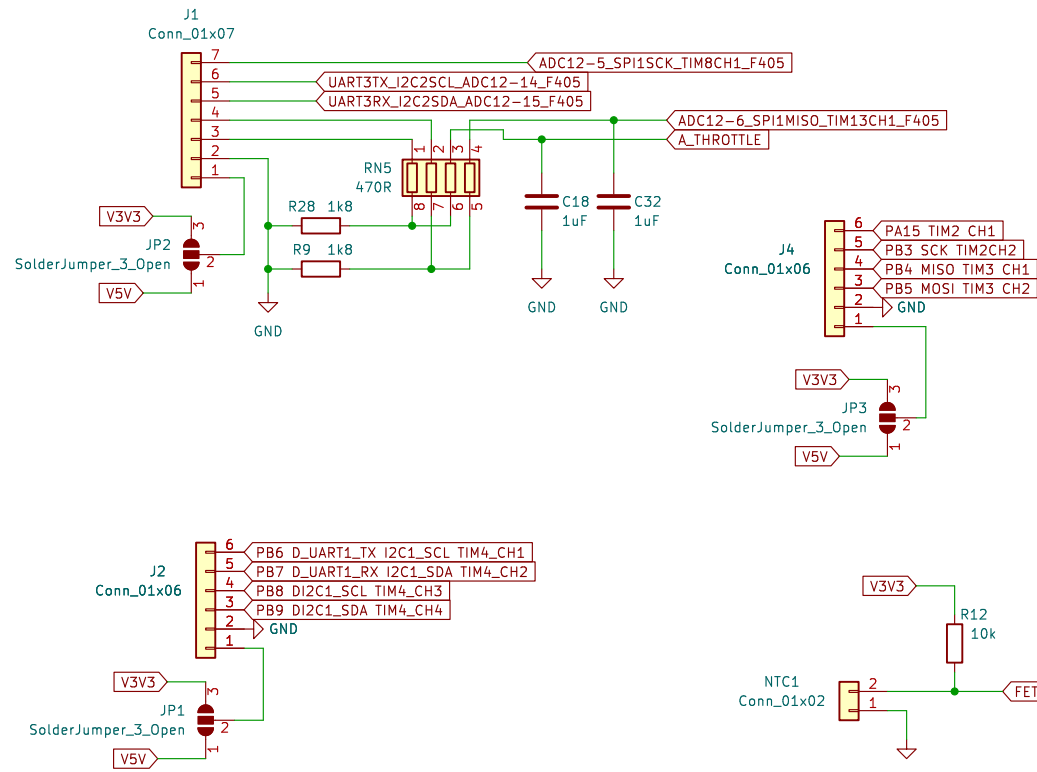
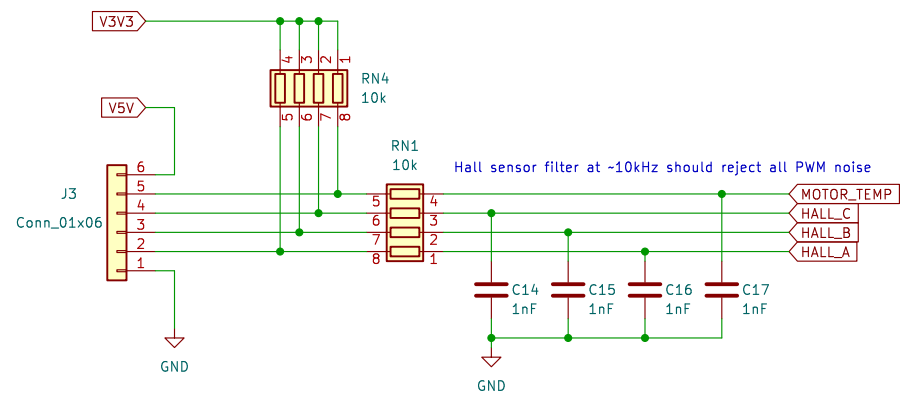
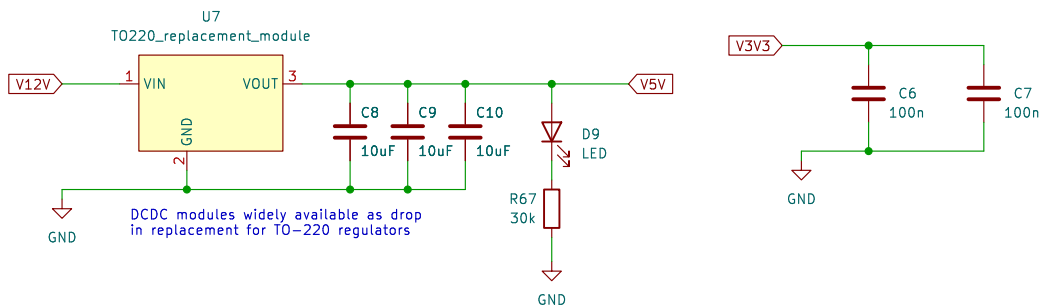
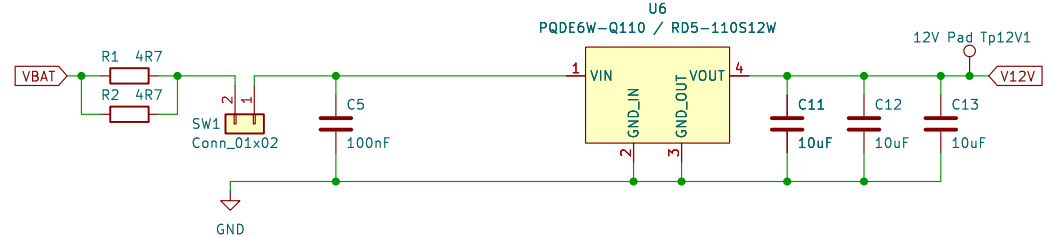
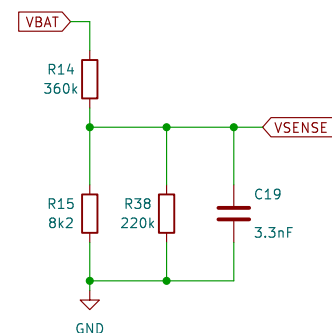


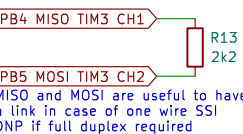
Footprint for CUI isolated module for up to 160V operation.
Only allows 500mA.
HiLine HLK-10011012
CUI PQDE6W-Q110
Or anything that exceeds your battery voltage and gives 12V out



R4, R15 and R38 were chosen to have exactly the same ratio as the phase voltage sense dividers, but significantly less current, since they are not also when ESC is off.
So you can use the 3.3k and 150k values exclusively in the software. error is 0.18%, less than resistor tolerances



The "Pill" is chosen as a generic STM32 module that should allow easy compatibility with multiple firmwares:
VESC with GD32F303CG pill (Netzplüschler mod. note CG)
VESC with STM32F405 pill (Owhite) (github.com/davidmolony/F405_pill)
EBICS with F103 Bluepill (Stancecok)
SmartESC V3 (Casalhol)
SmartESC V2 (Netzplüschler/Kox3)
MESC with F401 Blackpill (WiemeringFOC)
STM32 Motor Control Workbench (F401, F103)
Maybe others?
Pills are simply boards with an MCU, a regulator, USB and Boot0 button.



DO NOT CONNECT on blue/black pill

Likely use case:
PWM Throttle
Encoder on SPI, SSI
or Incremental Peripherals
GPIO

Likely use case:
PWM Throttle
Incremental Encoder
Screen Comms
Peripherals
GPIO

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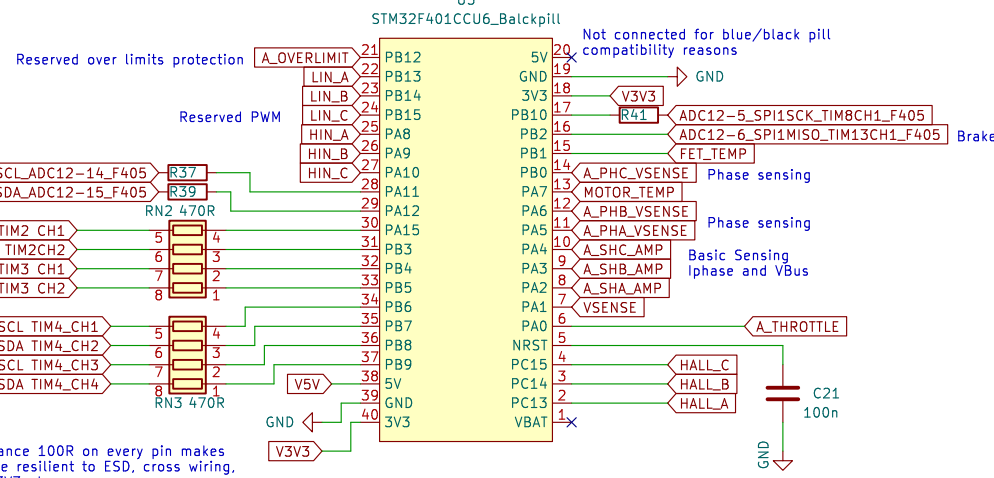
Likely use case:
PWM Throttle
Incremental Encoder
Screen Comms
Peripherals
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Input impedance 100R on every pin makes it much more resilient to ESD, cross wiring, GPIO-GND/3V3 etc

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Notes on power stage design:

Pulldowns optional, most gate drivers pull down the FETs when UVLO
MOS should have good Ciss/Crss ratio
Ciss/Crss>Vbat minimises the chance of parasitic turn-on.
Target gate time constant ~300ns
Rg = 15R(fet) + 6R(driver) + 18R (gate driver *3)
Ciss = 11.4nF
RC = 11.4nF x 26.6R = 303.24ns

