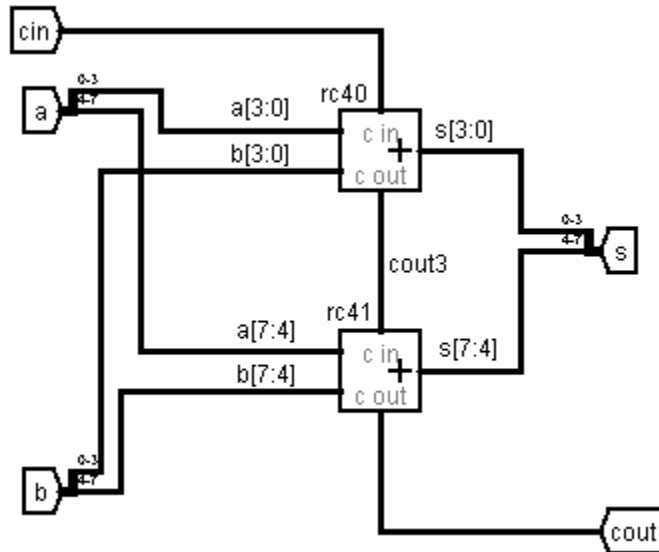


CECS 225: RIPPLE CARRY ADDER AND SUBTRACTOR 8-BIT

OBJECTIVE: Create an 8-bit adder and an 8-bit subtractor.

PROCEDURE: First import the halfadder, fulladder, RippleCarry4 module source files from the previous lab. *Be sure to use the exact same file names from the previous lab.*

Next create an 8-bit Ripple carry adder using 2 of the 4-bit ripple carry adders according to the block diagram below:

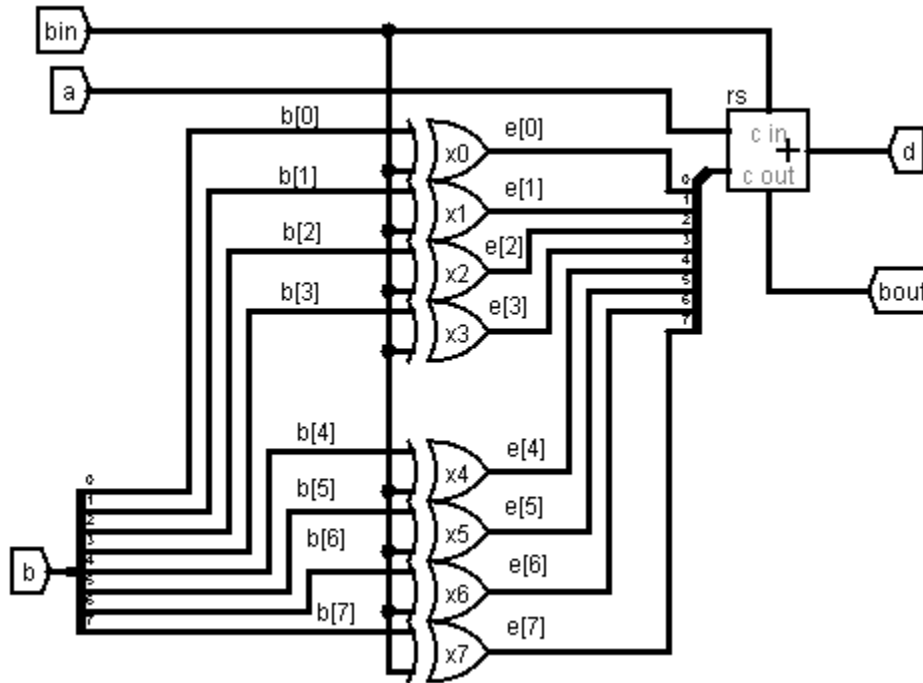


Name the file **ripplecarry8.v** and use the module skeleton below to get started:

```
1 `include "ripplecarry4.v"
2 module RippleCarry8(input cin,
3                     input [7:0] a, b,
4                     output [7:0] s,
5                     output cout);
6     wire cout3;
7     RippleCarry4
8     rc40(cin, a[3:0], b[3:0], s[3:0],cout3),
9     rc41(
10 endmodule
```

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Then create an 8-bit ripple subtractor according to the block diagram below:



Create a file named **ripplesubtractor8.v** and use the skeleton code below to get started:

```
1 module RippleSubtractor8(input bin,
2                           input [7:0] a, b,
3                           output [7:0] d,
4                           output bout);
5     wire [7:0] e;
6     xor
7     x0(e[0],    ,bin),
8     x1(e[1],    ,bin),
9     x2(e[ ],    ,bin),
10    x3(e[ ],    ,bin),
11    x4(e[ ],b[4], ),
12    x5(e[ ],b[5], ),
13    x6(e[6],b[6], ),
14    x7(e[7],b[7], );
15
16    RippleCarry8
17    rs(bin,    , e,    );
18 endmodule
```

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Leave the **design.sv** file empty as we will not be using it in this project.

Source code for testbench.sv is provided below:

```
1  `include "ripplecarry8.v"
2  `include "ripplesubtractor8.v"
3  module ripplecarrytester;
4      reg [7:0] a,b;  reg add0_sub1;
5      wire [7:0] sum,difference;
6
7      integer i;
8
9      RippleCarry8 //instantiate 8-bit Adder
10     uut0(add0_sub1, a,b,sum,);
11
12     RippleSubtractor8 //instantiate 8-bit Subtractor
13     uut1(add0_sub1, a, b, difference,);
14
15     initial begin
16         $display("\n\n");
17         for(i = 0; i < 10; i = i + 1) begin
18             {a,b,add0_sub1}=$random; test_case;
19         end
20         $finish;
21     end
22
23     task test_case;
24         #1
25         if(add0_sub1==1'b0) begin
26             $display("\nAdder Test");
27             $display("a = %b, b = %b, sum = %b",a,b,sum);
28         end
29         else begin
30             $display("\nSubtractor Test");
31             $display("a = %b, b = %b, difference = %b",a,b,difference);
32         end
33     endtask
34 endmodule
```

SV/Verilog Testben

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If everything works correctly then the following console output will be produced:

Adder Test

a = 10011010, b = 10010010, sum = 00101100

Subtractor Test

a = 10101111, b = 01000000, difference = 01101111

Subtractor Test

a = 01101011, b = 00000100, difference = 01100111

Subtractor Test

a = 00101011, b = 00110001, difference = 11111010

Subtractor Test

a = 10111101, b = 10000110, difference = 00110111

Subtractor Test

a = 11001100, b = 11000110, difference = 00000110

Subtractor Test

a = 01000010, b = 00110010, difference = 00010000

Adder Test

a = 10101001, b = 00001001, sum = 10110010

Subtractor Test

a = 11110001, b = 10000000, difference = 01110001

Subtractor Test

a = 11100110, b = 10000110, difference = 01100000

Done

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If your module did not work correctly get assistance from the instructor or a reputable student to troubleshoot your design.

WHAT TO TURN IN: Once the modules in this lab are working correctly:

- Copy the contents of your **ripplecarry8.v** module to a file named **ripplecarry8.txt**
- upload **ripplecarry8.txt** to the beachboard dropbox for **ripplecarry8**
- Copy the contents of your **ripplesubtractor8.v** module to a file named **ripplesubtractor8.txt**
- upload **ripplesubtractor8.txt** to the beachboard dropbox for **ripplesubtractor8**

NOTE:

Keep the source files from this lab as they will be used in future Labs!

halfadder, fulladder, ripplecarry4, ripplecarry8, and ripplesubtractor8 modules will be used in upcoming labs.