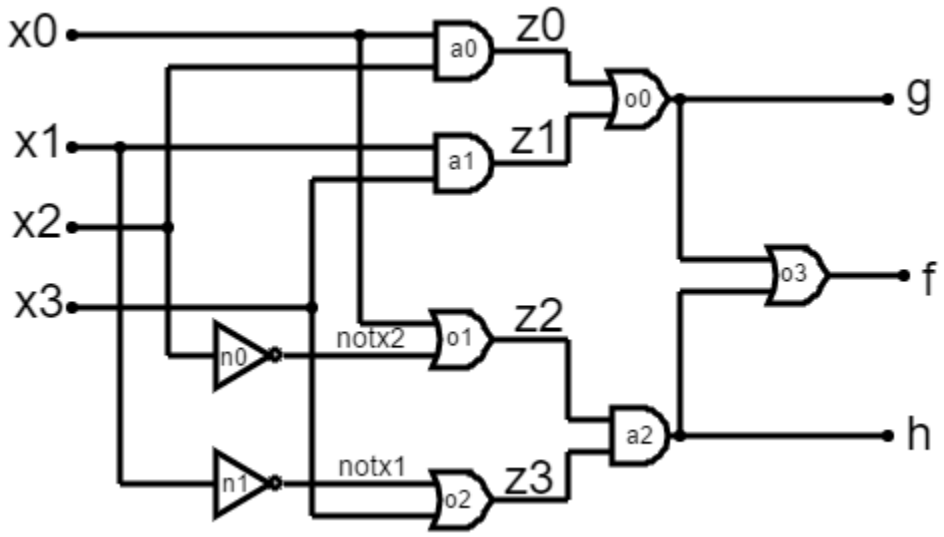
CECS 225: LAB 2 PART1

OBJECTIVE: Produce the truth table of a logic circuit to be used for K-Map minimization.

PROCEDURE: In this lab, model a logic circuit using gate level primitives to produce it's truth table. The Logic circuit is given below:



Use the given Verilog skeleton code below to get started:

```
1   // Code your design here
2   module Lab2p1(input x3, x2, x1, x0,
3                 output f, g, h);
4       wire z3, z2, z1, z0, notx2, notx1;
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21  endmodule
```

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Once you have modeled the circuit and verified it was created correctly, use the given testbench to produce a truth table for the circuit:

```
// Code your design here
// or browse Examples
module Lab2p1Tester();
    reg x3, x2, x1, x0;
    wire f, g, h;

    Lab2p1 dut(x3, x2, x1, x0, f, g, h);

    integer i;

    initial begin
        $display("x3\tx2\tx1\tx0\t|\tf\tg\th");
        $display("-----------------------------------------");
        for(i = 0; i < 16; i = i + 1)
            begin
                {x3, x2, x1, x0} = i;
                #1 $dislay("%b\t%b\t%b\t%b\t|%b\t%b\t%b\t",x3, x2, x1, x0, f, g, h);
            end
        $display("");
    end
endmodule
```

The truth table you produce should have the following contents.

x3	x2	x1	x0	f	g	h
0	0	0	0	1	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	0
1	0	0	0	1	0	1
1	0	0	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	1	1	1	1
1	1	1	0	1	1	0
1	1	1	1	1	1	1

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WHAT TO TURN IN: Once your Lab2p1 module is completed and proper test results are produced:

- Copy the contents of your **Lab2p1** module to a file named **Lab2p1.txt**
- Upload **Lab2p1.txt** to the beachboard dropbox named **Lab2 part 1**