CECS 225: LAB 2 PART2

OBJECTIVE: Create a reduced sum of products version of the circuit from Lab 2 Part 1

PROCEDURE: Use the truth table produced from Lab 2 Part 1 and fill the information into K-Maps (one K-Map for each of the outputs f, g, and h.) Use K-Map minimization to create a reduced sum of products logic equation for each of the outputs and then model the system using gate level primitives in a single Verilog module named Lab2p2. A skeleton code is given below for the create of Lab2p2 module:

```
// Code your design here
module Lab2p2(input x3, x2, x1, x0,
              output f, g, h);


endmodule
```

Once you have modeled the circuit and verified it was created correctly, use the given testbench to produce a truth table for the circuit (test code is identical to lab 2 part 1):

SV/Verilog Testbench

```
// Code your testbench here
// or browse Examples
module Lab2p2Tester();
  reg x3, x2, x1, x0;
  wire f, g, h;

  Lab2p2 dut(x3, x2, x1, x0, f, g, h);

  integer i;

  initial begin
    $display("x3\tx2\tx1\tx0\t|\tf\tg\th");
    $display("-----------------------------------------------------------------");
    for(i = 0; i < 16; i = i + 1)
      begin
        {x3, x2, x1, x0} = i;
        #1 $display("%b\t%b\t%b\t%b\t|\t%b\t%b\t%b", x3, x2, x1, x0, f, g, h);
      end
    $display("");
  end
endmodule
```

The truth table produced by the Lab2p2Tester should be identical to the one from Lab 2 part 1.

WHAT TO TURN IN: Once your Lab2p2 module is completed and proper test results are produced:

- Copy the contents of your **Lab2p2** module to a file named **Lab2p2.txt**
- Upload **Lab2p2.txt** to the beachboard dropbox for **Lab2 part 2**