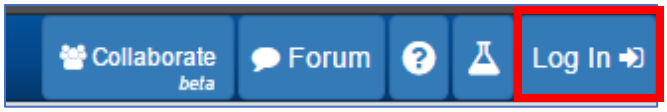
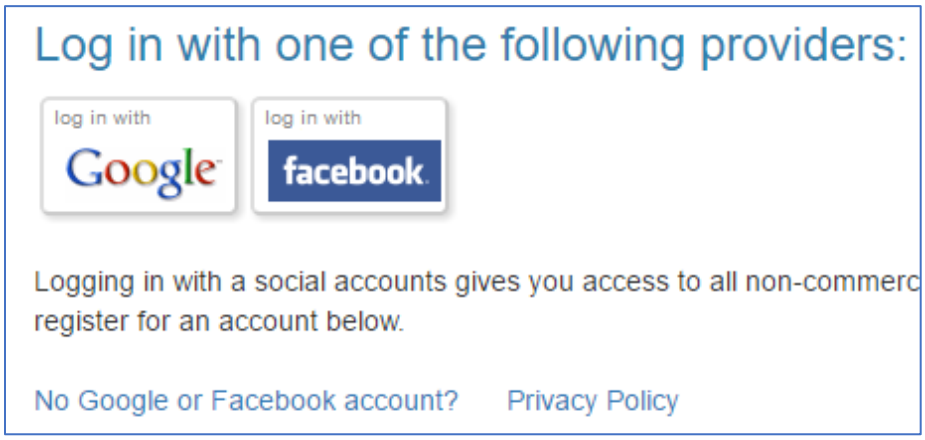
CECS 225 LAB0: EDA PLAYGROUND INTRO

OBJECTIVE: Learn to write a test cases in Verilog and use EDAplayground.com

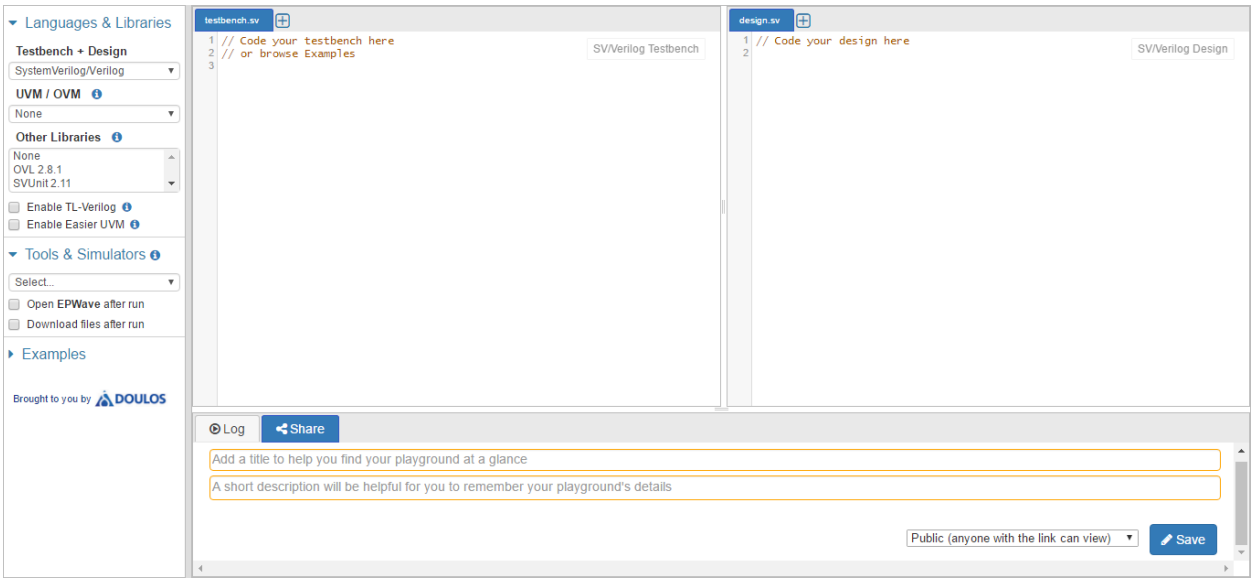
PROCEDURE: In this lab, an **adder** defined in Verilog will be tested using a Verilog **testbench**. The **adder** module will be provided along with a partially completed testbench. Also this lab will serve as an introduction to the edaplayground.com development environment.

1. Go to https://www.edaplayground.com/
2. Log in to EDA playground to Run a simulation. You may conveniently login using a **Google** or **Facebook** account. To log in using an email account, click the **No Google or Facebook account?** Link to go through an EDA playground account creation process.





3. After logging in a blank project will be available.



4. The given Verilog source code defines a 4-bit adder module that will receive 2 values in the **A** and **B** "variables", add the two values and assign the sum to the **SUM** variable. Enter the given source code below into the **design.sv** window:

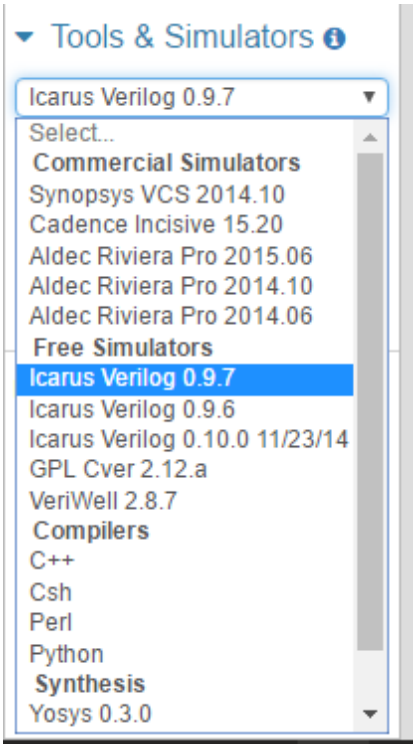
```
module adder4bit(
  input [3:0] A,B,
  output [3:0] SUM
);
  assign SUM = A + B;
endmodule

```

5. In the **testbench.sv** window enter the code given below.

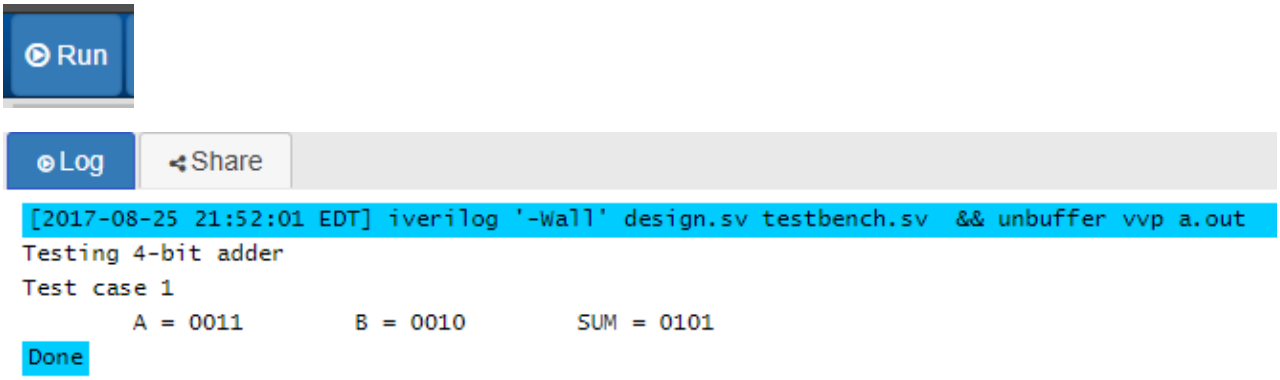
SV/Verilog Testbench

```
module adderTester;
  reg [3:0] a, b;
  wire [3:0] sum;

  adder4bit a4(a, b, sum);

  initial begin
    $display("Testing 4-bit adder");
    $display("Test case 1");
    a = 4'b0011;
    b = 4'b0010;
    #1;
    $display("\tA = %b\tB = %b\tSUM = %b",a,b,sum);
    $finish;
  end
endmodule
```

6. Once all the given code has been entered, select Icarus Verilog as the simulator tool (any version of Icarus Verilog can be used):



7. Click the Run button and the result of the test case will be written to the console if there are no project errors. Each window pane can be resized as needed to see all relevant information:



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ACTIVITY: Write Verilog code to add the test cases in the table below to the given Verilog Testbench.
The values in the table are given in decimal, convert the input values to binary in the Verilog testbench

	a	**B**
4-bit adder Test Case 2	4	6
4-bit adder Test Case 3	8	5
4-bit adder Test Case 4	3	12
4-bit adder Test Case 5	7	11

Use the code from the given test case (lines 9 through 13 of the **adderTester** module) as a reference to code the new test cases.

WHAT TO TURN IN: Once you have coded test cases 2 through 5 for the 4-bit adder and verified correctness of test results, copy the contents of the **testbench.sv** source file to a file named **Lab0.txt** and upload to the beachboard dropbox for **Lab0**.