

# 1. Description

## 1.1. Project

Project Name	INITIALIZATION
Board Name	NUCLEO-L432KC
Generated with:	STM32CubeMX 6.13.0
Date	12/06/2024

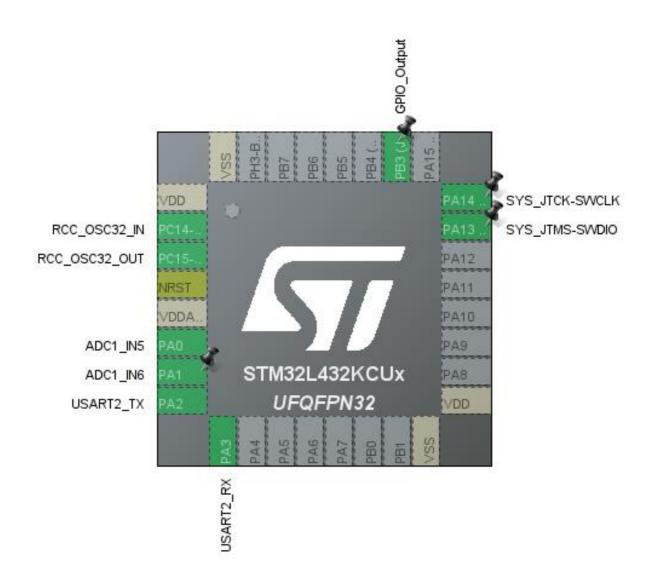
## 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L432KCUx
MCU Package	UFQFPN32
MCU Pin number	32

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4

# 2. Pinout Configuration

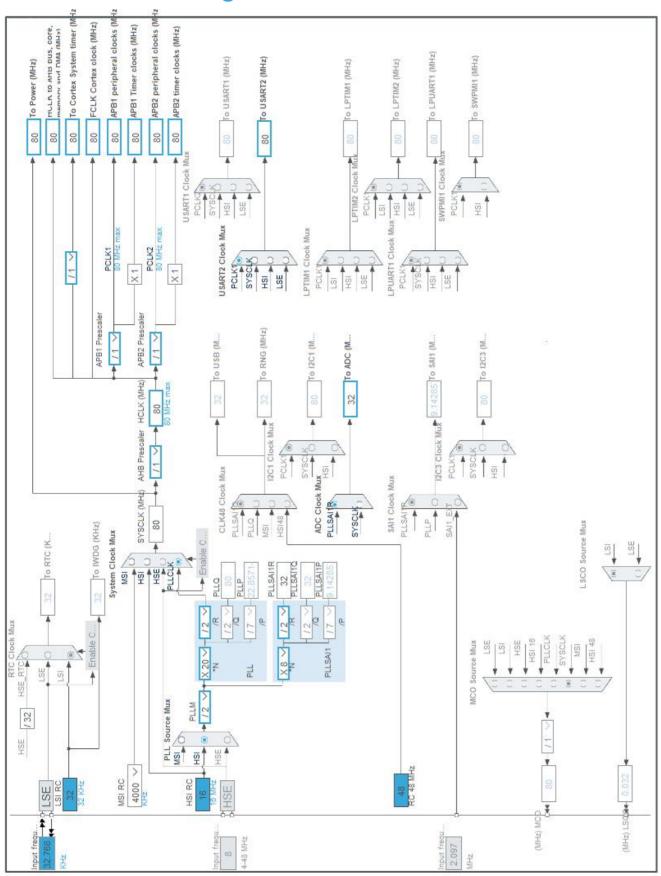


# 3. Pins Configuration

Pin Number UFQFPN32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
3	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	ADC1_IN5	
7	PA1	I/O	ADC1_IN6	
8	PA2	I/O	USART2_TX	
9	PA3	I/O	USART2_RX	
16	VSS	Power		
17	VDD	Power		
23	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
24	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
26	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Output	
32	VSS	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



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# 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
мси	STM32L432KCUx
Datasheet	DS11451_Rev2

## 1.2. Parameter Selection

Temperature	25
Vdd	3.0

## 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

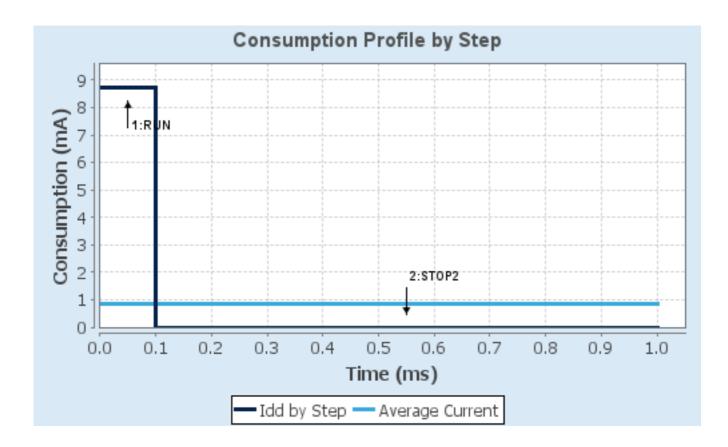
## 1.4. Sequence

	la	
Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.71 mA	1.06 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.98	105
Category	In DS Table	In DS Table

### 1.5. Results

Sequence Time	1 ms	Average Current	871.95 μA
Battery Life	5 months, 9 days,	Average DMIPS	100.0 DMIPS
	16 hours		

## 1.6. Chart



# 2. Software Project

## 2.1. Project Settings

Name	Value
Project Name	INITIALIZATION
Project Folder	C:\Users\asad1\OneDrive\Documentos\GitHub\Table-de-Mixage\INITIALIZATION
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.18.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_TIM1_Init	TIM1
6	MX_USART2_UART_Init	USART2

# 3. Peripherals and Middlewares Configuration

3.1. ADC1

IN5: IN5 Single-ended IN6: IN6 Single-ended

3.1.1. Parameter Settings:

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

Disabled

DimA Continuous Requests

ADC 12-bit resolution

Right alignment

Enabled

Disabled

Disabled

Enabled

\*

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten \*

Low Power Auto Wait Disabled

ADC Regular ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 2 \*

External Trigger Conversion Source Timer 1 Trigger Out event \*

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel 5

Sampling Time 6.5 Cycles \*

Offset Number No offset Rank 2 \*

Channel 6 \*

Sampling Time 6.5 Cycles \*

Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode

false

5000

#### 3.2. RCC

### Low Speed Clock (LSE): Crystal/Ceramic Resonator

### 3.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16

MSI Calibration Value 0

MSI Auto Calibration Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms)

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

#### 3.3. SYS

**Debug: Serial Wire** 

Timebase Source: SysTick

#### 3.4. TIM1

**Clock Source : Internal Clock** 

#### 3.4.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value ) 1759 \*
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value)

auto-reload preload Enable \*

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### 3.5. **USART2**

### **Mode: Asynchronous**

### 3.5.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 4. System Configuration

## 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
SYS	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PB3 (JTDO- TRACESWO	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	

## 4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: Circular \*

Peripheral Increment: Disable

Memory Increment: Enable \*

Peripheral Data Width: Half Word

Memory Data Width: Half Word

# 4.3. NVIC configuration

# 4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
RCC global interrupt	true	0	0	
DMA1 channel1 global interrupt	true	0	0	
TIM1 update interrupt and TIM16 global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused			
Flash global interrupt	unused			
ADC1 global interrupt	unused			
TIM1 break interrupt and TIM15 global interrupt	unused			
TIM1 trigger and commutation interrupts	unused			
TIM1 capture compare interrupt	unused			
USART2 global interrupt	unused			
FPU global interrupt	unused			

## 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
RCC global interrupt	false	true	false
DMA1 channel1 global interrupt	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
TIM1 update interrupt and TIM16 global interrupt	false	true	true

<sup>\*</sup> User modified value

# 5. System Views

5.1. Category view

5.1.1. Current



## 6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32l4\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32l4\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4\_svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

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recommendations-and-package-information-for-leadfree-ecopack-mcus-

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