UCF 管脚说明

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//设置 FSK 解调输出信号的管脚和电平
NET "FPGA_LED"       LOC=R19   |   IOSTANDARD = LVCMOS33;

//设置 AD_DA 实验板 J2 端采样的差分信号数据（P 端），7 位，设置为差分电平
NET "AD_DA_P[0]" LOC = N15   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[1]" LOC = L19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[2]" LOC = M19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[3]" LOC = M17   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[4]" LOC = L16   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[5]" LOC = L14   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_P[6]" LOC = K14   |   IOSTANDARD = DIFF_HSTL_II_18;
//设置 AD_DA 实验板 J2 端采样的差分信号数据（N 端），7 位，设置为差分电平
NET "AD_DA_N[0]" LOC = N16   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[1]" LOC = L20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[2]" LOC = M20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[3]" LOC = M18   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[4]" LOC = L17   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[5]" LOC = L15   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DA_N[6]" LOC = J14   |   IOSTANDARD = DIFF_HSTL_II_18;

//设置 AD_DA 实验板 J1 端采样的差分信号数据（P 端），7 位，设置为差分电平
NET "AD_DB_P[0]" LOC = K19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[1]" LOC = G19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[2]" LOC = F19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[3]" LOC = C20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[4]" LOC = B19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[5]" LOC = E18   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_P[6]" LOC = E17   |   IOSTANDARD = DIFF_HSTL_II_18;
//设置 AD_DA 实验板 J1 端采样的差分信号数据（N 端），7 位，设置为差分电平
NET "AD_DB_N[0]" LOC = J19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[1]" LOC = G20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[2]" LOC = F20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[3]" LOC = B20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[4]" LOC = A20   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[5]" LOC = E19   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_DB_N[6]" LOC = D18   |   IOSTANDARD = DIFF_HSTL_II_18;

//设置 AD 返回时钟对应的 FPGA 端口，同时设置端口为差分形式
NET "AD_CLKOUTP"       LOC = H16   |   IOSTANDARD = DIFF_HSTL_II_18;
NET "AD_CLKOUTM"       LOC = H17   |   IOSTANDARD = DIFF_HSTL_II_18;
//设置 FPGA 输出给 AD 时钟对应的 FPGA 端口，同时设置端口为差分形式
NET "FPGA_AD_CLK_P"   LOC = K17   |   IOSTANDARD = DIFF_HSTL_II_18;
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NET "FPGA_AD_CLK_M"  LOC = K18   |   IOSTANDARD = DIFF_HSTL_II_18;

//设置 FPGA 输出给 AD 控制信号对应的 FPGA 端口，设置信号为单端方式
NET "AD_RESET"          LOC = G17   |   IOSTANDARD = LVCMOS18;
NET "AD_SEN"            LOC = F16   |   IOSTANDARD = LVCMOS18;
NET "AD_SCLK"           LOC = D20   |   IOSTANDARD = LVCMOS18;
NET "AD_CTRL[0]"        LOC = M14   |   IOSTANDARD = LVCMOS18;
NET "AD_CTRL[1]"        LOC = G18   |   IOSTANDARD = LVCMOS18;
NET "AD_CTRL[2]"        LOC = H15   |   IOSTANDARD = LVCMOS18;
//设置 FPGA 输入时钟，设置信号为单端方式
NET "GCLK"              LOC = Y7    |   IOSTANDARD = LVCMOS33;
//设置 FPGA 输入的复位信号，设置信号为单端方式
NET "FPGA_RESET"        LOC = W6    |   IOSTANDARD = LVCMOS33;
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