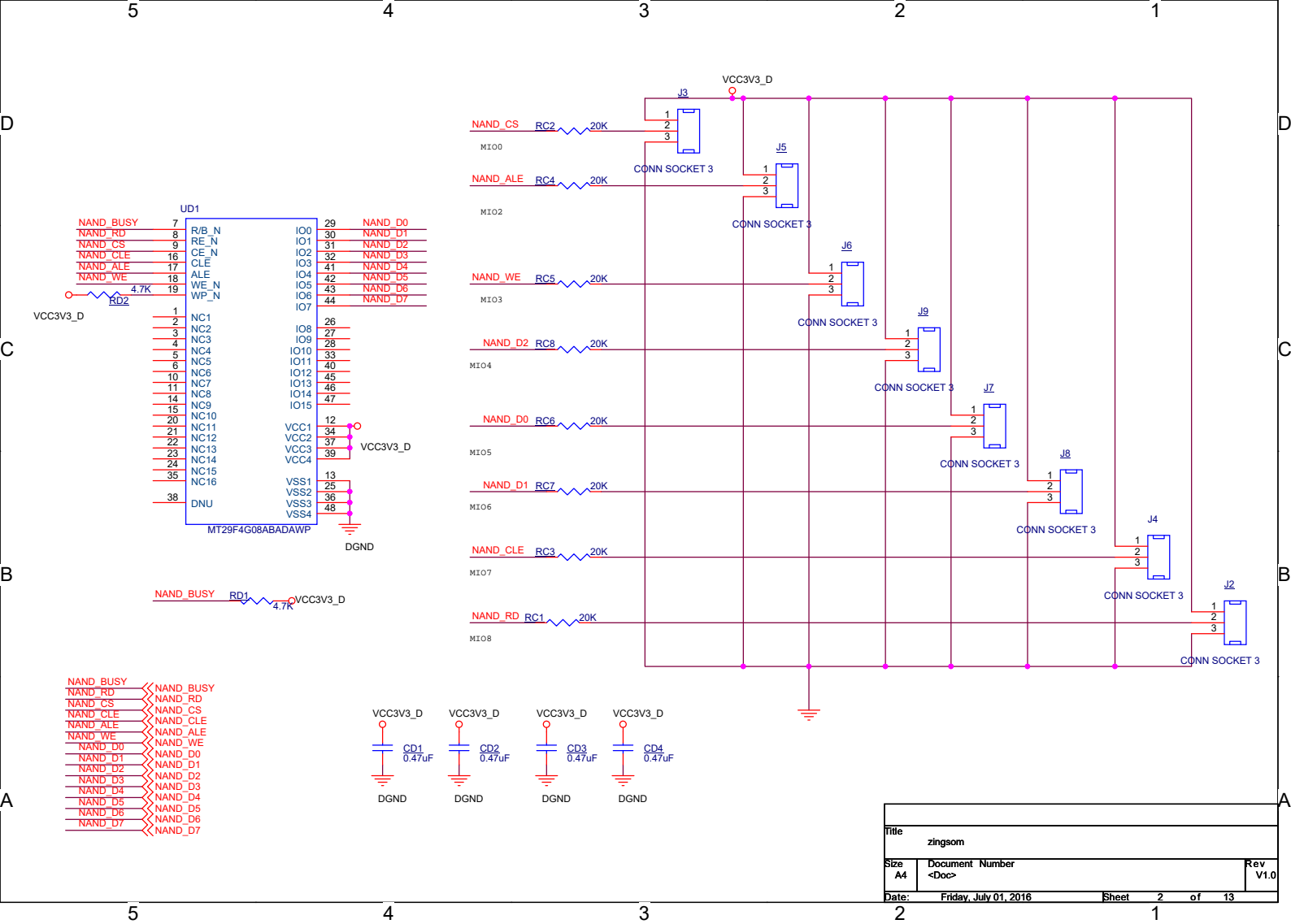
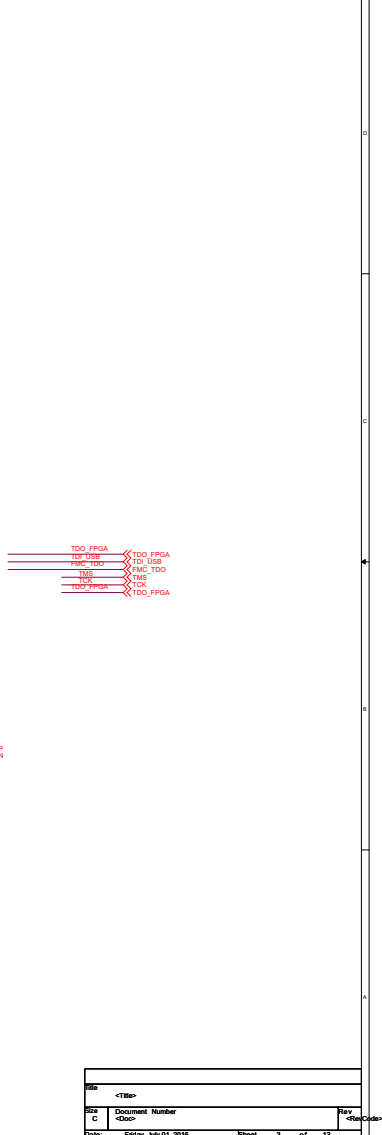
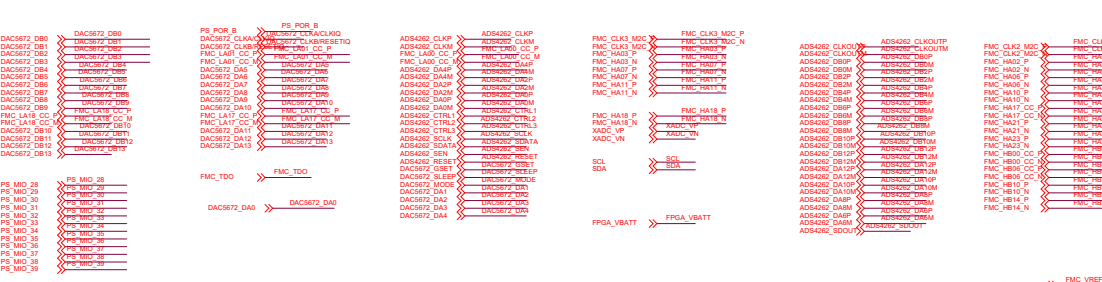
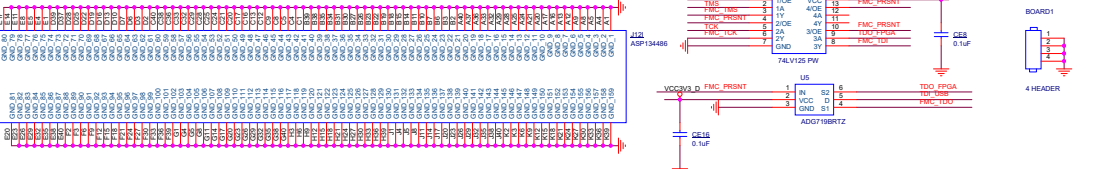
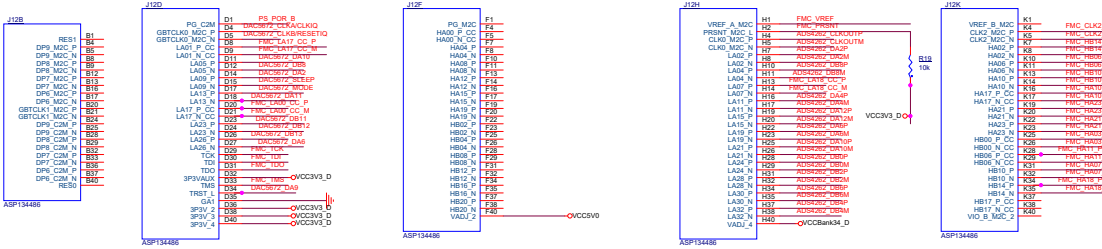
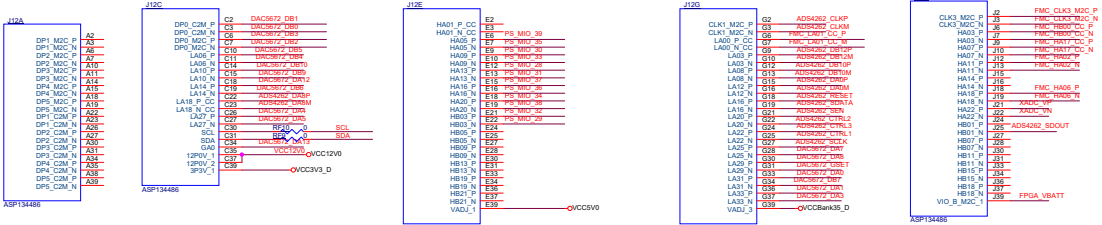
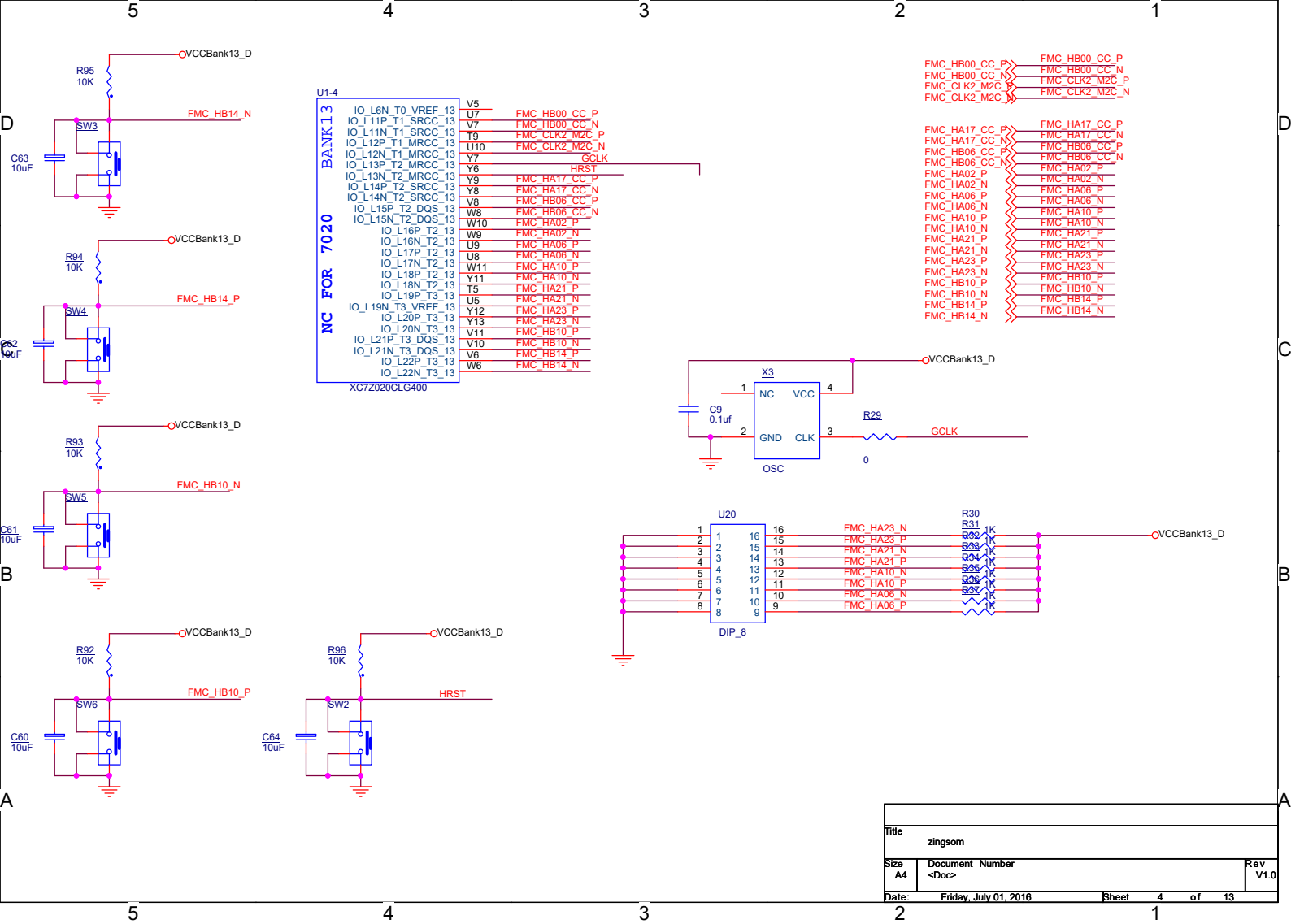


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BANK500

PS_CLK_500
PS_POR_B_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500

E7 PS_CLK
C7 PS_POR_B
E6 NAND_CS
A7 PHY_RESET
B8 NAND_ALE
D6 NAND_WE
B7 NAND_D2
A6 NAND_D0
A5 NAND_D1
D8 NAND_CLE
D5 NAND_RD
B5 NAND_D4
E9 NAND_D3
C6 NAND_D8
D9 NAND_D7
E8 NAND_D3
C5 NAND_BUSY
C8

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BANK501

PS_MIO_VREF_501
PS_SRST_B_501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
PS_MIO30_501
PS_MIO31_501
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PS_MIO45_501
PS_MIO46_501
PS_MIO47_501
PS_MIO48_501
PS_MIO49_501
PS_MIO50_501
PS_MIO51_501
PS_MIO52_501
PS_MIO53_501

E11 PS_MIO_VREF
B10 PS_SRST#
A19 PHY_TX_CLK
E14 PHY_TXD0
B18 PHY_TXD1
D10 PHY_TXD2
A17 PHY_TXD3
F14 PHY_TX_CTRL
B17 PHY_RX_CLK
D11 PHY_RXD0
A16 PHY_RXD1
F15 PHY_RXD2
A15 PHY_RXD3
D13 PHY_RX_CTRL
C16 PS_MIO_28
C13 PS_MIO_29
C15 PS_MIO_30
E16 PS_MIO_31
A14 PS_MIO_32
D15 PS_MIO_33
A12 PS_MIO_34
F12 PS_MIO_35
A11 PS_MIO_36
A10 PS_MIO_37
E13 PS_MIO_38
C18 PS_MIO_39
D14 SD_CCLK
C17 SD_CMD
E12 SD_D0
A9 SD_D1
F13 SD_D2
B15 SD_D3
D16
B14 SD_CD
B12 UART_RXD
C12 UART_TXD
B13 SCL
B9 SDA
C10 PHY_MDC
C11 PHY_MDIO

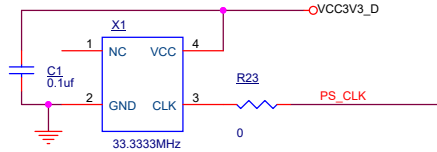
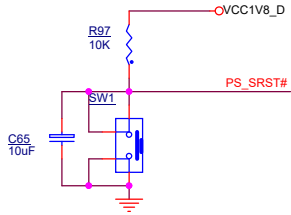
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PS_POR_B
NAND_CS
PHY_RESET
NAND_ALE
NAND_WE
NAND_D2
NAND_D0
NAND_D1
NAND_CLE
NAND_RD
NAND_D4
NAND_D5
NAND_D6
NAND_D7
NAND_D3
NAND_BUSY

PS_POR_B
NAND_CS
PHY_RESET
NAND_ALE
NAND_WE
NAND_D2
NAND_D0
NAND_D1
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NAND_D3
NAND_BUSY

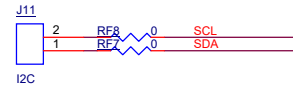
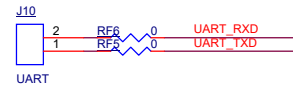
PS_SRST#
PHY_TX_CLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TX_CTRL
PHY_RX_CLK
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RX_CTRL
PS_MIO_28
PS_MIO_29
PS_MIO_30
PS_MIO_31
PS_MIO_32
PS_MIO_33
PS_MIO_34
PS_MIO_35
PS_MIO_36
PS_MIO_37
PS_MIO_38
PS_MIO_39
SD_CCLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
SD_CD

SCL
SDA
PHY_MDC
PHY_MDIO

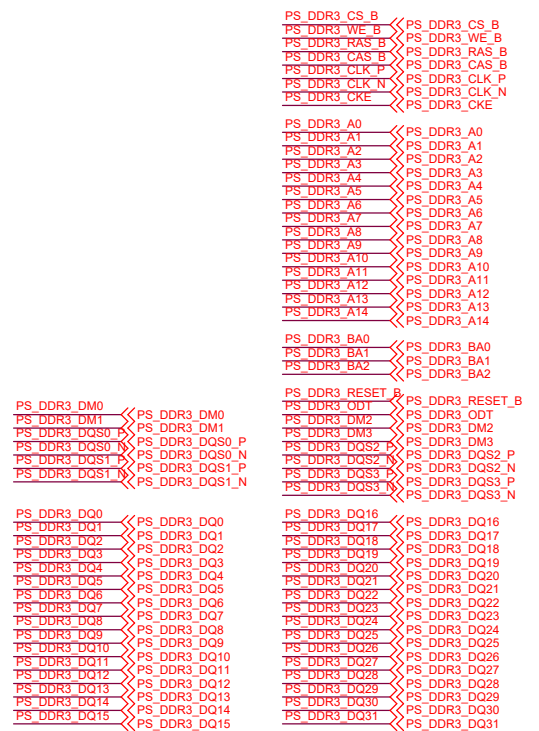


PS_MIO_VREFE12 10K DGND
PS_MIO_VREFE11 10K VCC1V8_D
PS_MIO_VREFE11 0.47uF DGND

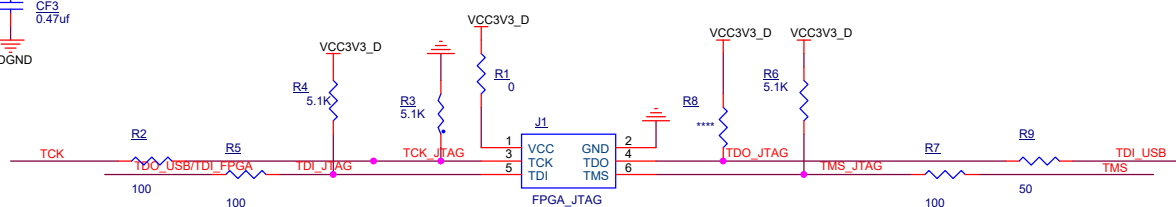
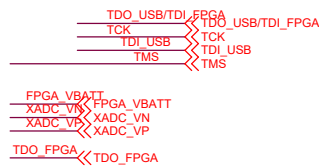
set to 0.9V with VCC0_MIO1 at 1.8V.
In any other case, tie to VCC0_MIO1



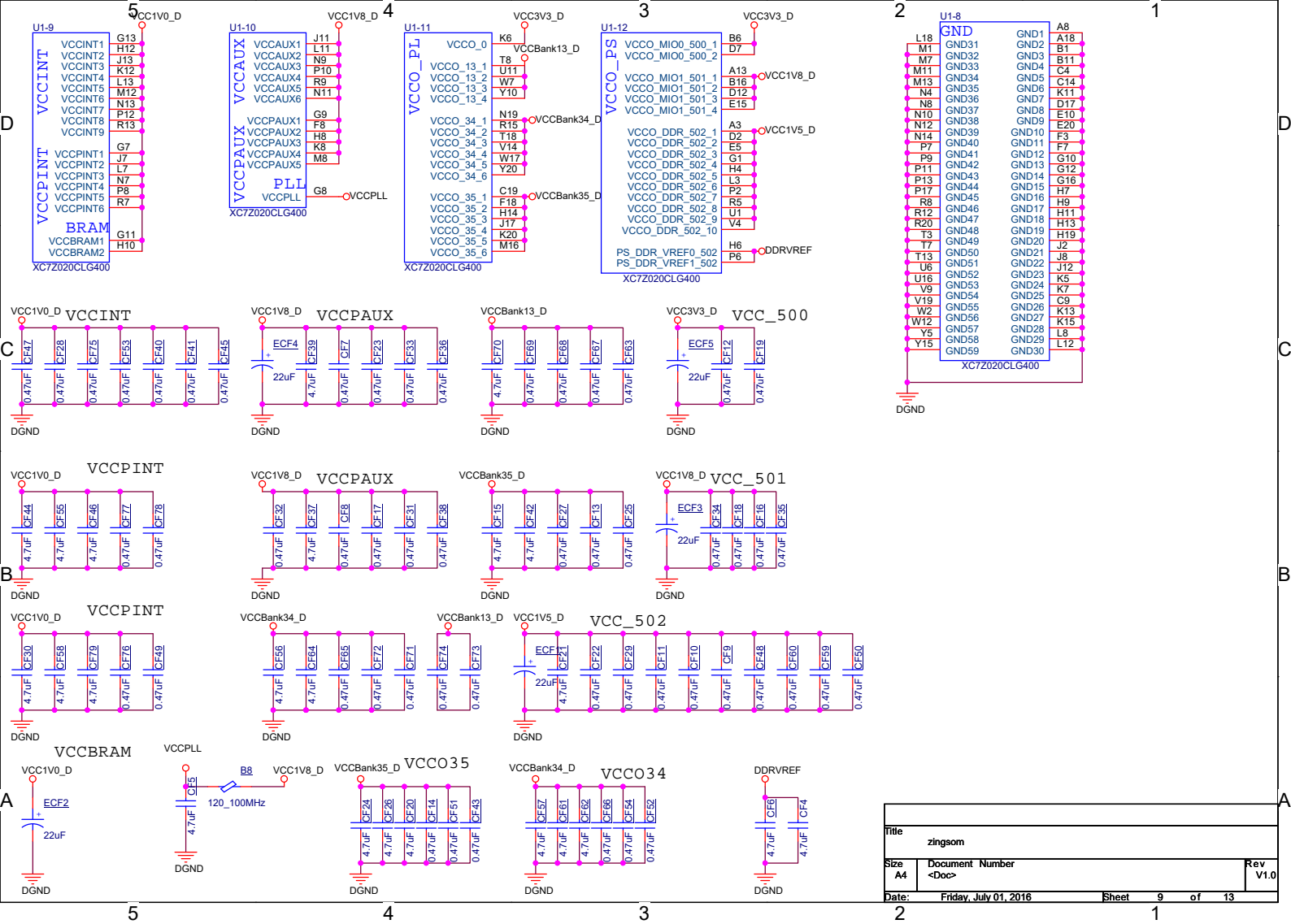
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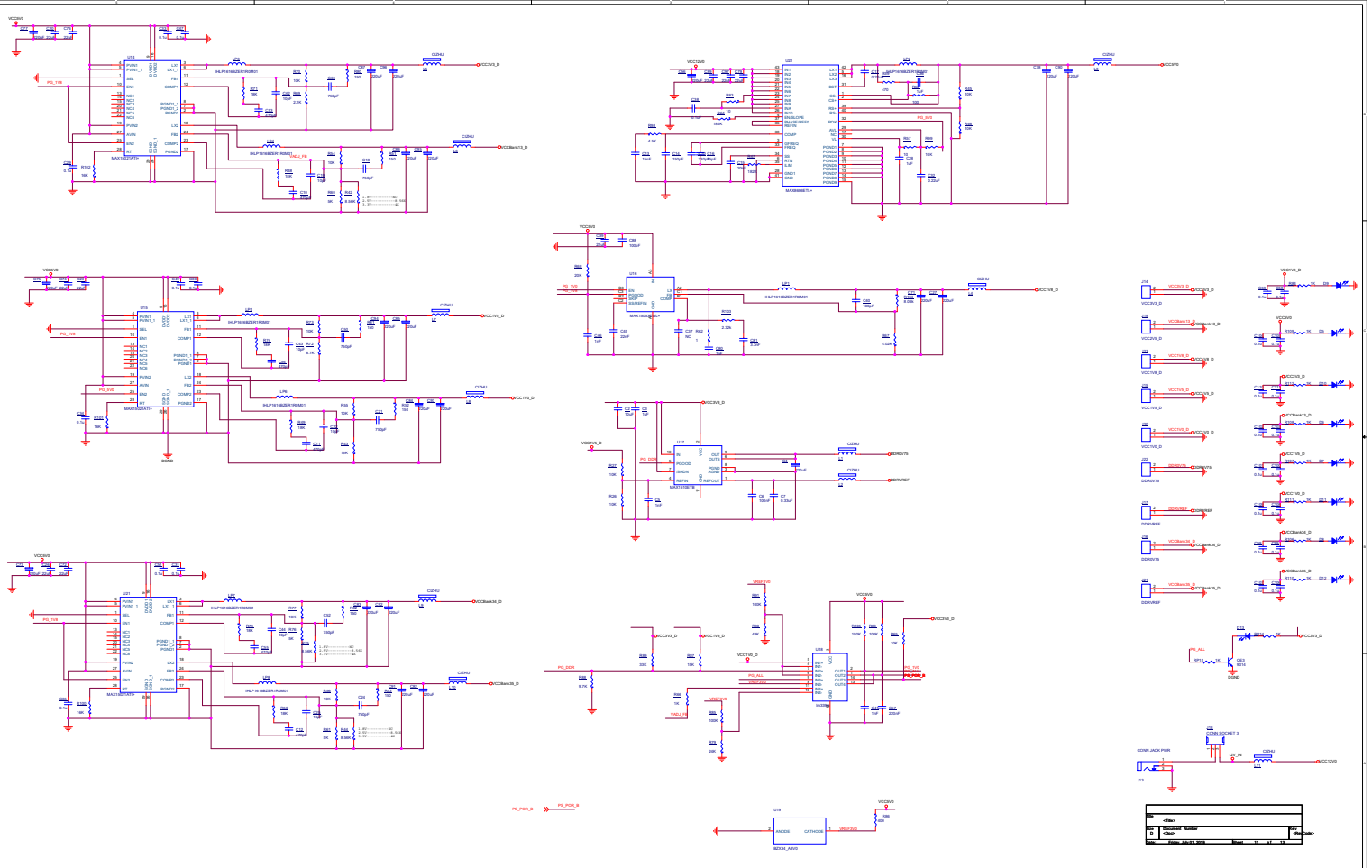


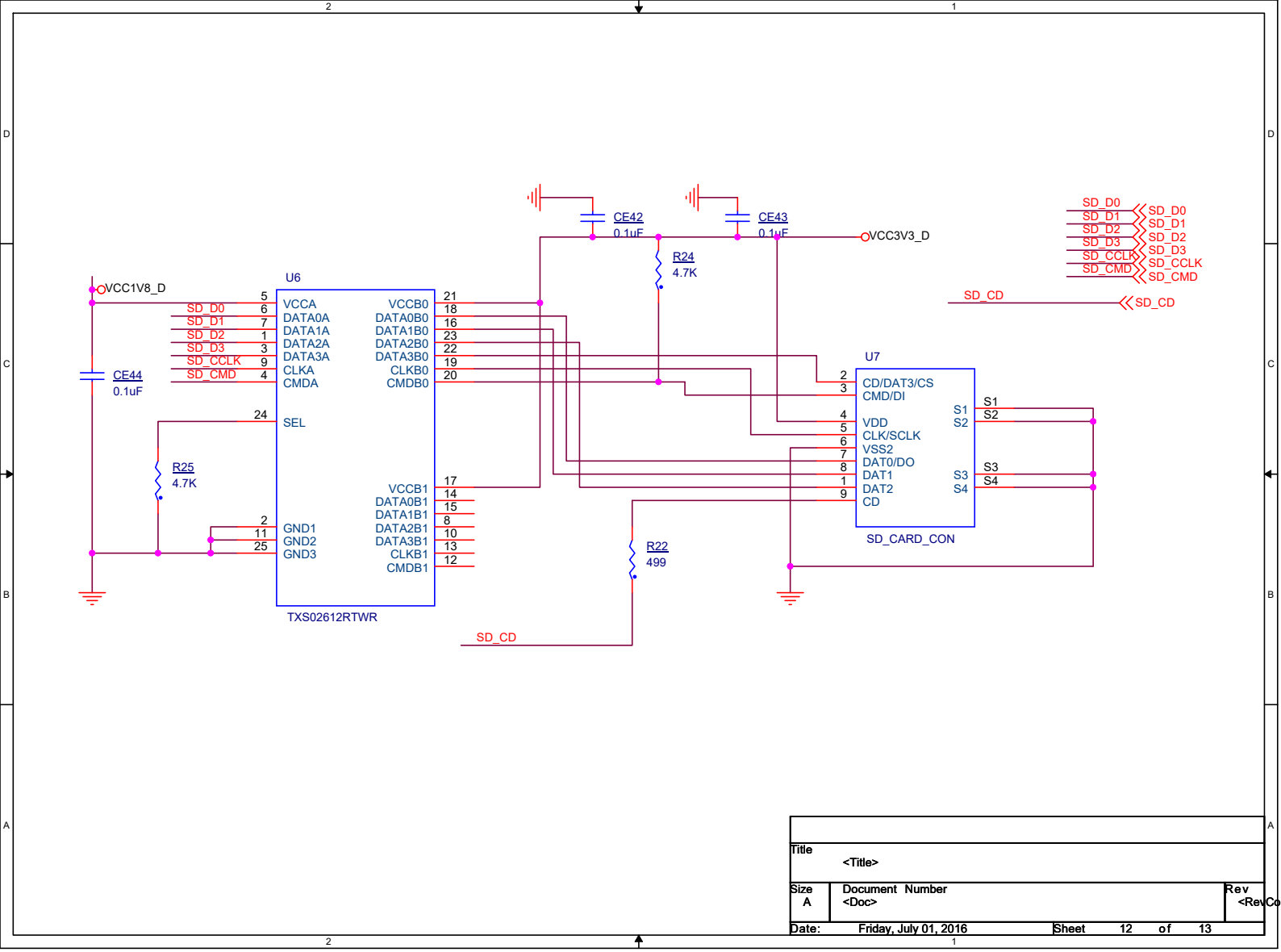
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