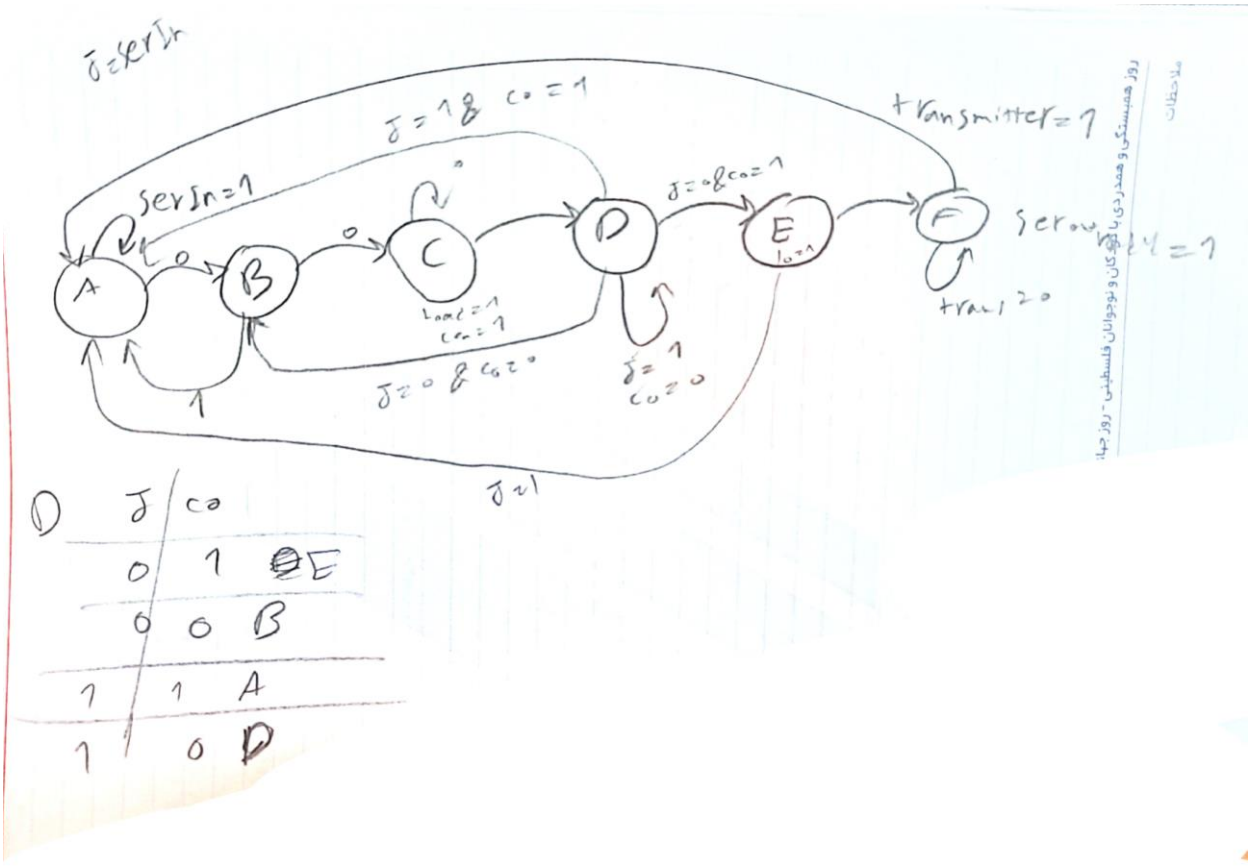
In the name of God

Mohammad Mashreghi: محمد مشرقی

SID = 810199492, logic number = 89

Q1-



Moore machine

```
module Qa_presynth3 (input clk,rst , serIn ,transmitted, output logic seroutvalid , i0);
  logic [3:0] pstate,nstate ; reg c_en,load;
  wire co;
  parameter [2:0] A = 0 ,B = 1 , C = 2 , D = 3 , E = 4 ,F=5;
    always @(pstate,serIn,co,transmitted) begin
    i0=0;
    c_en = 0 ;
    load = 0 ;
    seroutvalid=0;
    nstate=A;
    case(pstate)
      A: nstate = serIn ? A : B;
      B: nstate = serIn ? A : C;
      C : begin nstate = serIn ? D : C;  load = 1 ; end
      D: begin
        c_en = 1;
        nstate = ~serIn ? (co ? E : B) : (~co ? D : A);
      end
      E: begin
                    i0 = 1;
        nstate = serIn ? A : F;
      end
      F: begin
        seroutvalid=1;
        nstate = transmitted ? A : F;
      end
      default: nstate = A;
    endcase
  end
```

Edge clock

```
always @(posedge clk , posedge rst) begin
  if(rst)
    pstate <= A;
  else
    pstate <= nstate;
end
```

divide by 9

```
  logic [3:0] Count;//divider by 9
always @(posedge clk , posedge rst) begin
  if(rst) Count <= 4'd0;
  else if (load) Count <= 4'd6;
      else if (c_en) Count <= Count + 1;
end
  assign co = &Count;
```

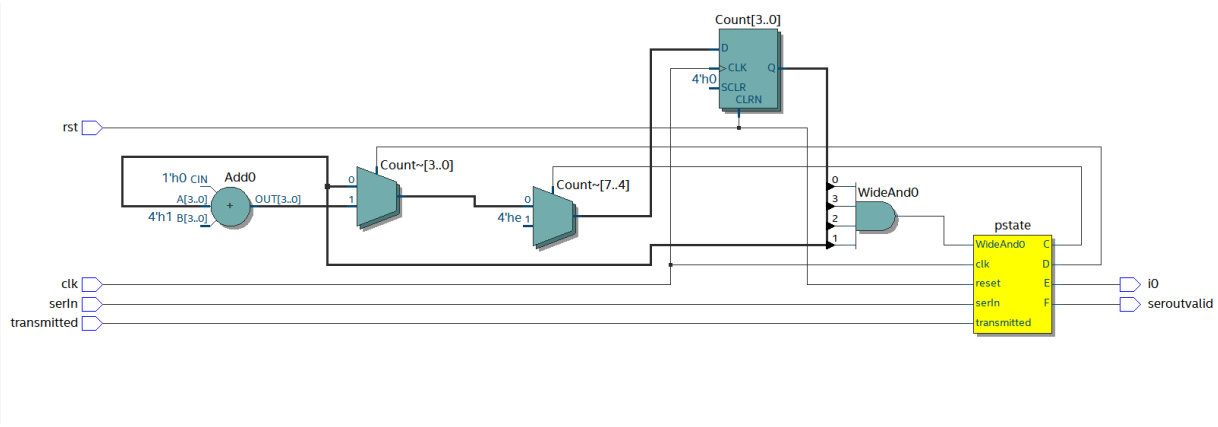
a)i

```
`timescale 1ns/1ns
module Qa_TB3();

wire seroutvalid , i0 ;

reg serIn = 1,transmitted = 0 ,clk = 0 ,rst = 0;

Qa_presynth3 cut1(.clk(clk) , .rst(rst) ,  .serIn(serIn) , .transmitted(transmitted) , .seroutvalid(seroutvalid) , .i0(i0));
always #25 clk = ~clk;


logic [20:0] seq = 21'b100111100111111111001011;
integer k ;
initial begin
#50 serIn = 1 ;



for (k = 23 ; k>0 ; k--) begin //k=4 servalid=1
    serIn = seq[k];
    #50 ;

end

#10 $stop ;
end
endmodule
```

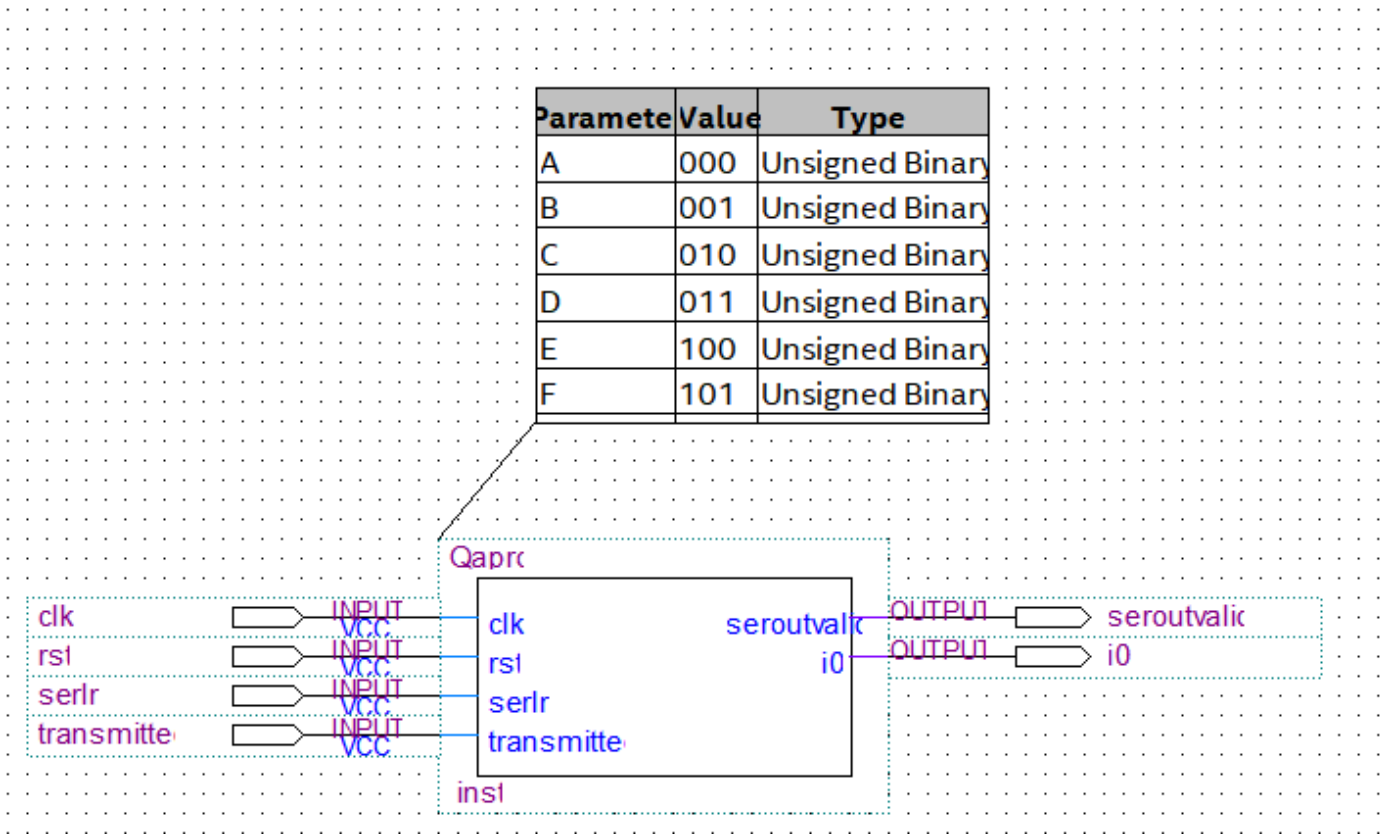
a)ii

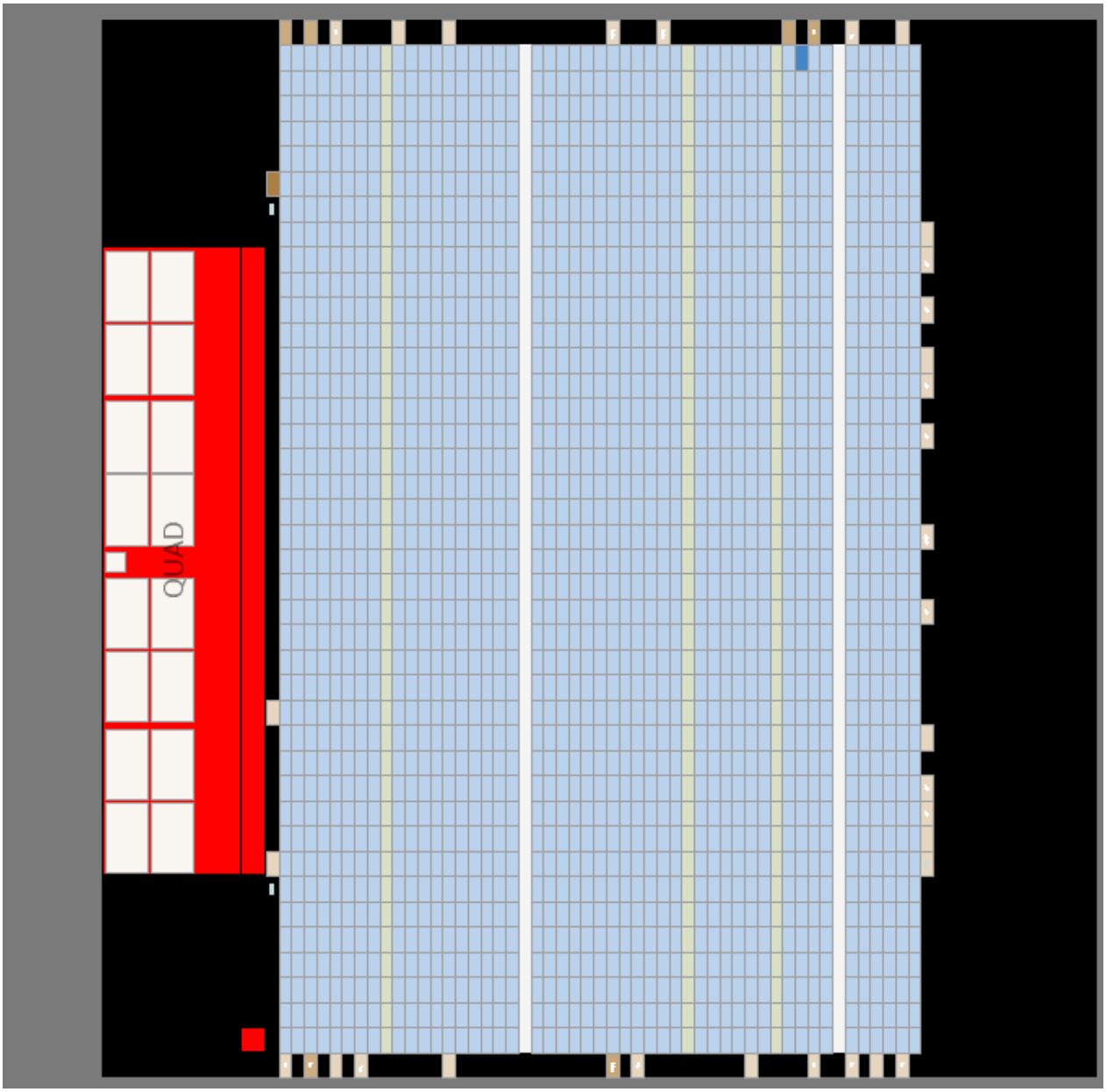
Flow Status	Successful - Mon Jun 13 18:26:39 2022
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Qapro
Top-level Entity Name	Qapro
Family	Cyclone IV GX
Device	EP4CGX22BF14C8
Timing Models	Final
Total logic elements	15 / 21,280 (< 1 %)
Total registers	10
Total pins	6 / 81 (7 %)
Total virtual pins	0
Total memory bits	0 / 774,144 (0 %)
Embedded Multiplier 9-bit elements	0 / 80 (0 %)
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

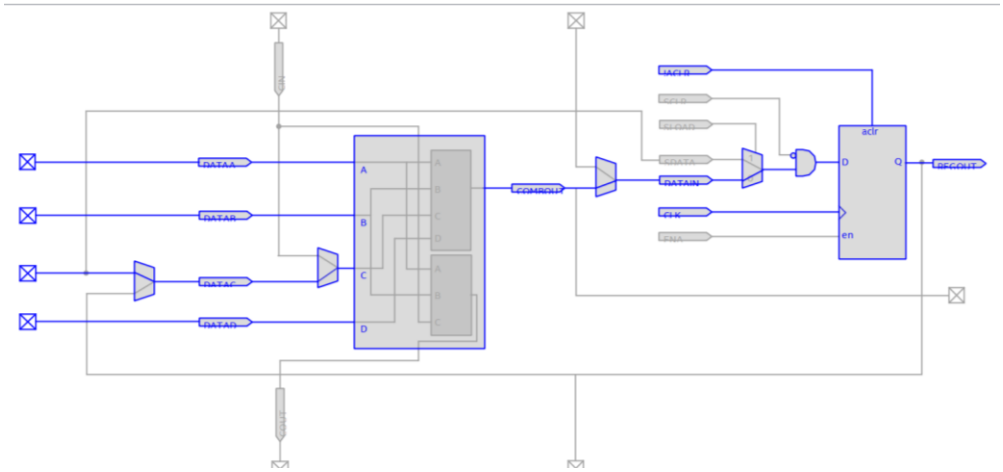
RTL viewer



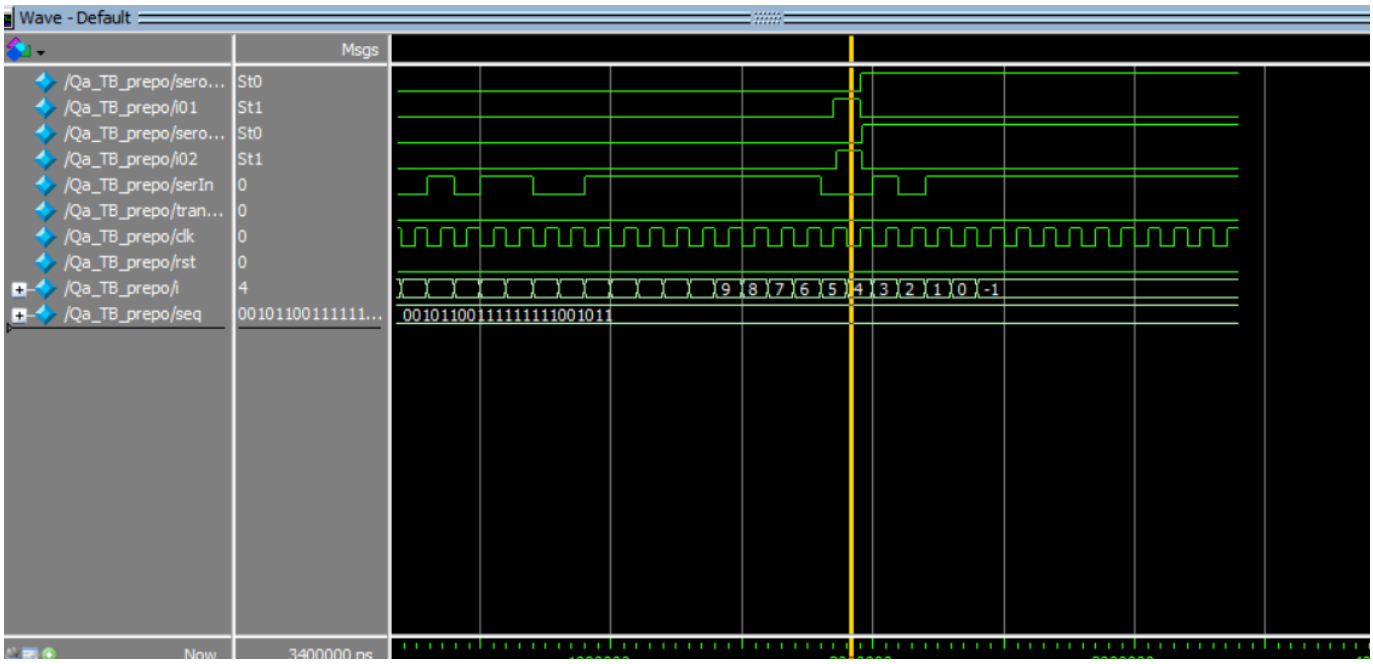
Symbol:



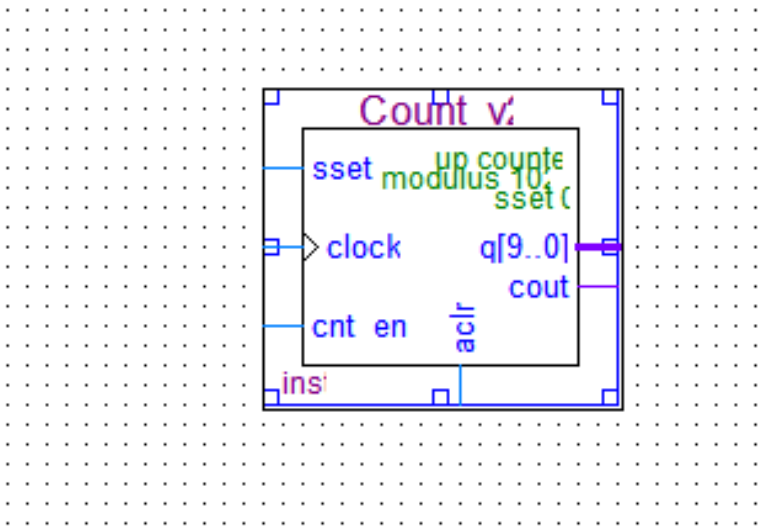

QUAD


DATAA
DATAB
DATAC
DATAD
COMBOUT
aclr
D
Q
REGOUT
clk
ena
en

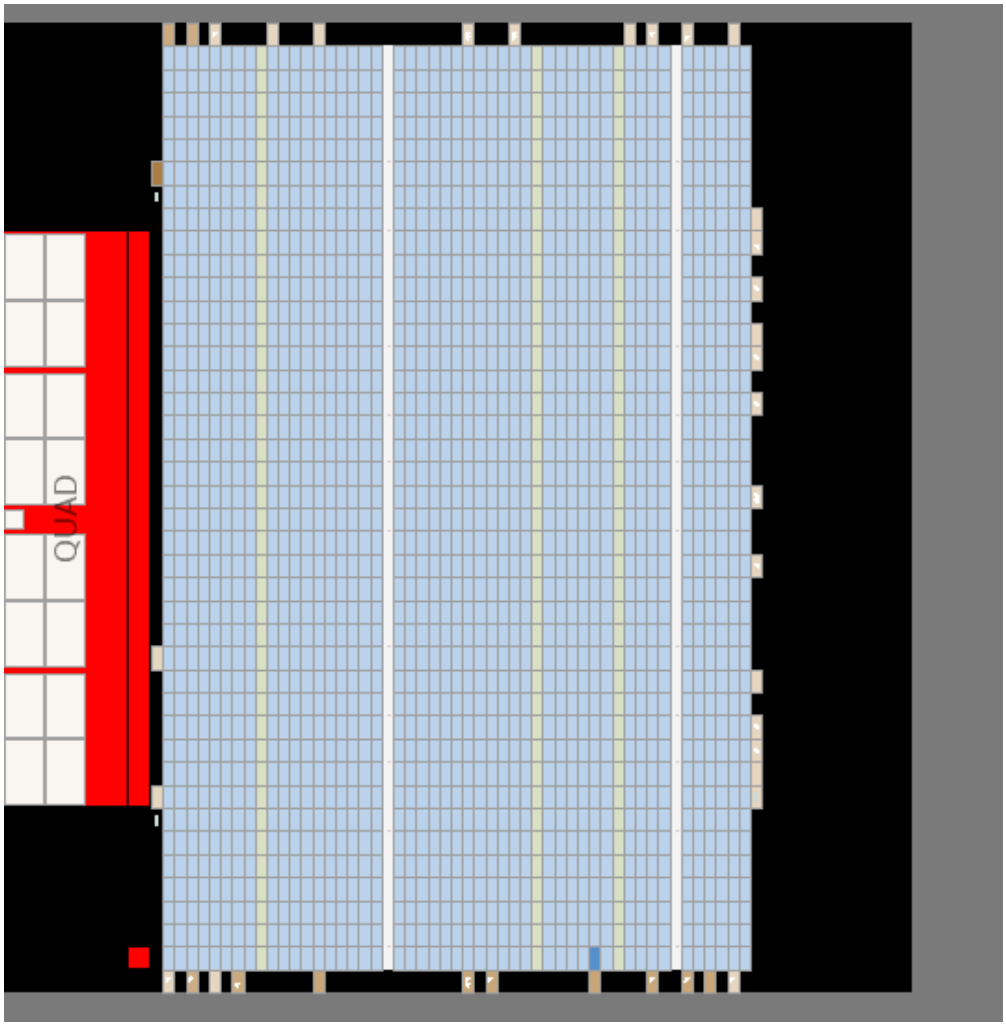
In test bench we can see delay in quartus output:

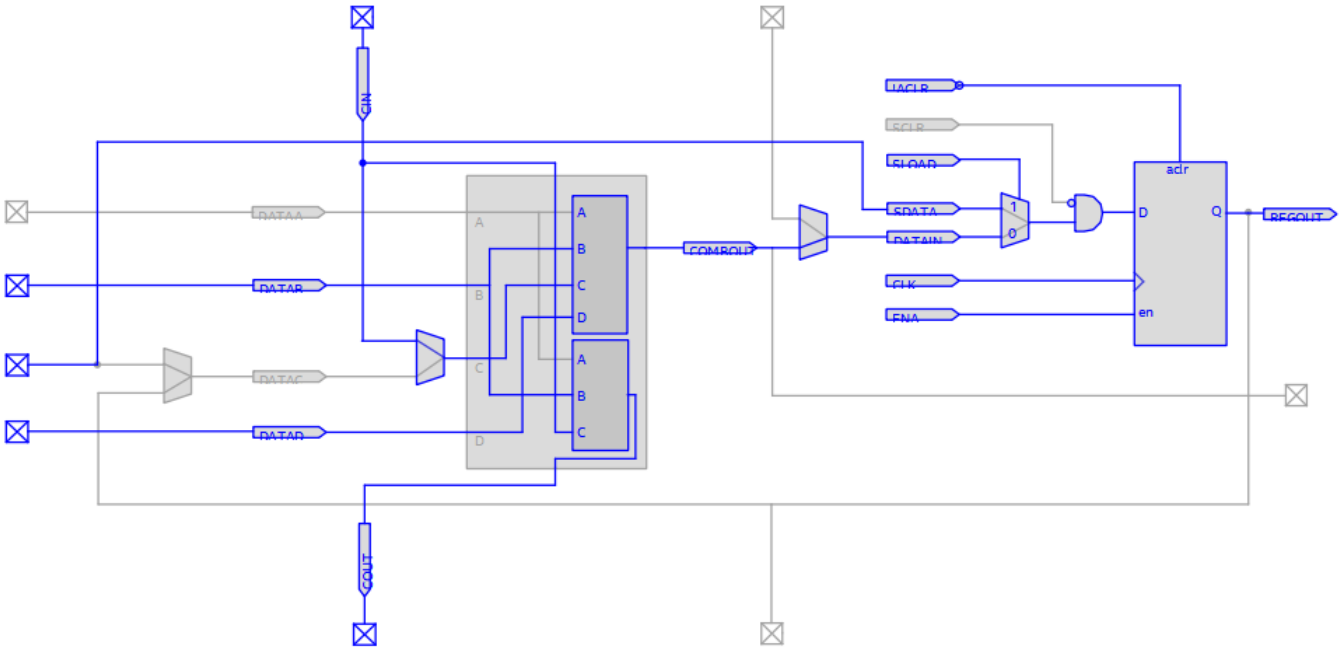


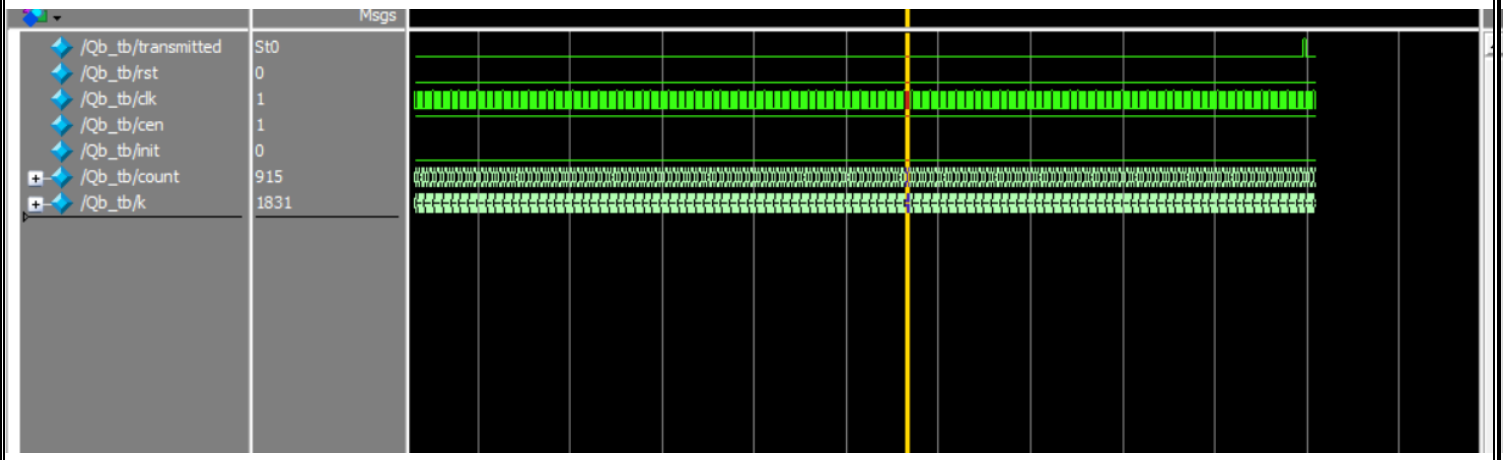
b)



Flow Status	Successful - Mon Jun 13 15:14:30 2022
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	transmitter
Top-level Entity Name	transmitter
Family	Cyclone IV GX
Device	EP4CGX22BF14C6
Timing Models	Final
Total logic elements	12 / 21,280 (< 1 %)
Total registers	10
Total pins	15 / 81 (19 %)
Total virtual pins	0
Total memory bits	0 / 774,144 (0 %)
Embedded Multiplier 9-bit elements	0 / 80 (0 %)
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)


QUAD


CIN
DATAA
DATAB
DATAC
DATAD
A
B
C
D
COMBOUT
SDATA
DATAIN
CLK
ENA
aclr
D
Q
en
REGOUT
COUT


Msgs
/Qb_tb/transmitted
/Qb_tb/rst
/Qb_tb/clk
/Qb_tb/cen
/Qb_tb/init
/Qb_tb/count
/Qb_tb/k
St0
0
1
1
0
915
1831

Part c)

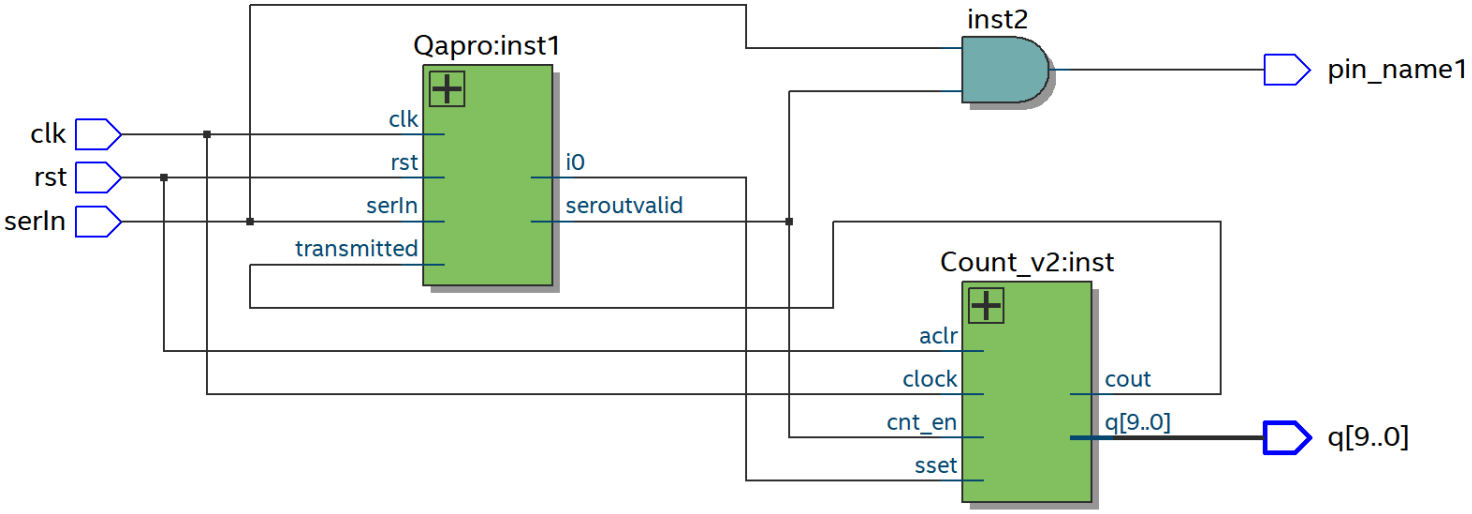
Compilation Report

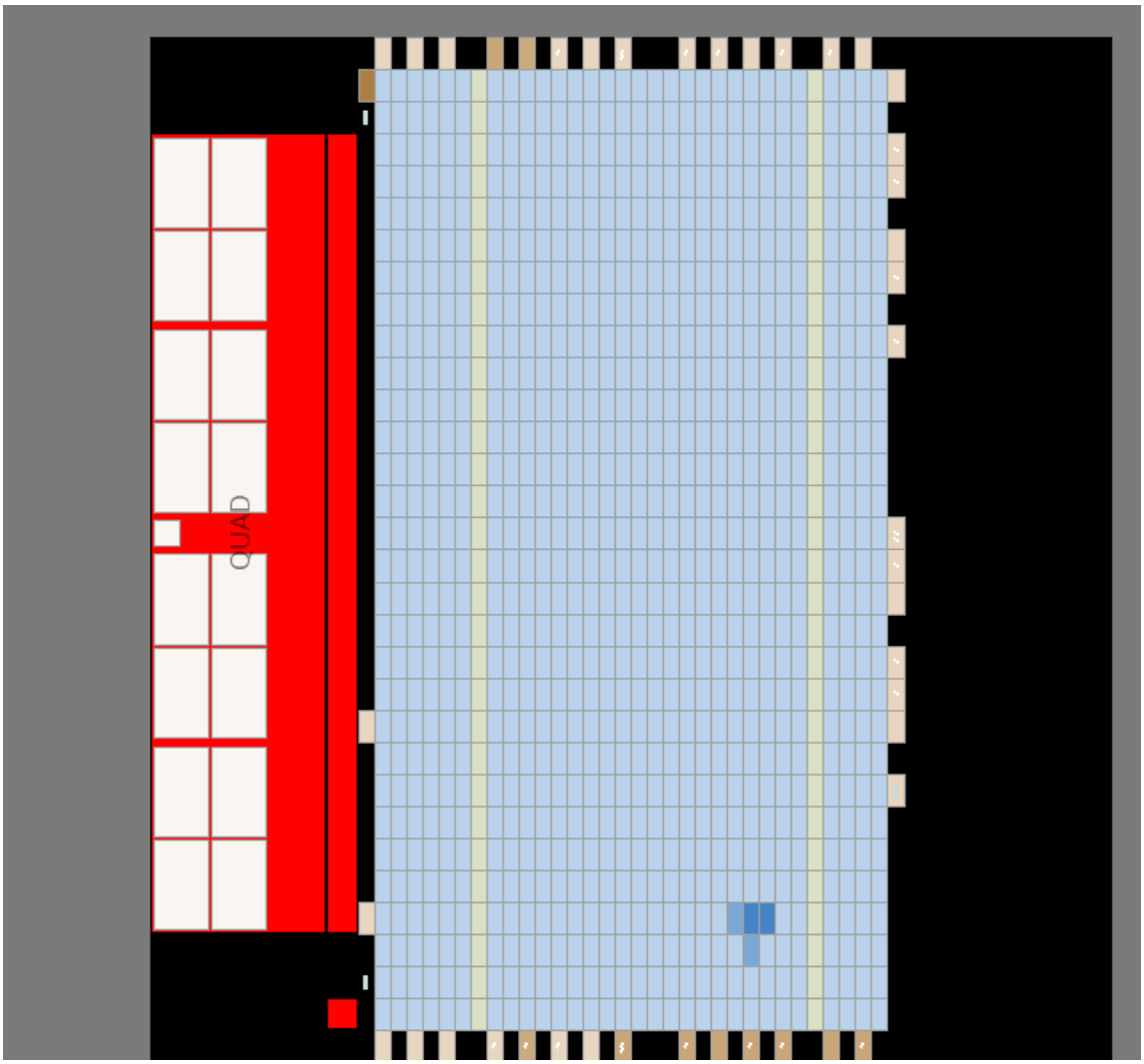
Flow Summary

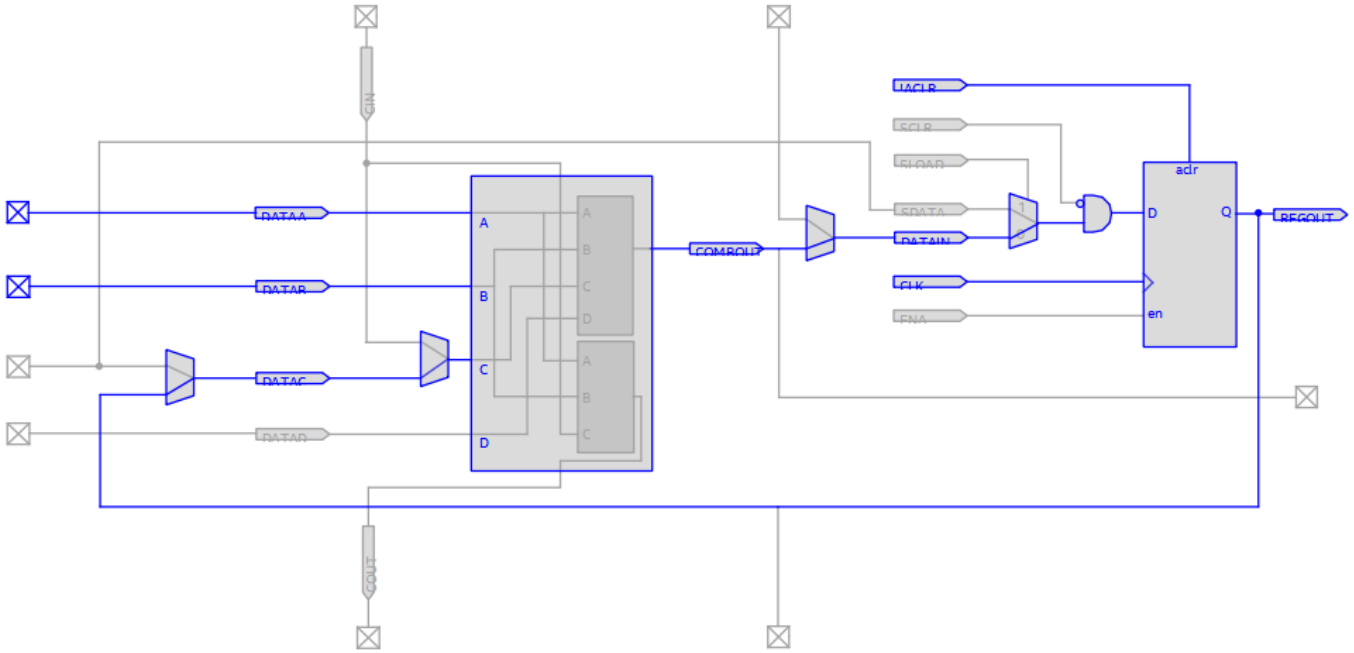
<<Filter>>

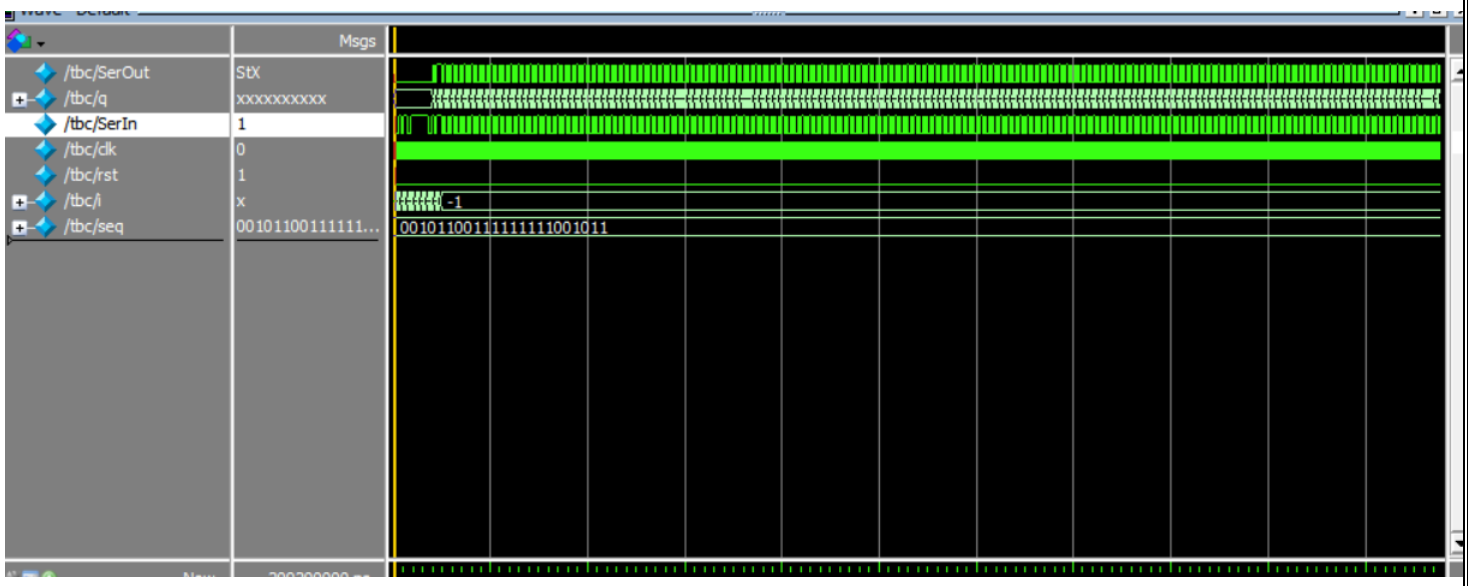
Top-level Entity Name	partc
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	34 / 14,400 (< 1 %)
Total registers	20
Total pins	14 / 81 (17 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Find Next




QUAD


CIN
DATAA
DATAB
DATAC
DATAD
A
B
C
D
COMBOUT
ACLR
SCLR
SLOAD
SDATA
DATAIN
CLK
ENA
aclr
D
Q
en
REGOUT
COUT


Msgs
/tbc/SerOut
/tbc/q
/tbc/SerIn
/tbc/clk
/tbc/rst
/tbc/i
/tbc/seq
StX
xxxxxxxxxx
1
0
1
x
00101100111111...
-1
00101100111111111001011