UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1400-01
Computer Assignment 1
Basic Switch and Gate Structures in SystemVerilog
Week 3

Name:
Date:

1. Generate switch level descriptions for a 3-input OAI (w = ~((a | b) & c)) as a complex gate, a 2-input NOR, and an inverter in Verilog. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. We refer to this as OAI1.

2. Using the NOR and NOT from Part 1, generate another version of OAI with separate gates. We refer to this as OAI2.

3. Generate a testbench for OAI1 and OAI2 and compare the results and timing. In this testbench, find the worst-case delay of the OAI1 and OAI2.

4. Write an OAI description using SystemVerilog primitives. Use delay values of the complex gate OAI1 obtained from the testbench of Part 3to back-annotate into this OAI structure. We refer to this as OAI4.

5. Generate a testbench that will simulate the OAI1, OAI2, and OAI4. Modify the delay values of the OAI4 to match those of OAI1 as closely as possible. We refer to this as OAI5.

6. Using OAI structures and necessary gates of Part 1 develop a circuit to detect if a 4-bit code is a valid BCD number.

7. Using OAI1, OAI2, OAI5 Implement three versions of the BCD detector of Part 6.

8. In a testbench, instantiate the three BCD detectors of the above part and compare their timings and simulations. Explain the differences between these two circuits as far as the number of transistors and other physical parameters such as power consumption.

Deliverables:

Generate a report that includes item discussed below for each of the five parts of this CA. Do not show any code without first showing its circuit diagram.

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.
B. Hand-simulate the circuits you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog descriptions of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your SV codes are properly indented and all line-up rules are followed.
D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulations are complete, or even if you have a partial simulation, include an image of the output waveforms showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.