UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1400-01
Computer Assignment 6
Complete RTL Circuits - Week 16

Tailor series is one of well-known methods to compute mathematical functions such as *sin(x)*, *cos(x)*, *exp*, etc. In this problem you are to design a sequential circuit that computes an approximation of *cosh()* using the first 8 terms of its Tailor expansion.

$$\cosh(x) \cong \sum_{k=0}^{7} \frac{x^{2k}}{(2k)!}$$

The following algorithm can be used to approximate *cosh()*:

```
e = 1;
a = 1;
for (k = 1; k < 16; k=k+2) {
    a = a * x;
    a = a * x;
    a = a * (1/k)
    a = a * (1/(k+1))
    e = e + a;
}
```

The *cosh ()* module accepts a 16-bit fixed point value on *x* after *start* is asserted. After that, computation is started. During the computation, the *busy* signal is asserted. After the completion of the computation, the result becomes available on output *y*, *busy* is deactivated, and *ready* is issued.

Assume $0 \le x < 1$, and all numbers are represented in 16-bit fixed point format. In addition, a 16-bit fixed point adder and a 16-bit fixed point array multiplier are available for you to use as datapath components. Moreover, values for $1/k$, for $1 \le k \le 16$, have been computed, and are stored in a combinational lookup table. The table has four address lines and a 16-bit data output.

A) Generate a ROM in Quartus II for the required memory of factorial calculations.
B) Design the datapath of module *cosh(x)*, and implement it in Quartus II.
C) Write SystemVerilog description for the controller of module *cosh(x)*.
D) Complete the datapath and controller of your circuit and develop a testbench for it.