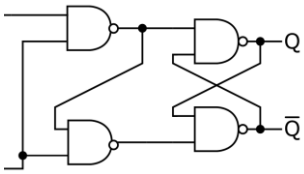
UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1400-01
Computer Assignment 4

Basic Memory Structures, Latches and Flip-flops - Week 10

Name:	**Date:**
Username:	

In this assignment, you will be experimenting with latches and flip-flops and see their timing and functionality differences.

1. Generate a clocked D-latch with D and Clock inputs as shown in the following diagram. Describe this circuit in Verilog using NAND primitives.



2. Annotate the circuit of Part 1 with gate delays that are based on switch level delays of 4 NS for the nMOS and 6 NS for the pMOS transistors.
3. Simulate the circuit of Part 2 to verify its operation. For the start of simulation, the outputs begin with X values. You need to create a *D* and *Clk* signaling that will force the latch into a known and stable state. Exercise this circuit for cases that you think a glitch on output of a gate is possible. Show situations that this structure behaves as a latch, thus, has transparency.
4. Provide a reset (*rst*) input for the above latch that, when active, it will force the output to 0 and will keep the output at this value after *rst* is no longer active.
5. Form an 8-bit multi-shift right rotate (MSRR8) using eight of the above latches. The circuit has four modes of operation, *mode*=00, 01, 10, and 11. Mode 00 is for do nothing, mode 01 is for rotate right one position, 10 is for rotate right two positions, and 11 is for serial right-shift one position. Use *sIn* (serial input) for the serial shift mode.
6. Simulate the circuit of Part 5 and explain why or why-not this circuit works as expected.
7. Build a D-type flip-flop using two of the above latches. Add an active high synchronous reset input to the flip-flop. Simulate this flip-flip and check its edge triggering behavior and the resetting mechanism that you inserted in the flip-flop.
8. Build an 8-bit multi-shift right rotate (MSRR8) using the flip-flops of Part 7 in a **generate** statement.
   a. Write a testbench for this circuit and verify its clocking and resetting operations.
   b. Extend the testbench to include its shift operation.

9. Use an **always** statement to describe the circuit of Part 7. Verify its operation using a SystemVerilog testbench.

10. In a testbench compare simulations of the shift register built by putting gates together and the one with the **always** statement. Explain the differences.

Deliverables:

Generate a report that includes all the items below:

A. Prior coming to the lab, for all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.

B. For all problems, be prepared to answer questions asked about the timings, minimum pulse widths, and time distance between various signals.

C. Below is an itemized list tasks for each of the above problems:
   1. Show diagram; Hand simulate; Write SystemVerilog
   2. Annotate circuit diagram;
   3. Perform simulation; Exercise with timing;
   4. Perform simulation; Hand analyze;
   5. Show diagram; Write SystemVerilog;
   6. Simulate and analyze;
   7. Show diagram; Write SystemVerilog; Hand simulate;
   8. Show diagram; Write SystemVerilog; Write testbench; Perform simulation
   9. Write SystemVerilog; Write testbench; Perform simulation; Compare results

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.