In the name of God

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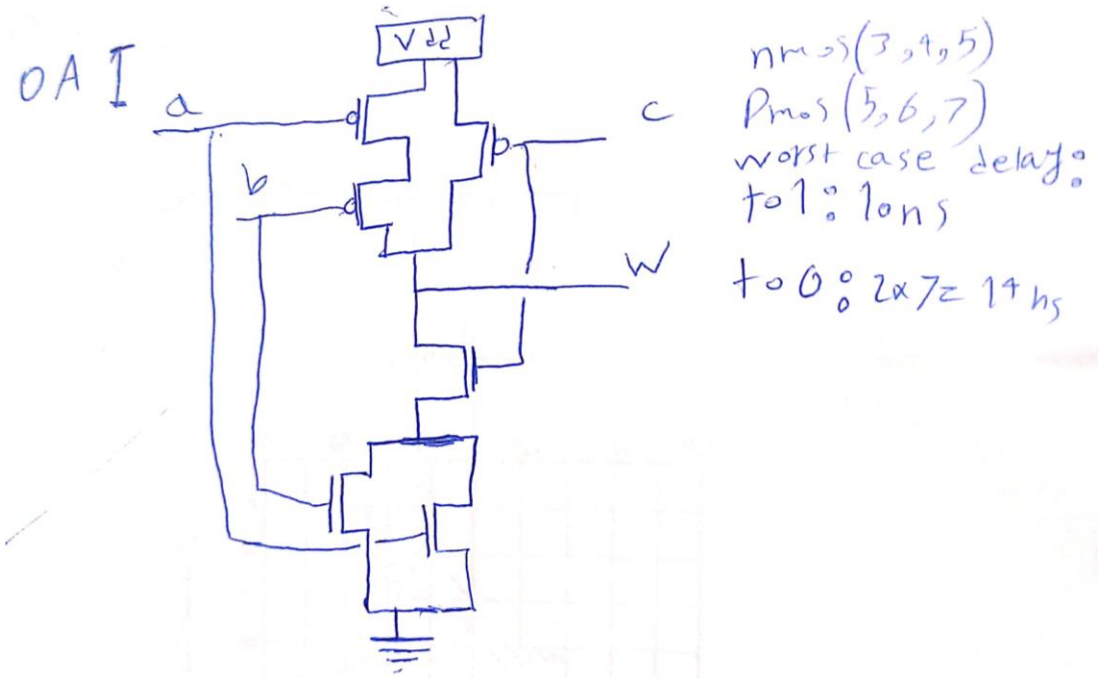
CA1

Q1:

For OAI1 :

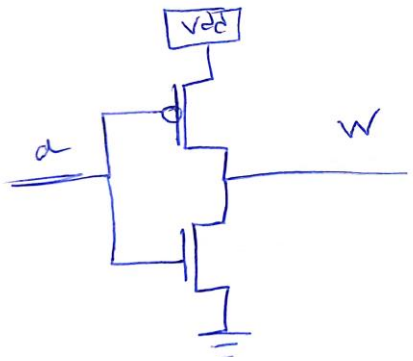
```
1
2   module OAI1(input a,b,c, output w);
3   supply1 Vdd;
4   supply0 Gnd;
5   wire y1,y2;
6
7   pmos #(5,6,7) T1 (y1,Vdd,a);
8   pmos #(5,6,7) T2 (w,y1,b);
9   pmos #(5,6,7) T3 (w,Vdd,c);
10
11  nmos #(3,4,5) T4 (y2,Gnd,a);
12  nmos #(3,4,5) T5 (y2,Gnd,b);
13  nmos #(3,4,5) T6 (w,y2,c);
14  endmodule
15
```



For nor & not:

```
2
3   module not1(input a, output w);
4   supply1 Vdd;
5   supply0 Gnd;
6
7   pmos #(5,6,7) T1 (w,Vdd,a);
8   nmos #(3,4,5) T2 (w,Gnd,a);
9   endmodule
10
```

inverter



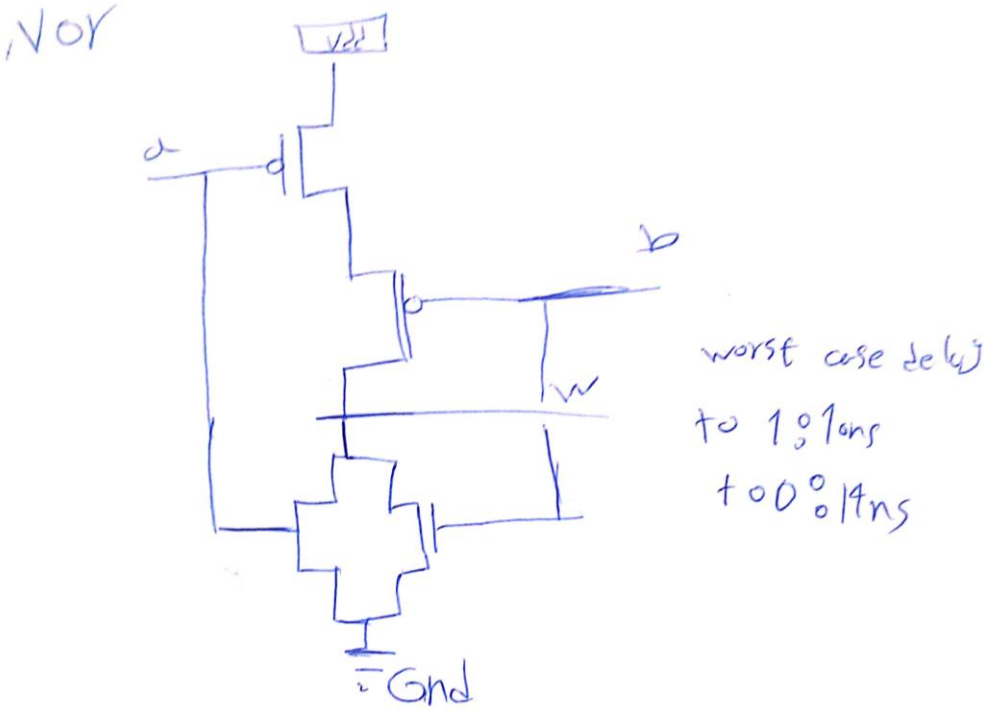
worst case delay:
to 1: 5ns
to 0: 7ns

```
module nor1(input a,b, output w);
supply1 Vdd;
supply0 Gnd;
wire y;

pmos #(5,6,7) T1 (y,Vdd,a);
pmos #(5,6,7) T2 (w,y,b);

nmos #(3,4,5) T3 (w,Gnd,a);
nmos #(3,4,5) T4 (w,Gnd,b);

endmodule
```

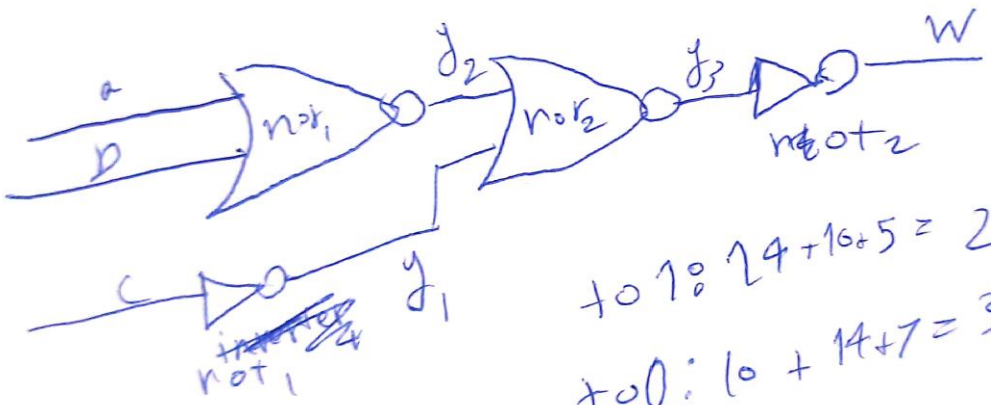


Q2:

```
module OAI2(input a,b,c, output w);


wire y1,y2,y3;
not1 t1(c, y1);
nor1 t2(a,b,y2);
nor1 t3(y2, y1,y3) ;
not1  t4 (y3,w);

endmodule
```



to 1: 14 + 10.5 = 29 ns
to 0: 10 + 14 + 7 = 31 ns
} worst case

Q3)

I:/CA!/3-benchtest.sv (/tb)

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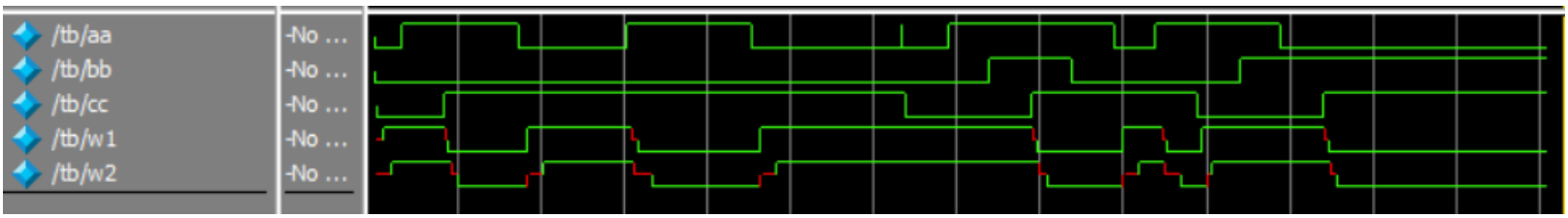
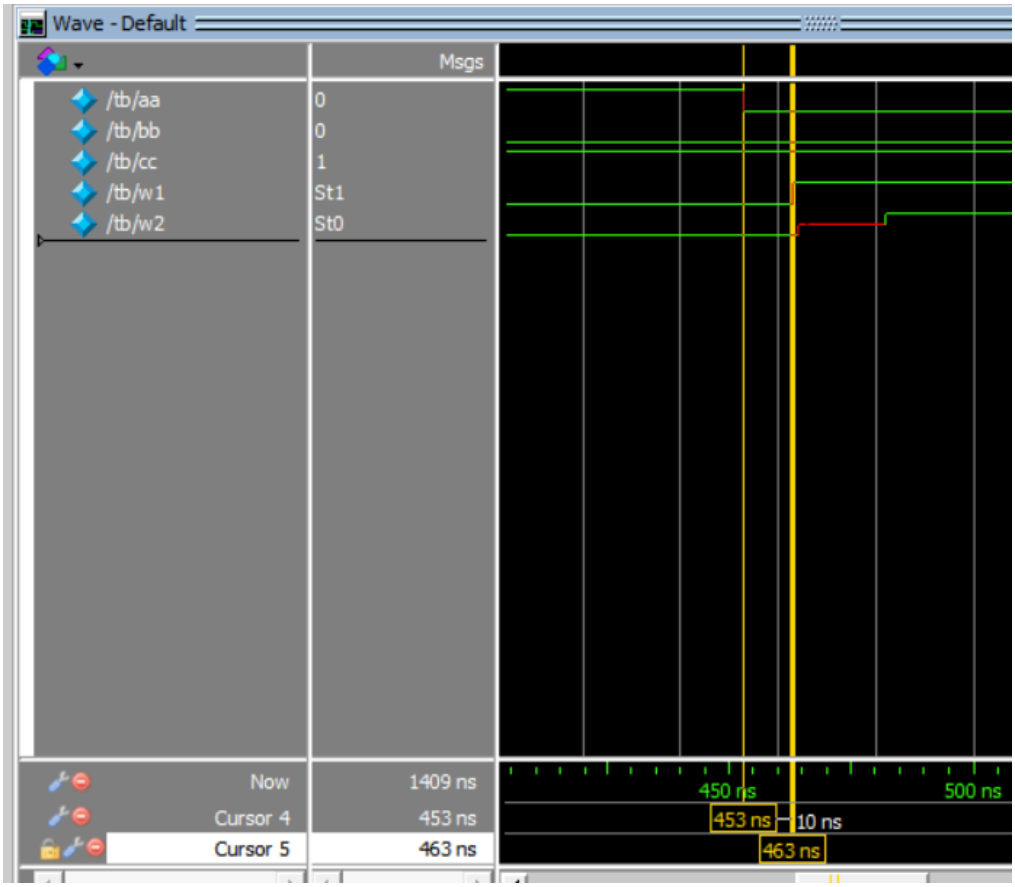
I:/CA!/3-benchtest.sv (/tb) - Default *

```
Ln#
 1  `timescale 1ns/1ns
 2
 3  module tb();
 4  logic aa , bb, cc;
 5  wire w1,w2;
 6
 7  OAI1 CUT_1(.a(aa),.b(bb),.c(cc),.w(w1));
 8  OAI2 CUT_2(.a(aa),.b(bb),.c(cc),.w(w2));
 9
10  initial begin
11  #1 aa=0;
12  #1 bb=0;
13  #1 cc=0;
14  #30 aa=1;
15  #50 cc=1;
16  #90 aa=0;
17  #130 aa=1;
18  #150 aa=0;
19  #180 aa=1;
20
21  #220 $stop;
22  end
23
24
25  endmodule
```



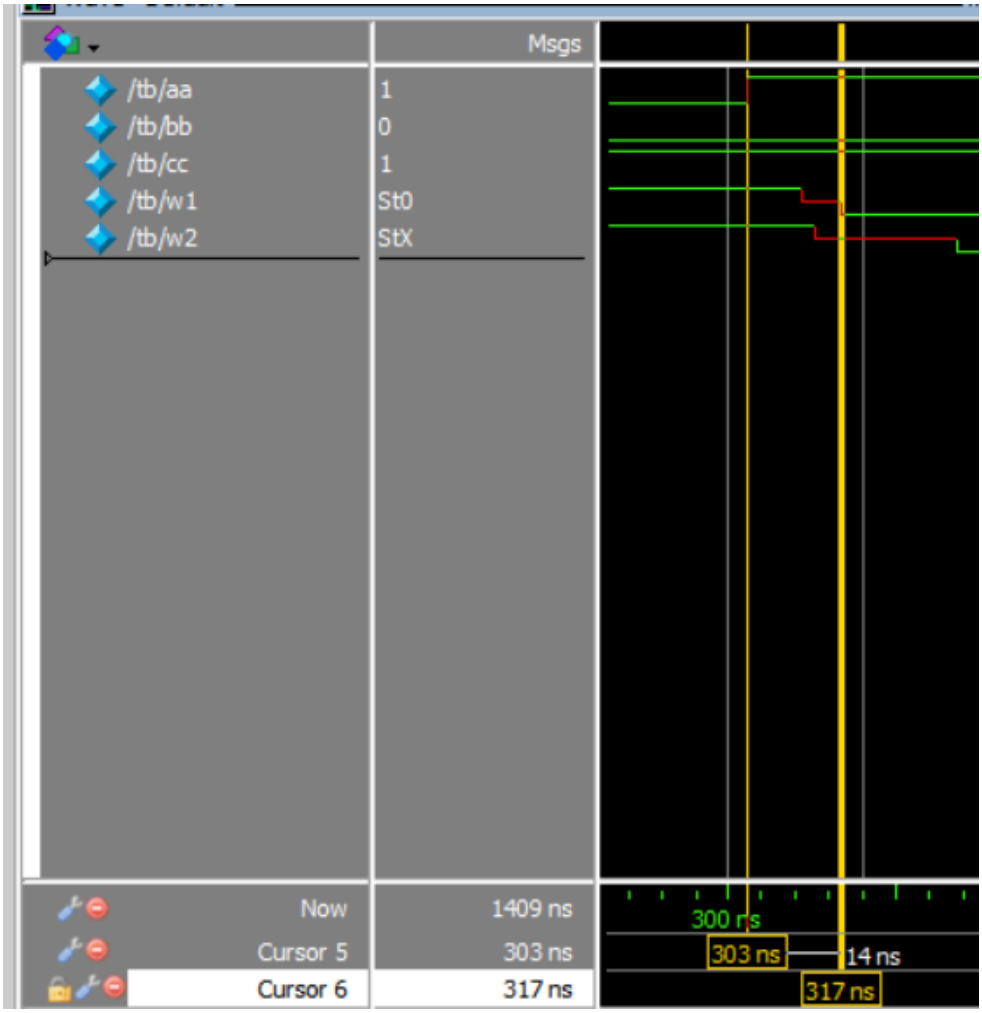
For OAI1:

Worst delay for to1 is 10ns



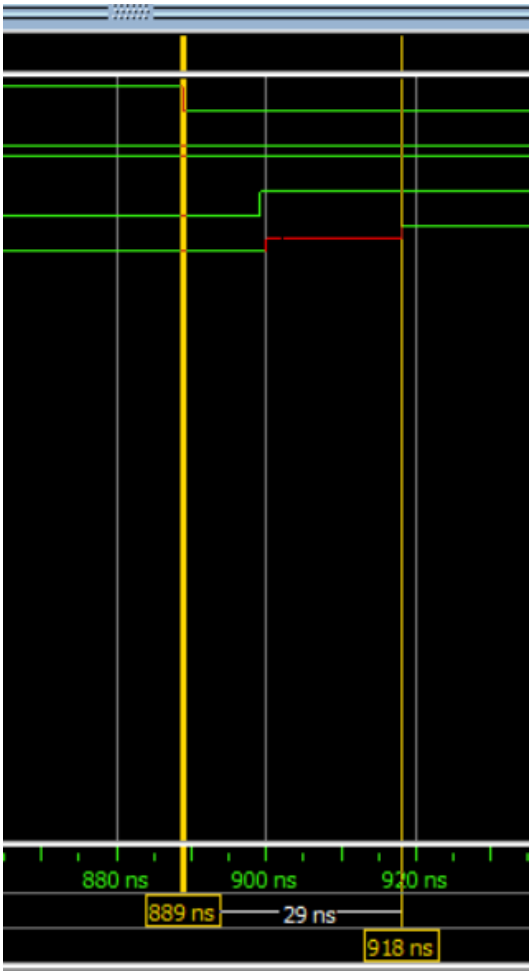
or OAI1:

Worst delay for to0 is 14ns



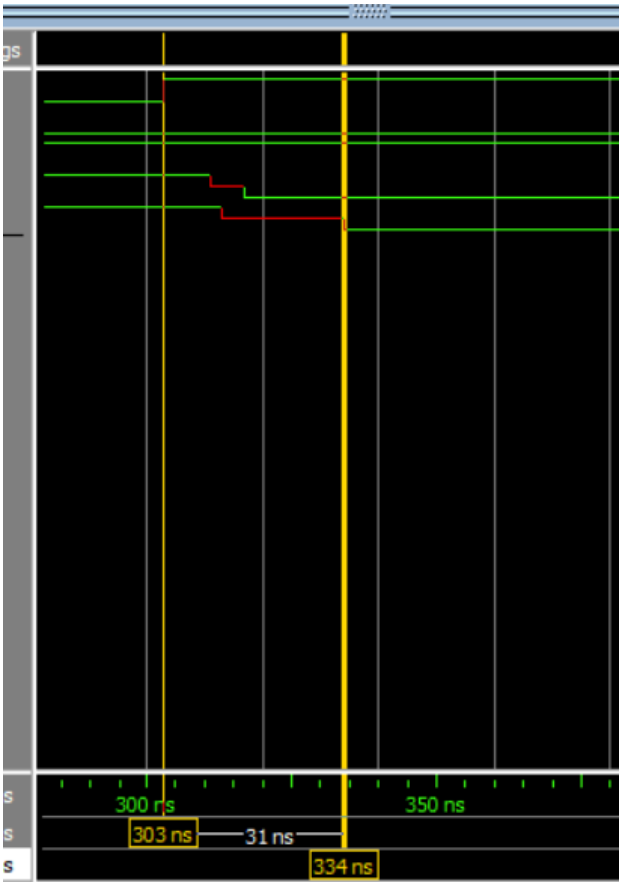
or OAI2:

Worst delay for to1 is 29ns



or OAI2:

Worst delay for to0 is 31ns



Q4)

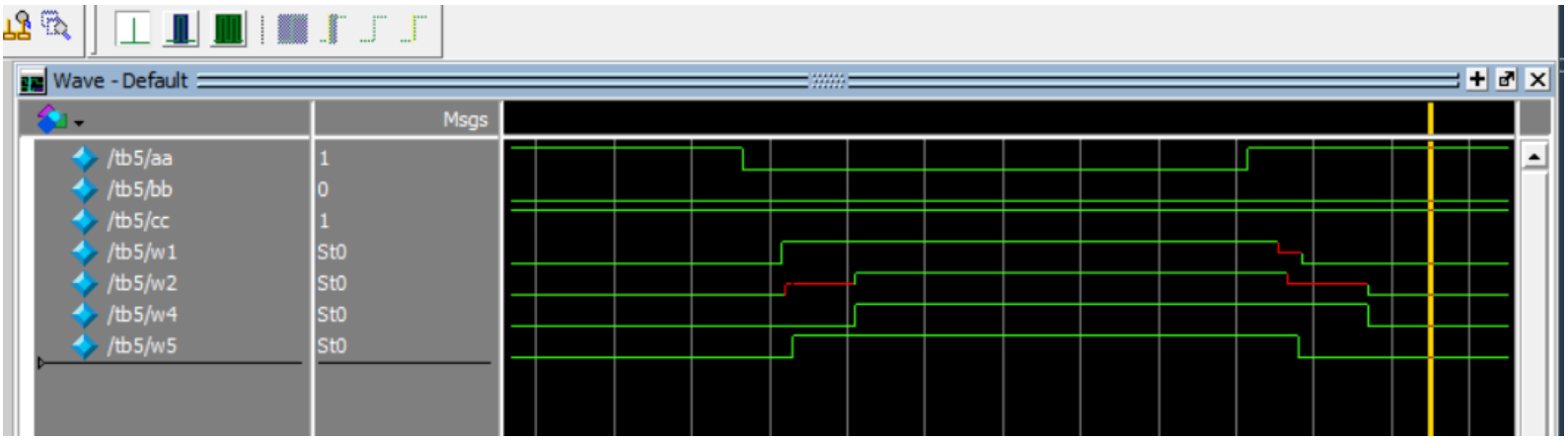
According to Q1 we create it with Not and Nor

```
`timescale 1ns/1ns
module OAI4(input a,b,c, output w);

wire y1,y2,y3;

not #(5,7) t1(y1, c);
nor #(10,14) t2(y2,b,a);
nor #(10,14) t3(y3, y1,y2) ;
not #(5,7) t4 (w,y3);

endmodule
```

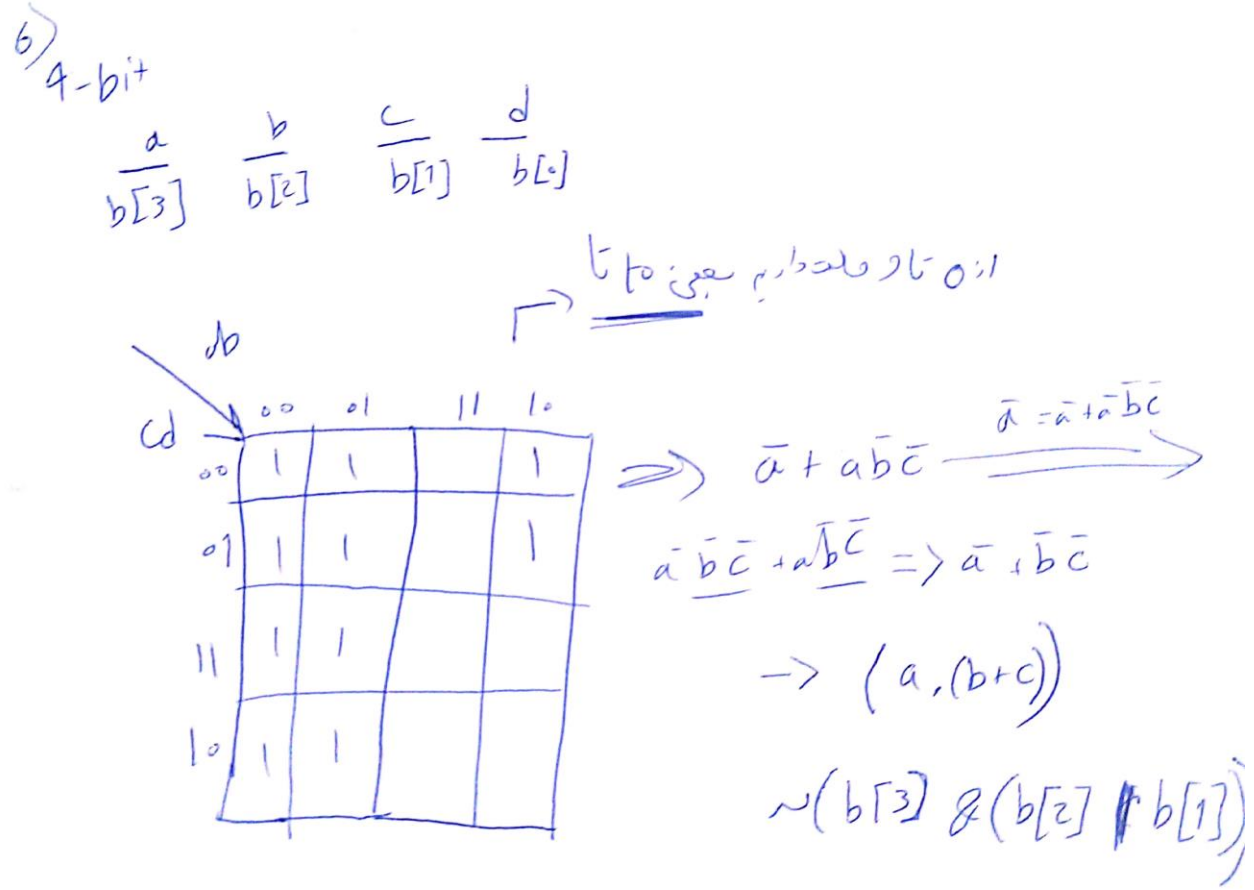
Q5:

```
`timescale 1ns/1ns
module OAI5(input a,b,c, output w);

wire y1,y2,y3;

not #(4,4) t1(y1, c);
nor #(4,5) t2(y2,b,a);
nor #(4,5) t3(y3, y1,y2) ;
not #(4,4) t4 (w,y3);

endmodule
```

```
1   `timescale 1ns/1ns
2
3   module tb5();
4   logic aa , bb, cc;
5   wire w1,w2,w4,w5;
6
7   OAI1 CUT_1(.a(aa),.b(bb),.c(cc),.w(w1));
8   OAI2 CUT_2(.a(aa),.b(bb),.c(cc),.w(w2));
9   OAI4 CUT_4(.a(aa),.b(bb),.c(cc),.w(w4));
10  OAI5 CUT_5(.a(aa),.b(bb),.c(cc),.w(w5));
11
12  initial begin
13  #1 aa=0;
14  #1 bb=0;
15  #1 cc=0;
16  #30 aa=1;
17  #50 cc=1;
18  #90 aa=0;
19  #130 aa=1;
20  #150 aa=0;
21  #180 aa=1;
22  #220 $stop;
23  end
24
25  endmodule
```



Q6



In here:

B1=c

B2=b

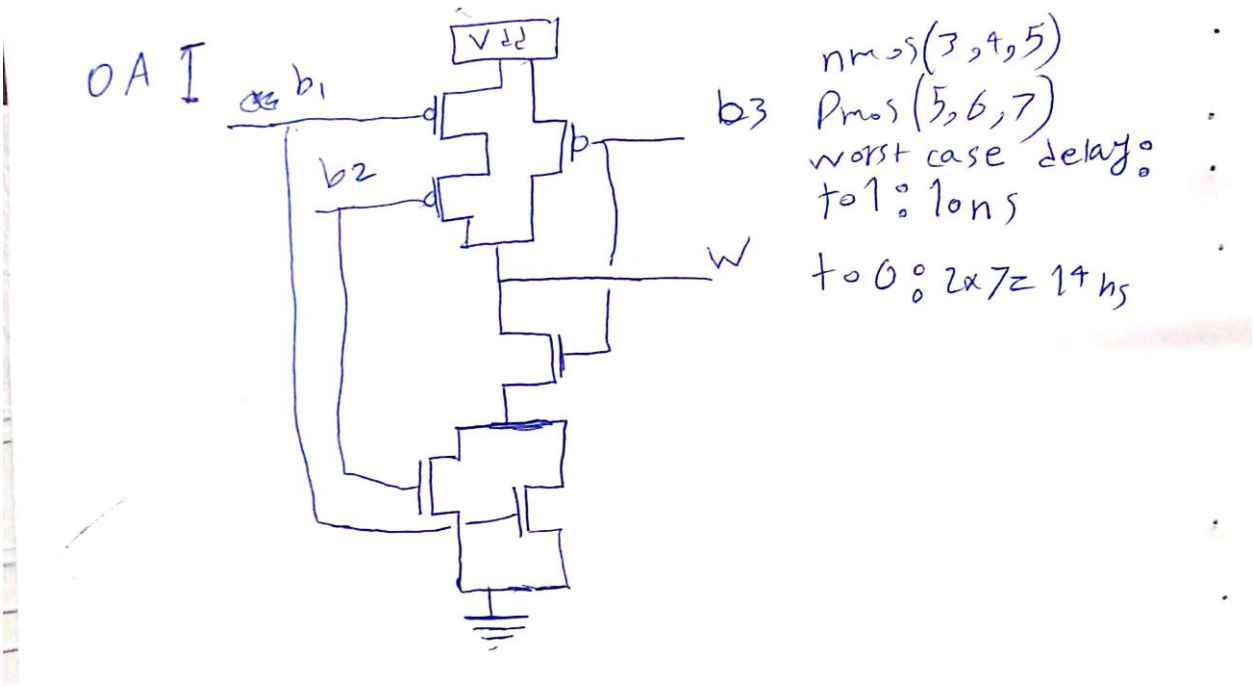
B3=a

Q7

I:/CA!/bcd1.sv - Default

Ln#

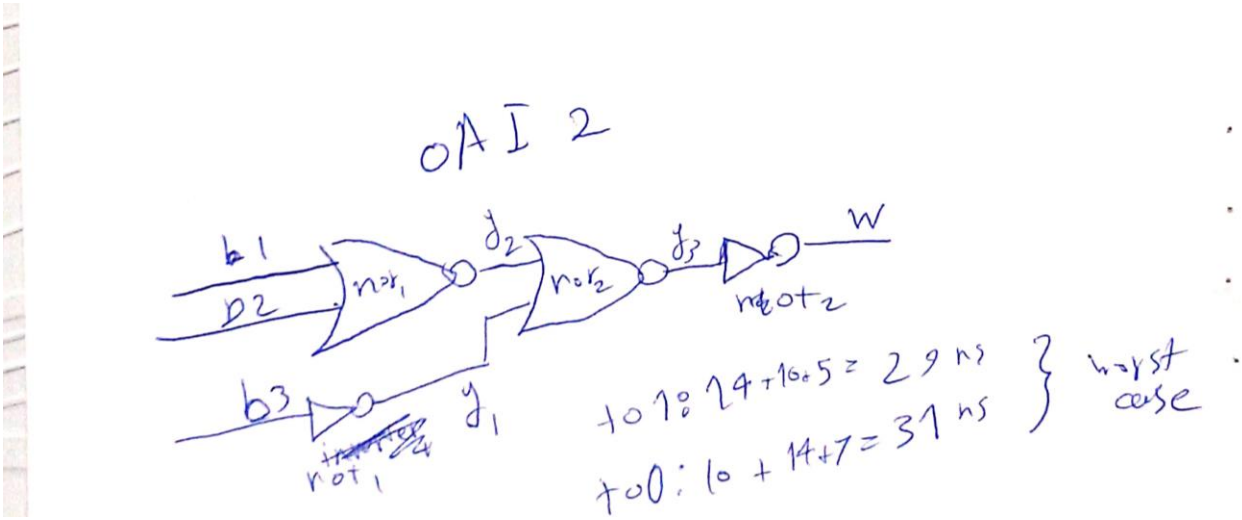
```
1  `timescale 1ns/1ns
2  module BCD1(input a,b,c,d, output w);
3  OAI1 bcd1(c,b,a,w);
4  endmodule
5
```



OAI2

I:/CA!/bcd2.sv - Default

```
Ln#
1   `timescale 1ns/1ns
2   module BCD2(input a,b,c,d, output w);
3   OAI2 bcd2(c,b,a,w);
4   endmodule
5
```

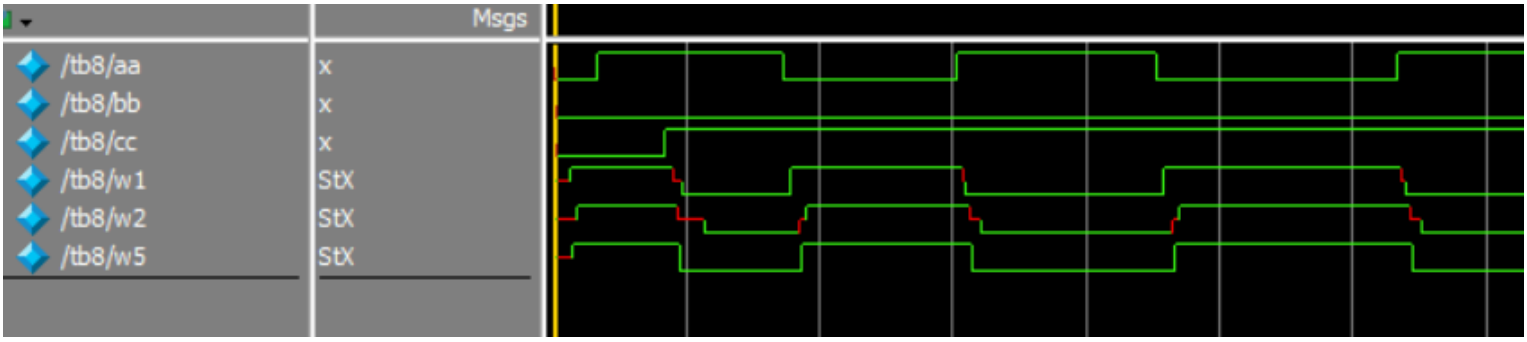


OAI5

```
1   `timescale 1ns/1ns
2   module BCD5(input a,b,c,d, output w);
3   OAI5 bcd5(c,b,a,w);
4   endmodule
```

Q8:

```
`timescale 1ns/1ns

module tb8();
logic aa , bb, cc;
wire w1,w2,w5;
BCD1 CUT_1(.a(aa),.b(bb),.c(cc),.w(w1));
BCD2 CUT_2(.a(aa),.b(bb),.c(cc),.w(w2));
BCD5 CUT_5(.a(aa),.b(bb),.c(cc),.w(w5));
initial begin
#1 aa=0;
#1 bb=0;
#1 cc=0;
#30 aa=1;
#50 cc=1;
#90 aa=0;
#130 aa=1;
#150 aa=0;
#180 aa=1;
#220 $stop;
end
endmodule
```



Comparison:

delay: BCD1 < BCD5< BCD2

having X dalay: BCD5 < BCD1< BCD2

number of the transistors have been used:

BCD1 = 6

BCD2= 12

BCD5 = 12

According to the waves and result, we can say that the more transistors and delay on passing X be more, it consumes more energy.

BCD1 < BCD5< BCD2