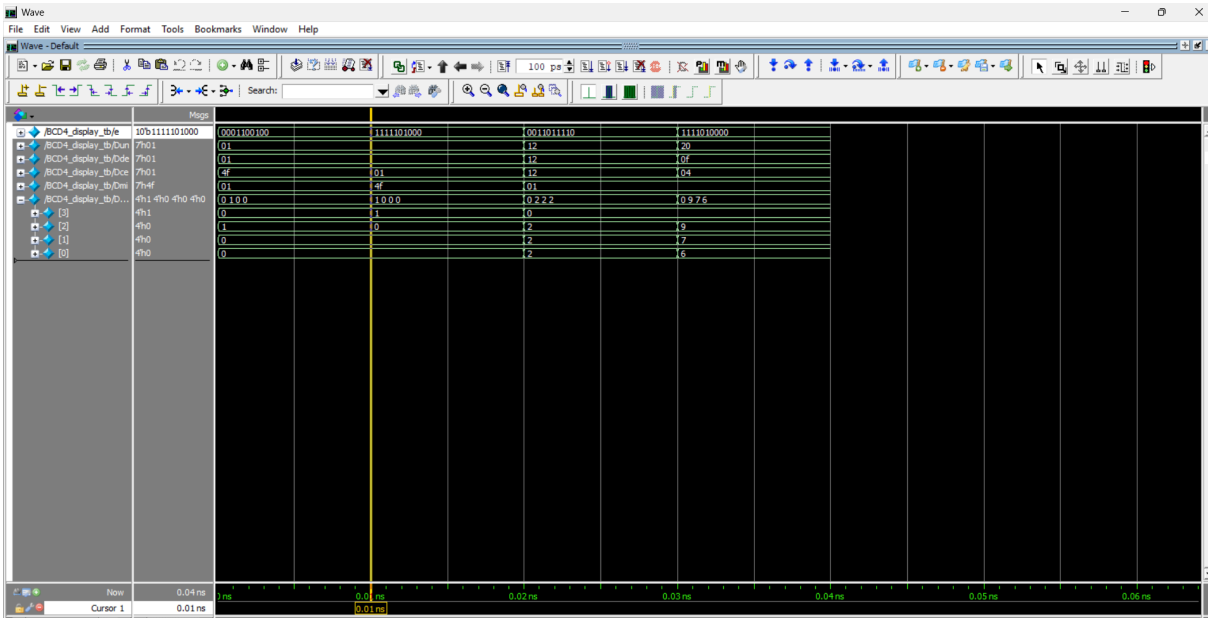
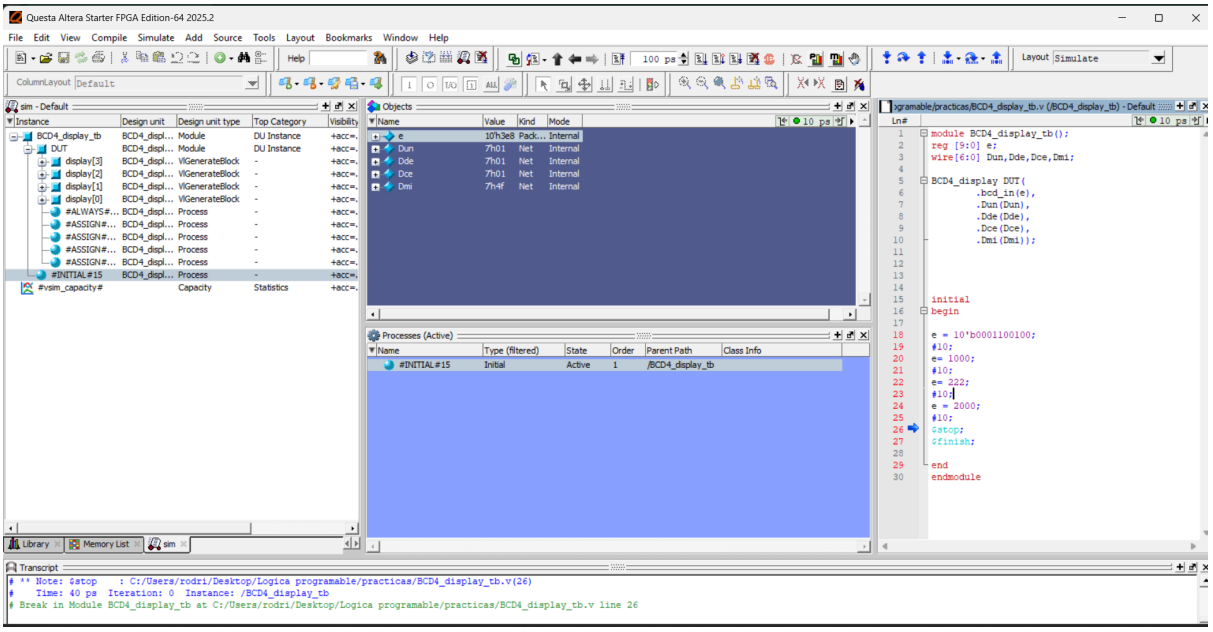
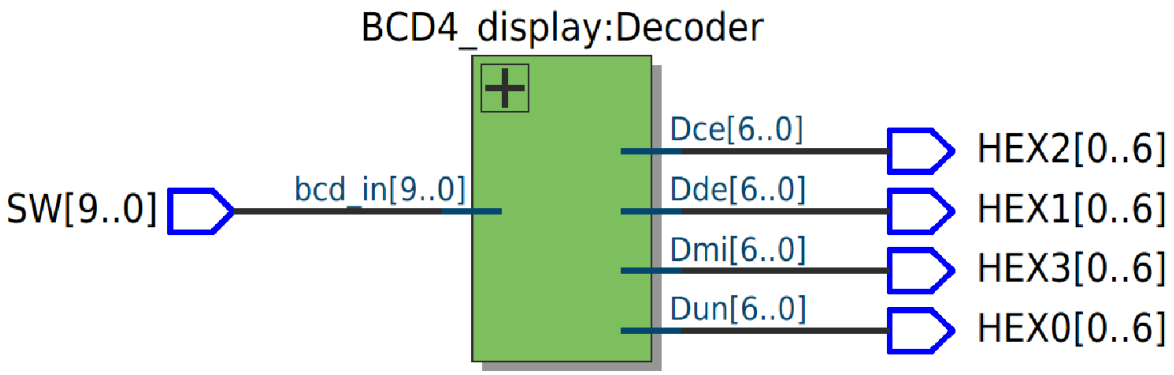
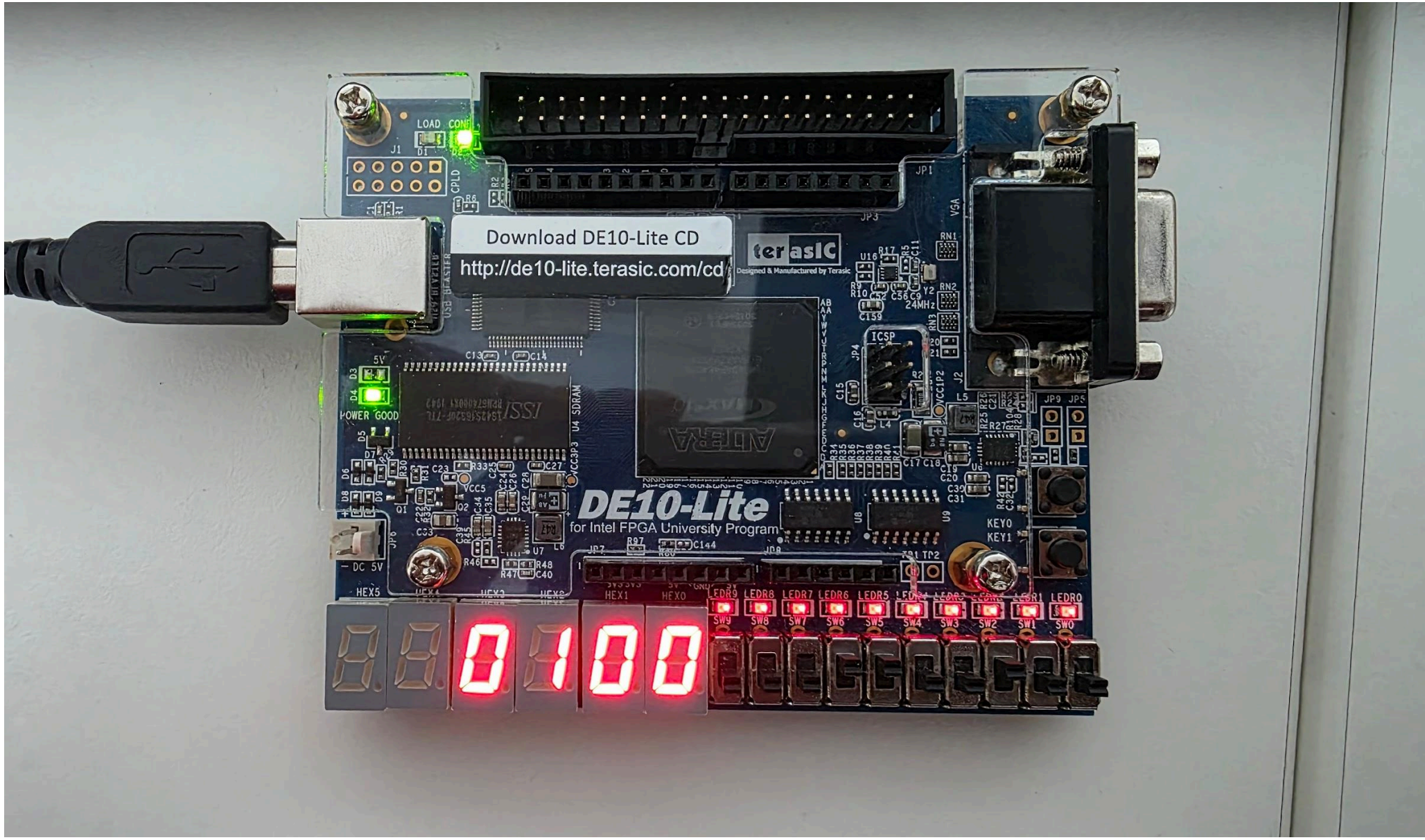
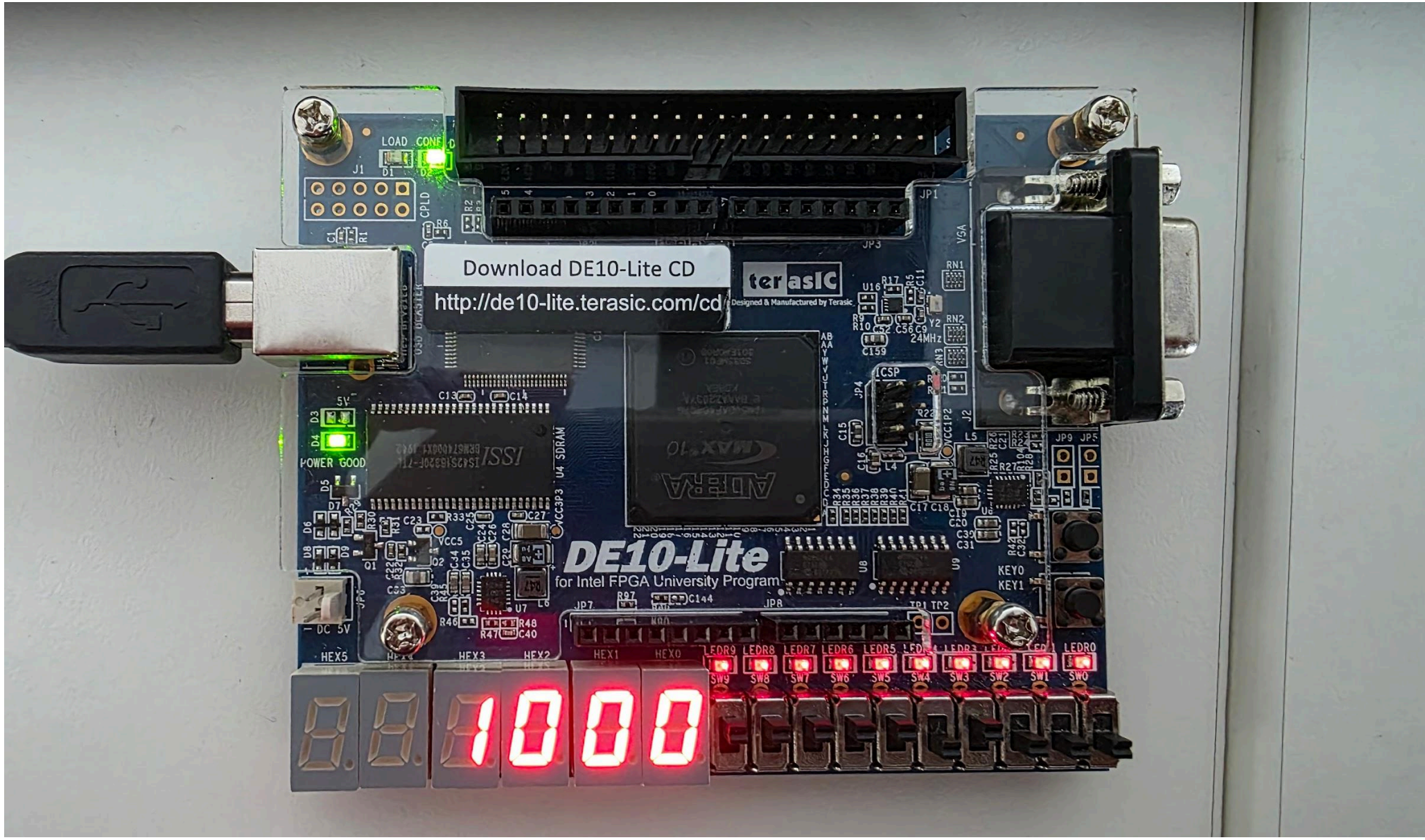
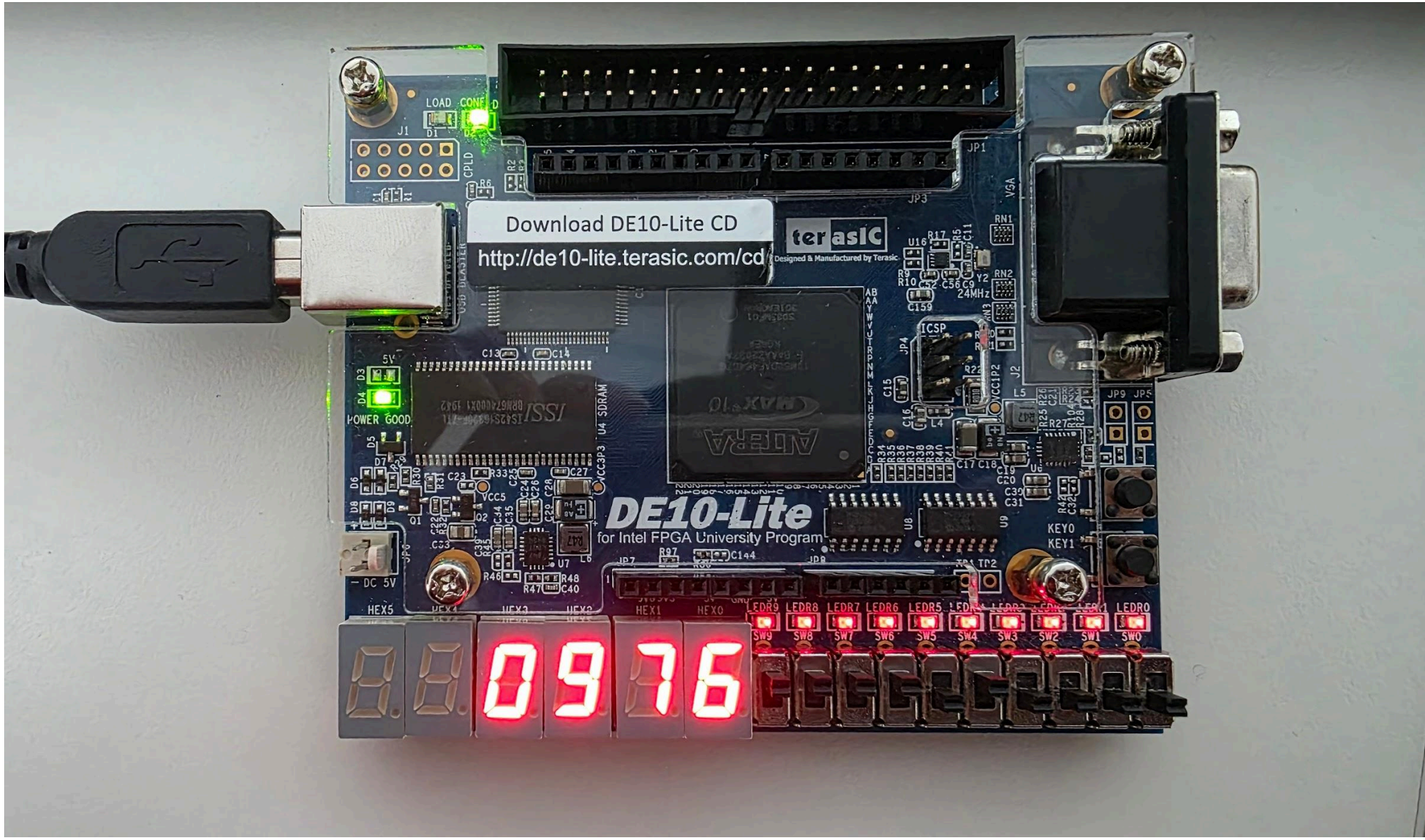

Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
/BCD4_display_tb/e
/BCD4_display_tb/Dun
/BCD4_display_tb/Dde
/BCD4_display_tb/Dce
/BCD4_display_tb/Dmi
/BCD4_display_tb/D...
[3]
[2]
[1]
[0]
Now
Cursor 1


Questa Altera Starter FPGA Edition-64 2025.2
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
sim - Default
Objects
Processes (Active)
Transcript
module BCD4_display_tb();
reg [9:0] e;
wire[6:0] Dun,Dde,Dce,Dmi;
BCD4_display DUT(
.bcd_in(e),
.Dun(Dun),
.Dde(Dde),
.Dce(Dce),
.Dmi(Dmi));
initial
begin
e = 10'b0001100100;
#10;
e= 1000;
#10;
e= 222;
#10;
e = 2000;
#10;
$stop;
$finish;
end
endmodule


BCD4_display:Decoder
SW[9..0]
bcd_in[9..0]
Dce[6..0]
Dde[6..0]
Dmi[6..0]
Dun[6..0]
HEX2[0..6]
HEX1[0..6]
HEX3[0..6]
HEX0[0..6]


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
Designed & Manufactured by Terasic
DE10-Lite
for Intel FPGA University Program
0100


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
Designed & Manufactured by Terasic
DE10-Lite
for Intel FPGA University Program
1000


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
Designed & Manufactured by Terasic
DE10-Lite
for Intel FPGA University Program
0976