Lab 1

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ECE 5440

1. Number Matching Game
   1. This game require 2 players, each player will take turn to input a single (4 bits) number. The first player will start out with the switches SW0 – SW3 with SW0 being the least significant bit. After the first player input the first number, the number will show up in the 7 segments display HEX3. After this, it is player 2 turn. The player 2 will input another number using switches SW14 – SW17 with SW14 being the least significant bit. After the second player input the number, their number will show up in the 7 segments display HEX6. Each time the player input a number, the sum of both number from player one and player two will show up in 7 segments display HEX5. All the number show up in the 7 segments display will be in base 16.
2. Module Presentations
   1. Adder module: Add two number from input\_A and input\_B.

out

Input\_A

4

4

4

Figure 1: adder module.

display

Input\_B

adder

* 1. 7segDesplay: display input number on a seven segments display (base 16).

7

4

Output

Input

Figure 2: display module.

* 1. Top level: architecture of the system. Take in inputs, display them, then add 2 inputs and display the sum. All displays will be shown in base 16

4

4

7

7

HEX5

HEX3

Input\_A

display

display

adder

display

Figure 3: top-level module.

7

HEX6

Input\_B

1. Stimulation

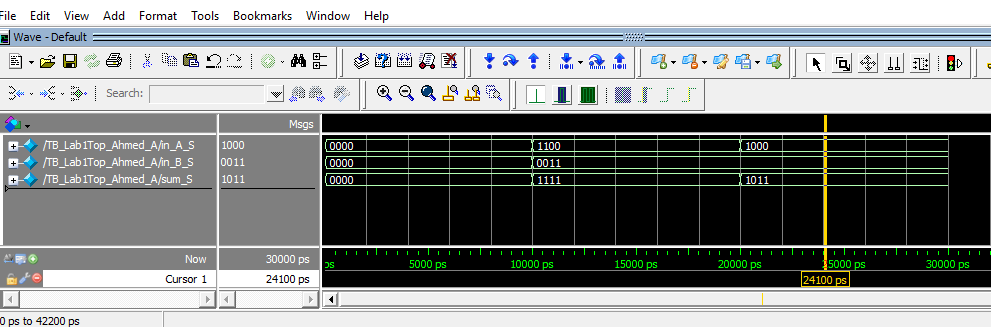


Figure 4: Test-bench stimulation waveform.

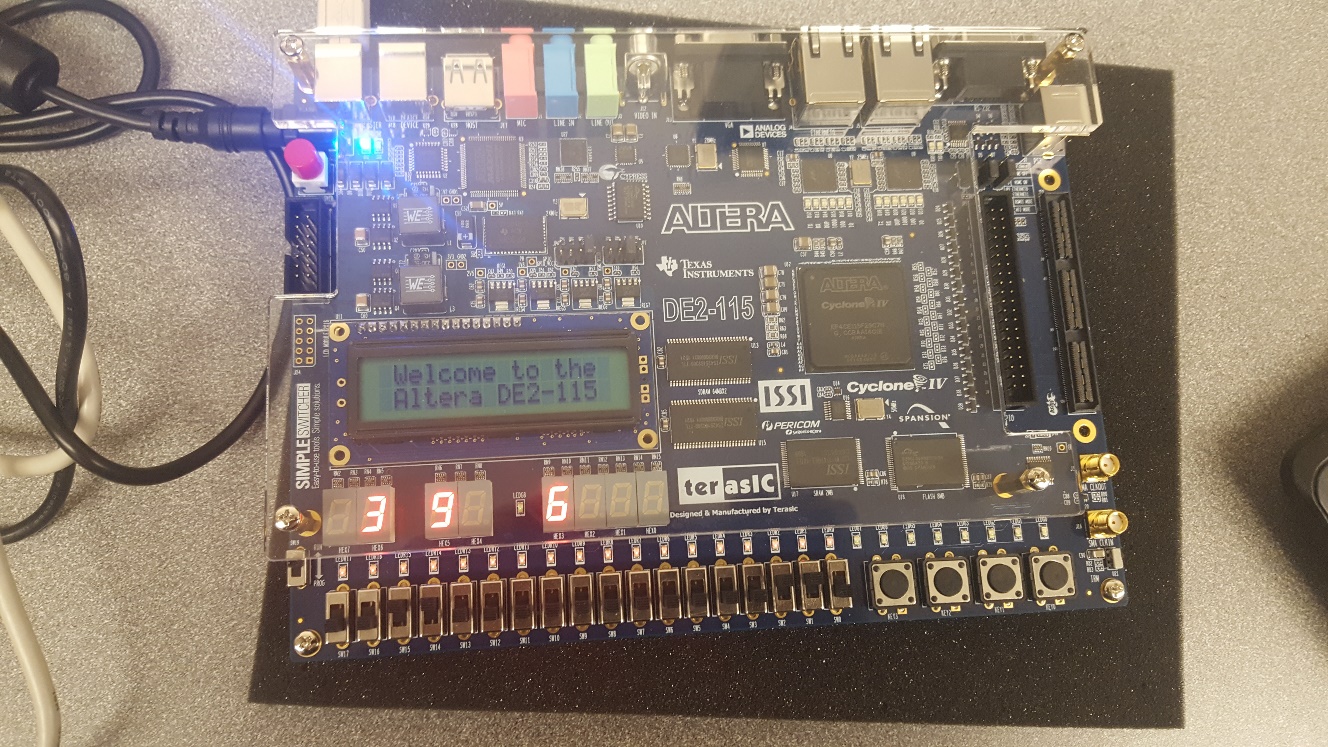
1. Tested System
   1. Non-Matching Pair (sum is not 1001 or 9)

Figure 5: Non-matching pair demonstration

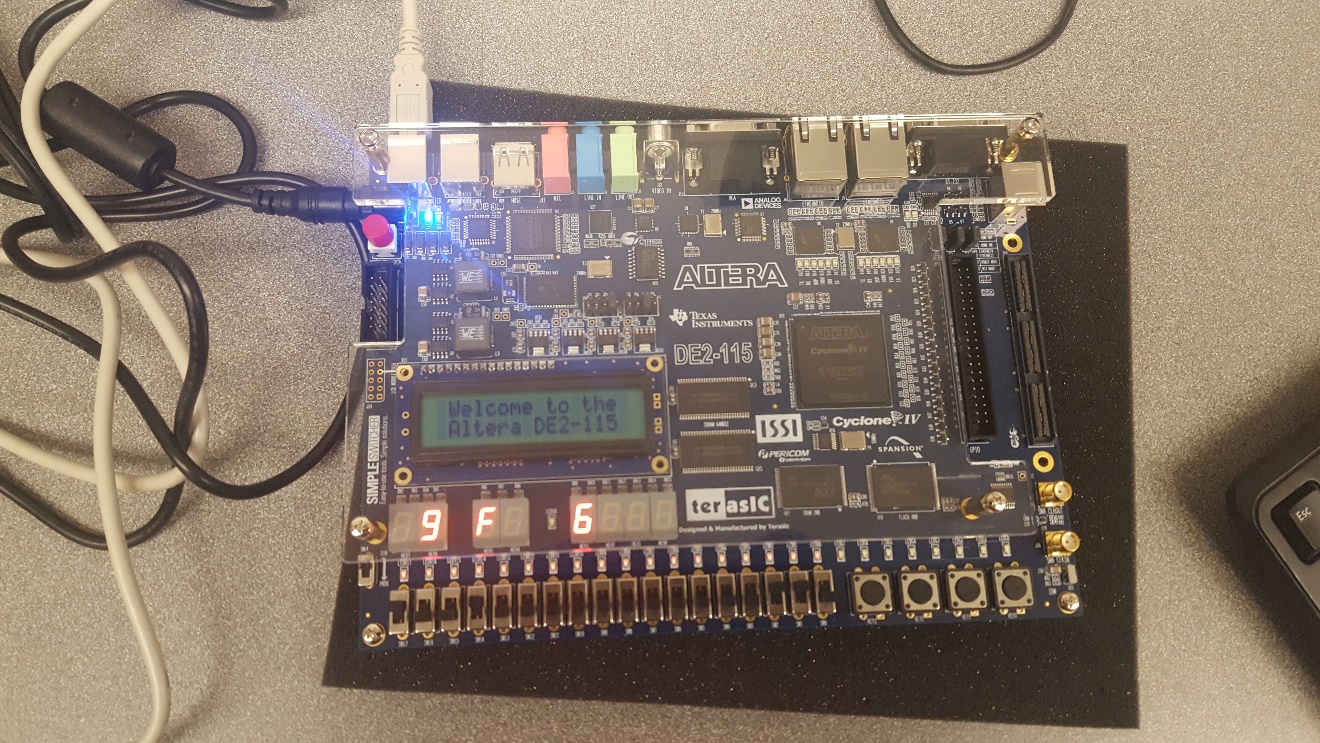
* 1. Matching Pair (sum is 1111 or F) 

Figure 6: matching pair demonstration.

1. Conclusion

The system is tested and work as intended. After the players input their number, the system should add 2 numbers and display them along with the input numbers. After this project, I have learned a lot about Verilog and how to program with FPGA. The status of this project is Complete.

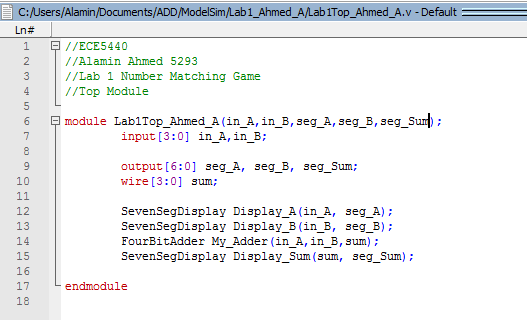
1. Appendix
   1. Top Level

Figure 7: top-level design code.

* 1. Adder

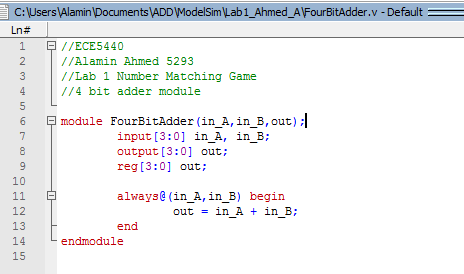


Figure 8: Adder design code.

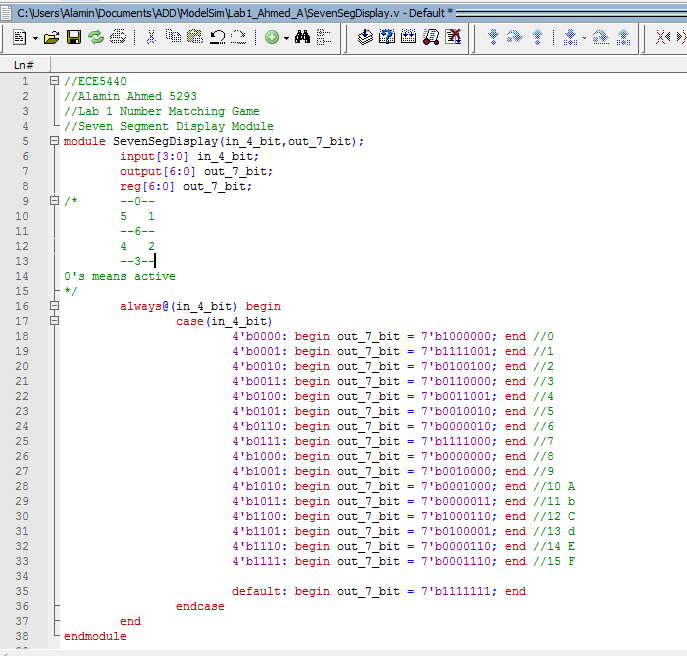
* 1. 7segDisplay

Figure 9: 7segDisplay design code.

d) Test Bench

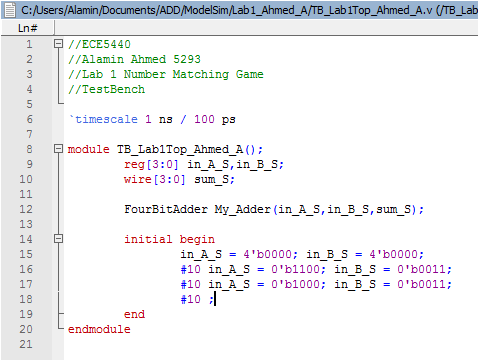


Figure 10: Test Bench for the Adder