Department of Computer Engineering

BLG 242E
Digital Circuits Laboratory
Experiment Report

Experiment : 7 Sequential Logic Circuits

Experiment Date : 03.05.2016

Group Number : 12

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1 INTRODUCTION

In this experiment we design 1 bit counter and we used 4 bit counter to build 0-9 counter.

2 REQUIREMENTS

Part 1.

Q1Q0	X = 0	X = 1	Y (Output)
00	10	11	1
01	10	10	0
11	10	10	1
10	00	00	1

Part 2.

We designed 2 bit counter and then built 0-1-2 state table, then we connect the circuit.

Part 3.

We used 4 bit counter and change it to count 0-9. We used reset signal to count 0-9. At 10 (1010) counter reset itself. When S1 and S3 (S3.S1) (AND Gate) are 1 counter reset itself. (S3 S2 S1 S0)

(S1 AND S3 connected to reset signal.)

3 CONCLUSION

We learnt how to use counters and how to implement different counting methods on them with using state diagrams.