02.03.2017

Istanbul Technical University
Department of Computer Engineering

# BLG 322E – Computer Architecture
# Assignment 2 - Solution

**a)** [50 points]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADD R6, R7, R8 | F | D | O | A | | | | | | | | | | | | | | |
| NOP | | F | D | O | A | | | | | | | | | | | | | |
| LD 0(R8), R1 | | | F | D | O | A | M | | | | | | | | | | | |
| LD 0(R11), R2 | | | | F | D | O | A | M | | | | | | | | | | |
| NOP | | | | | F | D | O | A | | | | | | | | | | |
| NOP | | | | | | F | D | O | A | | | | | | | | | |
| ADD R1, R2, R3 | | | | | | | F | D | O | A | | | | | | | | |
| NOP | | | | | | | | F | D | O | A | | | | | | | |
| ADD R0, R3, R4 | | | | | | | | | F | D | O | A | | | | | | |
| ST 0(R12), R3 | | | | | | | | | | F | D | O | A | M | | | | |
| BA L2 | | | | | | | | | | | F | D | O | A | | | | |
| NOP | | | | | | | | | | | | F | D | O | A | | | |
| NOP | | | | | | | | | | | | | F | D | O | A | | |
| NOP | | | | | | | | | | | | | | F | D | O | A | |
| L2: ADD R0, 0, R3 | | | | | | | | | | | | | | | F | D | O | A |

Total amount of penalty is 7 clock cycles.

**b)** [50 points]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADD R6, R7, R8 | F | D | O | A | | | | | | | | | | | | | | |
| LD 0(R11), R2 | | | F | D | O | A | M | | | | | | | | | | | |
| LD 0(R8), R1 | | | | F | D | O | A | M | | | | | | | | | | |
| NOP | | | | | F | D | O | A | | | | | | | | | | |
| NOP | | | | | | F | D | O | A | | | | | | | | | |
| ADD R1, R2, R3 | | | | | | | F | D | O | A | | | | | | | | |
| BA L2 | | | | | | | | F | D | O | A | | | | | | | |
| ADD R0, R3, R4 | | | | | | | | | F | D | O | A | | | | | | |
| ST 0(R12), R3 | | | | | | | | | | F | D | O | A | M | | | | |
| NOP | | | | | | | | | | | F | D | O | A | | | | |
| L2: ADD R0, 0, R3 | | | | | | | | | | | | F | D | O | A | | | |

Total amount of penalty is 3 clock cycles.

**Note:** Red arrows show the operations, which must be performed in different clock cycles. Since the instruction **ADD R0, 0, R4** cannot enter the pipeline, it is not shown in the diagrams.