

BLG 322E HW4

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a) Active -> 0, Deactive -> 1 (This table constructed in logisim. Output logical expression -> Table)

BG'	BR1'	BR2'	BR3'	BR'	BG1'	BG2'	BG3'
0	0	0	0	0	0	1	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	1
1	0	1	1	0	1	1	1
1	1	0	0	0	1	1	1
1	1	0	1	0	1	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	1	1

b) Outputs:

$BR' = BR1' || BR2' || BR3'$

$BG1' = BR1' \&\& BG'$

$BG2' = BR2' \&\& BG' \&\& BR1$

$BG3' = BR3' \&\& BG' \&\& BR1 \&\& BR2$

c) Signals:

CPU (Fetch), AS = 1

BR1 = 0, BR2 = 0

BR = 0

BG = 0

BG1 = 0

AS = 0

BGACK = 0 (DMAC1)

BR1 = 1

DMAC1 Opetations

BGACK = 1, AS = 1

CPU(Bus Master)

BR2 = 0

BR = 0

BG = 0

BG2 = 0

AS = 0

BGACK = 0 (DMAC2)

BR2 = 1

DMAC2 Operations

BGACK = 1, AS = 1

CPU(Bus Master)

Both send request to the Bus arbiter

Bus arbiter sends request to the CPU

CPU accepts request and return BG signal

Bus arbiter accepts bus grant signal and active the DMAC1's BG1 sig.

When CPU stop using bus it activates the AS signal

When DMAC sees the AS is active it activates the BGACK signal

While DMAC1 using the bus it deactivates BR1 signal for other BRs

DMAC uses the bus

When it finished its job, it deactivates the BGACK and AS signals

If CPU needs the bus, it uses the bus

DMAC2 sends request

Bus arbiter sends request to the CPU

CPU accepts request and return BG signal

Bus arbiter accepts bus grant signal and active the DMAC2's BG2 sig.

When CPU stop using bus it activates the AS signal

When DMAC sees the AS is active it activates the BGACK signal

While DMAC2 using the bus it deactivates BR2 signal for other BRs

DMAC uses the bus

When it finished its job, it deactivates the BGACK and AS signals

If CPU needs the bus, it uses the bus