11.12.2015

Istanbul Technical University
Department of Computer Engineering

BLG 231E - Digital Circuits
Assignment 5

Due Date: 17.12.2015, **Thursday,** 17.00.

- **Consequences of plagiarism:** Disciplinary regulations of The Council of Higher Education and of the university are applied.
- **No late submissions** will be accepted.

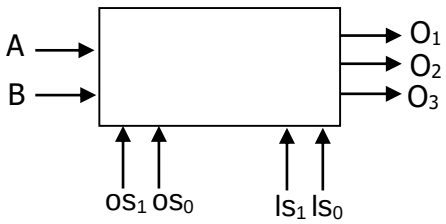
Submissions:

- Implement the circuit using the simulation program and submit the *.circ* file to Ninova.

Assignment:

The digital circuit on the right has two (1-bit) data inputs (**A, B**) and three data outputs (**O_1, O_2,** and **O_3**).

The circuit includes **three D latches** with enable inputs. The outputs of the latches are directly connected to the three outputs of the circuit.



This circuit can calculate and store results of four different logic operations which are defined as {A▪B, A+B, (A+B)′, A′ }.

The "operation selection" inputs **OS_1** and **OS_0** determine which logical operation {A▪B, A+B, (A+B)′, or A′ } will be performed respectively.

Similarly, the "latch selection" inputs **IS_1** and **IS_0** determine the latch to which the result of the operation will be written.

For example, if **OS_1,OS_0 = 00** and **IS_1,IS_0 = 11**, the AND operation (A▪B) will be performed, and the result will be written to the third latch. Thus, the result can be read at the output **O_3**. If **IS_1,IS_0 = 00**, all tree latches preserve their previous values.

Design this circuit using **only one multiplexer, one decoder, D latches**, and **only NAND gates.** You do not need to show the internal structure of D latches.
Finally, implement the circuit in the simulation program.