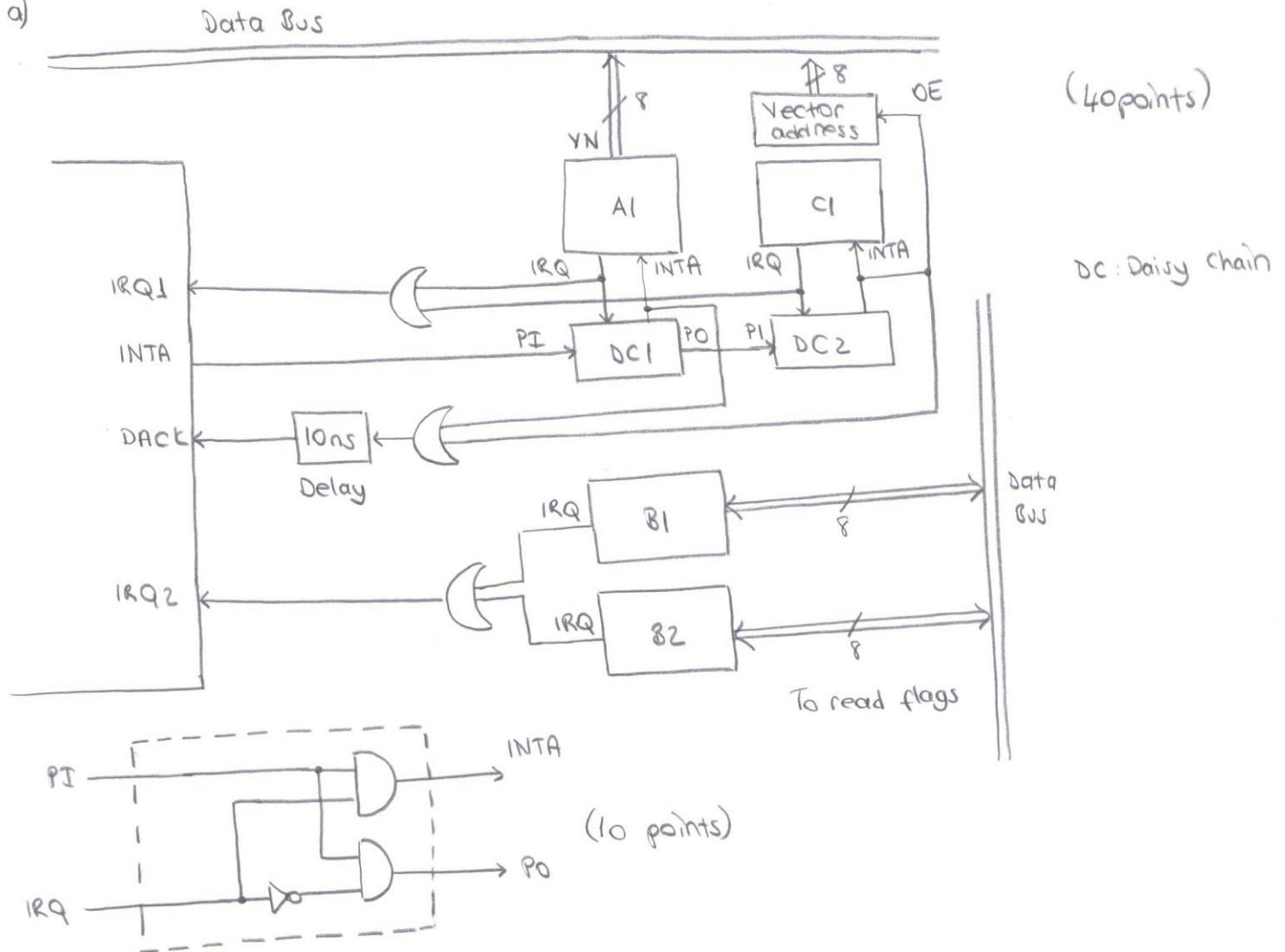


a)



b) Type A: Device A1 puts the VN on the data bus, when its request is acknowledged ($INTA=1$). The CPU reads the number and using it gets the starting address of the ISR from the vector table. (10 points)

Type B: These devices do not present their vector numbers. The CPU has only one auto vectored interrupt request input (IRQ2). To determine the source of the interrupt request the CPU checks the flag of the devices B1 and B2 (software-based polling) in the interrupt service program for IRQ2 (there may be only one interrupt service program for IRQ2). Then, it jumps to the program of B1 or B2. (10 points)

Type C: Device C1 has no VN output, therefore its vector address is stored outside of the device and put to the data bus with an output enable (OE) signal. (10 points)

c)

IRQ (C1) = 1, IRQ (B2) = 1 (Two devices assert interrupt requests.)

IRQ1 = 1, IRQ2 = 1 (IRQ1 has higher priority.)

INTA (CPU) = 1 (Interrupt request from IRQ1 is accepted.)

PI (DC1) = 1 (Stage 1), PO (DC1) = 1 (Source of request is not A1.)

PI (DC2) = 1 (Stage 2), INTA (DC2) = 1 (Source of request is C1.)

INTA (C1) = 1 (C1 gets the acknowledgement), OE=1 and vector address is put to Data Bus.

IRQ (C1) = 0 (C1 removes interrupt request.)

DACK = 1, CPU reads vector address of C1, gets the start address from the vector table, runs ISR of C1. CPU returns from ISR of C1.

IRQ1 = 0, IRQ2 = 1 (B1 still holds the request)

The CPU accepts the autovectored interrupt.

CPU runs the ISR of IRQ2 (common to autovectored sources).

The program (ISR of IRQ) checks the flags of B1 and B2 (software-based polling). It determines the source (B1). This program removes the request of B1 (by reading or writing necessary registers of the devices). IRQ (B1) = 0.

The ISR of IRQ2 jumps to the service procedure of B1. Procedure of B1 returns to the ISR of IRQ2. ISR returns to the main program.