BLG 222E
COMPUTER ORGANIZATION
PROJECT 2 REPORT

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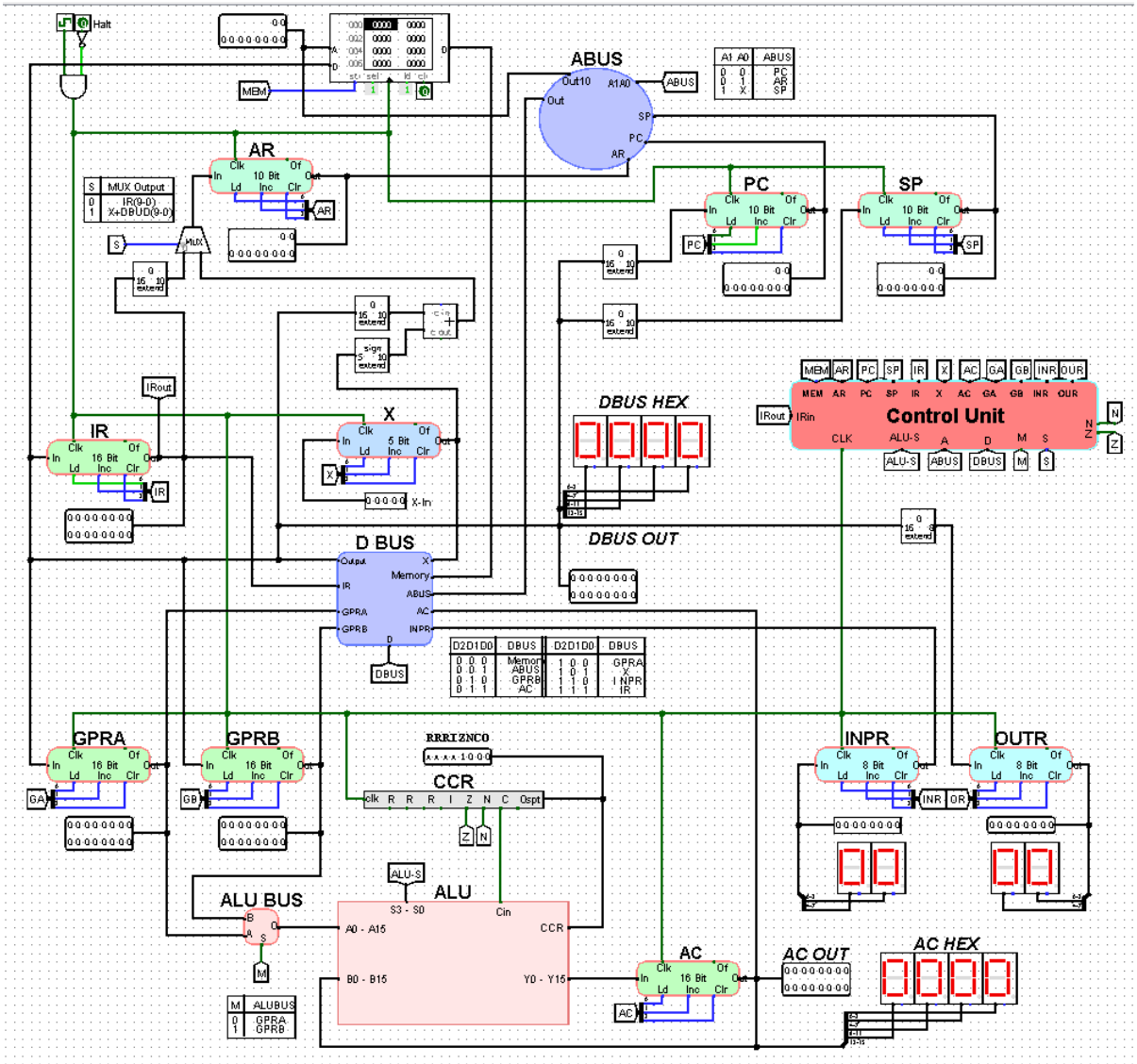

Image 1: The design of simple computer

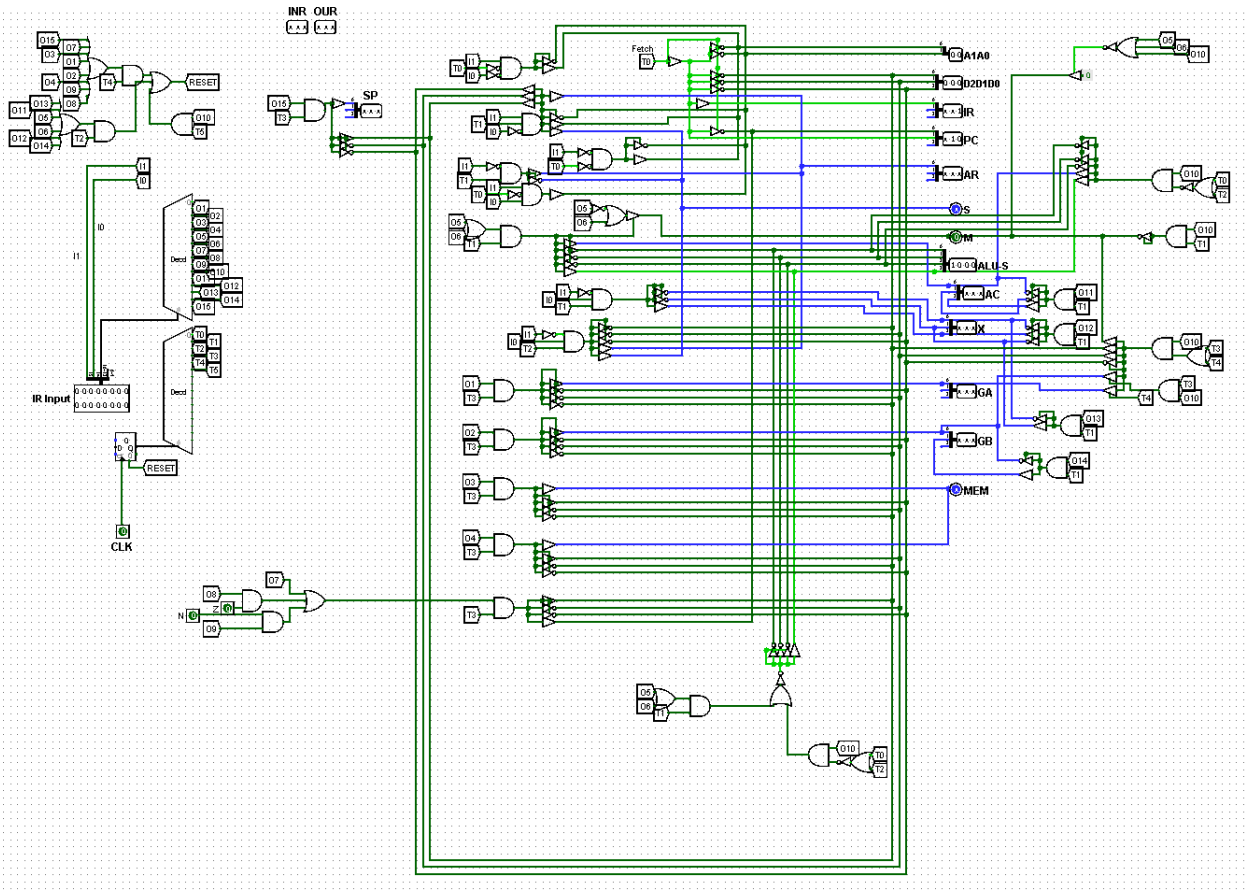

Image 2: Inside of the control unit

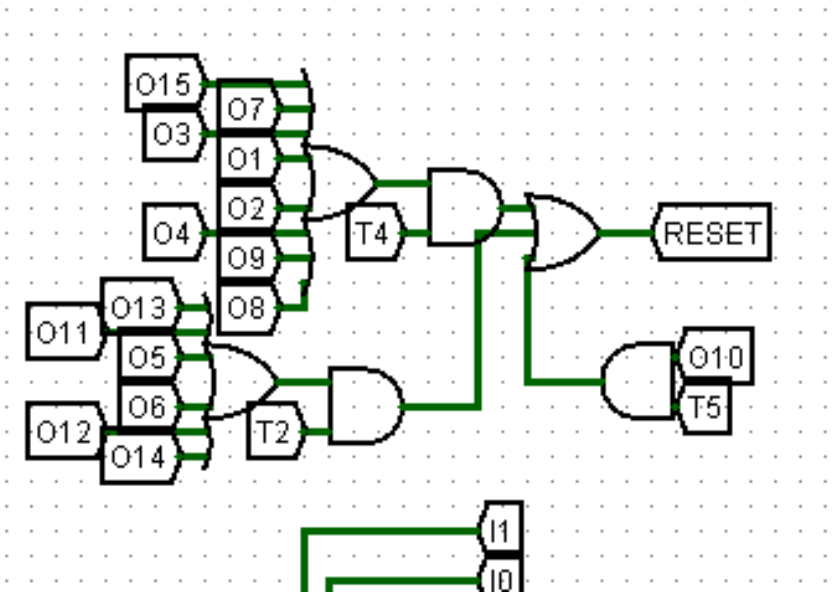

Image 3: Sequence counter's reset function

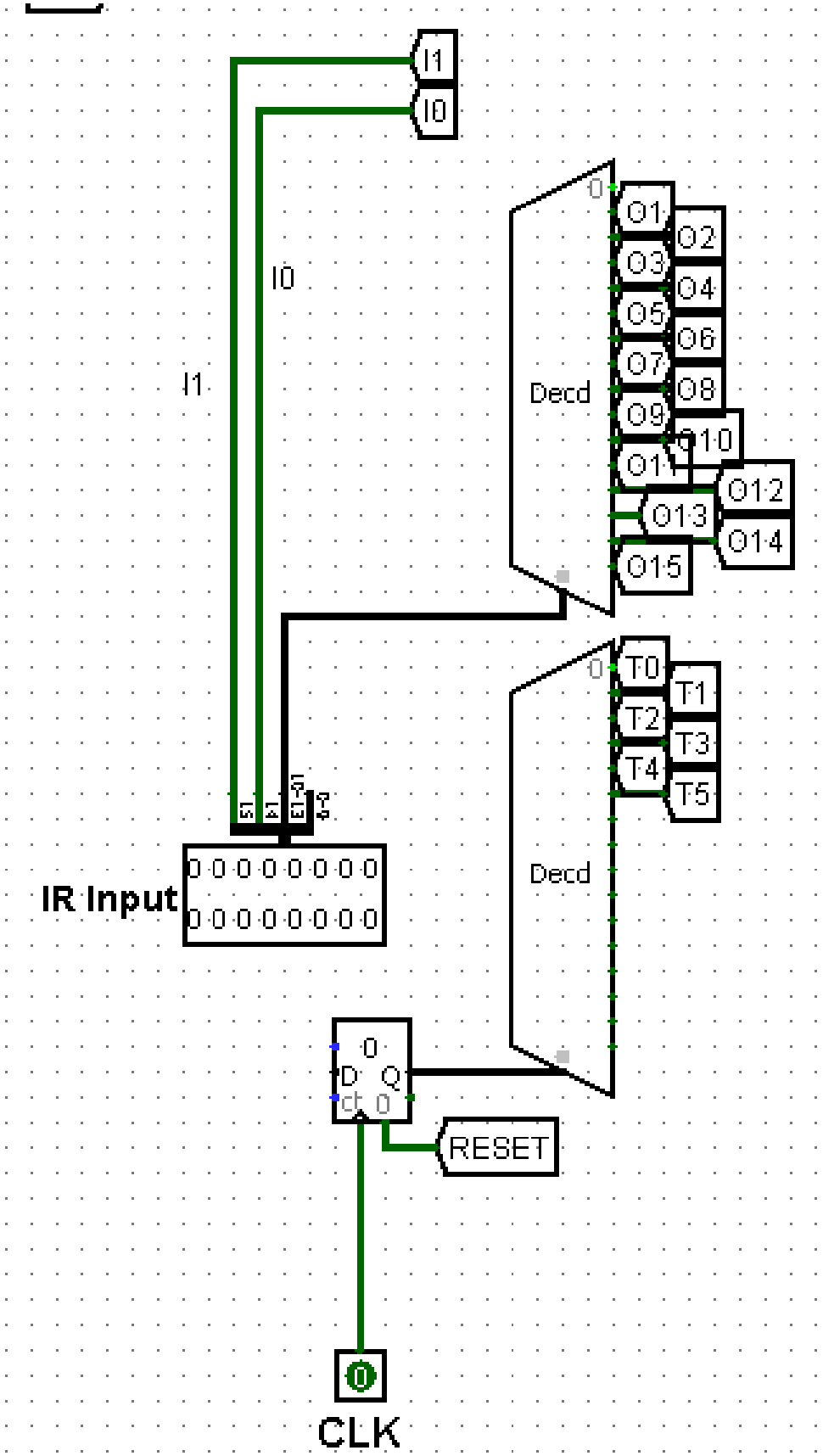

Image 4: Time and opcode decoders

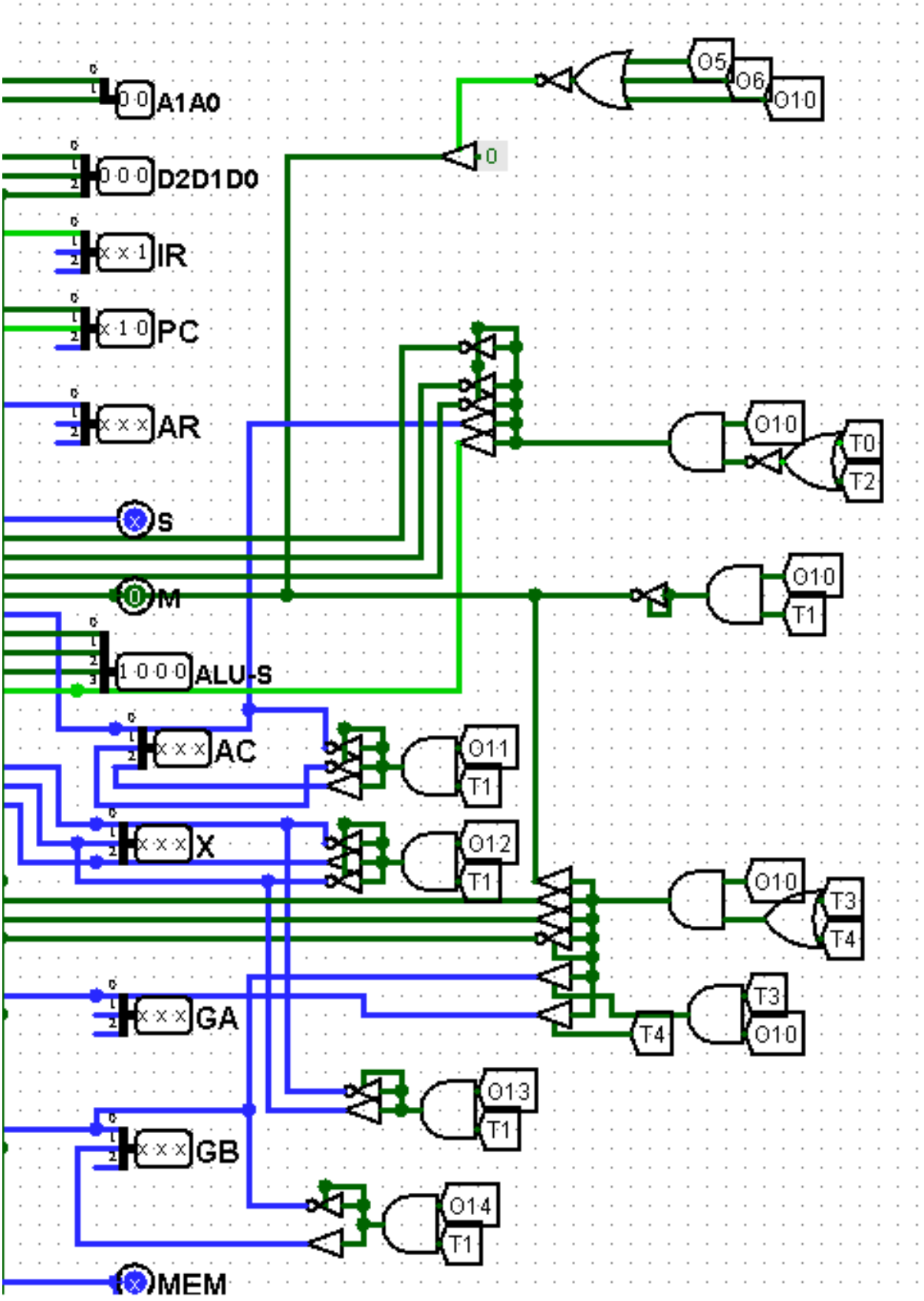
A1A0
D2D1D0
IR
PC
AR
S
M
ALU-S
AC
X
GA
GB
MEM
0
O5
O6
O10
O11
O12
O13
O14
T0
T1
T2
T3
T4

Image 5: Outputs of the CU (Control signals)

Ld	Inc	Clr	Function
1	X	X	Loads from input
0	1	X	Increments the content by '1'
0	0	1	Clears the content to '0'
0	0	0	Keeps the content unchanged

Table 1: Control signals and corresponding functions of the registers

Control signal			Register to write DBUS
D_2	D_1	D_0	
0	0	0	Memory
0	0	1	ABUS
0	1	0	GPRB
0	1	1	AC
1	0	0	GPRA
1	0	1	X
1	1	0	INPR
1	1	1	IR

Control signal		Register to write ABUS
A_1	A_0	
0	0	PC
0	1	AR
1	dont care	SP

Control signal M	Register to write ALUBUS
0	GPRA
1	GPRB

Table 2: Control signals those enables to write each bus

S_3	S_2	S_1	S_0	C (bit 0) in CCR	Operation	Function	Flag updates Z	N	O	C
1	0	0	0	0	$F \leftarrow A$	Transfer A	√	√	√	√
1	0	0	0	1	$F \leftarrow A+1$	Increment A	√	√	√	√
1	0	0	1	0	$F \leftarrow A+B$	Addition	√	√	√	√
1	0	0	1	1	$F \leftarrow A+B+1$	Add with carry	√	√	√	√
1	X	1	0	0	$F \leftarrow A+\bar{B}$	Subtract with borrow	√	√	√	√
1	0	1	0	1	$F \leftarrow A+\bar{B}+1$	Subtraction	√	√	√	√
1	0	1	1	0	$F \leftarrow A-1$	Decrement A	√	√	√	√
1	0	1	1	1	$F \leftarrow A$	Transfer A	√	√	√	√
0	1	0	0	0	$F \leftarrow A \wedge B$	AND	√	√	–	–
0	1	0	0	1	$F \leftarrow \overline{A \wedge B}$	NAND	√	√	–	–
0	1	1	0	0	$F \leftarrow A \vee B$	OR	√	√	–	–
0	1	1	0	1	$F \leftarrow A \oplus B$	XOR	√	√	–	–
0	1	0	1	1	$F \leftarrow \overline{A \vee B}$	NOR	√	√	–	–
0	1	0	1	1	$F \leftarrow \overline{A \oplus B}$	XNOR	√	√	–	–
0	1	1	1	X	$F \leftarrow \bar{A}$	Complement A	√	√	–	–
0	0	0	0	0	$F \leftarrow shrA$	Logical shift right A into F	√	√	–	–
0	0	0	0	1	$F \leftarrow ashrA$	Arithmetic shift right A into F	√	√	–	–
0	0	0	1	0	$F \leftarrow cshrA$	Circular shift right A into F	√	√	–	–
0	0	0	1	1	$F \leftarrow shlA$	Logical shift left A into F	√	√	–	–
0	0	1	X	0	$F \leftarrow ashlA$	Arithmetic shift left A into F	√	√	√	–
0	0	1	0	1	$F \leftarrow cshlA$	Circular shift left A into F	√	√	–	–

Table 3: ALU functions

Instruction subset:

Symbol	Opcode (binary)	Description
LDA	0001	GPRA ←M[EA]
LDB	0010	GPRB ←M[EA]
STA	0011	M[EA] ←GPRA
STB	0100	M[EA] ←GPRB
ADDA	0101	AC ←AC + GPRA
ADDB	0110	AC ←AC + GPRB
BUN	0111	PC ←EA
BZE	1000	if Z=1 then PC ←EA
BNE	1001	if N=1 then PC ←EA
XCH	1010	Exchange values in GPRA and GPRB
CLRAC	1011	AC ←0
CLRX	1100	X ←0
INCX	1101	X ←X+1
INCB	1110	GPRB ←GPRB+1
LDSP	1111	SP←M[EA]

Table 4: Instruction table