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Homework 2

Coverage Report

The goal of our coverage is to ensure we are providing the design with enough stimulus to cover the most possible cases. We want to make sure that when we test all possible operations, the design is capable of outputting the correct data. For example, in CSM we want to make sure we test read, write, hold and release operations. In addition, we also want to test that the design is capable of outputting all possible error codes. While it is impossible to test every single combination of input and output at the bit level, testing the most used operations or in case of CSM making sure every operation is simulated is important.

We wrote coverage to cover all possible A and B operations. We also want make interaction between A and B is tested and we wrote coverage to interactions such as A write and B read. In addition to the operations we also added signals coverage to give us insight on how much of the possible bit combinations we are covering. In the case of CSM, this helps with error and ack signals full coverage. Signal coverage lead to bit toggle coverage to ensure we toggle every bit in the design.

The input address and data pins are driven with a constrained random generator where the data is constrained to 25% 0x00, 25% 0xFF, and 50% to the values in between. The address is limited to the range of the 8 registers (3'b000 to 3'b111) and has an equal random distribution. For each iteration through the test, a new set of random addresses and data are randomly generated. Along with newly generated address and data, the operations are also randomly generated which are selected from a pool of normal operations (e.g. read, write, read then write, etc.).

With stimulus written to the inputs, we ran the simulator to only discover the design has bug in the hold and release operations. The goal of the our test stimulus is to send 1000 random transactions to the design but the bug prevented the test from running all 1000 transactions. We disabled hold and release test stimulus and reran. While now we have zero coverage for hold and release operations, but are able to run the entire gamut of 1000 transactions. We plan to fix the design bug in the future and rerun the test. The testbench and coverage showed immediate effectiveness of discovering a bug in the design. Our overall coverage is about 64%. This include signal coverage and valid operations. Our valid operation coverage is about 50%. This mainly because we disabled hold and release operations. Our goal is to hit 100% coverage on valid operations and we must fix the bug and retry. While we have some stimulus and coverage, the design still needs more validation. Some. The effect of disabling hold and release operations was not getting 100% coverage of the error codes.