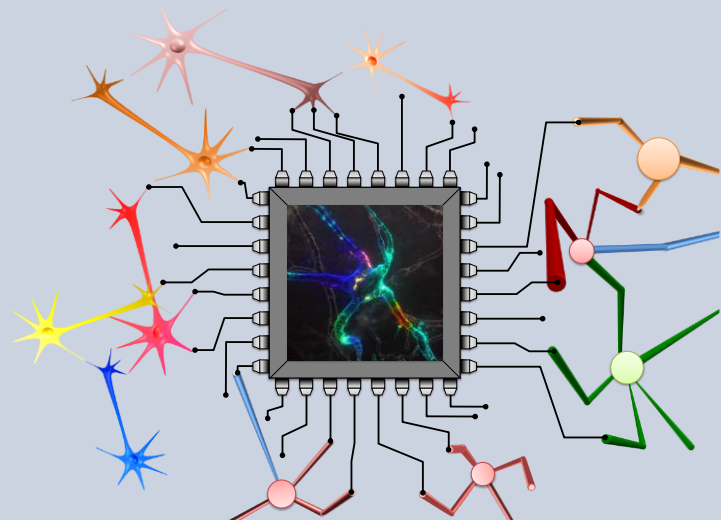


Universidade de São Paulo
Instituto de Ciências Matemáticas e de Computação
Departamento de Sistemas de Computação

SSC108
Prática em Sistemas Digitais

Tutorial ROM Quartus

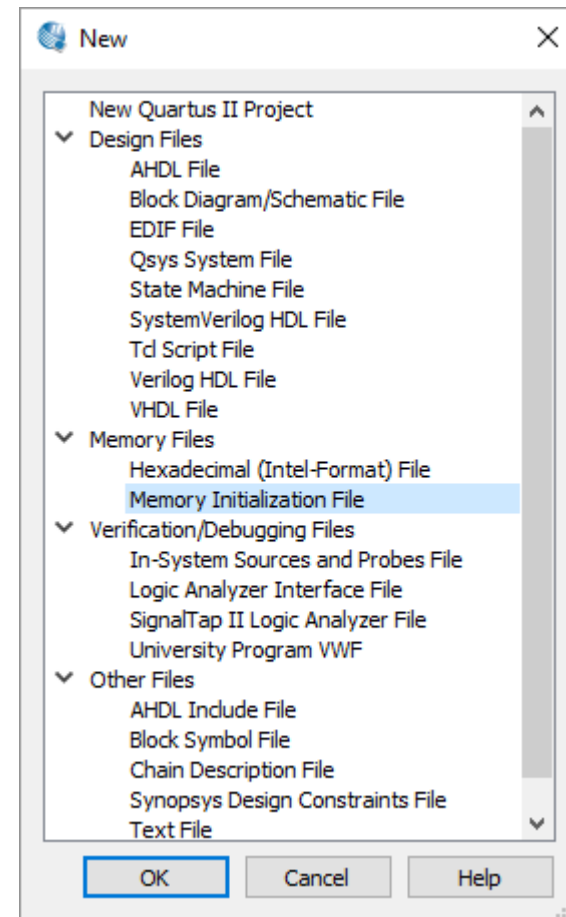


GE4Bio – Grupo de Estudos em Sinais Biológicos

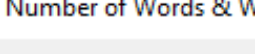
Prof.Dr. Danilo Spatti

São Carlos

- Criar um arquivo de inicialização de memória (MIF).
- Inserir os dados e testar usando chaves na entrada de endereços e displays na saída de dados.



- Definir o tamanho da memória (256x16).
- Definir o conteúdo e salvar. Cada célula corresponde a uma palavra de dados.



Number of Words & Word Size

Number of words: 256

Word size: 16

OK Cancel Help

[illegible]

Quartus II 64-Bit - B:/Documentos/QuartusProjects/Projeto-teste/teste - teste

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity
Cyclone IV E: EP4ACE115F29C7

romtest

Hierarchy Files Design Unit

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming file)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

Addr	+0	+1	+2	+3	+4	+5	+6	+7	ASCII
0	300	500	250	1000	65535	2	3	10
8	50	0	0	0	0	0	0	0	2.....
16	0	54	0	0	0	0	0	0	6.....
24	654	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0
40	0	0	0	0	0	0	0	0
48	0	0	0	0	0	0	0	0
56	0	0	0	0	0	0	0	0
64	0	0	0	0	0	0	0	0
72	0	0	0	0	0	0	0	0
80	0	0	0	0	0	0	0	0
88	0	0	0	0	0	0	0	0
96	0	0	0	0	0	0	0	0
104	0	0	0	0	0	0	0	0
112	0	0	0	0	0	0	0	0
120	0	0	0	0	0	0	0	0
128	0	0	0	0	0	0	0	0
136	0	0	0	0	0	0	0	0
144	0	0	0	0	0	0	0	0
152	0	0	0	0	0	0	0	0
160	0	0	0	0	0	0	0	0

Search altera.com

Installed IP

Project

Library

- > Basic
- > DSP
- > Interface Protocols
- > Memory Interfaces and Controllers
- > Processors and Peripherals

Search for Partner IP

<<Search>>

Type ID Message

204019 Generated file teste_7_1200mv_0c_slow.vho in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

204019 Generated file teste_min_1200mv_0c_fast.vho in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

204019 Generated file teste.vho in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

204019 Generated file teste_7_1200mv_85c_vhd_slow.sdo in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

204019 Generated file teste_7_1200mv_0c_vhd_slow.sdo in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

204019 Generated file teste_min_1200mv_0c_vhd_fast.sdo in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

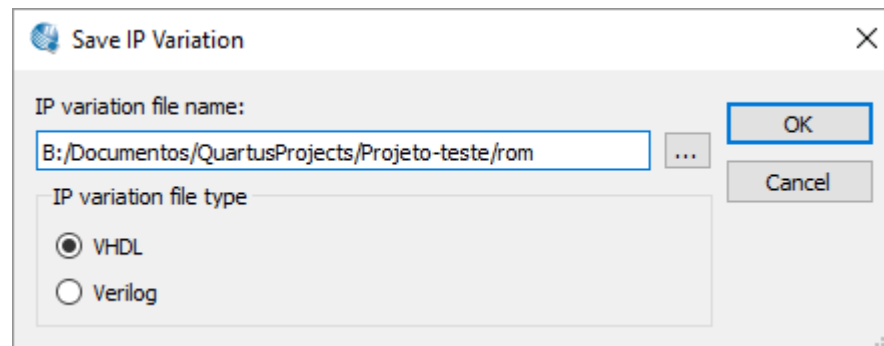
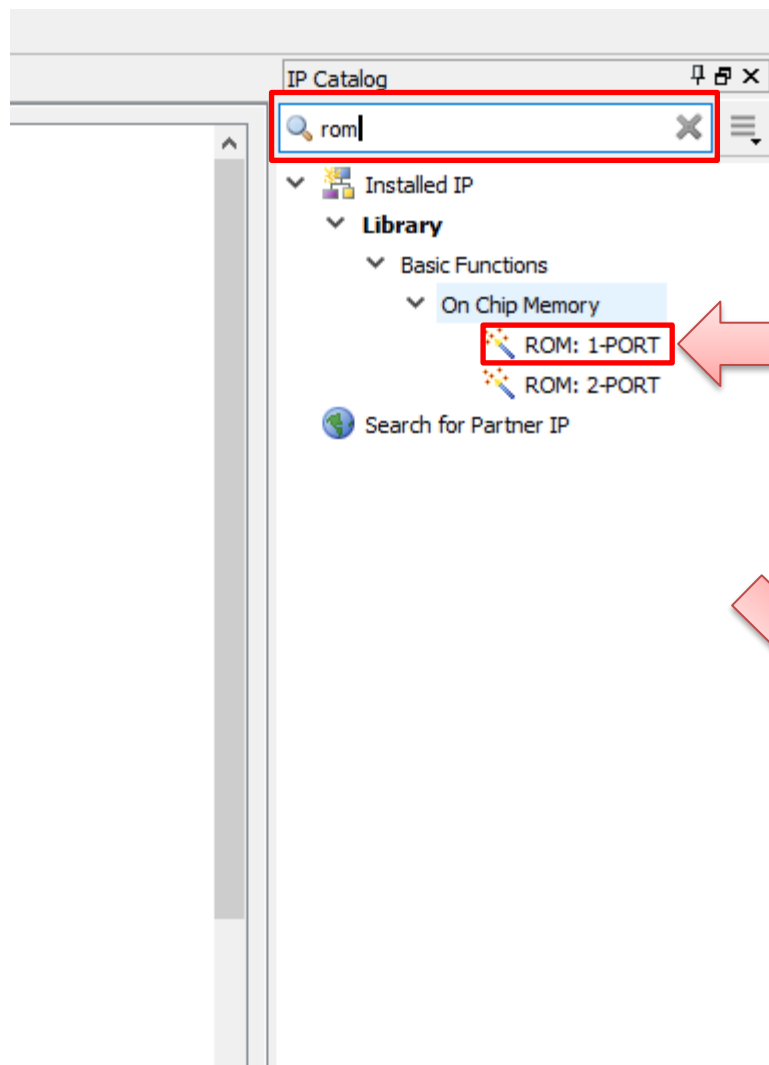
204019 Generated file teste_vhd.sdo in folder "B:/Documentos/QuartusProjects/Projeto-teste/simulation/modelsim/" for EDA simulation tool

Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings

System (3) Processing (133)

100% 00:00:41



MegaWizard Plug-In Manager [page 1 of 5]

ROM: 1-PORT

About Documentation

1 Parameter Settings 2 EDA 3 Summary

General > Regs/Clock/Acrs > Mem Init >

Currently selected device family: Cyclone IV E

☒ Match project/default

How wide should the 'q' output bus be? 16 bits

How many 16-bit words of memory? 256 words

Note: You could enter arbitrary values for width and depth

What should the memory block type be?

☒ Auto ☐ MLAB ☐ M9K
☐ M144K ☐ LCs Options...




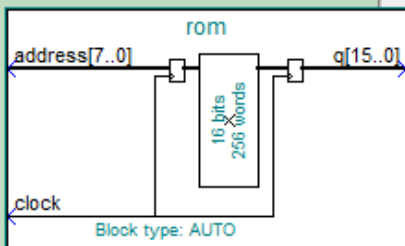
Set the maximum block depth to Auto words

What clocking method would you like to use?

☒ Single clock ☐ Dual clock: use separate 'input' and 'output' clocks

Resource Usage
1 M9K

Cancel < Back Next > Finish



MegaWizard Plug-In Manager [page 2 of 5]

ROM: 1-PORT

About Documentation

1 Parameter Settings 2 EDA 3 Summary

General > Regs/Clock/Adrs > Mem Init >

Block type: AUTO

```
graph LR
    address[address[7..0]] --> rom[rom]
    clock[clock] --> rom
    rom --> q[q[15..0]]
```

Which ports should be registered?

- ☐ 'data' input port
- ☒ 'address' input port
- ☐ 'q' output port

☐ Create one clock enable signal for each clock signal.
Note: All registered ports are controlled by the enable signal(s) More Options...

☐ Create byte enable for port A

What is the width of a byte for byte enables? bits

☐ Create an 'aclr' asynchronous clear for the registered ports More Options...

☐ Create a 'rden' read enable signal

Resource Usage

1 M9K

Cancel < Back Next > Finish

MegaWizard Plug-In Manager [page 3 of 5]

ROM: 1-PORT

[About](#) [Documentation](#)

1 Parameter Settings 2 EDA 3 Summary

General > Regs/Clock/Adrs > Mem Init >

Diagram showing a ROM block with inputs: address[7..0], clock, and output q[15..0]. The block is labeled "rom" and "Block type: AUTO".

Resource Usage

1 M9K

Do you want to specify the initial content of the memory?

☐ No, leave it blank

☐ Initialize memory content data to XX..X on power-up in simulation

☒ Yes, use this file for the memory content data
(You can use a Hexadecimal (Intel-format) File [.hex] or a Memory Initialization File [.mif])

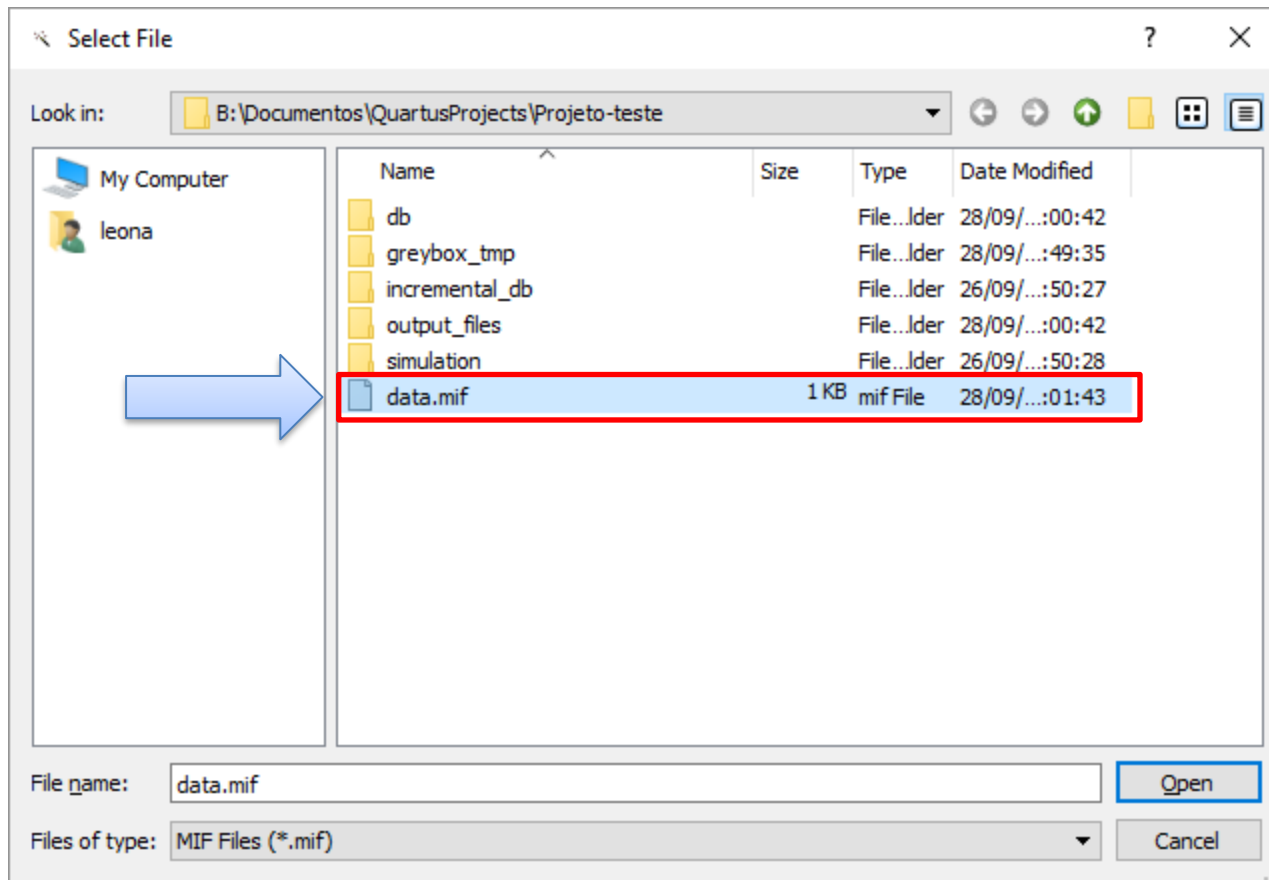
File name: [Browse...](#)

The initial content file should conform to which port's dimensions?


☐ Allow In-System Memory Content Editor to capture and update content independently of the system clock

The 'Instance ID' of this ROM is:

[Cancel](#) [< Back](#) [Next >](#) [Finish](#)

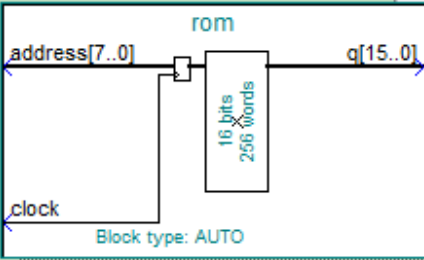


MegaWizard Plug-In Manager [page 4 of 5]

**ROM: 1-PORT**

AboutDocumentation

1Parameter Settings2EDASummary



Simulation Libraries

To properly simulate the generated design files, the following simulation model file(s) are needed

File	Description
altera_mf	Altera megafunction simulation library

Timing and resource estimation

Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party EDA synthesis tool, using a timing and resource estimation netlist can allow for better design optimization.

Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.

Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.


☐ Generate netlist

Resource Usage

1 M9K

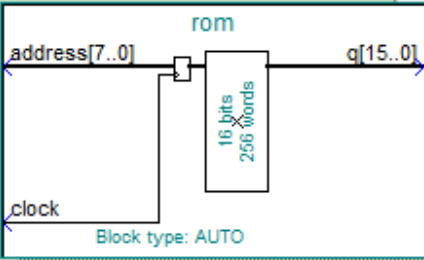
Cancel< BackNext >Finish

MegaWizard Plug-In Manager [page 5 of 5]

**ROM: 1-PORT**

AboutDocumentation

1Parameter Settings2EDA3Summary



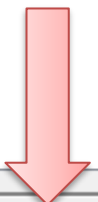
Resource Usage
1 M9K

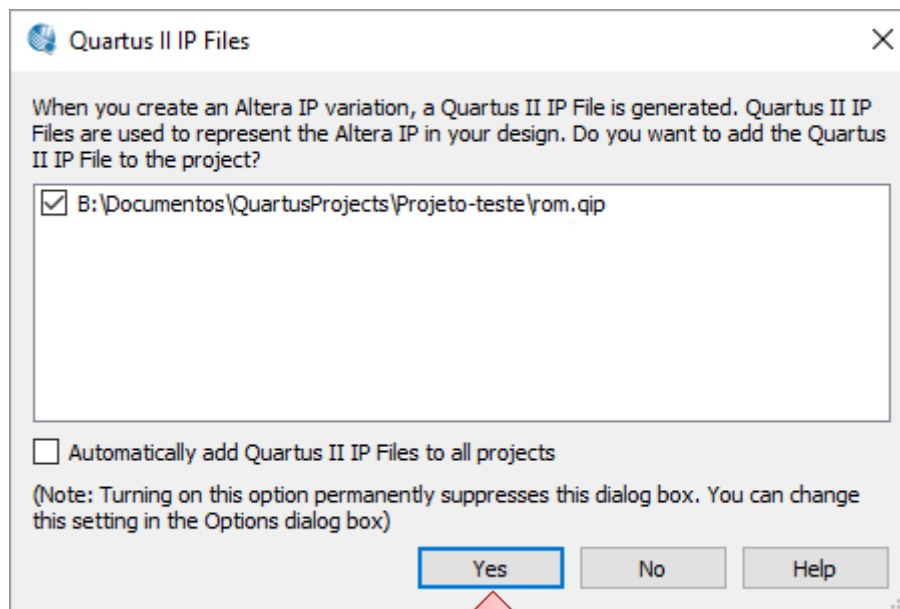
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

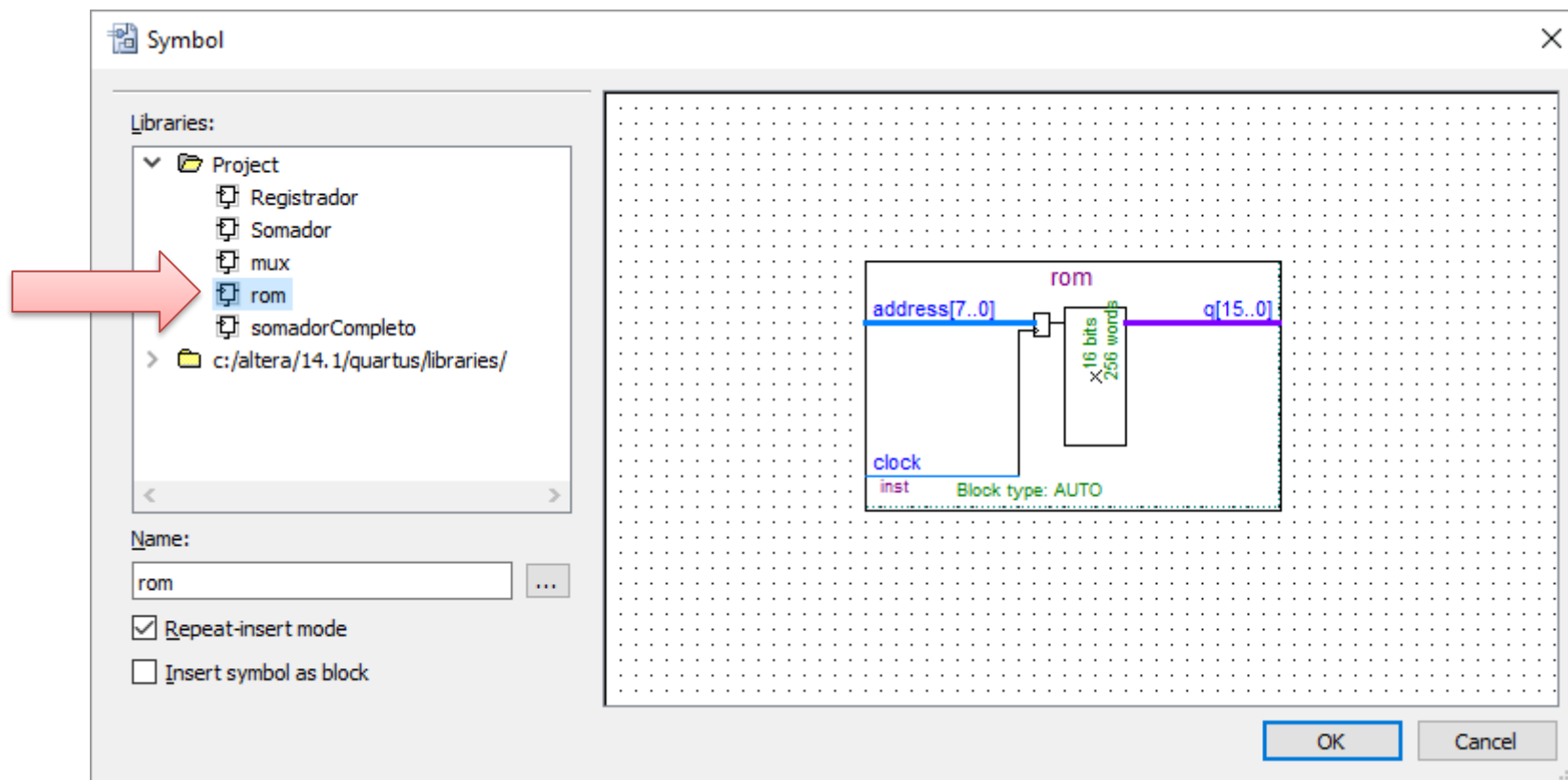
The MegaWizard Plug-In Manager creates the selected files in the following directory:
B:\Documentos\QuartusProjects\Projeto-teste\

File	Description
<input checked="" type="checkbox"/> rom.vhd	Variation file
<input checked="" type="checkbox"/> rom.inc	AHDL Include file
<input checked="" type="checkbox"/> rom.cmp	VHDL component declaration file
<input checked="" type="checkbox"/> rom.bsf	Quartus II symbol file
<input type="checkbox"/> rom_inst.vhd	Instantiation template file

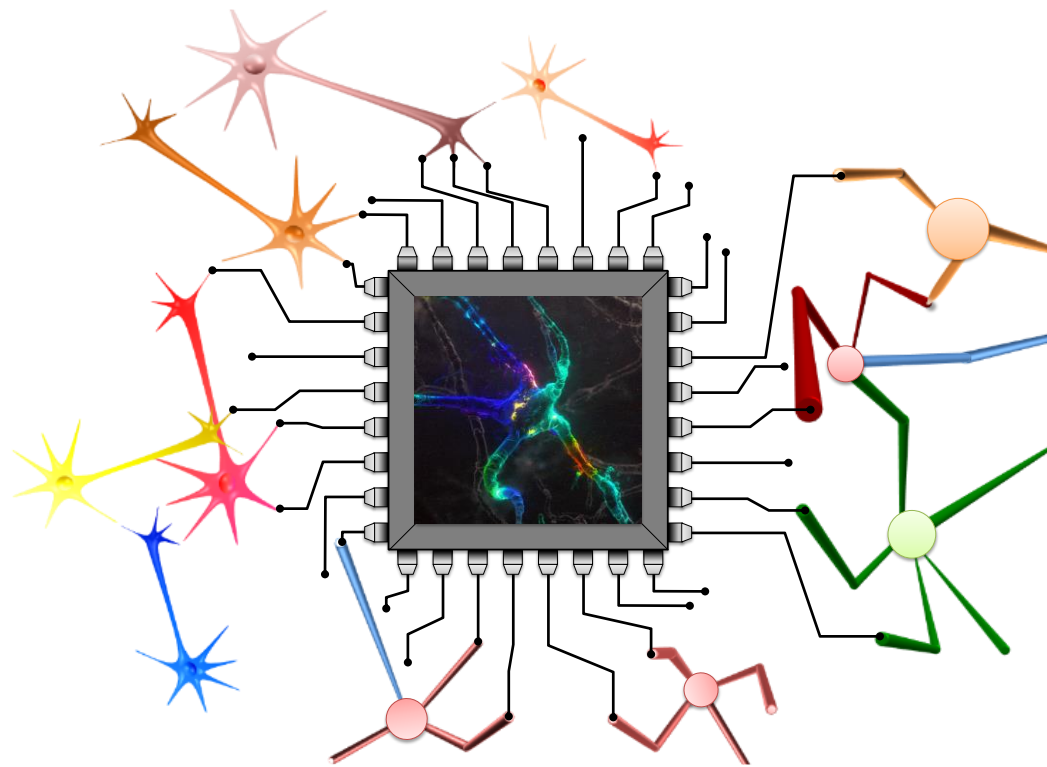
Cancel< BackNext >Finish







spatti@icmc.usp.br



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