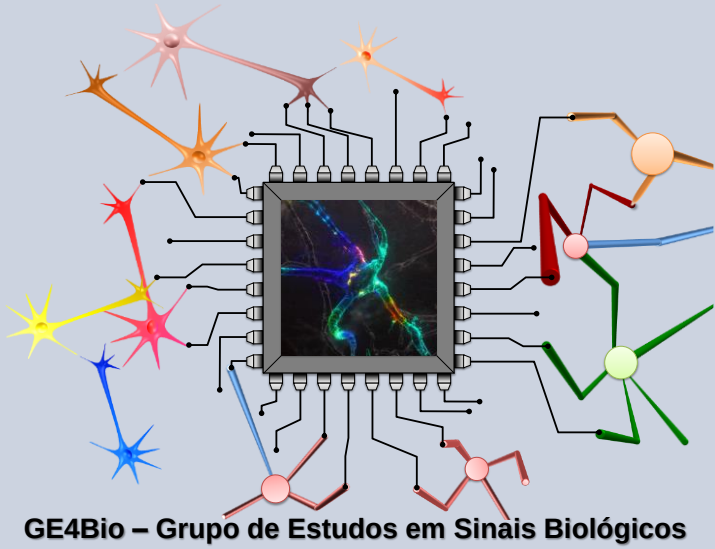
Universidade de São Paulo
Instituto de Ciências Matemáticas e de Computação
Departamento de Sistemas de Computação

SSC108
Prática em Sistemas Digitais

Tutorial Configuração Quartus – Parte III



Prof.Dr. Danilo Spatti

São Carlos

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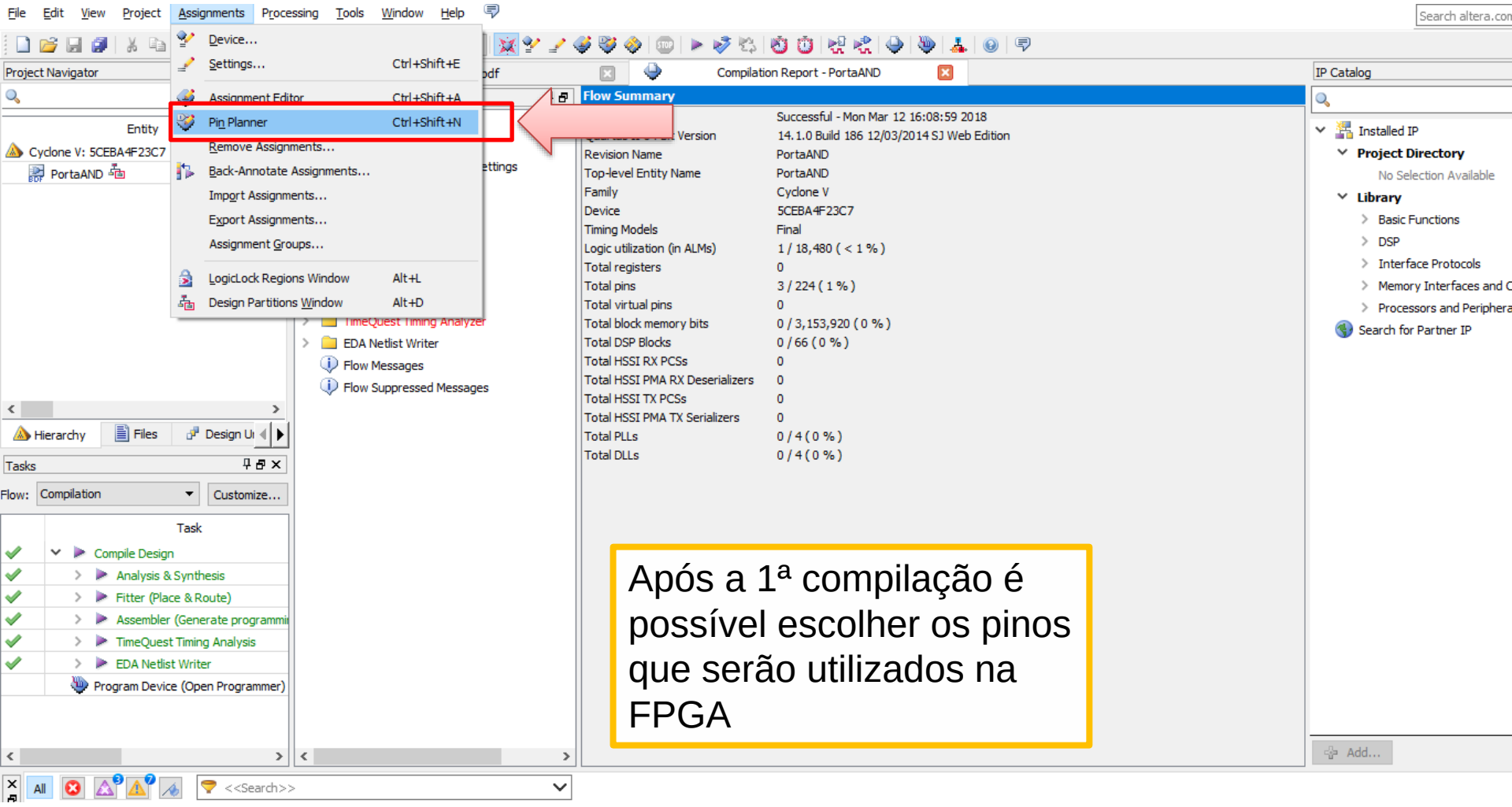
Configuração do Quartus
98 - Escolha de Pinos (I)



Após a 1ª compilação é possível escolher os pinos que serão utilizados na FPGA

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Configuração do Quartus
9 - Escolha de Pinos (II)

Pin Planner - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

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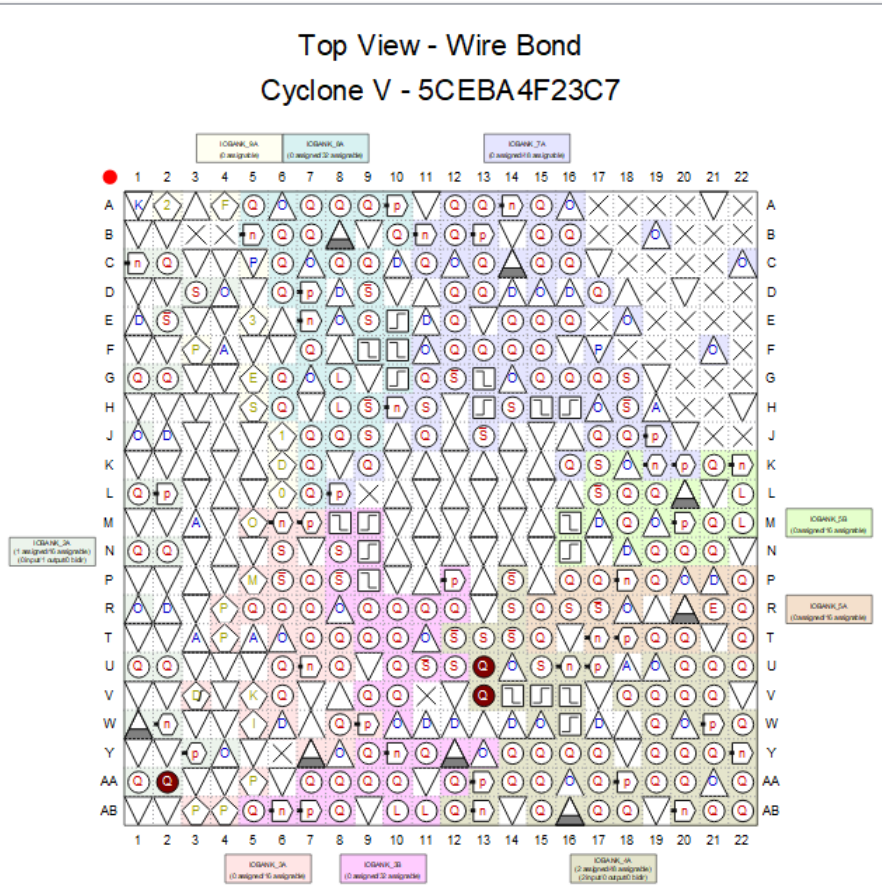
Groups Report

Tasks

- Early Pin Planning
  - Early Pin Planning...
  - Run I/O Assignment Analysis
  - Export Pin Assignments...
- Pin Finder...
- Highlight Pins
  - I/O Banks
  - VREF Groups
  - Edges
  - Clock Pins
    - Clock
    - PLL/DLL Input



Named: * Edit: Filter: Pins: al

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	/er Analog Settings	_GXB/VCCT_G
in A	Input	PIN_U13	4A	B4A_N0	PIN_L17	2.5 V (default)		12mA (default)				
in B	Input	PIN_V13	4A	B4A_N0	PIN_K17	2.5 V (default)		12mA (default)				
out Y	Output	PIN_AA2	2A	B2A_N0	PIN_M21	2.5 V (default)		12mA (default)	1 (default)			
<<new node>>												

Table 3-2 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description
KEY0	PIN_U7	Push-button[0]
KEY1	PIN_W9	Push-button[1]
KEY2	PIN_M7	Push-button[2]
KEY3	PIN_M6	Push-button[3]
RESET_N	PIN_P22	Push-button which connected to DEV_CLRN Pin of FPGA

Table 3-3 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]

Table 4-1 Pin Assignments for Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_AB28	Slide Switch[0]	Depending on JP7
SW[1]	PIN_AC28	Slide Switch[1]	Depending on JP7
SW[2]	PIN_AC27	Slide Switch[2]	Depending on JP7
SW[3]	PIN_AD27	Slide Switch[3]	Depending on JP7
SW[4]	PIN_AB27	Slide Switch[4]	Depending on JP7
SW[5]	PIN_AC26	Slide Switch[5]	Depending on JP7
SW[6]	PIN_AD26	Slide Switch[6]	Depending on JP7
SW[7]	PIN_AB26	Slide Switch[7]	Depending on JP7
SW[8]	PIN_AC25	Slide Switch[8]	Depending on JP7
SW[9]	PIN_AB25	Slide Switch[9]	Depending on JP7
SW[10]	PIN_AC24	Slide Switch[10]	Depending on JP7
SW[11]	PIN_AB24	Slide Switch[11]	Depending on JP7
SW[12]	PIN_AB23	Slide Switch[12]	Depending on JP7
SW[13]	PIN_AA24	Slide Switch[13]	Depending on JP7
SW[14]	PIN_AA23	Slide Switch[14]	Depending on JP7
SW[15]	PIN_AA22	Slide Switch[15]	Depending on JP7
SW[16]	PIN_Y24	Slide Switch[16]	Depending on JP7
SW[17]	PIN_Y23	Slide Switch[17]	Depending on JP7

Table 4-2 Pin Assignments for Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY[0]	PIN_M23	Push-button[0]	Depending on JP7
KEY[1]	PIN_M21	Push-button[1]	Depending on JP7
KEY[2]	PIN_N21	Push-button[2]	Depending on JP7
KEY[3]	PIN_R24	Push-button[3]	Depending on JP7

Table 3-4 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description
LEDR0	PIN_AA2	LED [0]
LEDR1	PIN_AA1	LED [1]
LEDR2	PIN_W2	LED [2]
LEDR3	PIN_Y3	LED [3]
LEDR4	PIN_N2	LED [4]
LEDR5	PIN_N1	LED [5]
LEDR6	PIN_U2	LED [6]
LEDR7	PIN_U1	LED [7]
LEDR8	PIN_L2	LED [8]
LEDR9	PIN_L1	LED [9]

Table 4-3 Pin Assignments for LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_G19	LED Red[0]	2.5V
LEDR[1]	PIN_F19	LED Red[1]	2.5V
LEDR[2]	PIN_E19	LED Red[2]	2.5V
LEDR[3]	PIN_F21	LED Red[3]	2.5V
LEDR[4]	PIN_F18	LED Red[4]	2.5V
LEDR[5]	PIN_E18	LED Red[5]	2.5V
LEDR[6]	PIN_J19	LED Red[6]	2.5V
LEDR[7]	PIN_H19	LED Red[7]	2.5V
LEDR[8]	PIN_J17	LED Red[8]	2.5V
LEDR[9]	PIN_G17	LED Red[9]	2.5V
LEDR[10]	PIN_J15	LED Red[10]	2.5V
LEDR[11]	PIN_H16	LED Red[11]	2.5V
LEDR[12]	PIN_J16	LED Red[12]	2.5V
LEDR[13]	PIN_H17	LED Red[13]	2.5V
LEDR[14]	PIN_F15	LED Red[14]	2.5V

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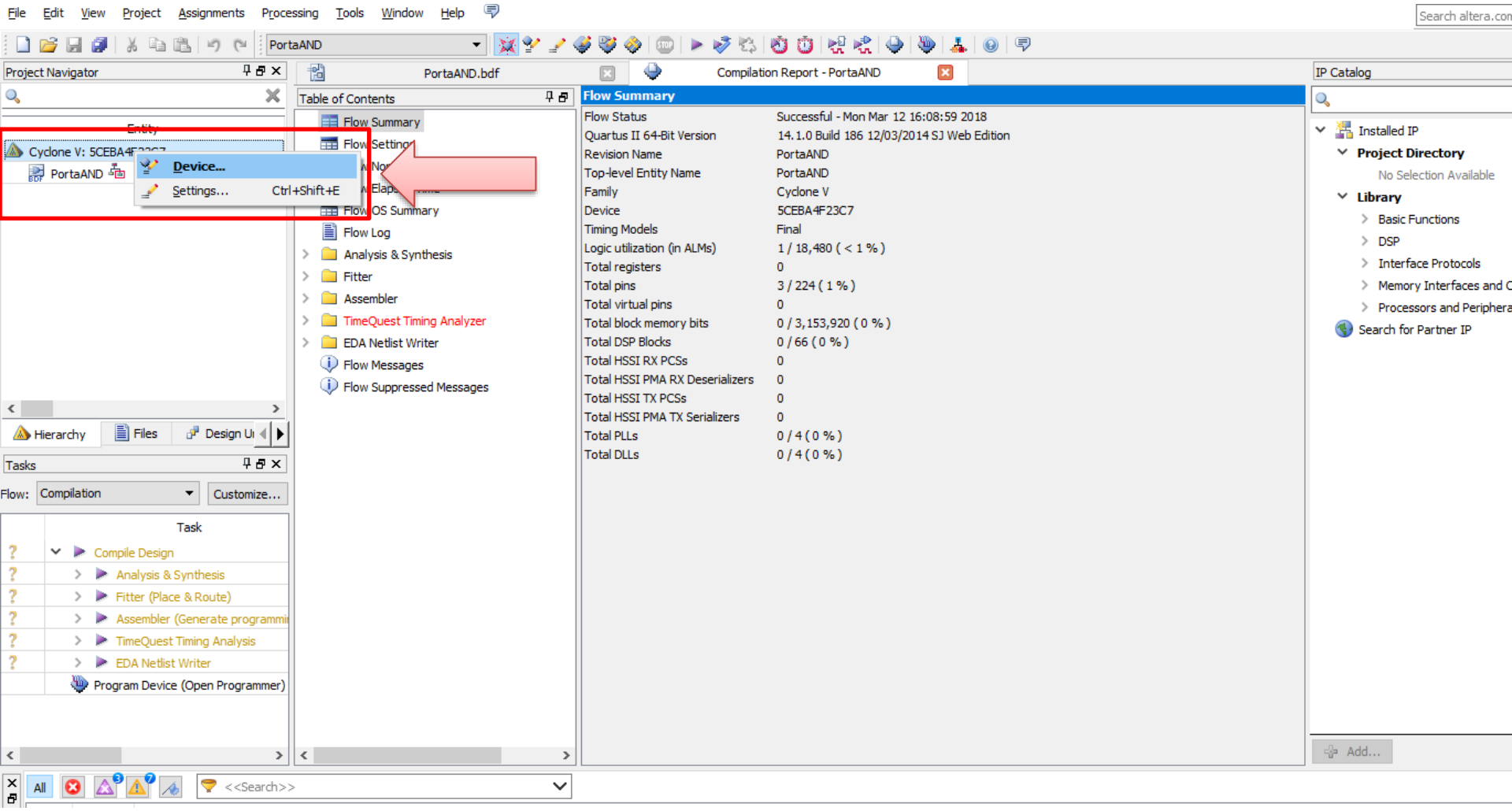
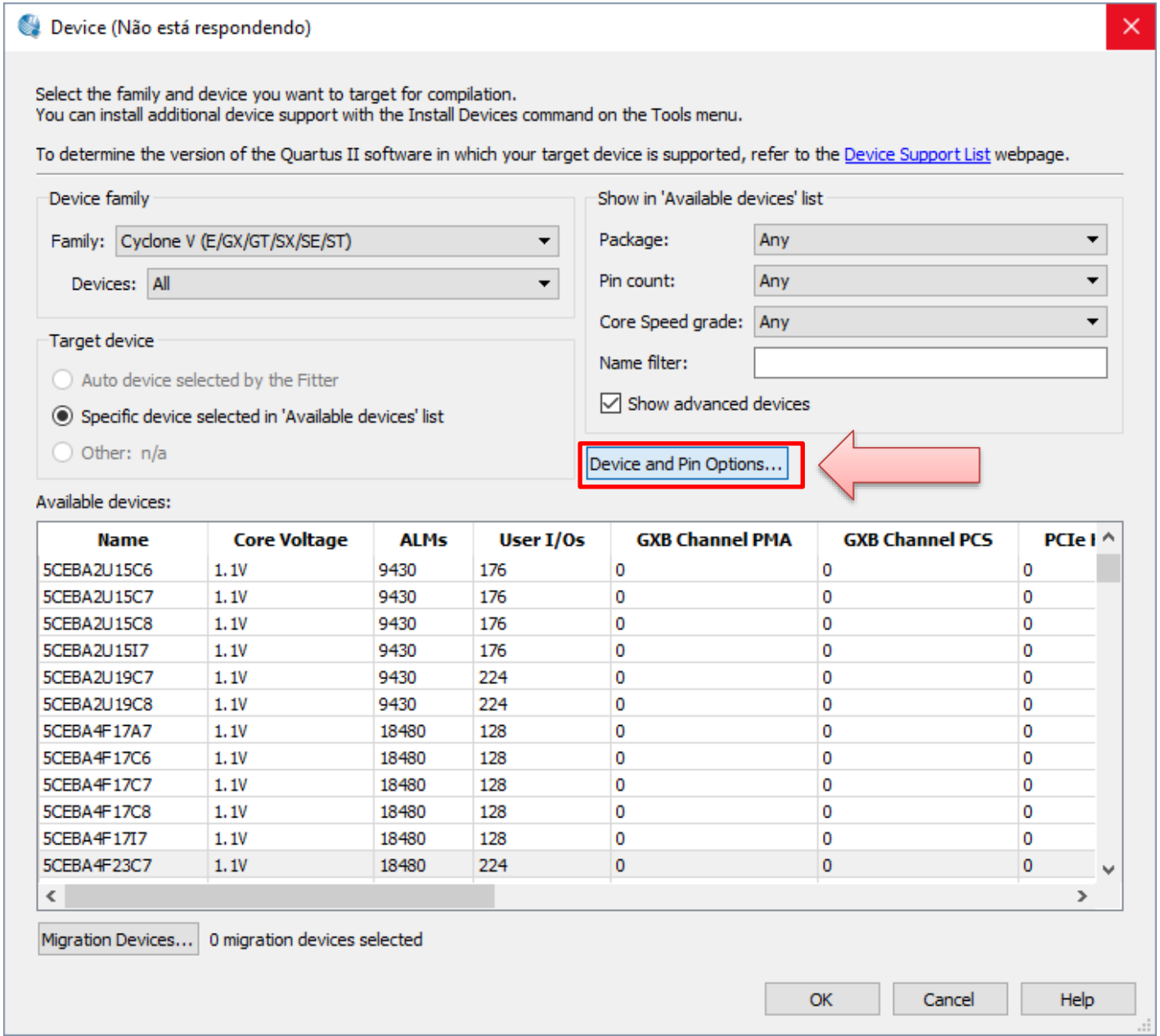
9 - Escolha de Pinos (V)



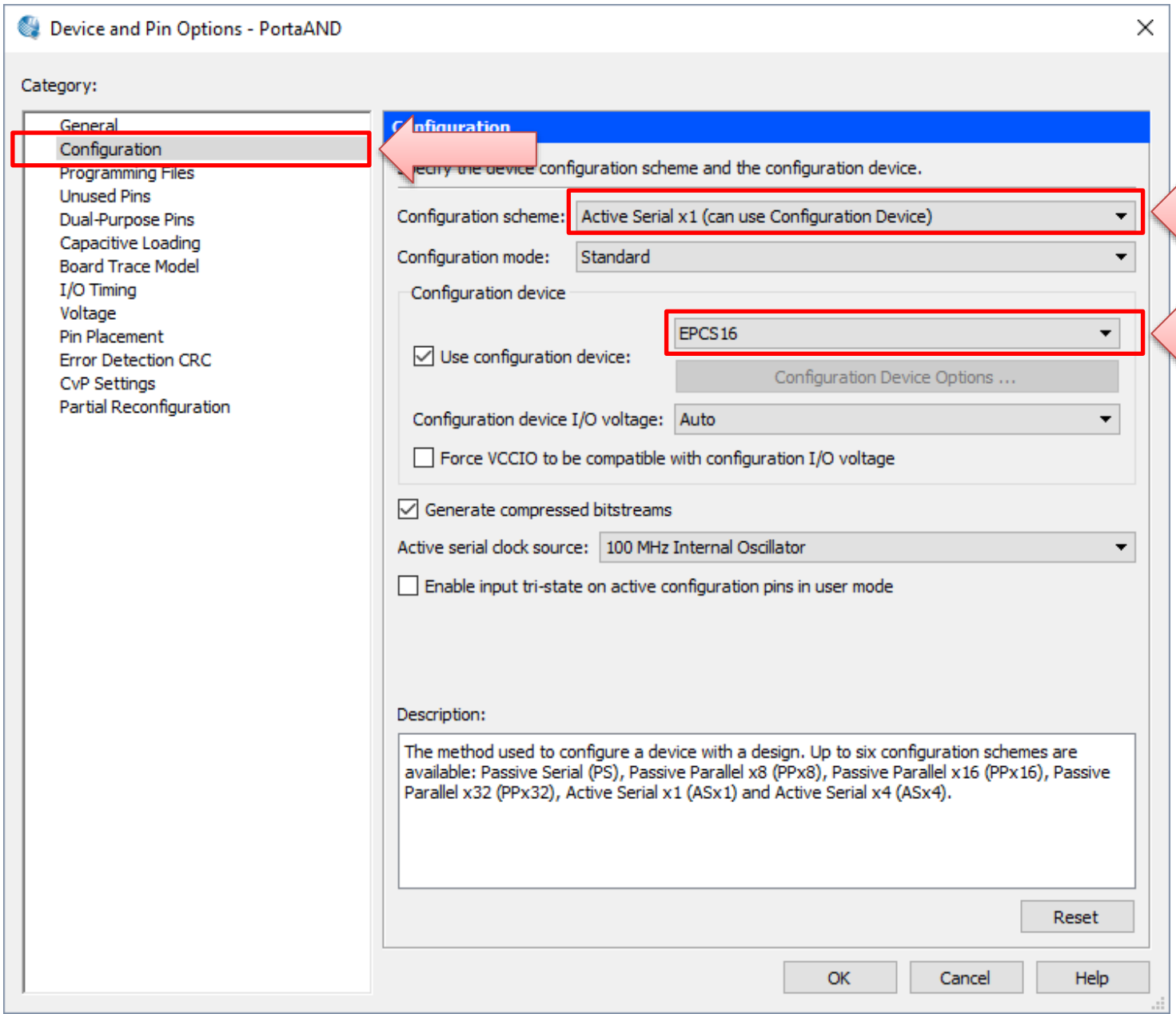
Configuração do Quartus

9 - Escolha de Pinos (VI)



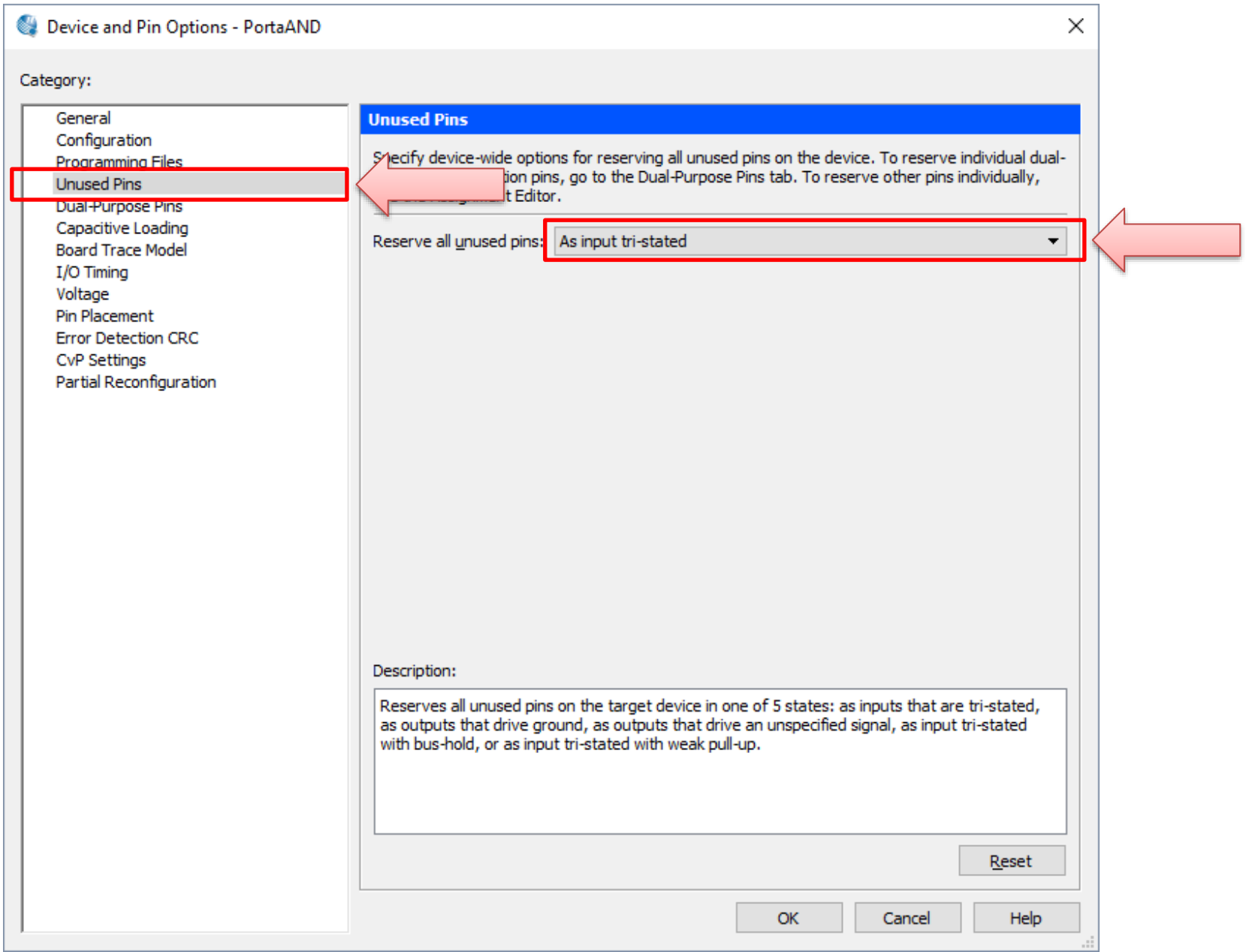
Configuração do Quartus

9 - Escolha de Pinos (VII)



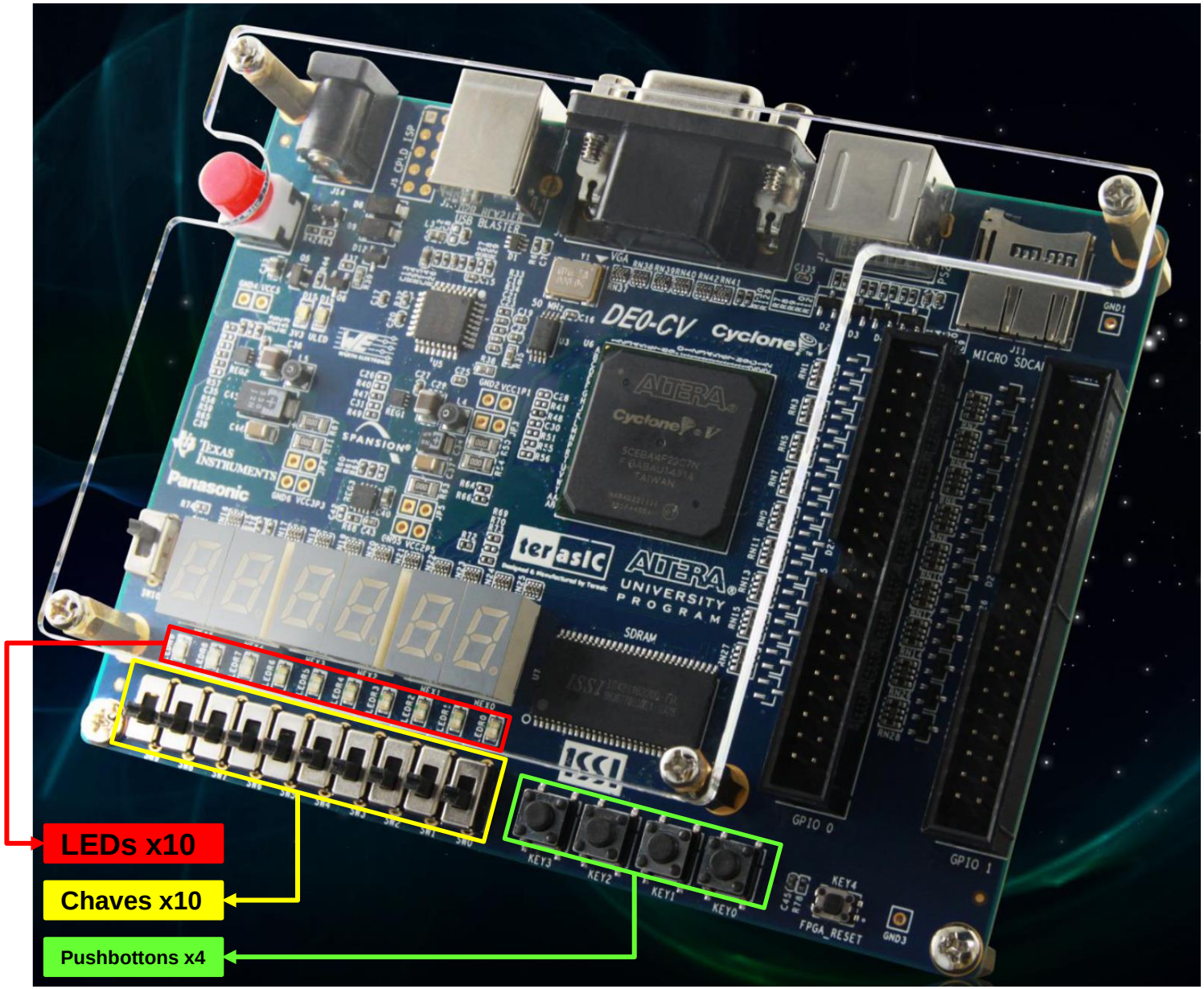
Configuração do Quartus

9 - Escolha de Pinos (VIII)



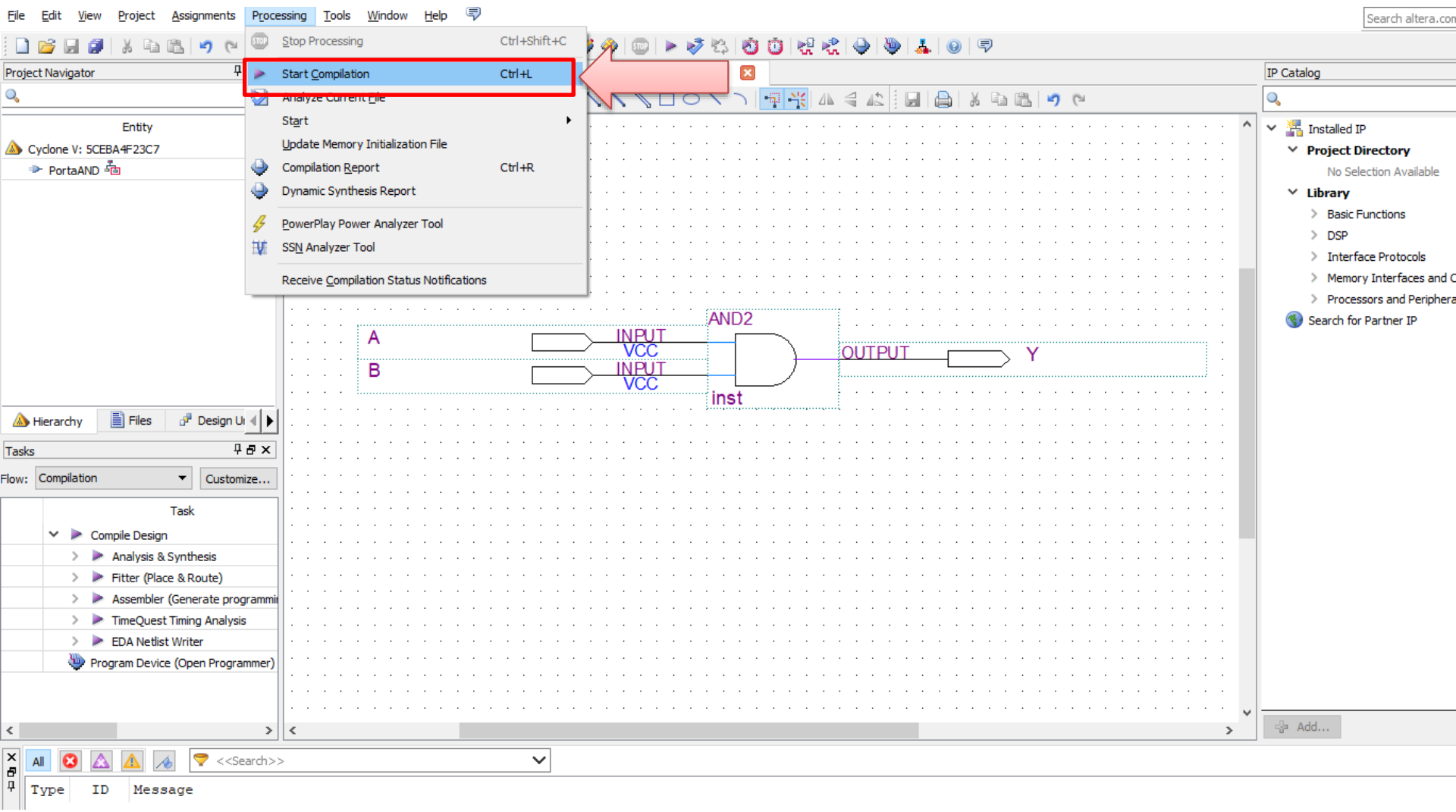
Configuração do Quartus

9 - Escolha de Pinos (IX)



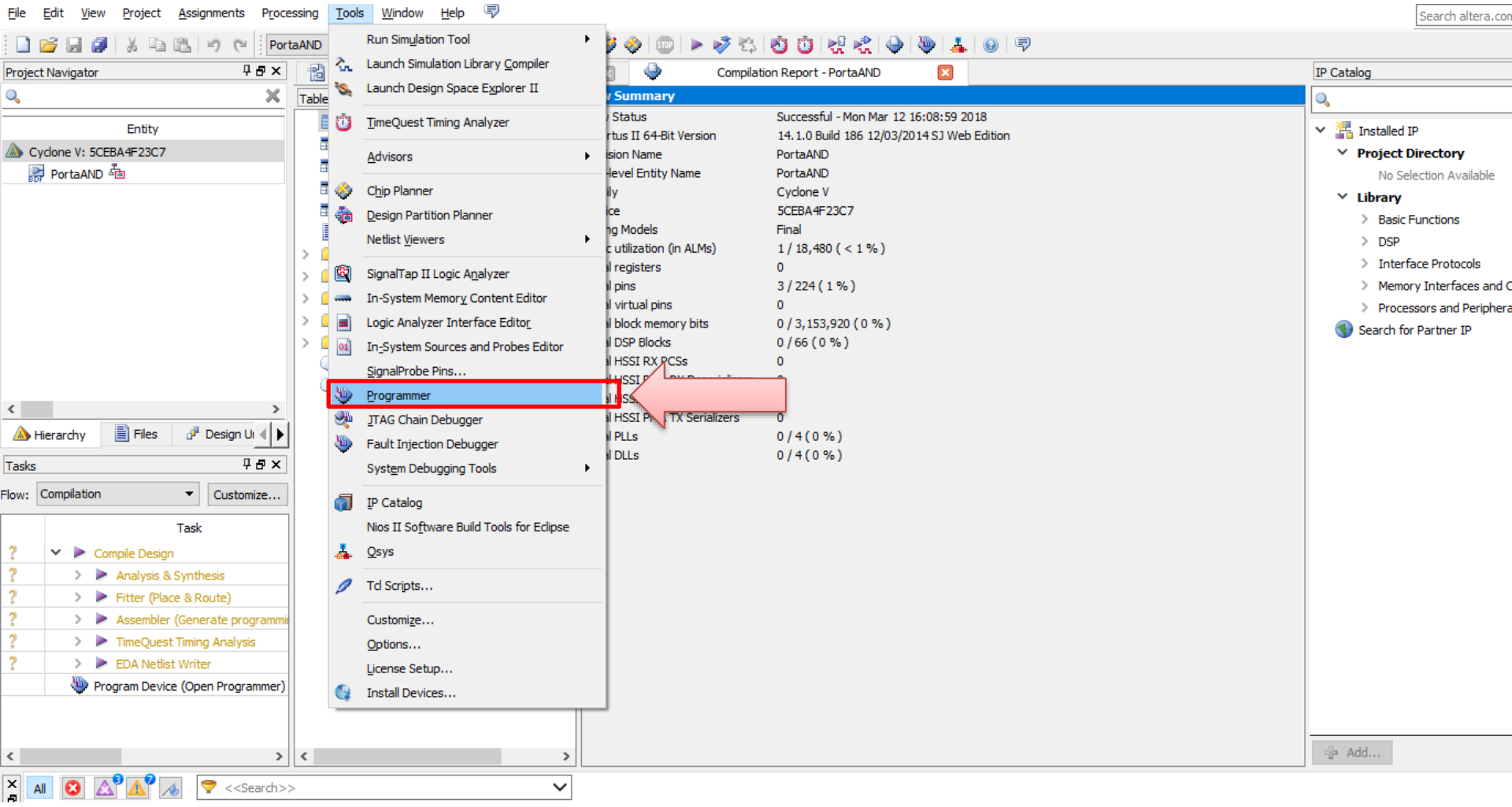
Configuração do Quartus

10 - Compilar Novamente



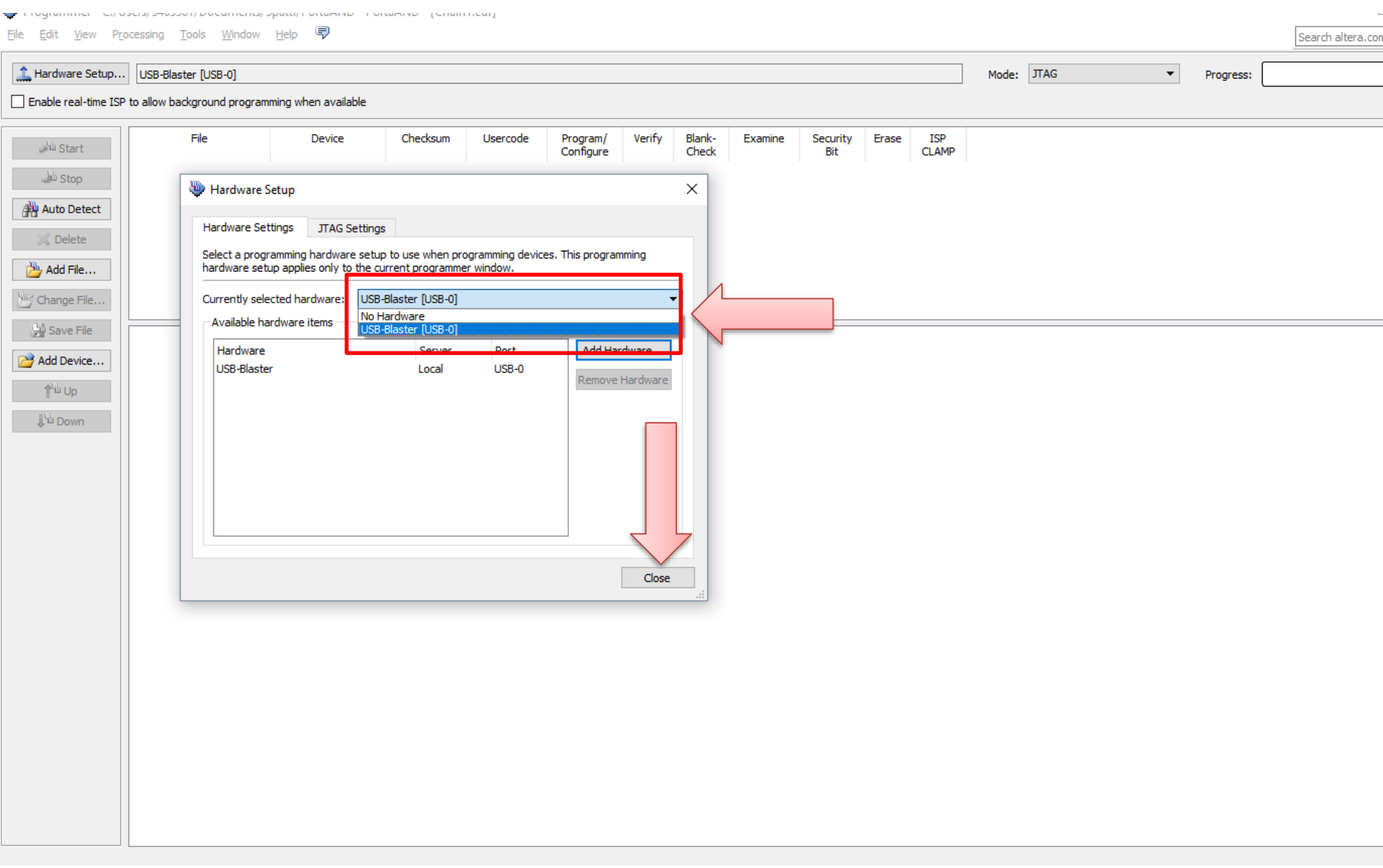
Configuração do Quartus

11 - Ligar a FPGA e Programar



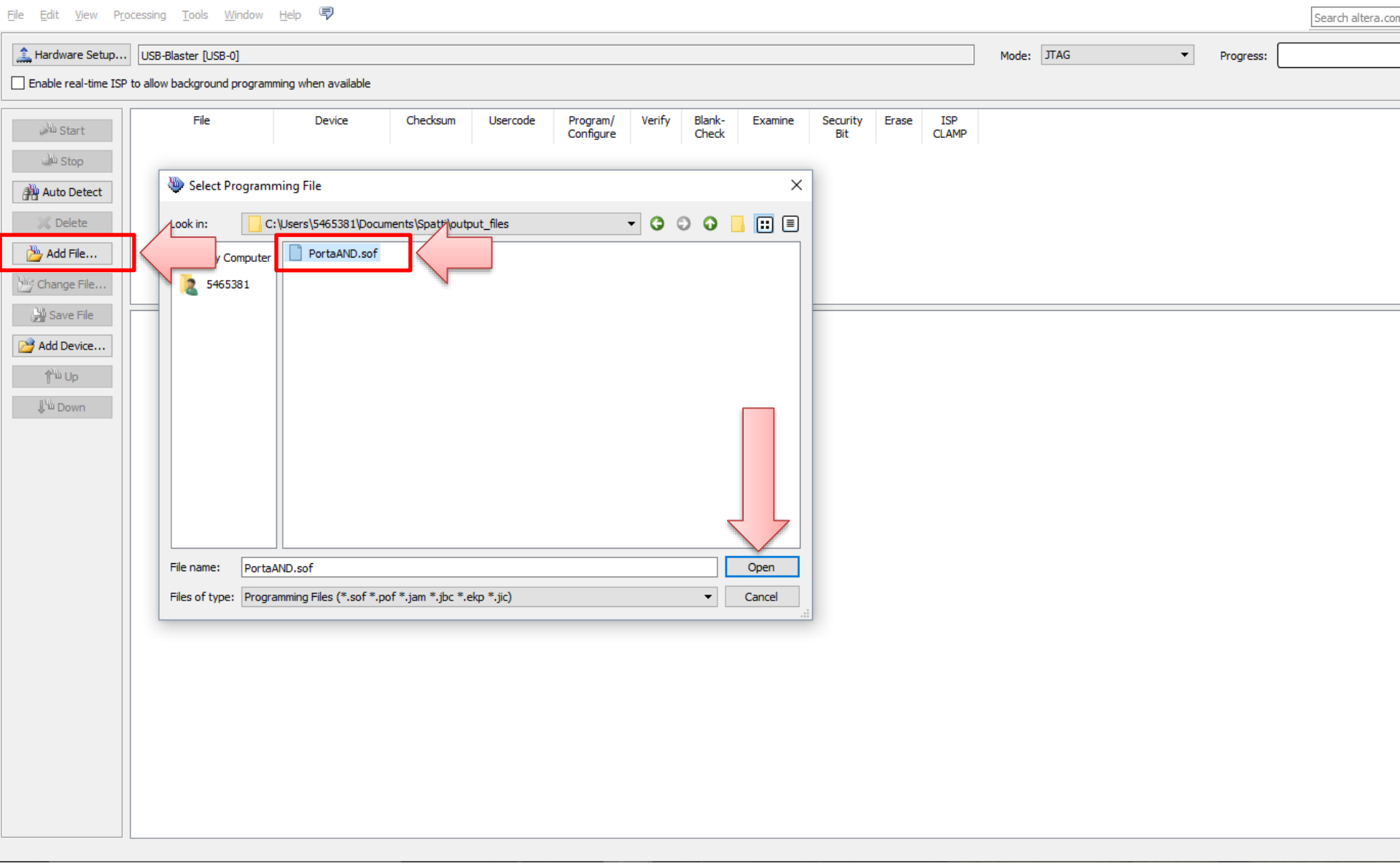
Configuração do Quartus

12 - Verificar se o Driver USB está Instalado



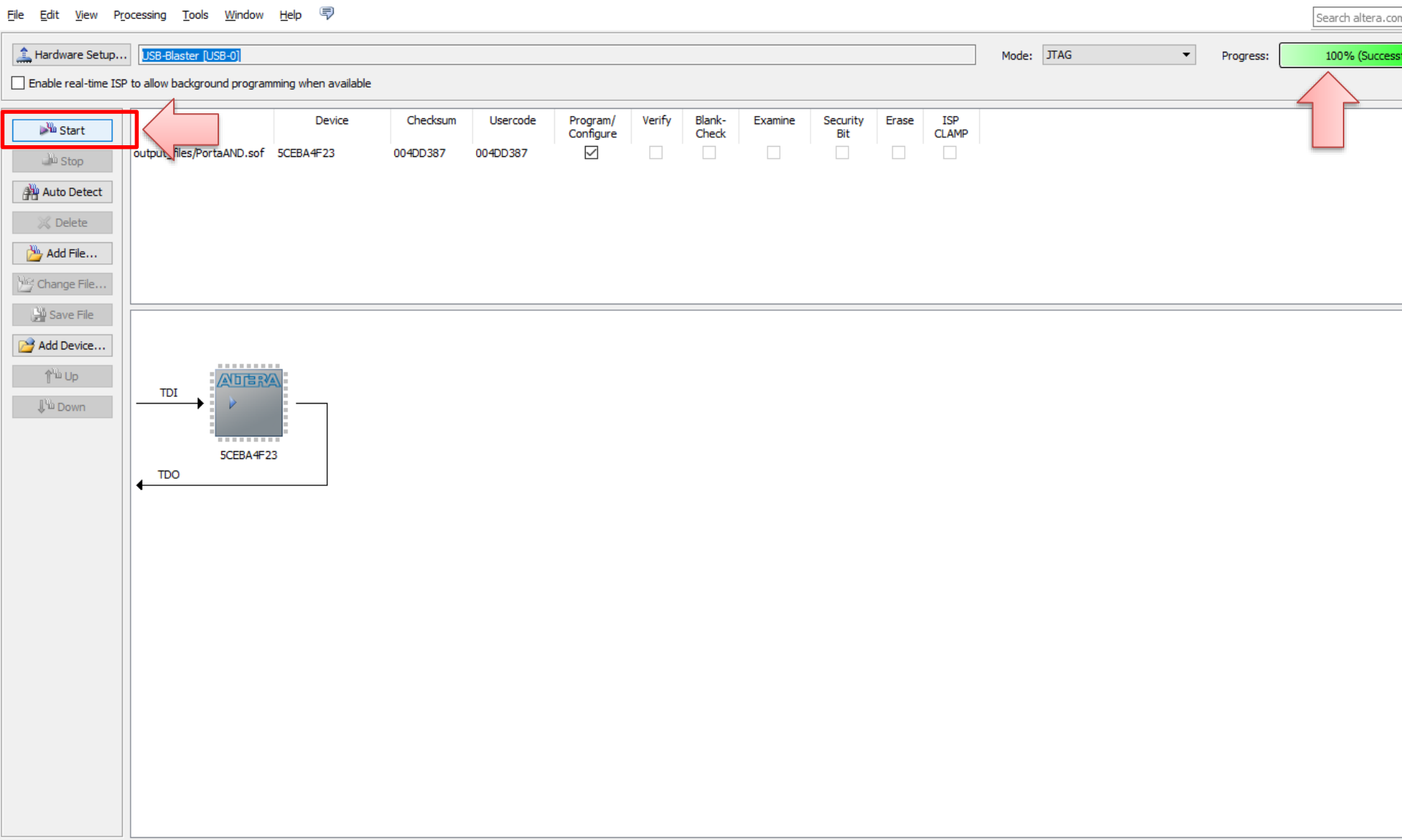
Configuração do Quartus

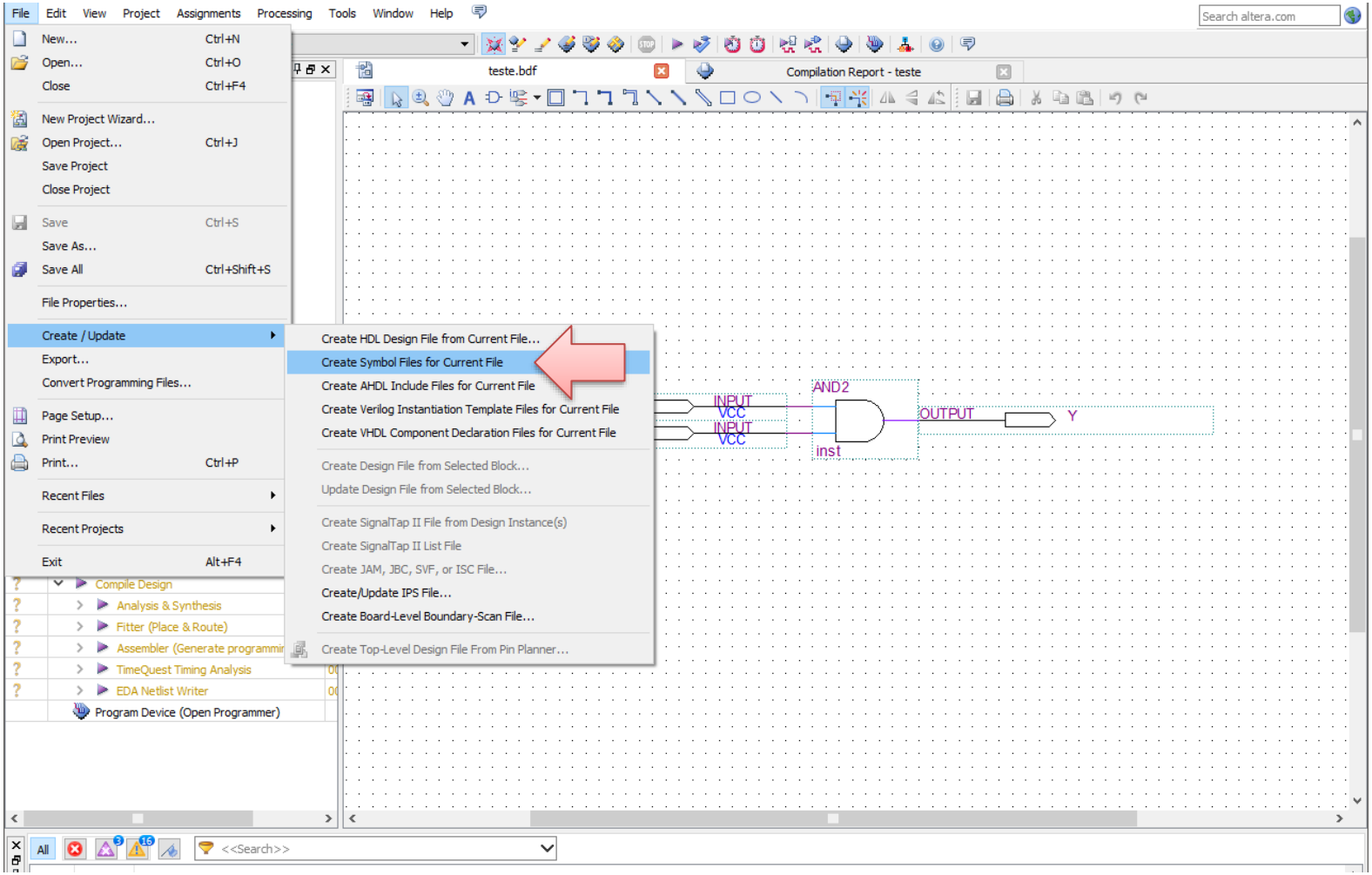
13 - Adicionar Esquemático para Execução



Configuração do Quartus

14 - Executar

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Open Project... Ctrl+J
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Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
Create HDL Design File from Current File...
Create Symbol Files for Current File
Create AHDL Include Files for Current File
Create Verilog Instantiation Template Files for Current File
Create VHDL Component Declaration Files for Current File
Create Design File from Selected Block...
Update Design File from Selected Block...
Create SignalTap II File from Design Instance(s)
Create SignalTap II List File
Create JAM, JBC, SVF, or ISC File...
Create/Update IPS File...
Create Board-Level Boundary-Scan File...
Create Top-Level Design File From Pin Planner...
teste.bdf
Compilation Report - teste
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VCC
AND2
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OUTPUT
Y
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmi
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
All
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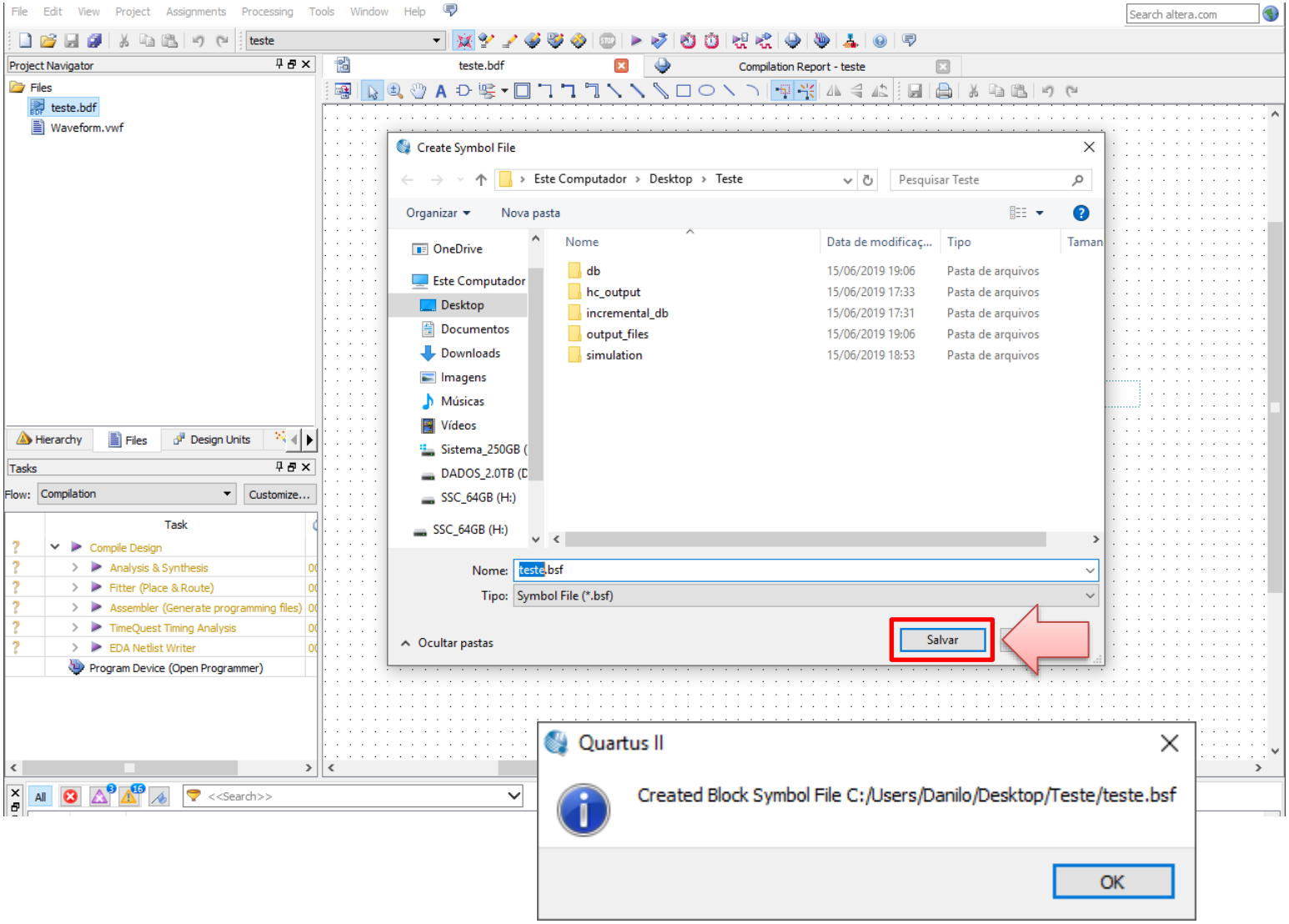
*15 - Criando Blocos - Arquivo *.bsf*



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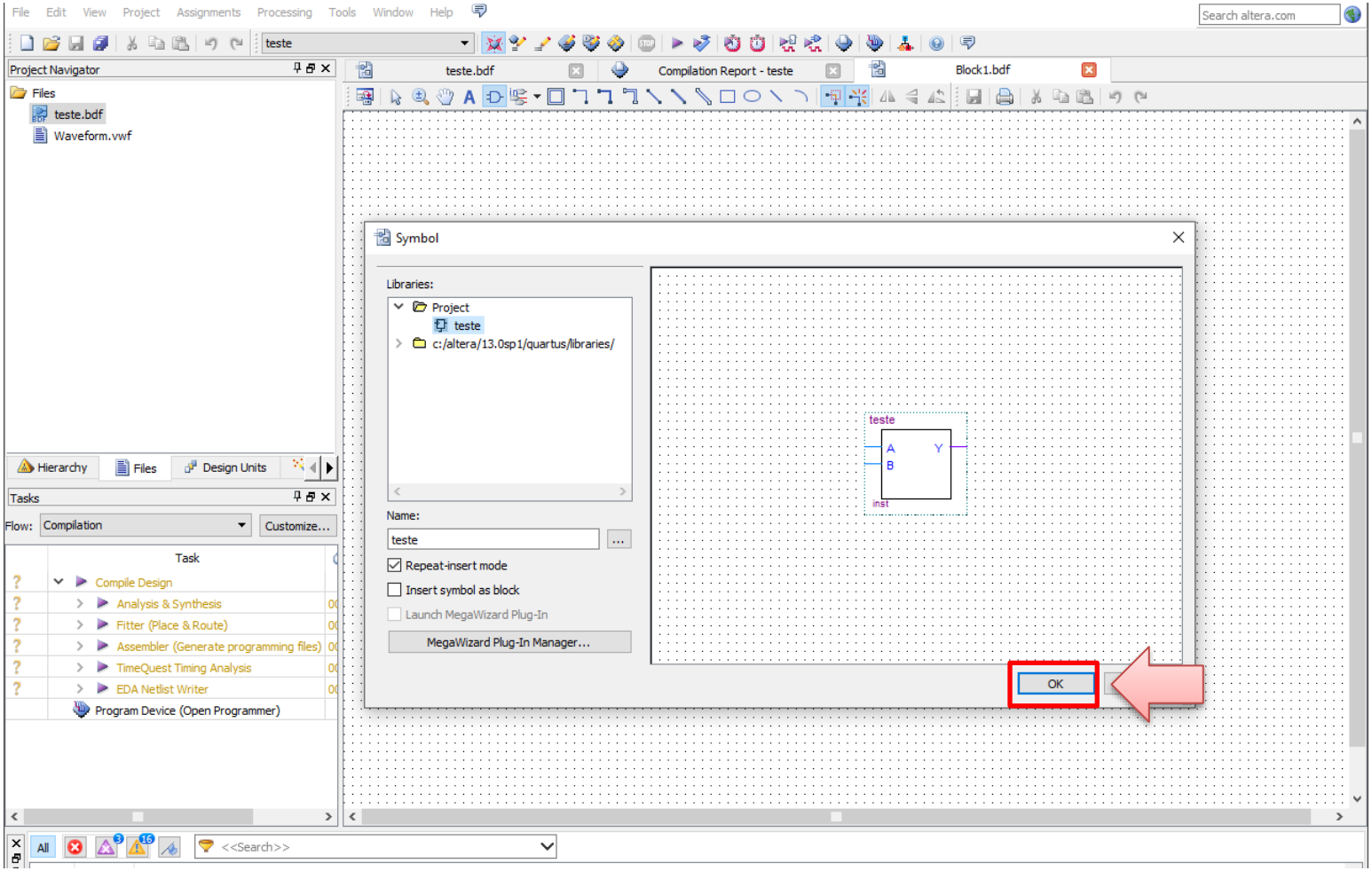
Configuração do Quartus

15 - Criando Blocos - Adicionar do Symbol Tool



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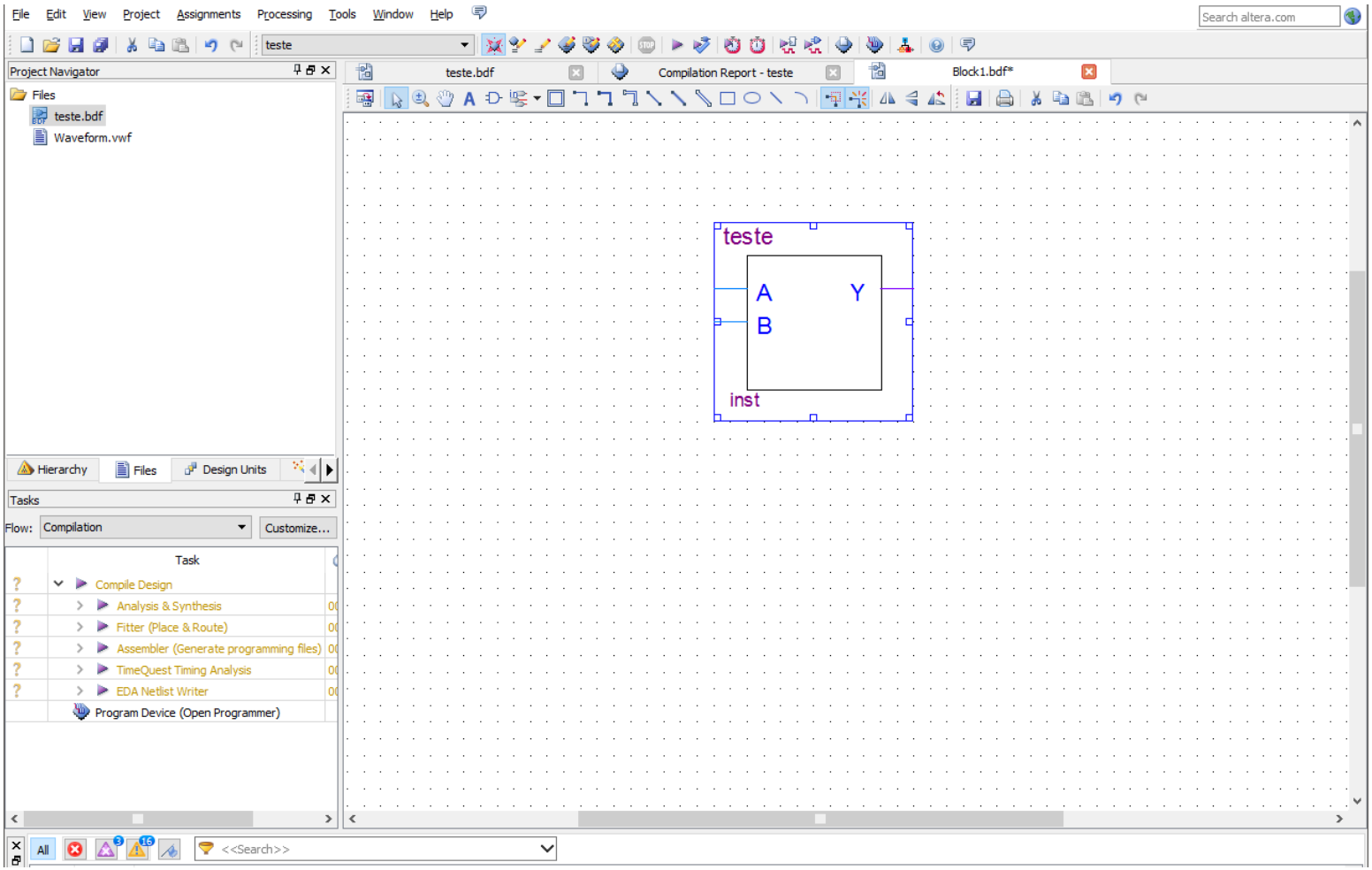
Prática em Digitais

Configuração do Quartus

*15 - Criando Blocos - Adicionar em novo arquivo *.bdf*



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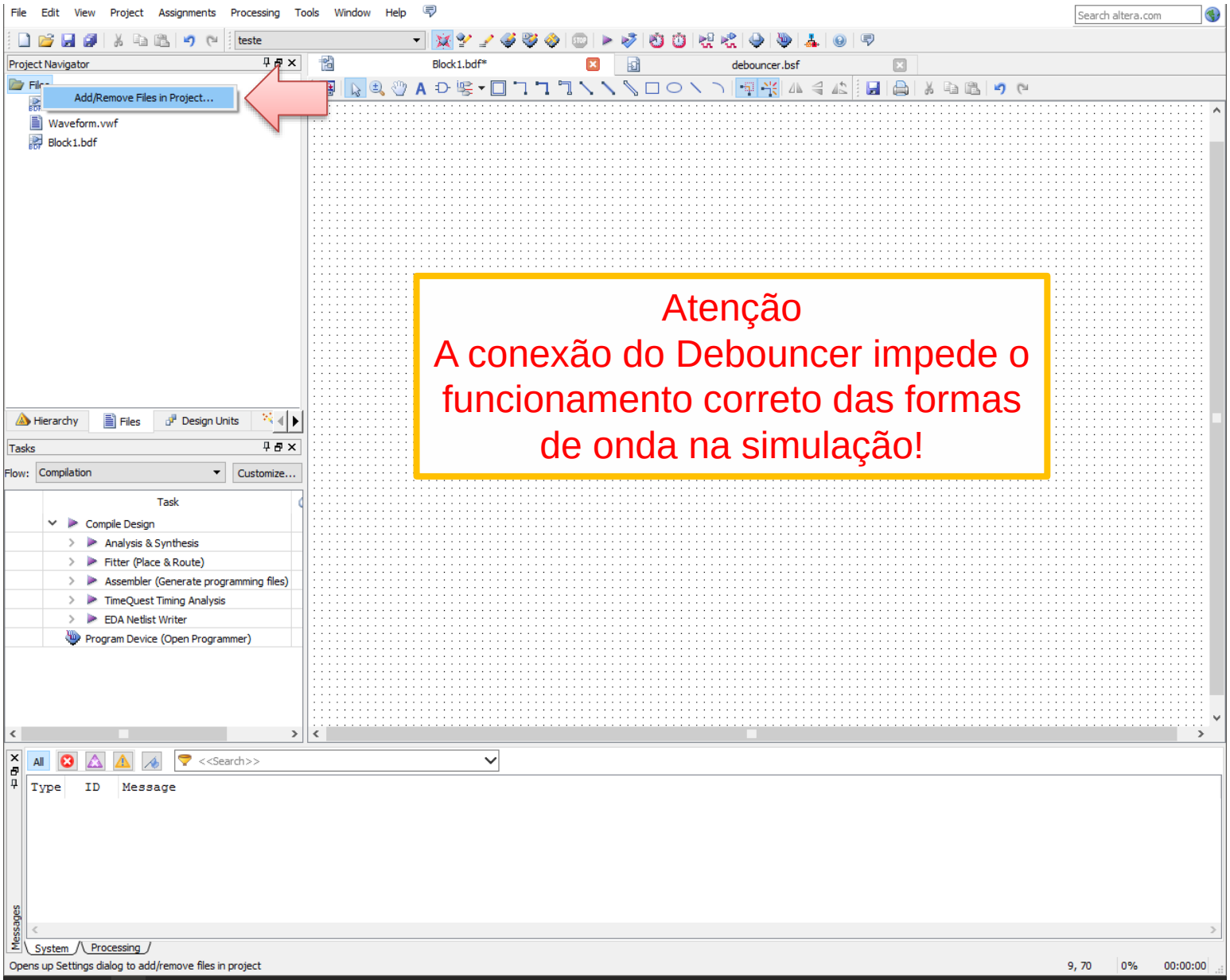
Configuração do Quartus
16 - Filtrar entradas - Debouncer



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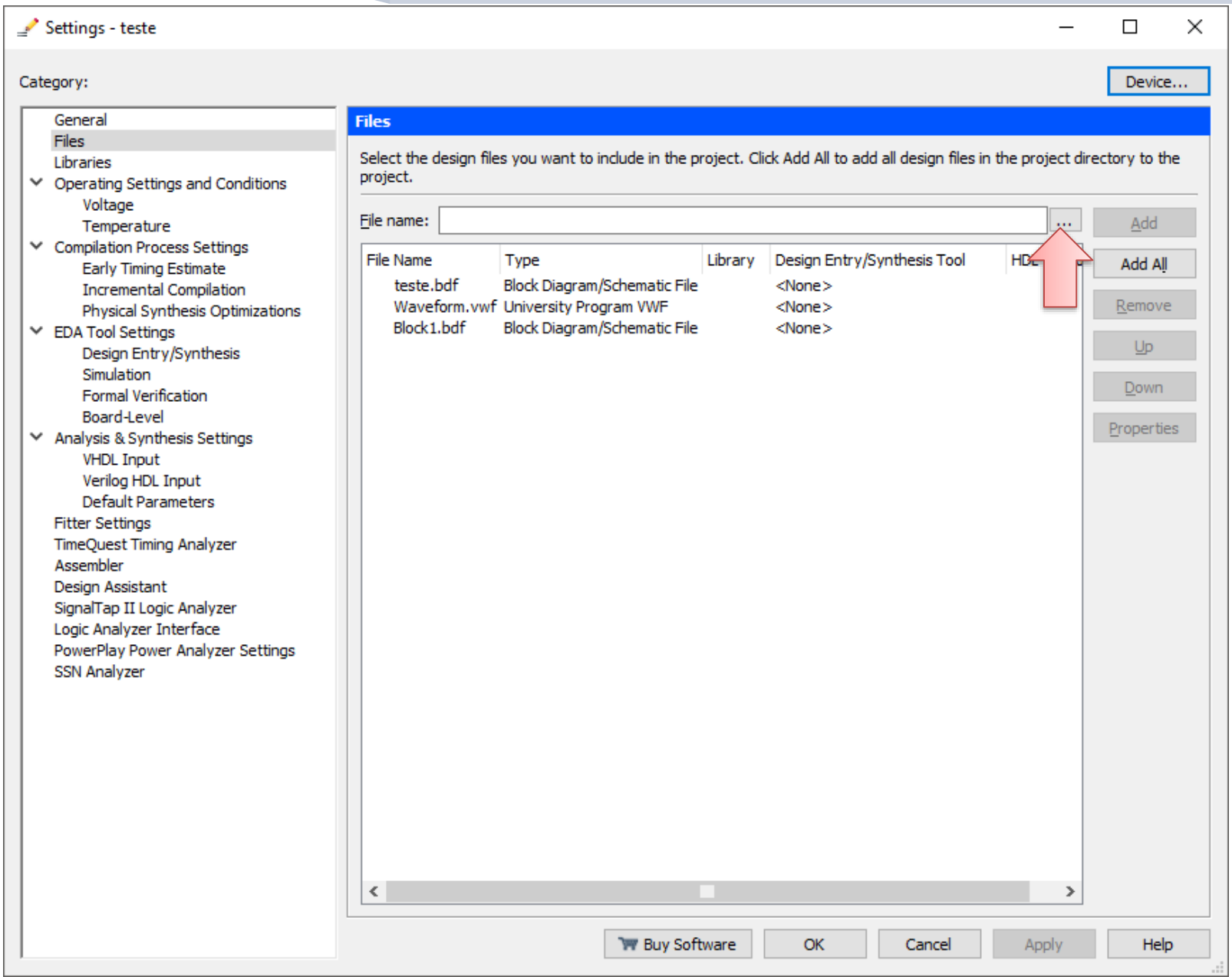
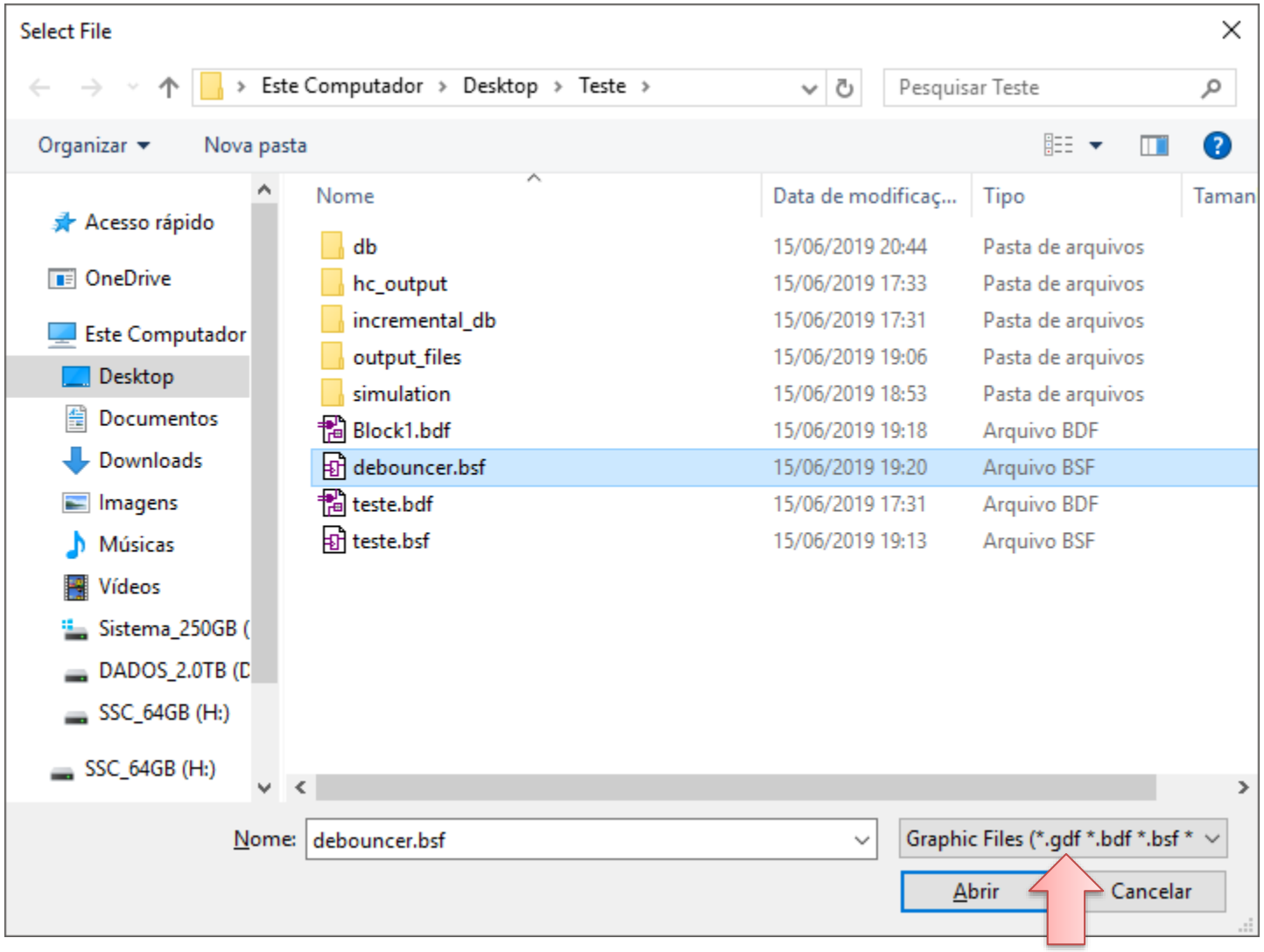
Configuração do Quartus

16 - Filtrar entradas - Adicionar debouncer.bsf



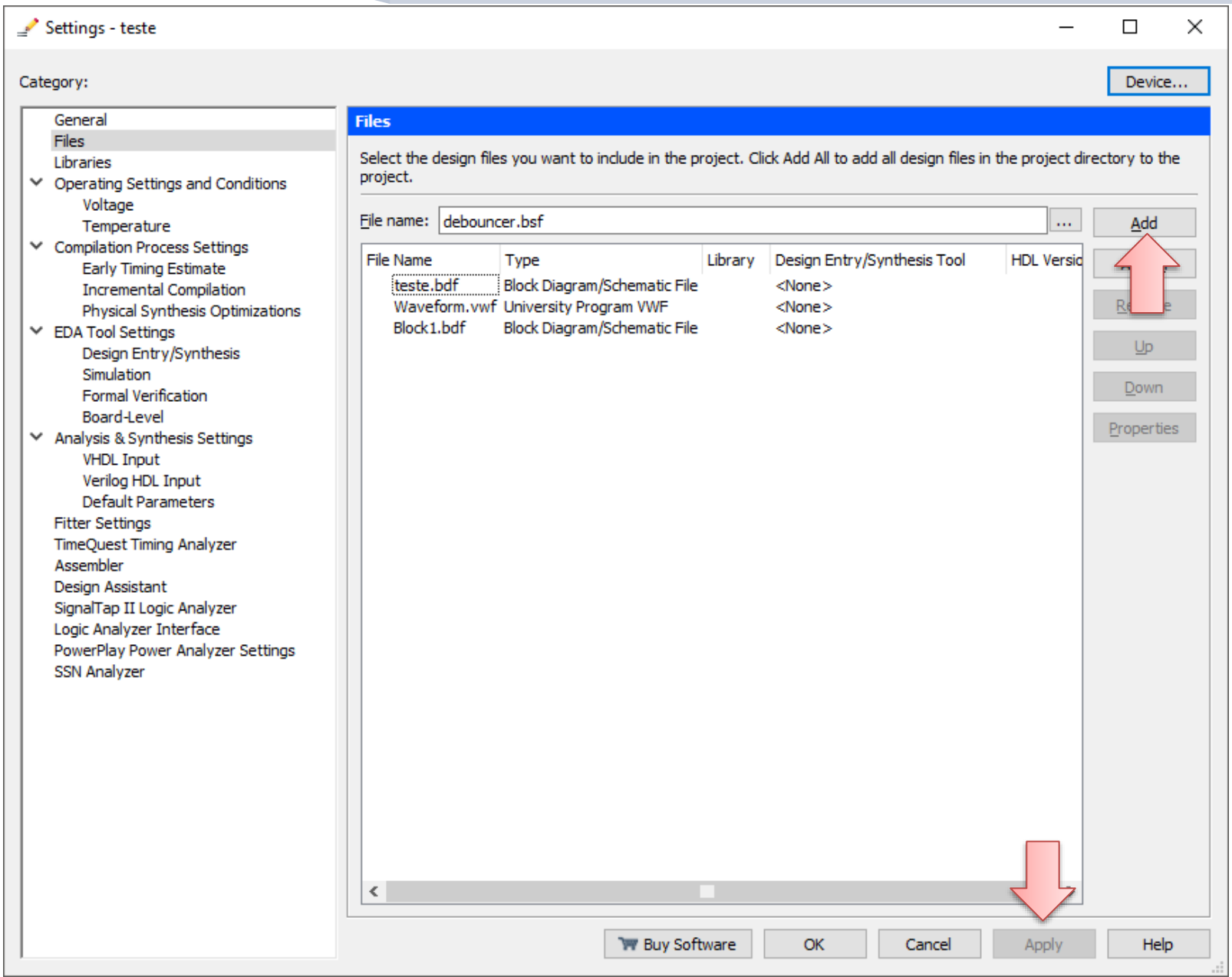
Configuração do Quartus

16 - Filtrar entradas - Selecionar e Abrir



Configuração do Quartus

16 - Filtrar entradas - Add e Apply



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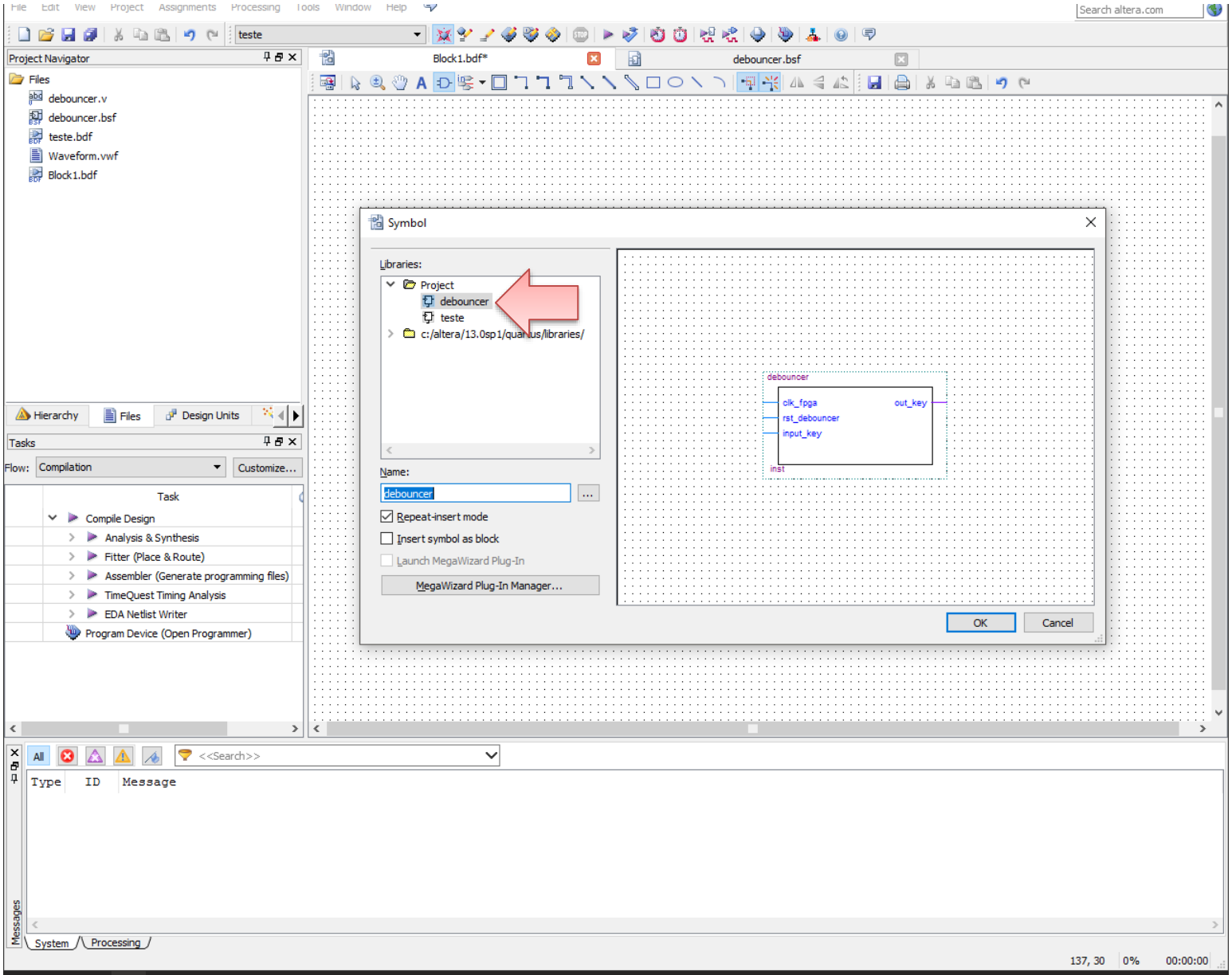
Configuração do Quartus
16 - Filtrar entradas - Adicionar a partir do Symbol Tool



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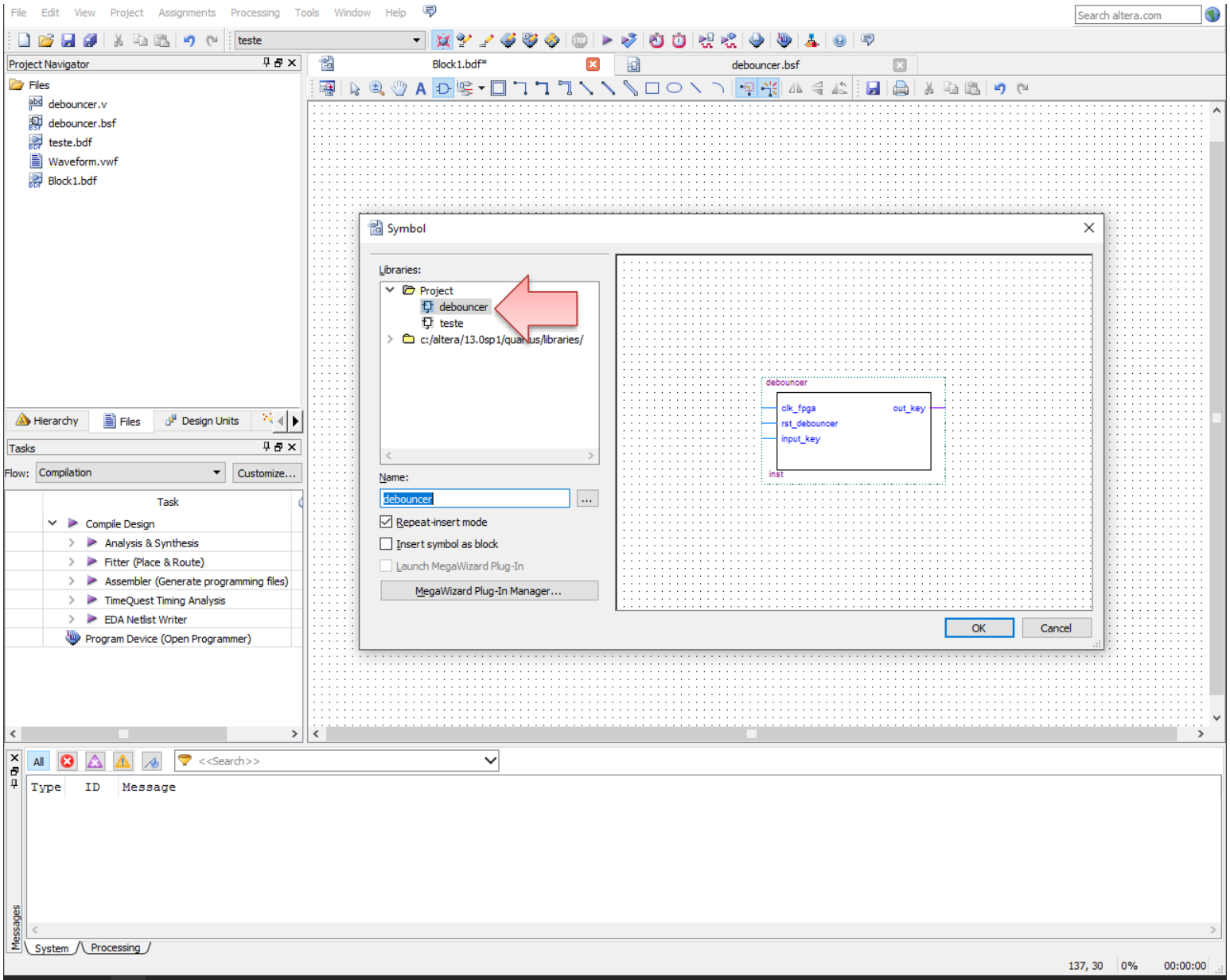
Configuração do Quartus

16 - Filtrar entradas - Adicionar a partir do Symbol Tool



Configuração do Quartus

16 - Filtrar entradas - Configuração

clk_fpga – clock interno da placa (CLOCK_50)
rst_debouncer – reset do contador do Debouncer
input_key – entrada com ruído
out_key – saída filtrada

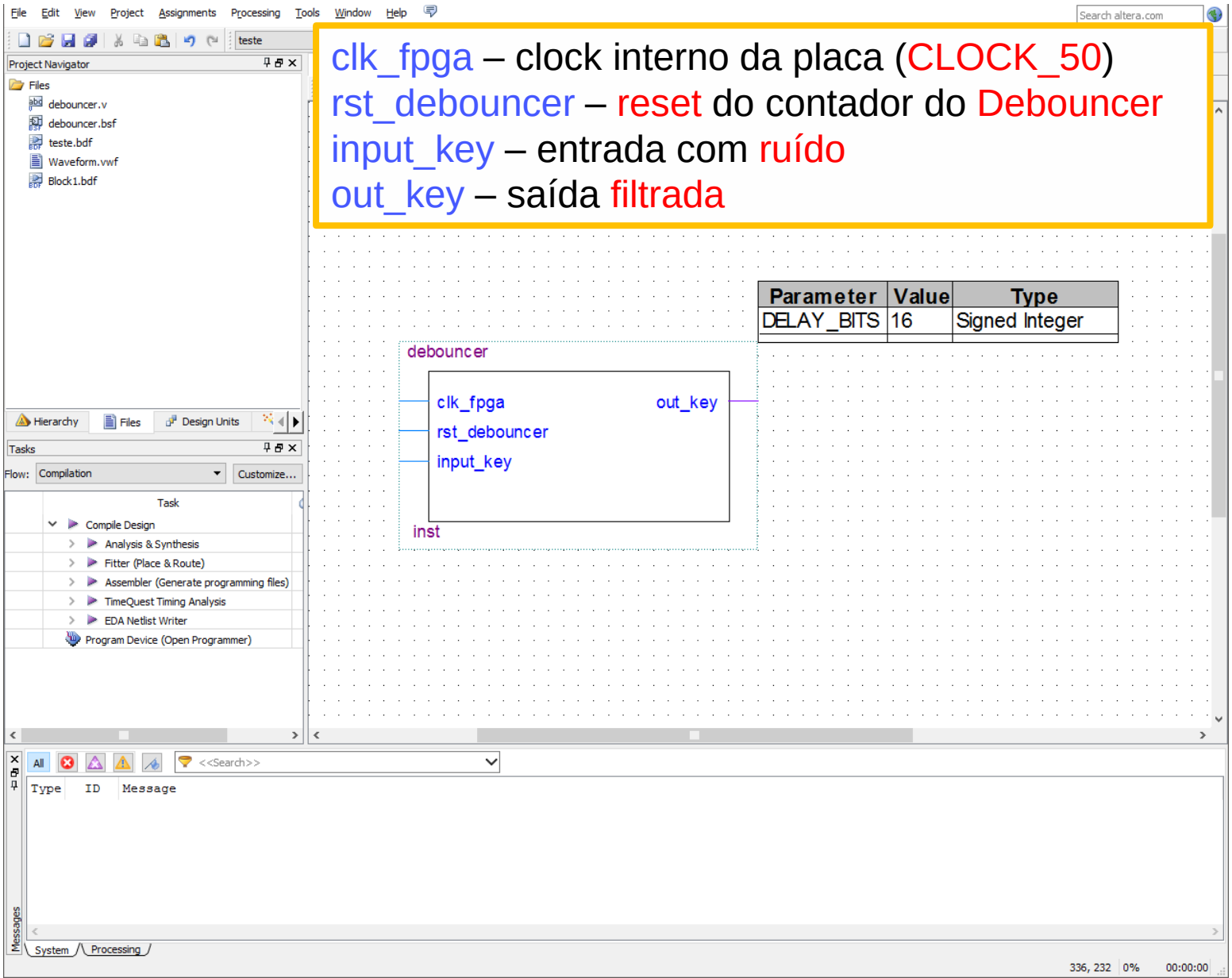


Table 3-6 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description
CLOCK_50	PIN_M9	50 MHz clock input(Bank 3B)
CLOCK2_50	PIN_H13	50 MHz clock input(Bank 7A)
CLOCK3_50	PIN_E10	50 MHz clock input(Bank 8A)
CLOCK4_50	PIN_V15	50 MHz clock input(Bank 4A)

Table 4-5 Pin Assignments for Clock Inputs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
CLOCK_50	PIN_Y2	50 MHz clock input	3.3V
CLOCK2_50	PIN_AG14	50 MHz clock input	3.3V
CLOCK3_50	PIN_AG15	50 MHz clock input	Depending on JP6
SMA_CLKOUT	PIN_AE23	External (SMA) clock output	Depending on JP6
SMA_CLKIN	PIN_AH14	External (SMA) clock input	3.3V

Fim

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