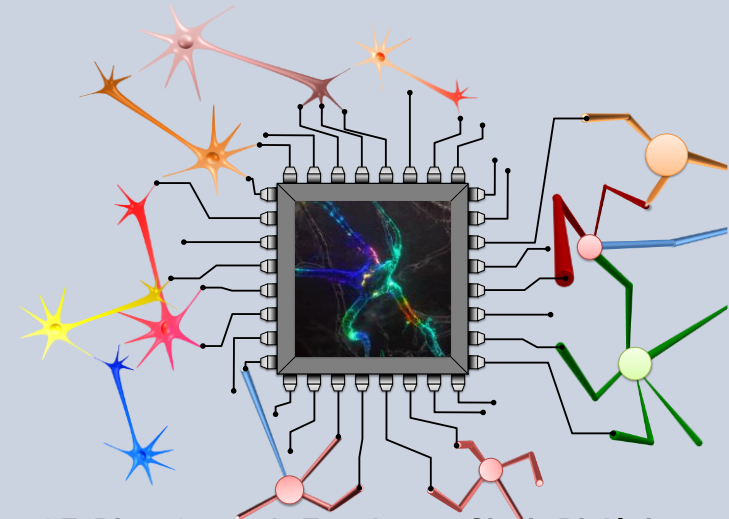


Universidade de São Paulo
Instituto de Ciências Matemáticas e de Computação
Departamento de Sistemas de Computação

SSC108
Prática em Sistemas
Digitais

Tutorial Configuração
Quartus – Parte I

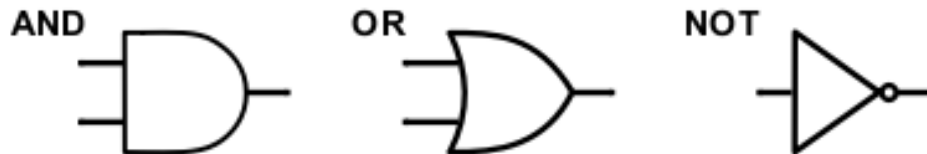


GE4Bio – Grupo de Estudos em Sinais Biológicos

Prof.Dr. Danilo Spatti

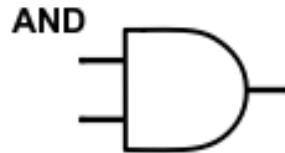
São Carlos

- A Álgebra de Boole pode ser **desenvolvida** a partir de **símbolos** pré-definidos, **tabela de funcionamento (verdade)** e **equações lógicas**.
- As ditas operações lógicas **primitivas** são formadas por **AND**, **OR** e **NOT**, sendo as demais derivadas a partir destas.

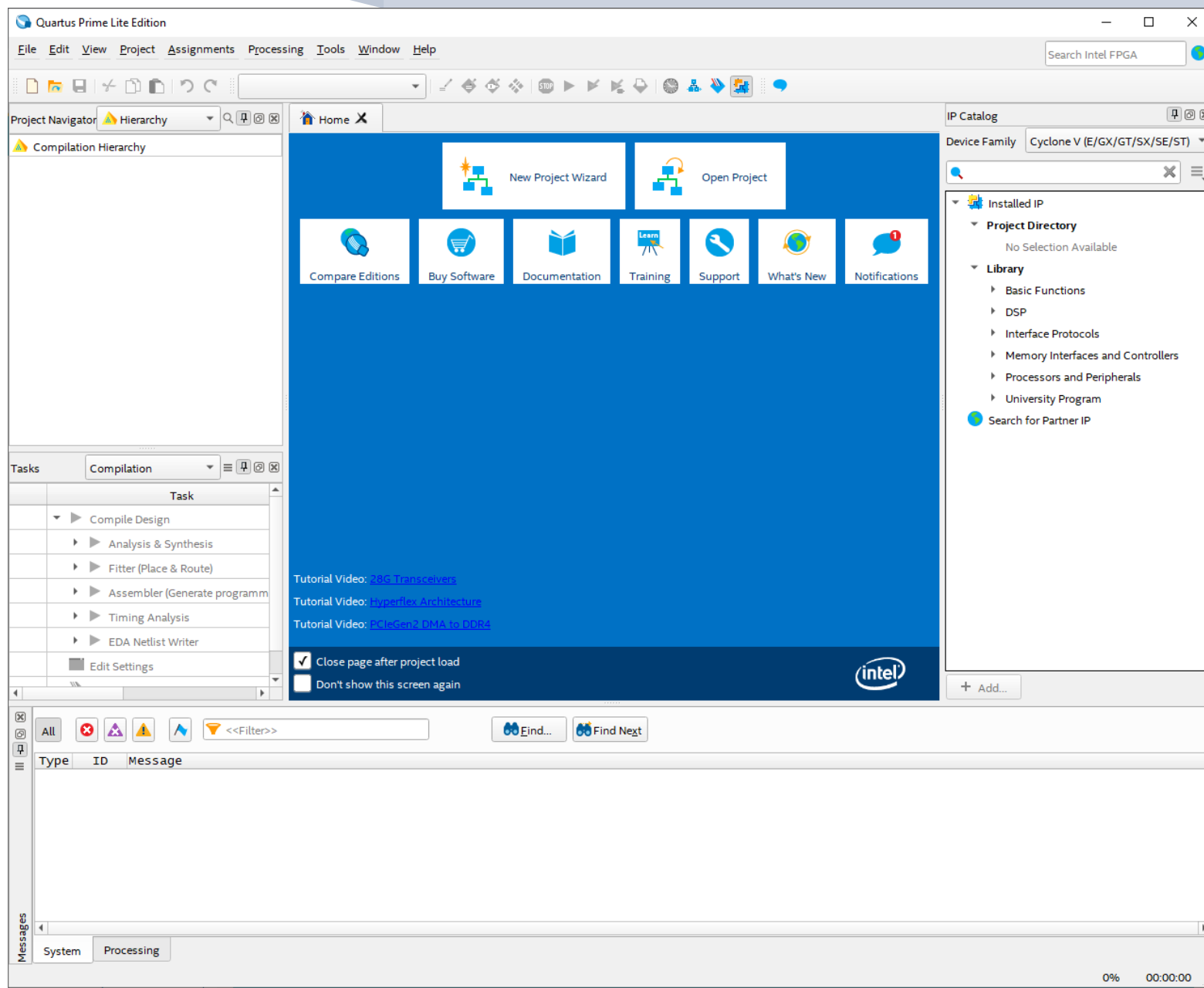


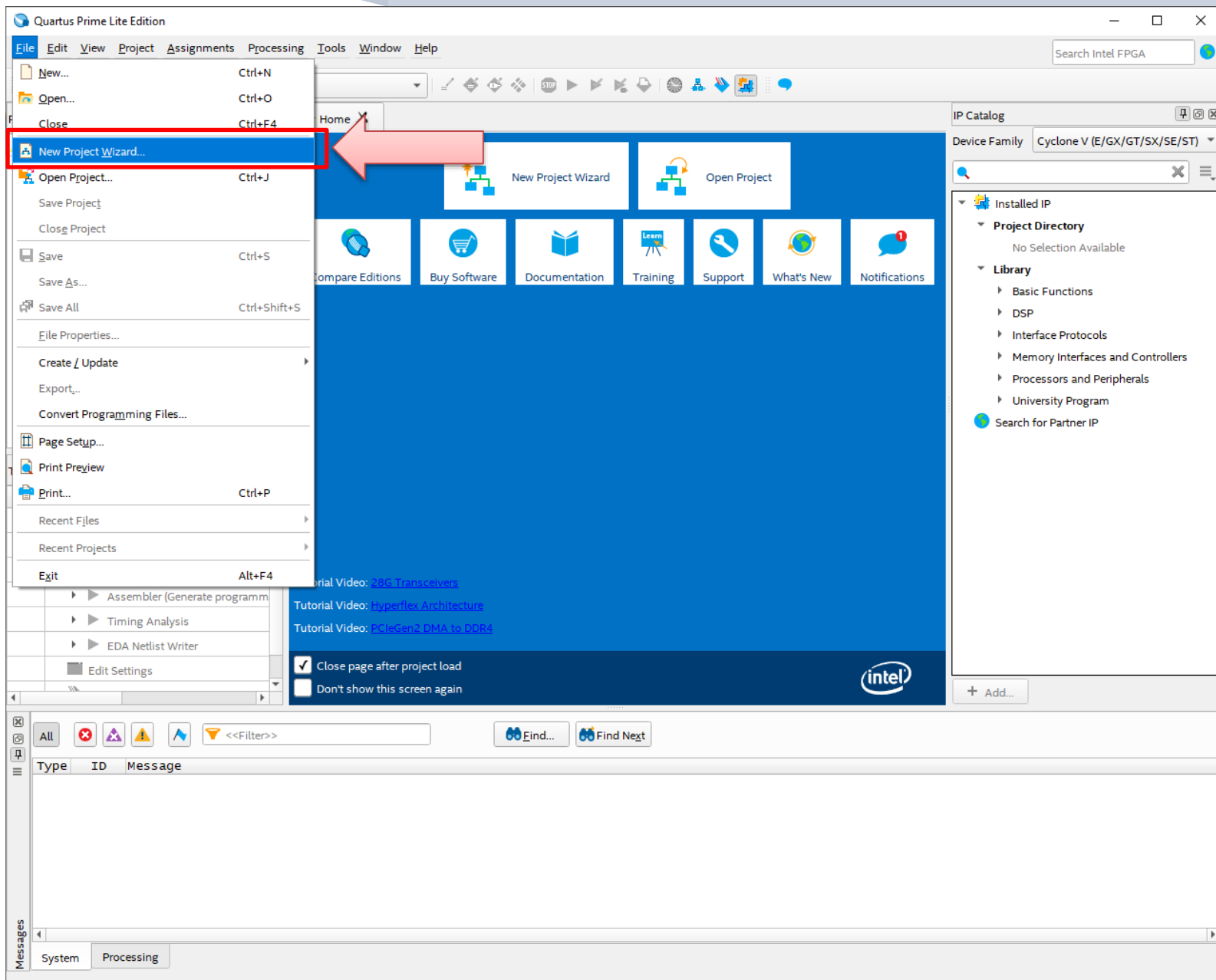
- Resulta em **verdadeira** se, e somente se, **todas** as proposições forem verdadeiras.
- A operação AND (E) é dita **conjunção** ou também **produto lógico** e é representada pela conectiva “.” (ponto).

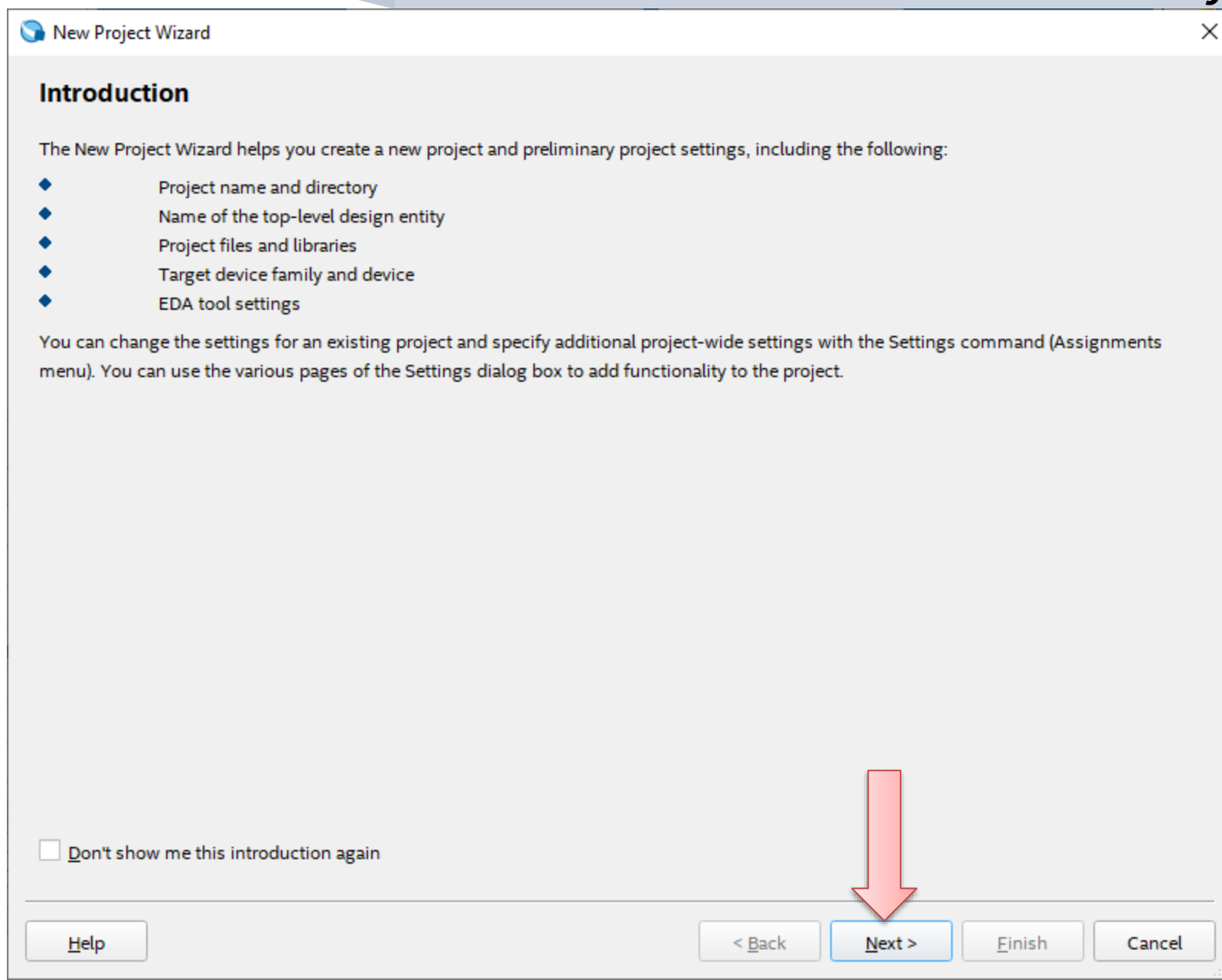
$$S(a, b) = a \cdot b$$



<i>a</i>	<i>b</i>	<i>S</i>
0	0	0
0	1	0
1	0	0
1	1	1







New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

C:/Users/Danilo/Desktop/ELD ...

What is the name of this project?

PortaAND ...

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

PortaAND| ...

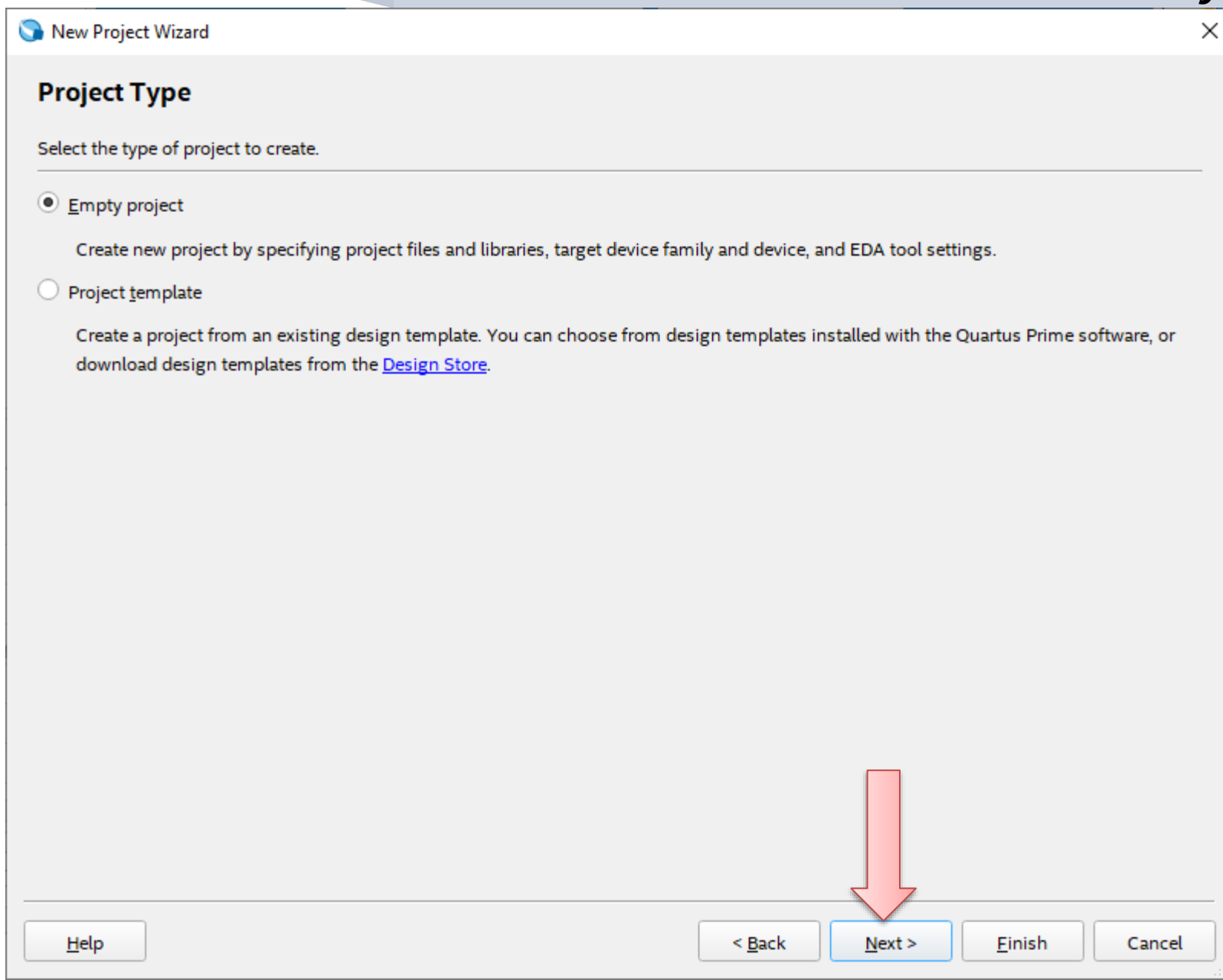
Use Existing Project Settings...

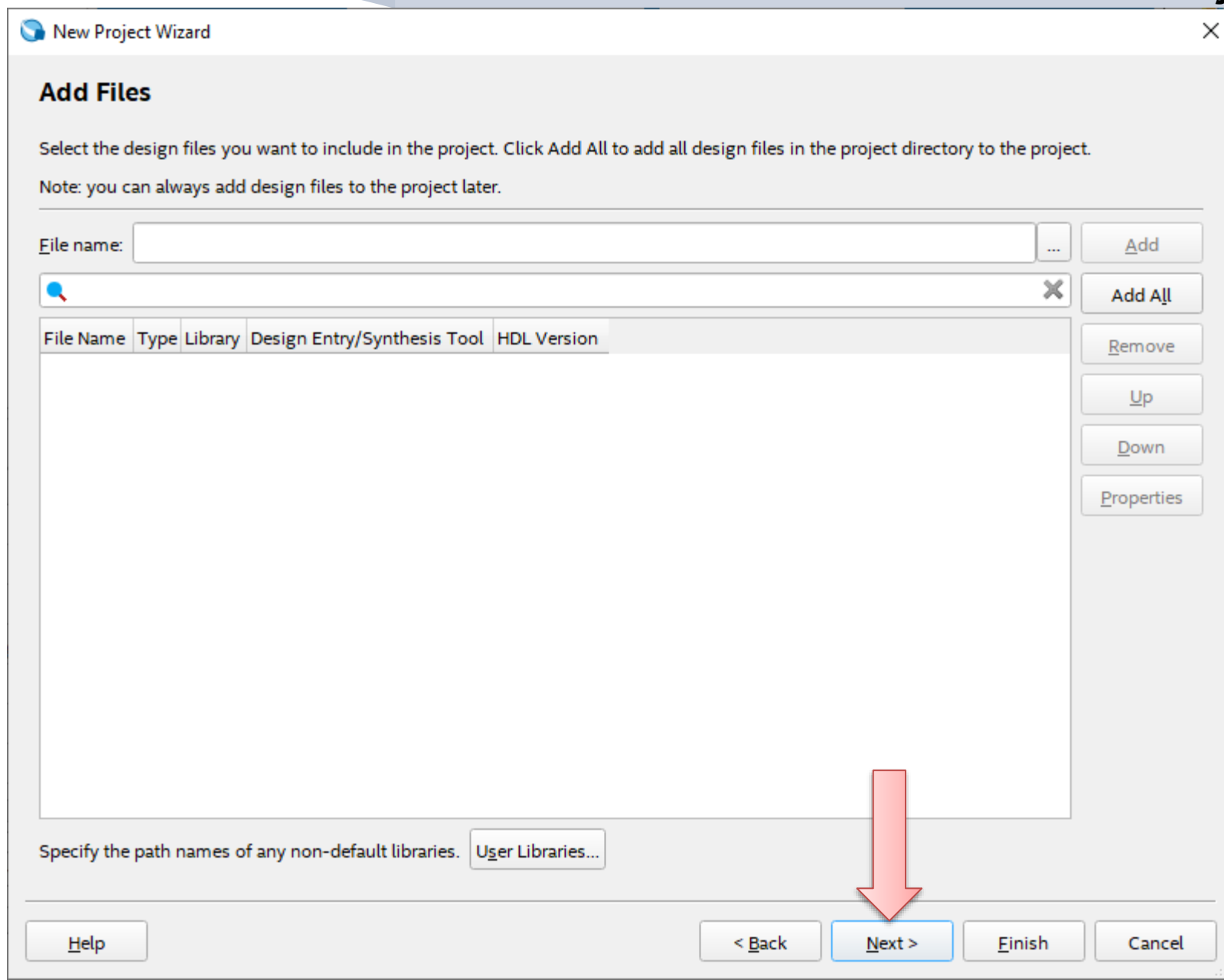
Crie uma pasta com nomes curtos, sem espaços, fora da área de disco do Quartus

Crie um nome para o projeto também contendo nomes curtos e sem caracteres especiais

Project e Entity devem ter o mesmo nome

Help < Back Next > Finish Cancel





New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone IV E

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter: EP4CE115F29C7

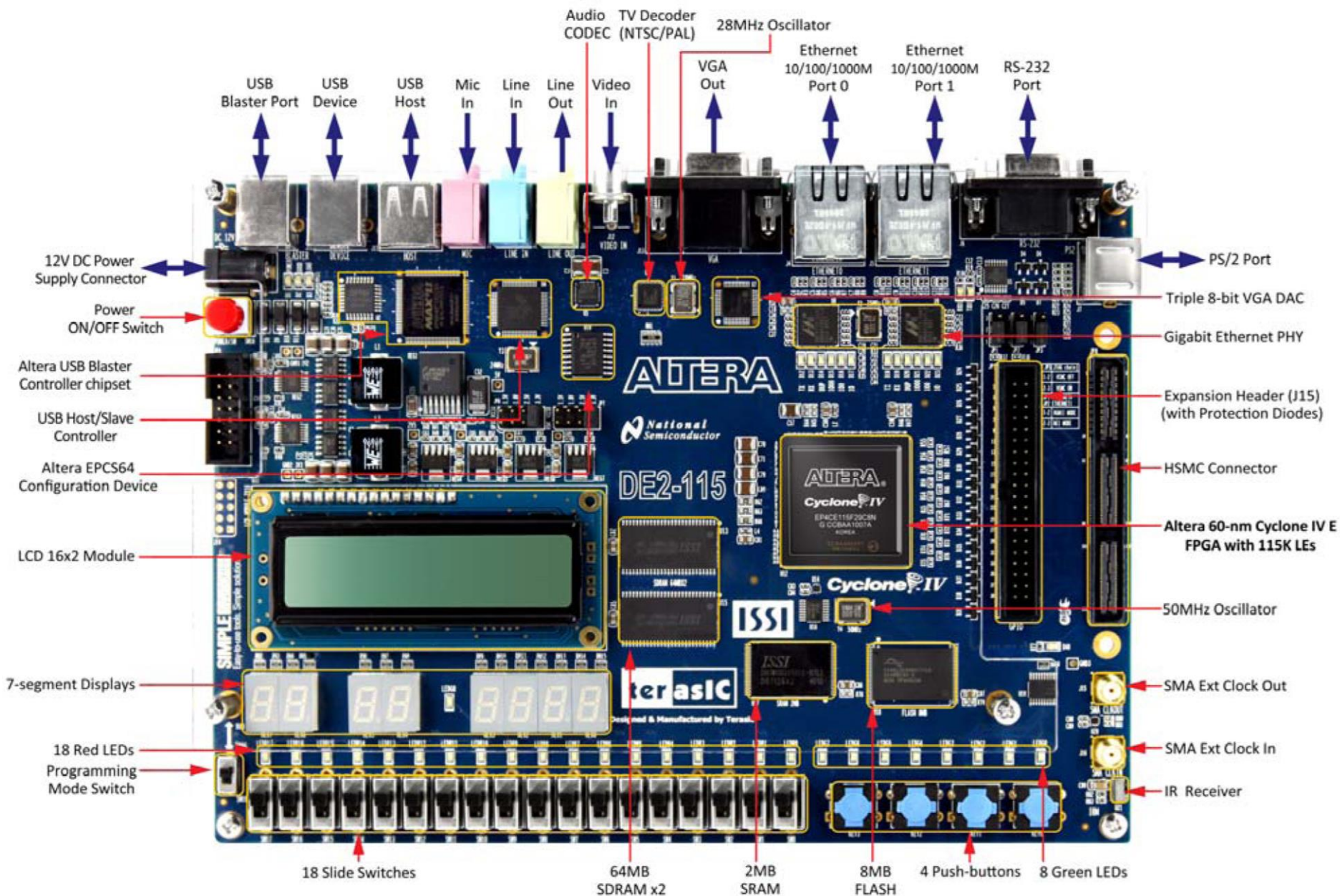
☒ Show advanced devices

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit elements
EP4CE115F29C7	1.2V	114480	529	529	3981312	532

Em Name Filter digite EP4CE115F29C7 para Cyclone IV E

Help < Back Next > Finish Cancel



New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter: 5CEBA4F23C7

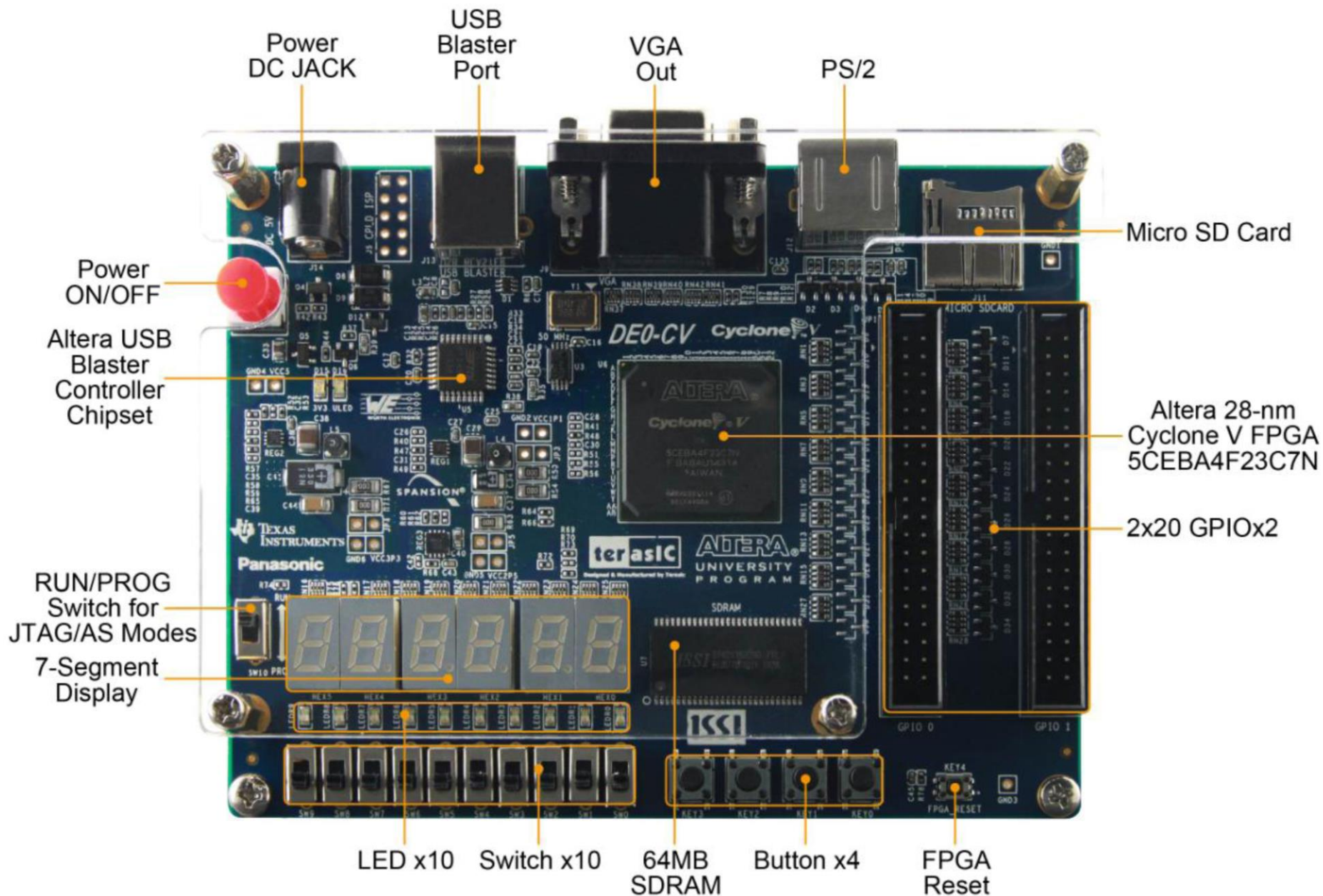
☒ Show advanced devices

Em Name Filter digite 5CEBA4F23C7 para Cyclone V

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	PCIe
5CEBA4F23C7	1.1V	18480	224	224	0	0	0

Help < Back Next > Finish Cancel



New Project Wizard

✕

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

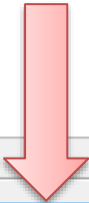
Help

< Back

Next >

Finish

Cancel



New Project Wizard

×

Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:/Users/Danilo/Desktop/ELD
Project name:	PortaAND
Top-level design entity:	PortaAND
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	5CEBA4F23C7
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	ModelSim (VHDL)
Timing analysis:	()
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

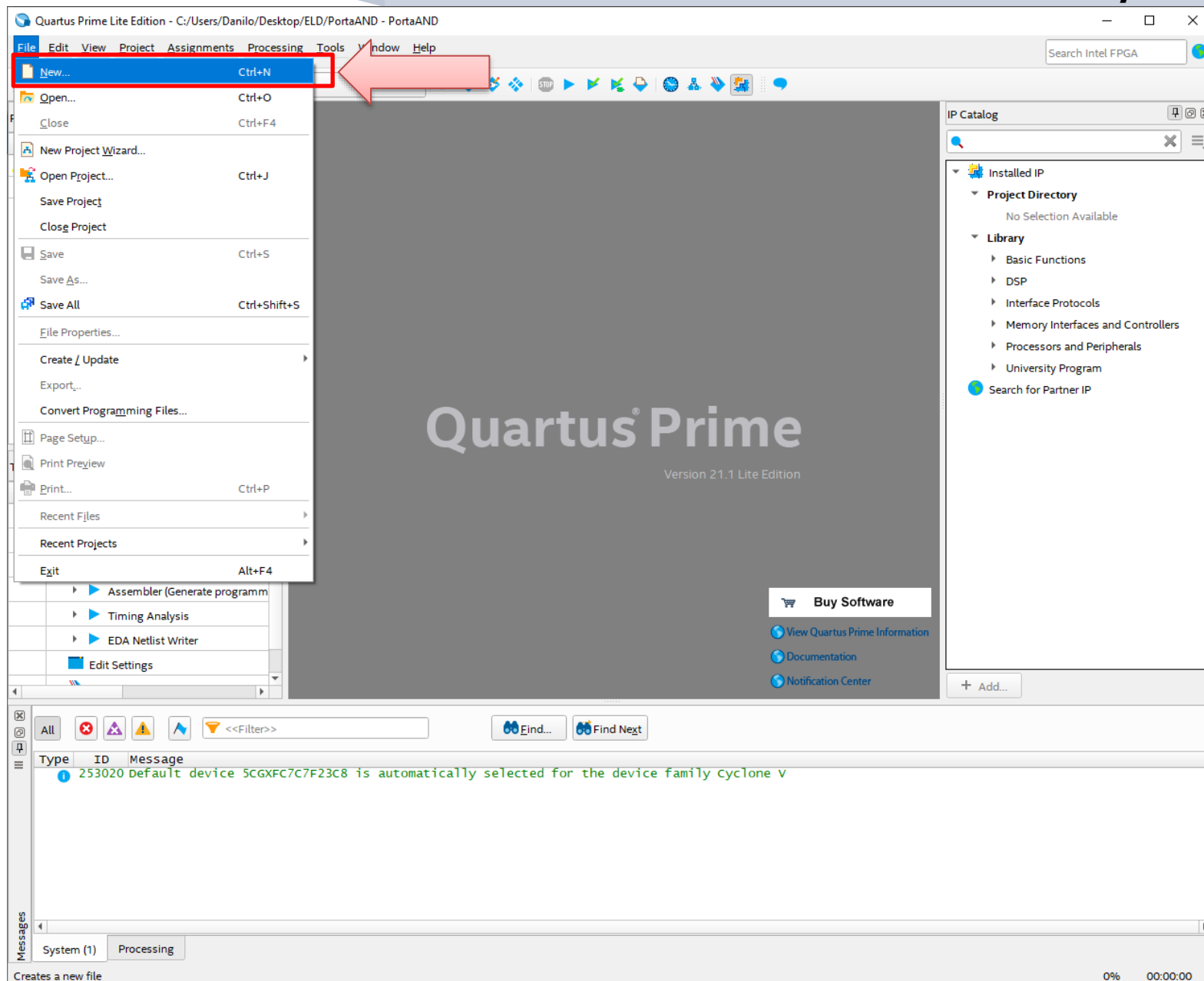
Help

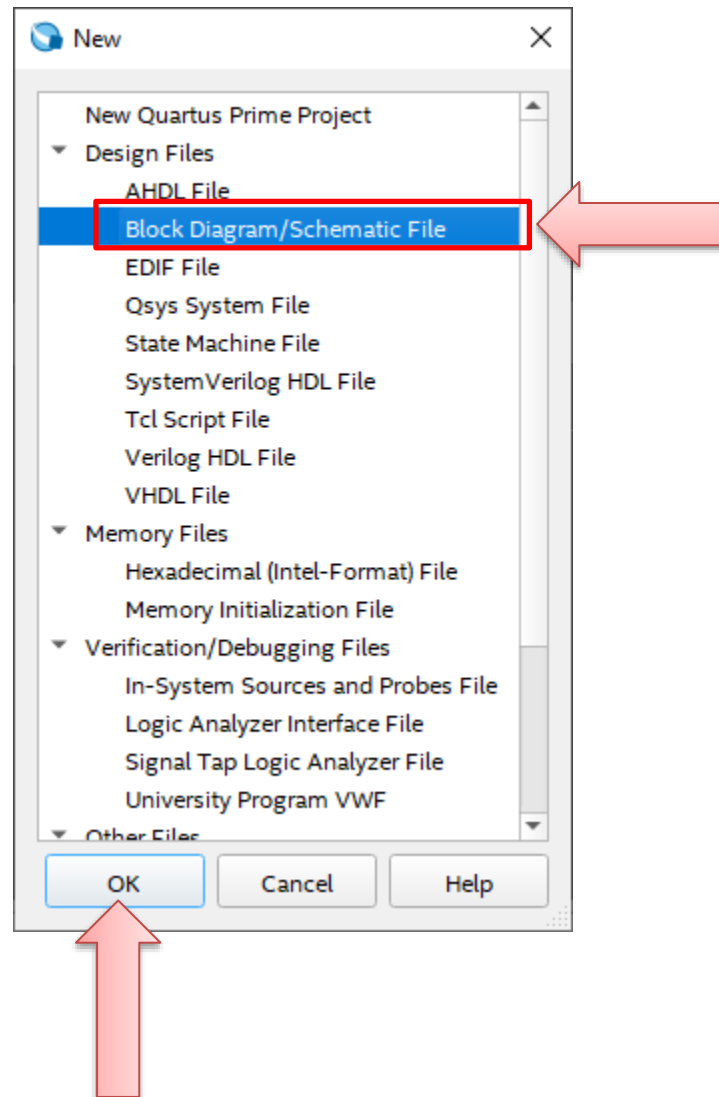
< Back

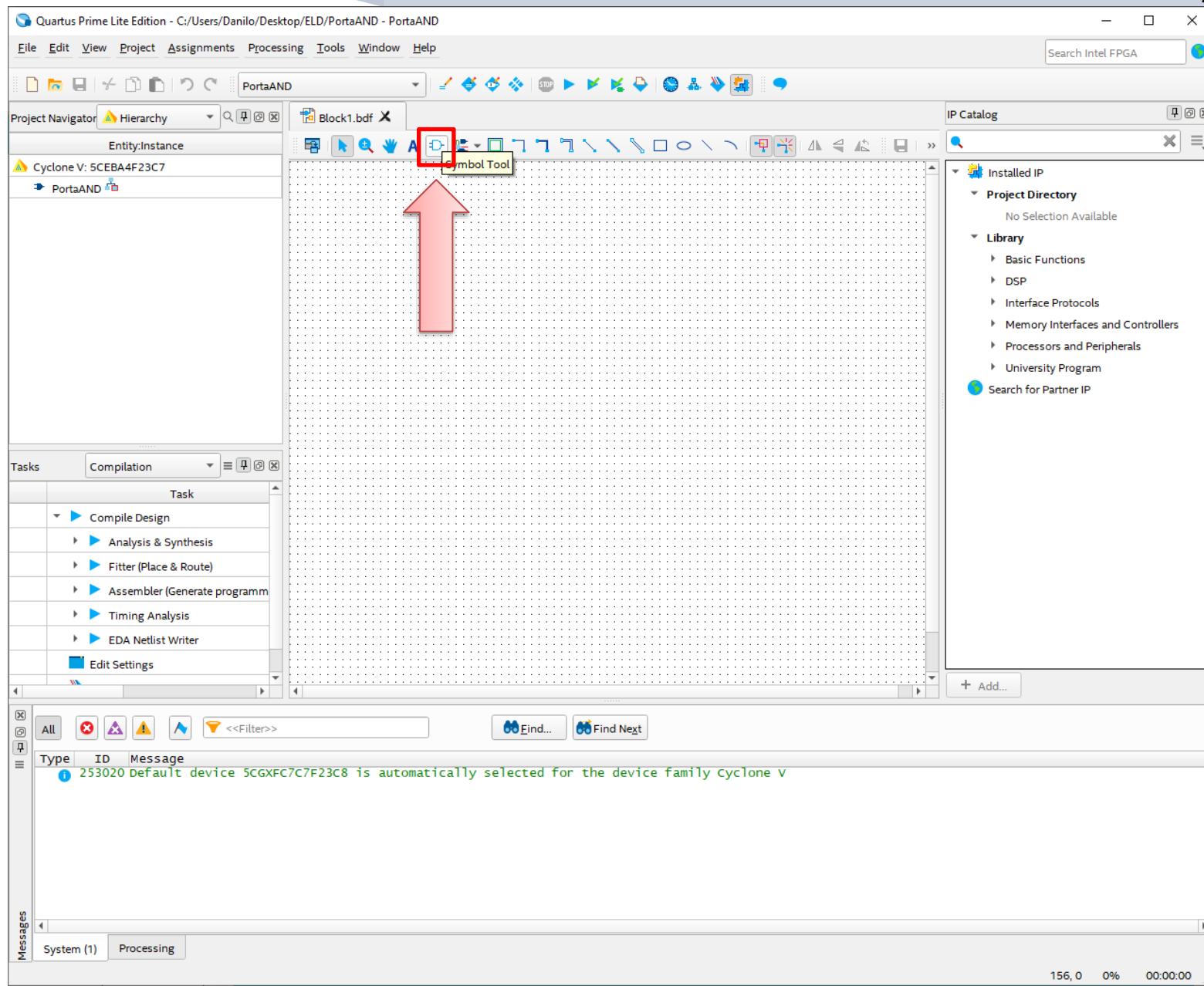
Next >

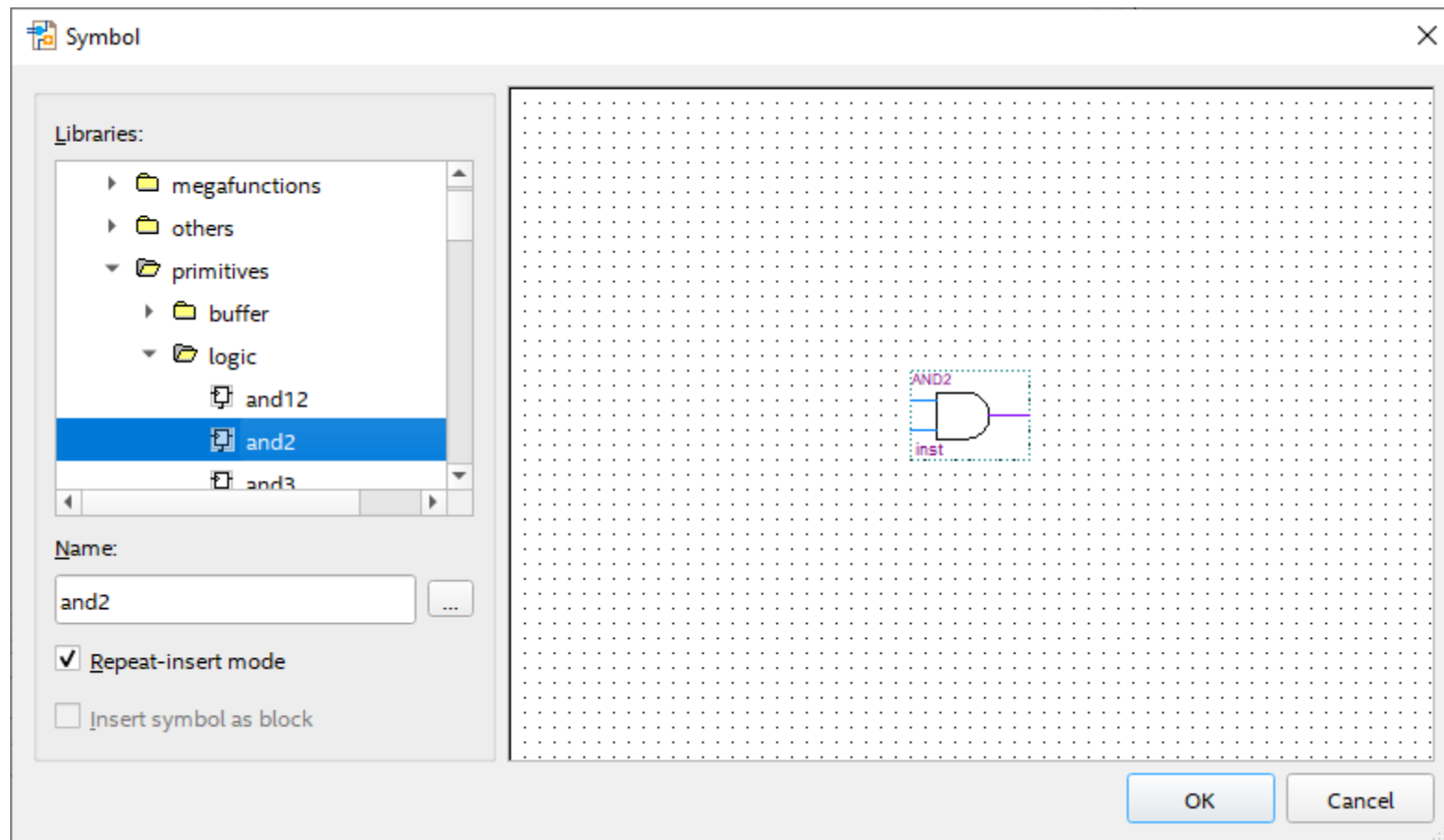
Finish

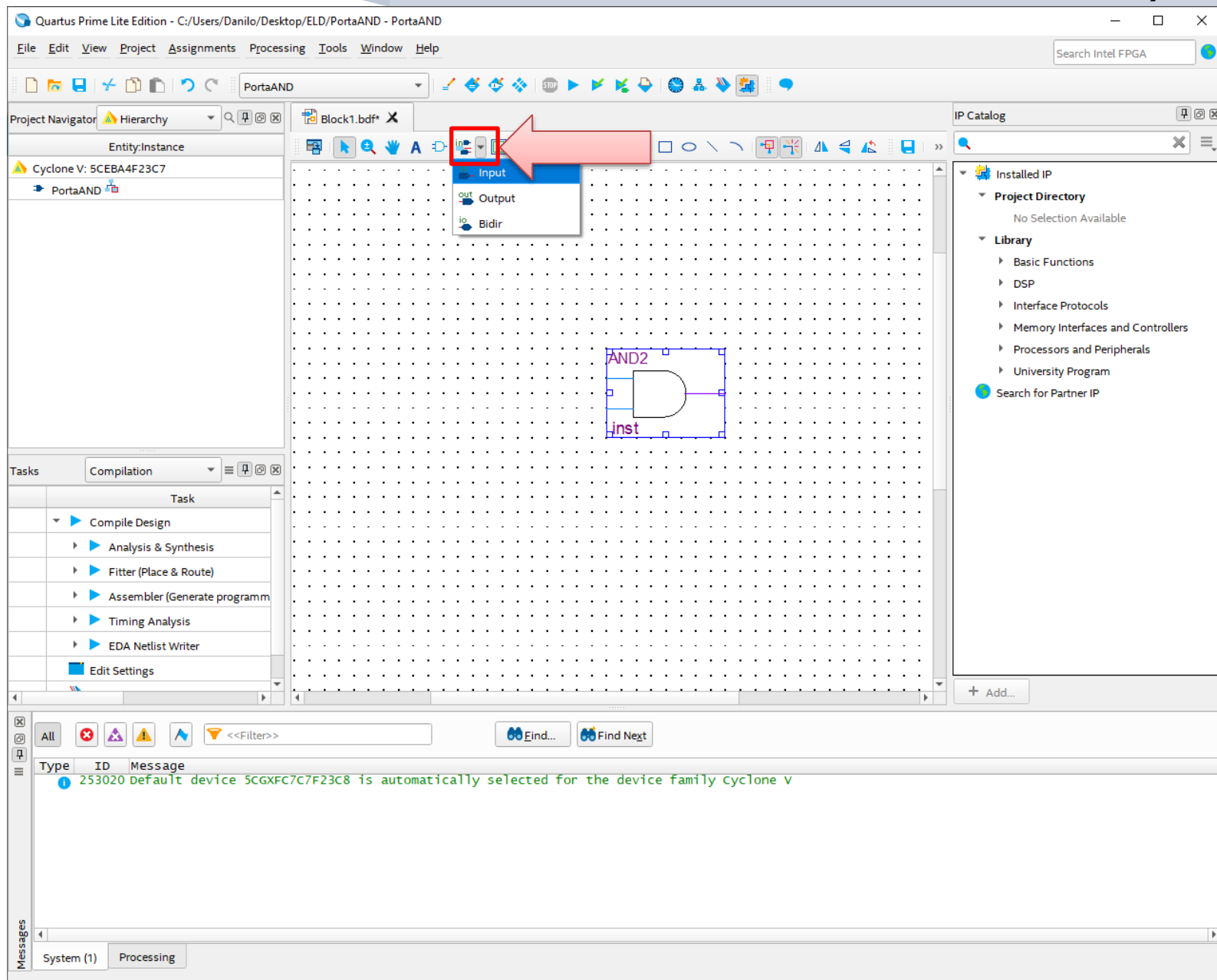
Cancel











Quartus Prime Lite Edition - C:/Users/Danilo/Desktop/ELD/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

Project Navigator Hierarchy

Entity: Instance

Cyclone V: 5CEBA4F23C7

PortaAND

Block1.bdf

Tasks Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate program)
 - Timing Analysis
 - EDA Netlist Writer
 - Edit Settings

Diagram showing an AND gate (AND2) with inputs A and B, and output Y. The inputs are connected to VCC and the output is connected to Y.

IP Catalog

Installed IP

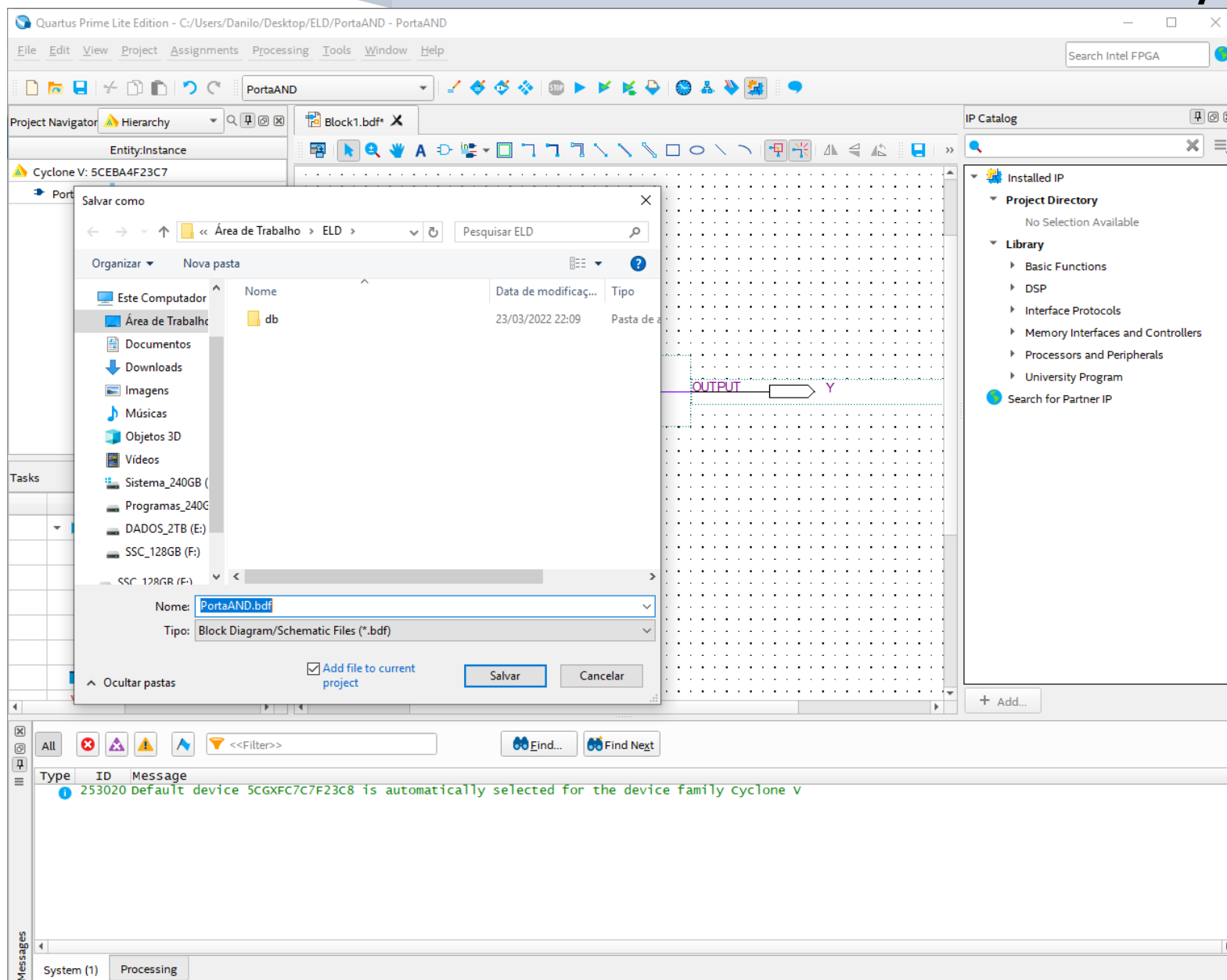
- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

Messages

System (1) Processing

253020 Default device 5CGXC7C7F23C8 is automatically selected for the device family cyclone v

508,93 0% 00:00:00



The screenshot displays the Quartus Prime Lite Edition interface. The main window shows a logic diagram of a 2-input AND gate (AND2) with inputs A and B, and output Y. The gate is labeled 'inst'. The 'Processing' menu is open, and the 'Start Compilation' option is highlighted with a red rectangle and a red arrow. The 'Tasks' pane on the left shows the 'Compilation' task list, including 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate program)', 'Timing Analysis', 'EDA Netlist Writer', and 'Edit Settings'. The 'Messages' pane at the bottom shows a message: '253020 Default device 5CGXFC7C7F23C8 is automatically selected for the device family cyclone v'. The status bar at the bottom indicates 'System (1) Processing' and 'Starts a new compilation'.

Quartus Prime Lite Edition - C:/Users/Danilo/Desktop/ELD/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Stop Processing Ctrl+Shift+C

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

Power Analyzer Tool

SSN Analyzer Tool

Project Navigator Hierarchy

Entity: Instance

Cyclone V: 5CEBA4F23C7

PortaAND

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and Controllers
- Processors and Peripherals
- University Program

Search for Partner IP

Tasks

Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate program)
 - Timing Analysis
 - EDA Netlist Writer
- Edit Settings

Messages

Type ID Message

253020 Default device 5CGXFC7C7F23C8 is automatically selected for the device family cyclone v

System (1) Processing

Starts a new compilation

262,70 0% 00:00:00

Quartus Prime Lite Edition - C:/Users/Danilo/Desktop/ELD/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

PortaAND

Project Navigator Hierarchy

Entity: Instance

Cyclone V: 5CEBA4F23C7

PortaAND

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

Timing Analyzer Summary

Quartus Prime Version Version 21.1.0 Build 842 10/21/2021 SJ Lite Edition

Timing Analyzer Legacy Timing Analyzer

Revision Name PortaAND

Device Family Cyclone V

Device Name 5CEBA4F23C7

Timing Models Final

Delay Model Combined

Rise/Fall Delays Enabled

IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

Messages

All

Find...

Find Next

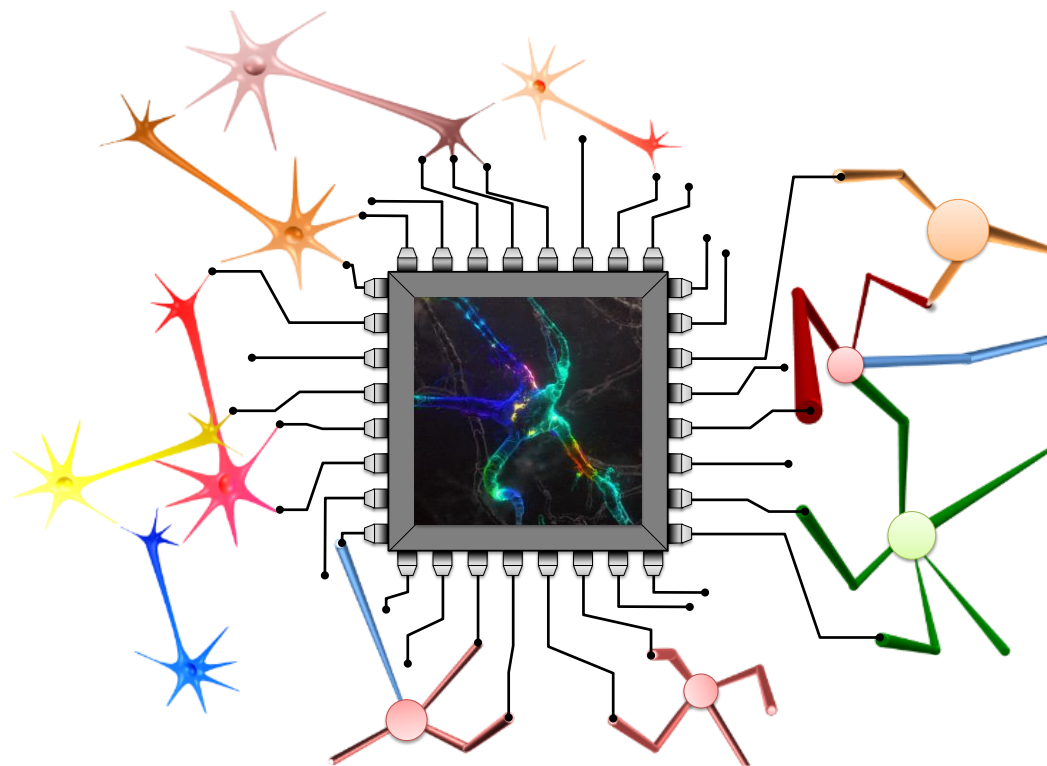
Type ID Message

- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off PortaAND -c PortaAND
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS
- 204019 Generated file PortaAND.vho in folder "C:/Users/Danilo/Desktop/ELD/simulation/modelsim/" for EDA simulation tool
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings

System (1) Processing (131)

241,68 100% 00:00:46

spatti@icmc.usp.br



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