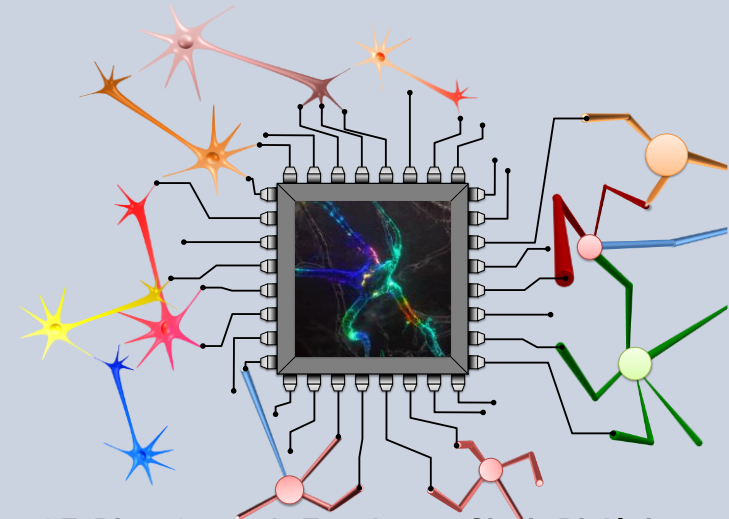


Universidade de São Paulo  
Instituto de Ciências Matemáticas e de Computação  
Departamento de Sistemas de Computação

**SSC108**  
**Prática em Sistemas**  
**Digitais**

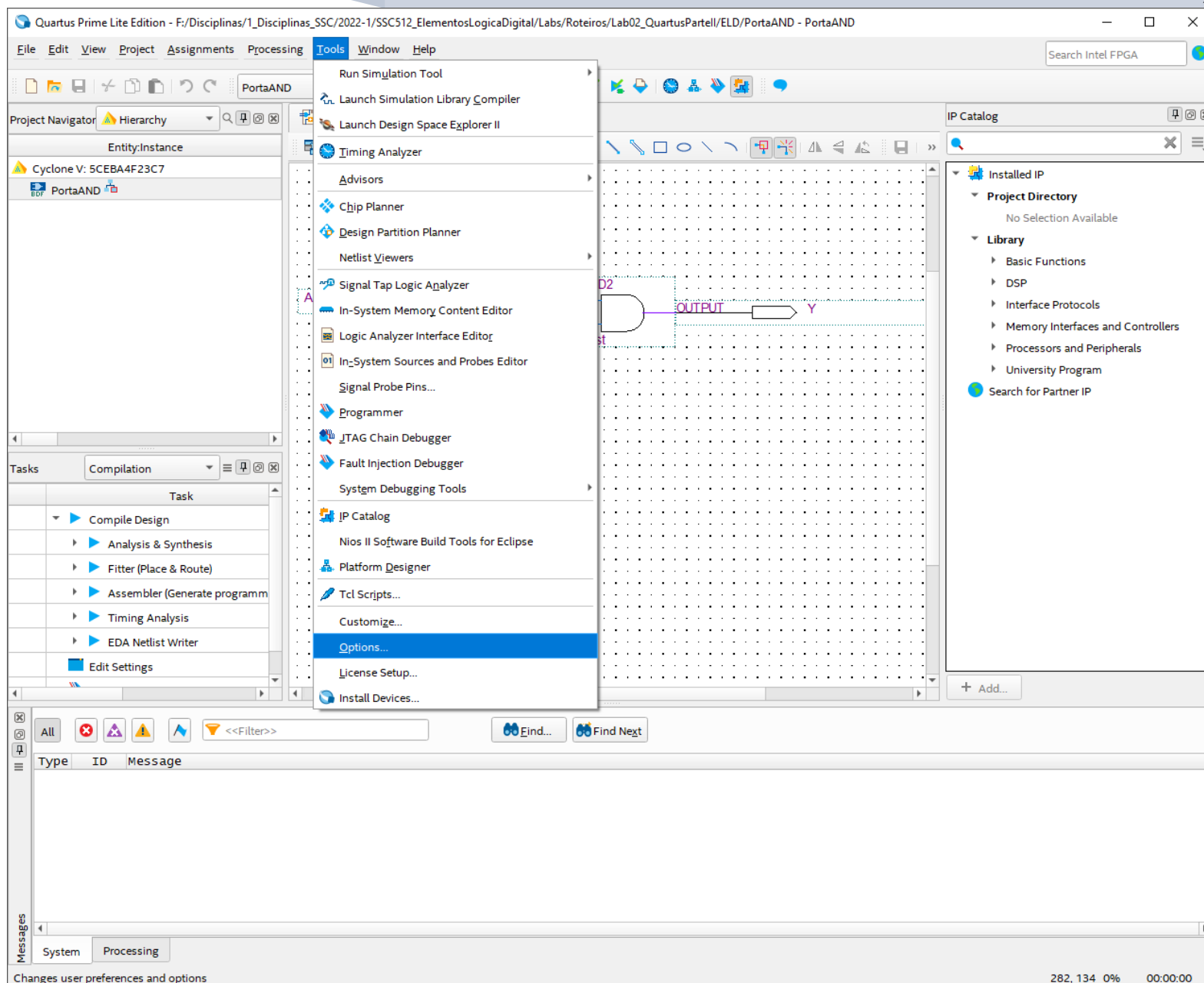
**Tutorial Configuração**  
**Quartus – Parte II**

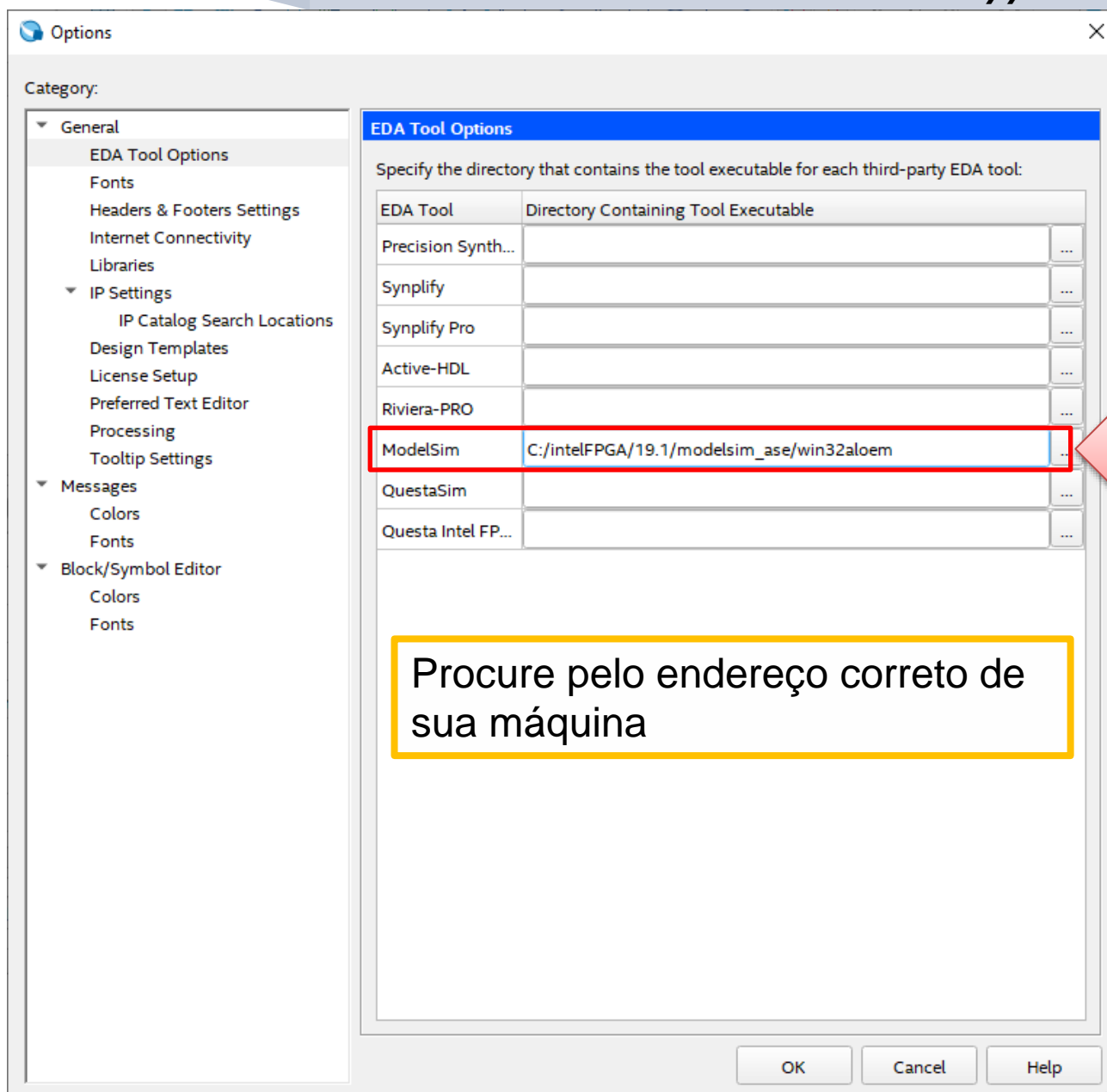


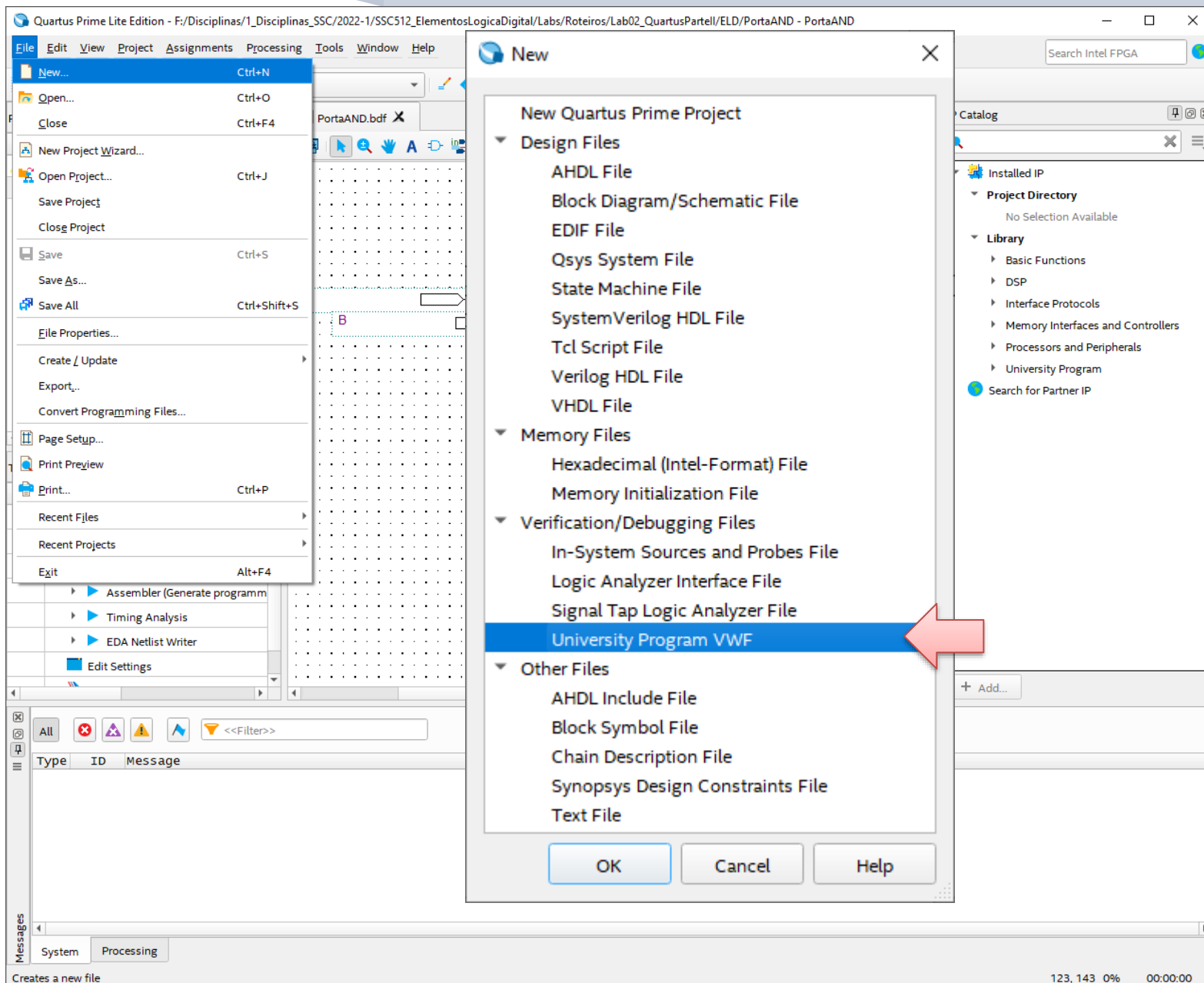
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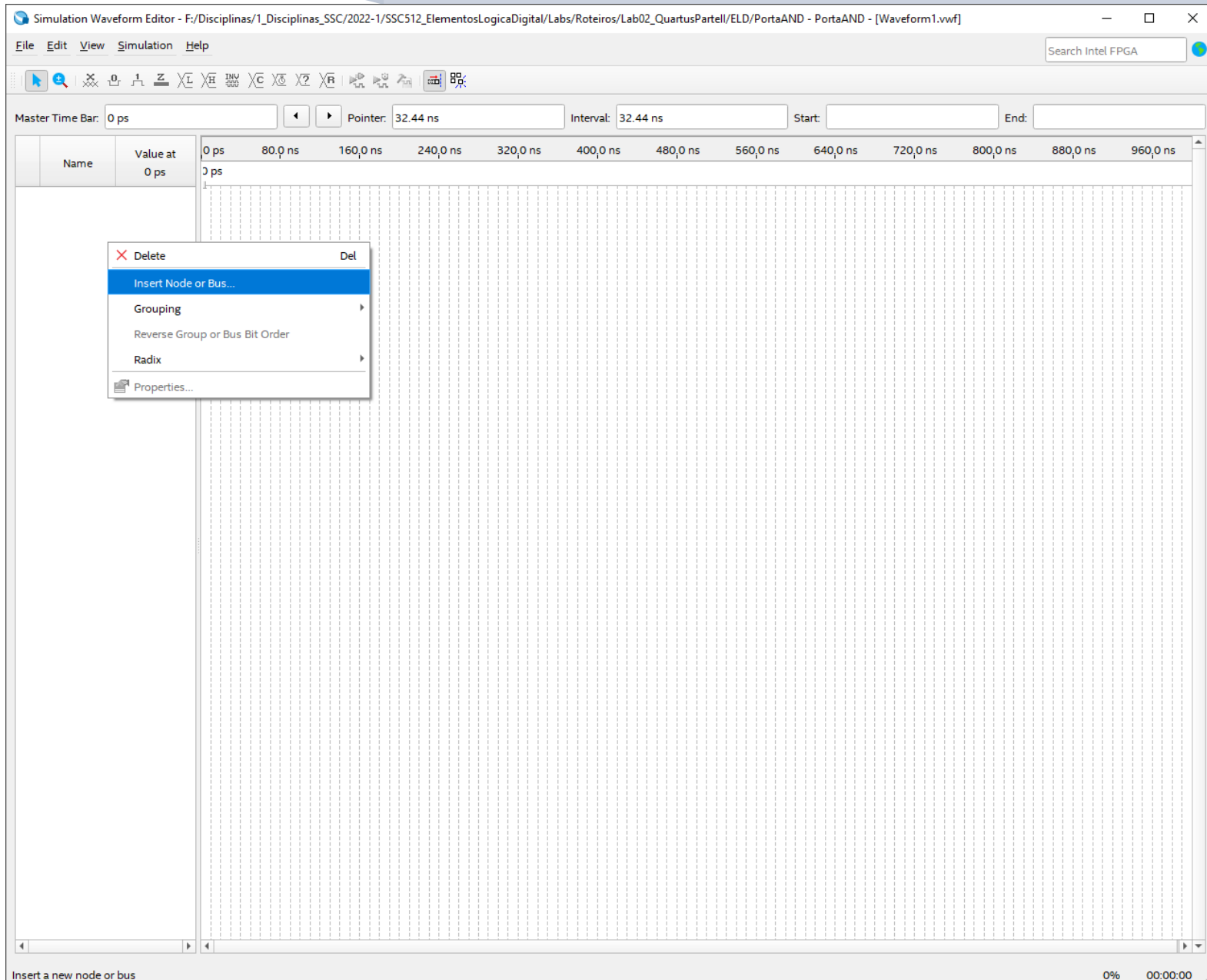
**Prof.Dr. Danilo Spatti**

**São Carlos**









Simulation Waveform Editor - F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/PortaAND - PortaAND - [Waveform1.vwf]

File Edit View Simulation Help

Search Intel FPGA

Master Time Bar: 0 ps Pointer: 430.25 ns Interval: 430.25 ns Start: End:

Name Value at 0 ps

0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns

**Insert Node or Bus**

Name: Use Node Finder t... OK

Type: INPUT Cancel

Value type: 9-Level

Radix: Binary

Bus width: 1

Start in: 0

☐ Display gray code count as binary count

**Node Finder...**

**Node Finder**

Named: \* Filter: Pins: all OK

Look in: \* ... List

Nodes Found:

Name	Type
------	------

Selected Nodes:

Name	Type
------	------

> >> < <<

0% 00:00:00

Simulation Waveform Editor - F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/PortaAND - PortaAND - [Waveform1.vwf]

File Edit View Simulation Help

Search Intel FPGA

Master Time Bar: 0 ps Pointer: 430.25 ns Interval: 430.25 ns Start: End:

0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns

Name Value at 0 ps

Node Finder

Named: \* Filter: Pins: all OK

Look in: \* List Cancel

Nodes Found:

Name	Type
in A	Input
in B	Input
out Y	Output

Selected Nodes:

Name	Type
------	------

> >> < <<

Node Finder

Named: \* Filter: Pins: all OK

Look in: \* List Cancel

Nodes Found:

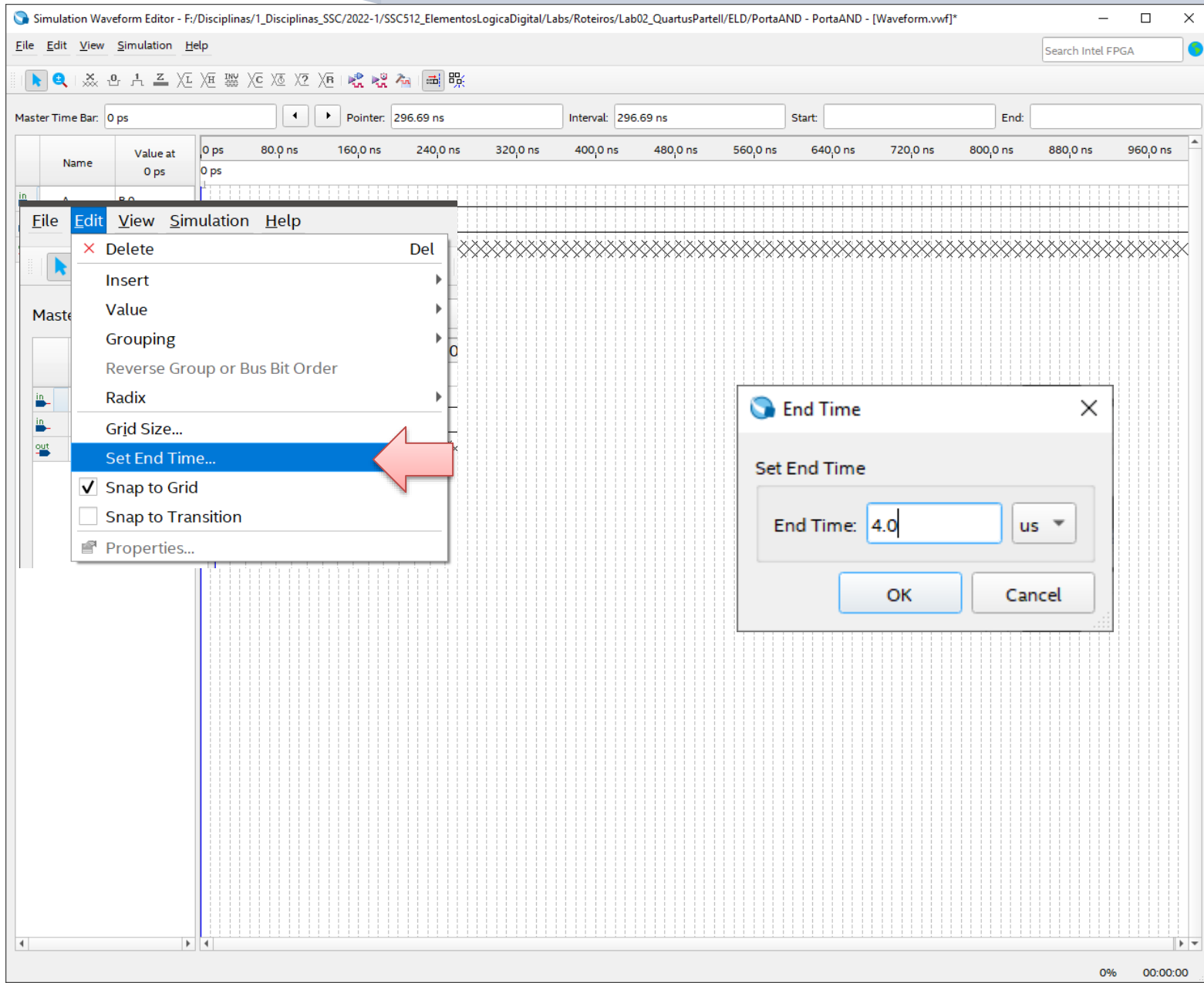
Name	Type
in A	Input
in B	Input
out Y	Output

Selected Nodes:

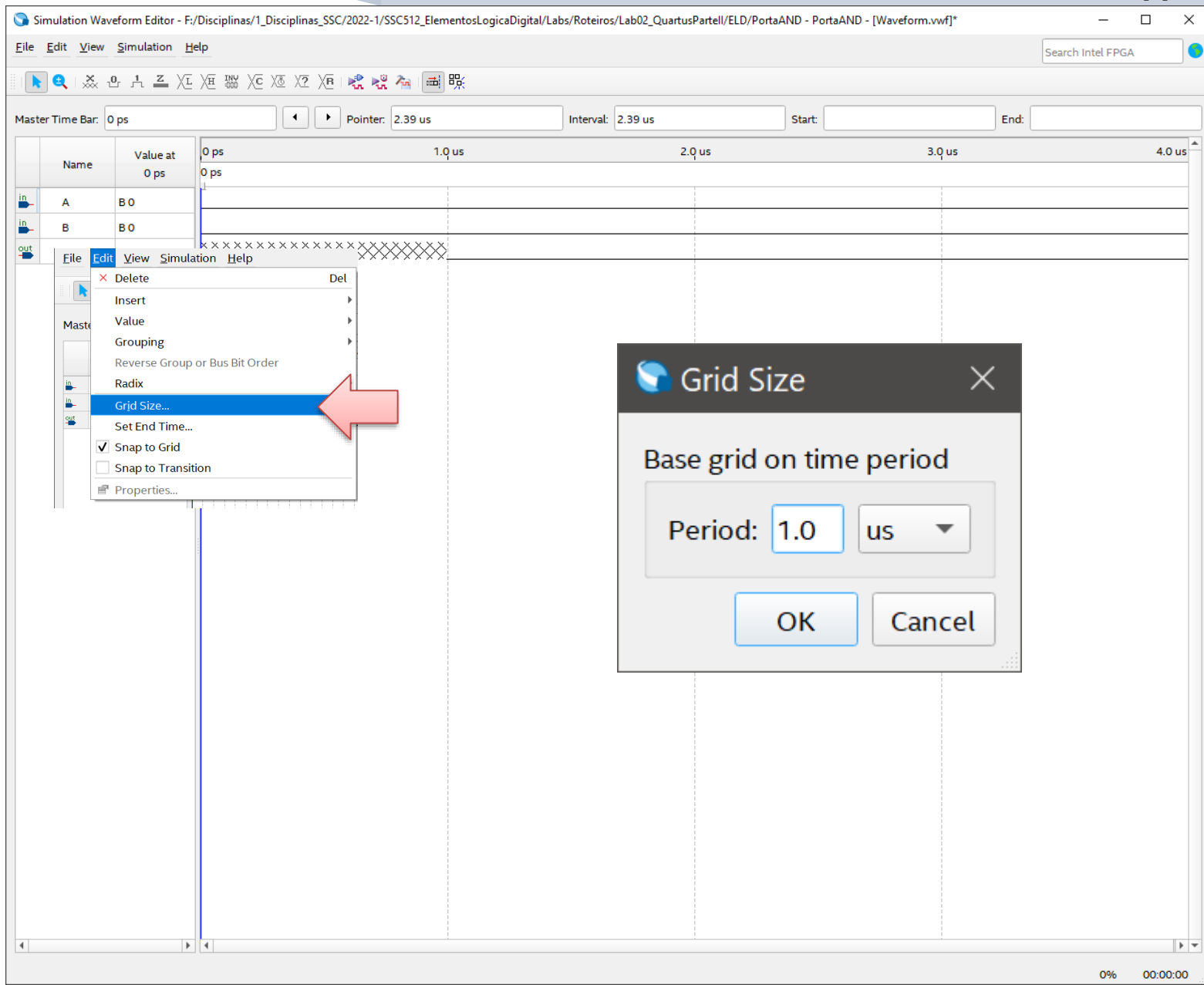
Name	Type
------	------

> >> < <<

0% 00:00:00







The screenshot shows the Simulation Waveform Editor interface. The top toolbar includes an 'Overwrite Clock' button, which is highlighted with a red arrow. Below the toolbar, the 'Master Time Bar' shows a time scale from 0 ps to 4.0 us. A table on the left lists signals A, B, and Y, with their values at 0 ps. Signal A is selected, and a red arrow points to its row. A yellow box contains the text: 'O sinal A tem que estar selecionado para habilitar a barra de ferramentas'. The 'Clock' dialog box is open, showing the 'Base waveform on time period' settings: Period: 1.0 us, Offset: 0.0 us, and Duty cycle (%): 50. The 'OK' button is highlighted.

Name	Value at 0 ps
A	B 0
B	B 0
Y	X

O sinal A tem que estar selecionado para habilitar a barra de ferramentas

Overwrite Clock

Base waveform on time period

Period: 1.0 us

Offset: 0.0 us

Duty cycle (%): 50

OK Cancel

Simulation Waveform Editor - F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/PortaAND - PortaAND - [Waveform.vwf]\*

File Edit View Simulation Help

Search Intel FPGA

Master Time Bar: 0 ps Pointer: 854.78 ns Interval: 854.78 ns Start: 0 ps End: 4.0 us

	Name	Value at 0 ps
in	A	B 0
in	B	B 0
out	Y	B X

O sinal B tem que estar selecionado para habilitar a barra de ferramentas

Clock

Base waveform on time period

Period: 2 us

Offset: 0.0 us

Duty cycle (%): 50

OK Cancel

0% 00:00:00

Simulation Waveform Editor - F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/PortaAND - PortaAND - [Waveform.vwf]\*

File Edit View Simulation Help

Search Intel FPGA

Master Time Bar: 0 ps

Run Functional Simulation

Interval: 3.95 us

Start: 0 ps

End: 0 ps

	Name	Value at 0 ps
In	A	B 0
In	B	B 0
Out	Y	B X

Simulation Flow Progress

Generating netlist...

2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/Waveform.vwf --  
testbench\_file=F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/SSC512\_ElementosLogicaDigital/Labs/Roteiros/  
Lab02\_QuartusPartell/ELD/simulation/qsim/Waveform.vwf.vt

Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

**Completed successfully.**

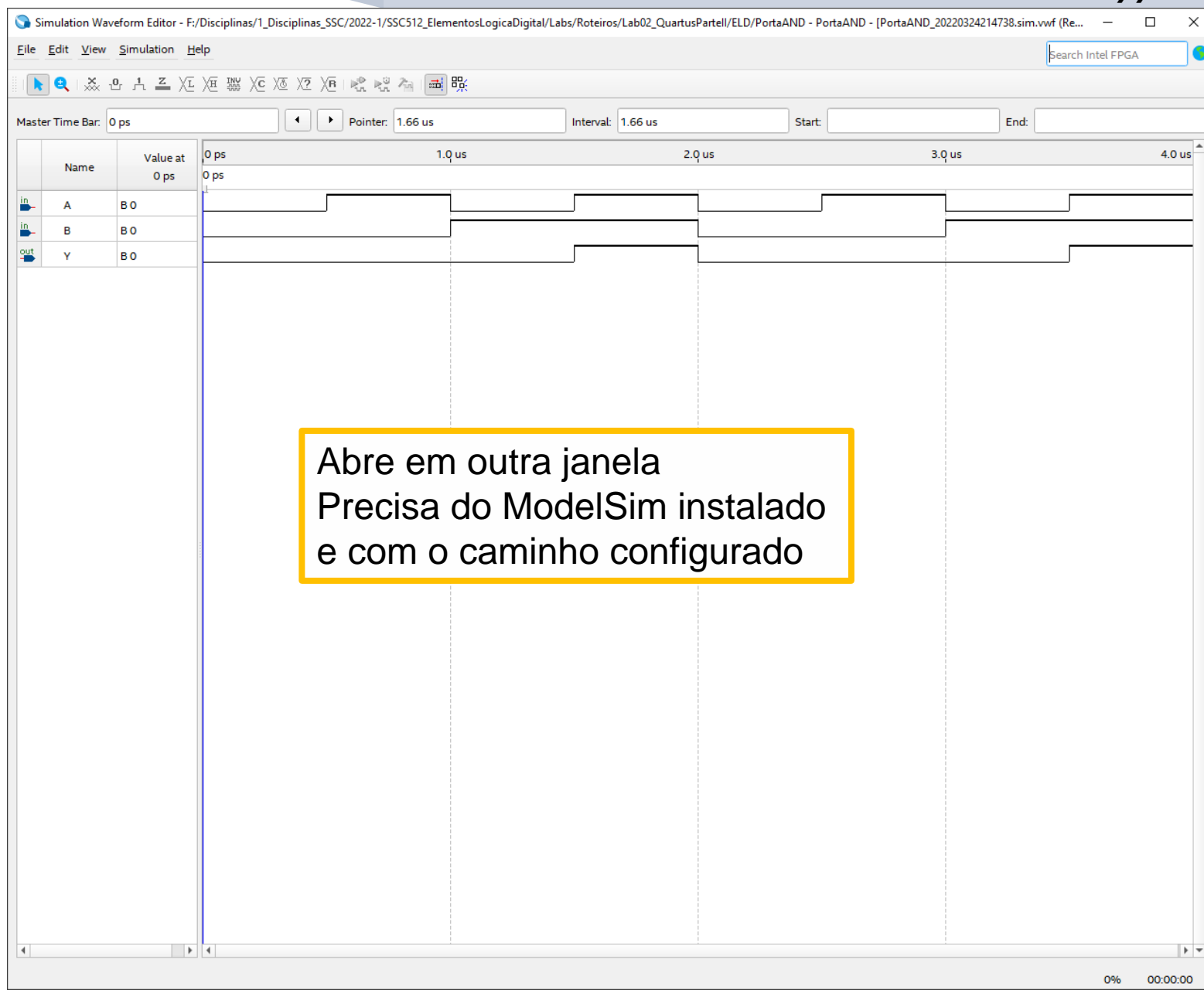
**Completed successfully.**

\*\*\*\* Generating the functional simulation netlist \*\*\*\*

quartus\_eda --write\_settings\_files=off --simulation --functional=on --flatten\_buses=off --  
tool=modelsim\_oem --format=verilog --output\_directory="F:/Disciplinas/1\_Disciplinas\_SSC/2022-1/  
SSC512\_ElementosLogicaDigital/Labs/Roteiros/Lab02\_QuartusPartell/ELD/simulation/qsim/"  
PortaAND -c PortaAND

Run a functional simulation

0% 00:00:00



Simulation Waveform Editor - C:/Users/.../Desktop/Teste/teste - teste - [Waveform1.vwf]

File Edit View Simulation Help

Master Time Bar: 0 ps Count Value Pointer: 671.7 ns Interval: 671.7 ns Start: 0 ps End: 16.0 us

Name	Value at 0 ps
CLK	B 0
CLR_reg	B 1
DataIn	B 0000
DataOut	B XXXX

0 ps 1.0 us 2.0 us 3.0 us 4.0 us 5.0 us 6.0 us 7.0 us 8.0 us 9.0 us 10.0 us 11.0 us 12.0 us 13.0 us 14.0 us 15.0 us 16.0 us

0 ps

0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111

XXXX 0000

Para barramentos, utilize Count Value

Count Value

Radix: Binary

Start value: 0000

Increment by: 1

Count type

☒ Binary

☐ Gray code

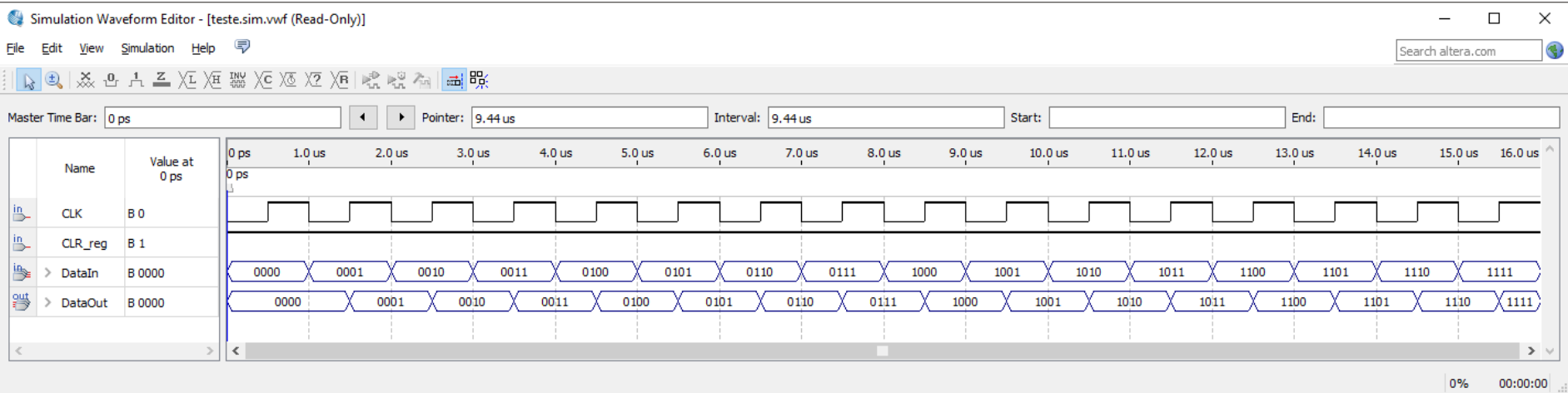
Transitions occur

Count every: 1.0 us

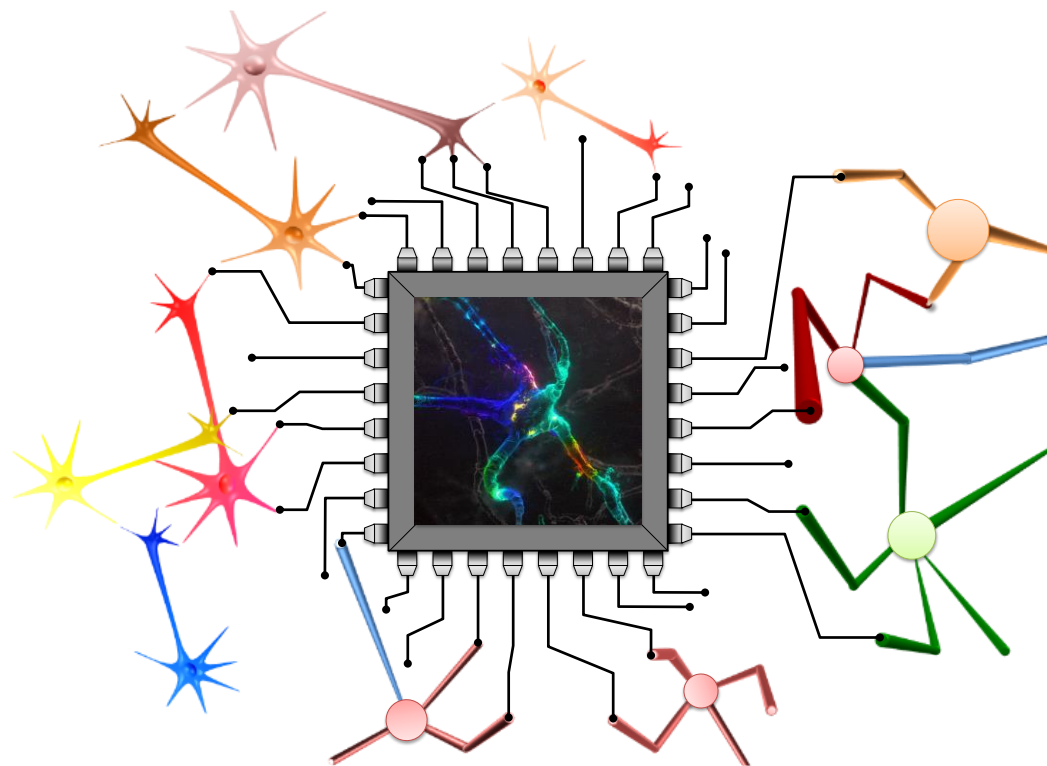
OK Cancel

Overwrite Count Value

0% 00:00:00



spatti@icmc.usp.br



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