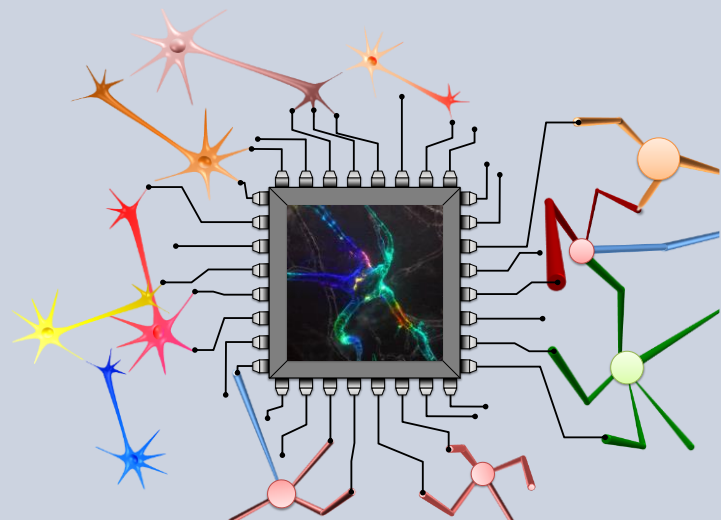


Universidade de São Paulo  
Instituto de Ciências Matemáticas e de Computação  
Departamento de Sistemas de Computação

**SSC108**  
**Prática em Sistemas**  
**Digitais**

**Tutorial Configuração**  
**Quartus – Parte III**



GE4Bio – Grupo de Estudos em Sinais Biológicos

**Prof.Dr. Danilo Spatti**

**São Carlos**


The screenshot displays the Quartus II software interface. The 'Assignments' menu is open, and the 'Pin Planner' option is highlighted with a red box and a red arrow. The 'Flow Summary' window is also open, showing the results of a successful compilation. The 'Tasks' pane on the left shows the compilation process, including 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming file)', 'TimeQuest Timing Analysis', 'EDA Netlist Writer', and 'Program Device (Open Programmer)'. The 'IP Catalog' pane on the right shows the installed IP and project directory.

**Flow Summary**

Item	Value
Successful - Mon Mar 12 16:08:59 2018	
Quartus Version	14.1.0 Build 186 12/03/2014 SJ Web Edition
Revision Name	PortaAND
Top-level Entity Name	PortaAND
Family	Cyclone V
Device	5CEBA4F23C7
Timing Models	Final
Logic utilization (in ALMs)	1 / 18,480 (< 1 %)
Total registers	0
Total pins	3 / 224 (1 %)
Total virtual pins	0
Total block memory bits	0 / 3,153,920 (0 %)
Total DSP Blocks	0 / 66 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 4 (0 %)
Total DLLs	0 / 4 (0 %)

Após a 1ª compilação é possível escolher os pinos que serão utilizados na FPGA

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


Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	per Analog Settings	_GXB/VCCT_G
 A	Input	PIN_U13	4A	B4A_N0	PIN_I_17	2.5 V (default)		12mA (default)				
 B	Input	PIN_V13	4A	B4A_N0	PIN_K17	2.5 V (default)		12mA (default)				
 Y	Output	PIN_AA2	2A	B2A_N0	PIN_M21	2.5 V (default)		12mA (default)	1 (default)			
<<new node>>												

Table 3-2 Pin Assignment of Push-buttons

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>
KEY0	PIN_U7	Push-button[0]
KEY1	PIN_W9	Push-button[1]
KEY2	PIN_M7	Push-button[2]
KEY3	PIN_M6	Push-button[3]
RESET_N	PIN_P22	Push-button which connected to DEV_CLRN Pin of FPGA

Table 3-3 Pin Assignment of Slide Switches

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]

Table 4-1 Pin Assignments for Slide Switches

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
SW[0]	PIN_AB28	Slide Switch[0]	Depending on JP7
SW[1]	PIN_AC28	Slide Switch[1]	Depending on JP7
SW[2]	PIN_AC27	Slide Switch[2]	Depending on JP7
SW[3]	PIN_AD27	Slide Switch[3]	Depending on JP7
SW[4]	PIN_AB27	Slide Switch[4]	Depending on JP7
SW[5]	PIN_AC26	Slide Switch[5]	Depending on JP7
SW[6]	PIN_AD26	Slide Switch[6]	Depending on JP7
SW[7]	PIN_AB26	Slide Switch[7]	Depending on JP7
SW[8]	PIN_AC25	Slide Switch[8]	Depending on JP7
SW[9]	PIN_AB25	Slide Switch[9]	Depending on JP7
SW[10]	PIN_AC24	Slide Switch[10]	Depending on JP7
SW[11]	PIN_AB24	Slide Switch[11]	Depending on JP7
SW[12]	PIN_AB23	Slide Switch[12]	Depending on JP7
SW[13]	PIN_AA24	Slide Switch[13]	Depending on JP7
SW[14]	PIN_AA23	Slide Switch[14]	Depending on JP7
SW[15]	PIN_AA22	Slide Switch[15]	Depending on JP7
SW[16]	PIN_Y24	Slide Switch[16]	Depending on JP7
SW[17]	PIN_Y23	Slide Switch[17]	Depending on JP7

Table 4-2 Pin Assignments for Push-buttons

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
KEY[0]	PIN_M23	Push-button[0]	Depending on JP7
KEY[1]	PIN_M21	Push-button[1]	Depending on JP7
KEY[2]	PIN_N21	Push-button[2]	Depending on JP7
KEY[3]	PIN_R24	Push-button[3]	Depending on JP7

Table 3-4 Pin Assignment of LEDs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>
LEDR0	PIN_AA2	LED [0]
LEDR1	PIN_AA1	LED [1]
LEDR2	PIN_W2	LED [2]
LEDR3	PIN_Y3	LED [3]
LEDR4	PIN_N2	LED [4]
LEDR5	PIN_N1	LED [5]
LEDR6	PIN_U2	LED [6]
LEDR7	PIN_U1	LED [7]
LEDR8	PIN_L2	LED [8]
LEDR9	PIN_L1	LED [9]

Table 4-3 Pin Assignments for LEDs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
LEDR[0]	PIN_G19	LED Red[0]	2.5V
LEDR[1]	PIN_F19	LED Red[1]	2.5V
LEDR[2]	PIN_E19	LED Red[2]	2.5V
LEDR[3]	PIN_F21	LED Red[3]	2.5V
LEDR[4]	PIN_F18	LED Red[4]	2.5V
LEDR[5]	PIN_E18	LED Red[5]	2.5V
LEDR[6]	PIN_J19	LED Red[6]	2.5V
LEDR[7]	PIN_H19	LED Red[7]	2.5V
LEDR[8]	PIN_J17	LED Red[8]	2.5V
LEDR[9]	PIN_G17	LED Red[9]	2.5V
LEDR[10]	PIN_J15	LED Red[10]	2.5V
LEDR[11]	PIN_H16	LED Red[11]	2.5V
LEDR[12]	PIN_J16	LED Red[12]	2.5V
LEDR[13]	PIN_H17	LED Red[13]	2.5V
LEDR[14]	PIN_F15	LED Red[14]	2.5V

The screenshot displays the Quartus II software interface. The 'Project Navigator' on the left shows the 'PortaAND.bdf' project. A red box highlights the 'Device...' menu option, which is also highlighted by a red arrow. The 'Table of Contents' pane shows the 'Flow Summary' selected. The 'Flow Summary' pane displays the following information:

Flow Summary	
Flow Status	Successful - Mon Mar 12 16:08:59 2018
Quartus II 64-Bit Version	14.1.0 Build 186 12/03/2014 SJ Web Edition
Revision Name	PortaAND
Top-level Entity Name	PortaAND
Family	Cyclone V
Device	5CEBA4F23C7
Timing Models	Final
Logic utilization (in ALMs)	1 / 18,480 ( < 1 % )
Total registers	0
Total pins	3 / 224 ( 1 % )
Total virtual pins	0
Total block memory bits	0 / 3,153,920 ( 0 % )
Total DSP Blocks	0 / 66 ( 0 % )
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 4 ( 0 % )
Total DLLs	0 / 4 ( 0 % )

The 'Tasks' pane at the bottom left shows the 'Compile Design' task selected. The 'IP Catalog' pane on the right shows the 'Project Directory' and 'Library' sections.



Device (Não está respondendo) ✕

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST) ▾

Devices: All ▾

Show in 'Available devices' list

Package: Any ▾

Pin count: Any ▾

Core Speed grade: Any ▾

Name filter:

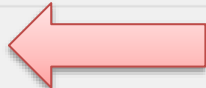
☒ Show advanced devices

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

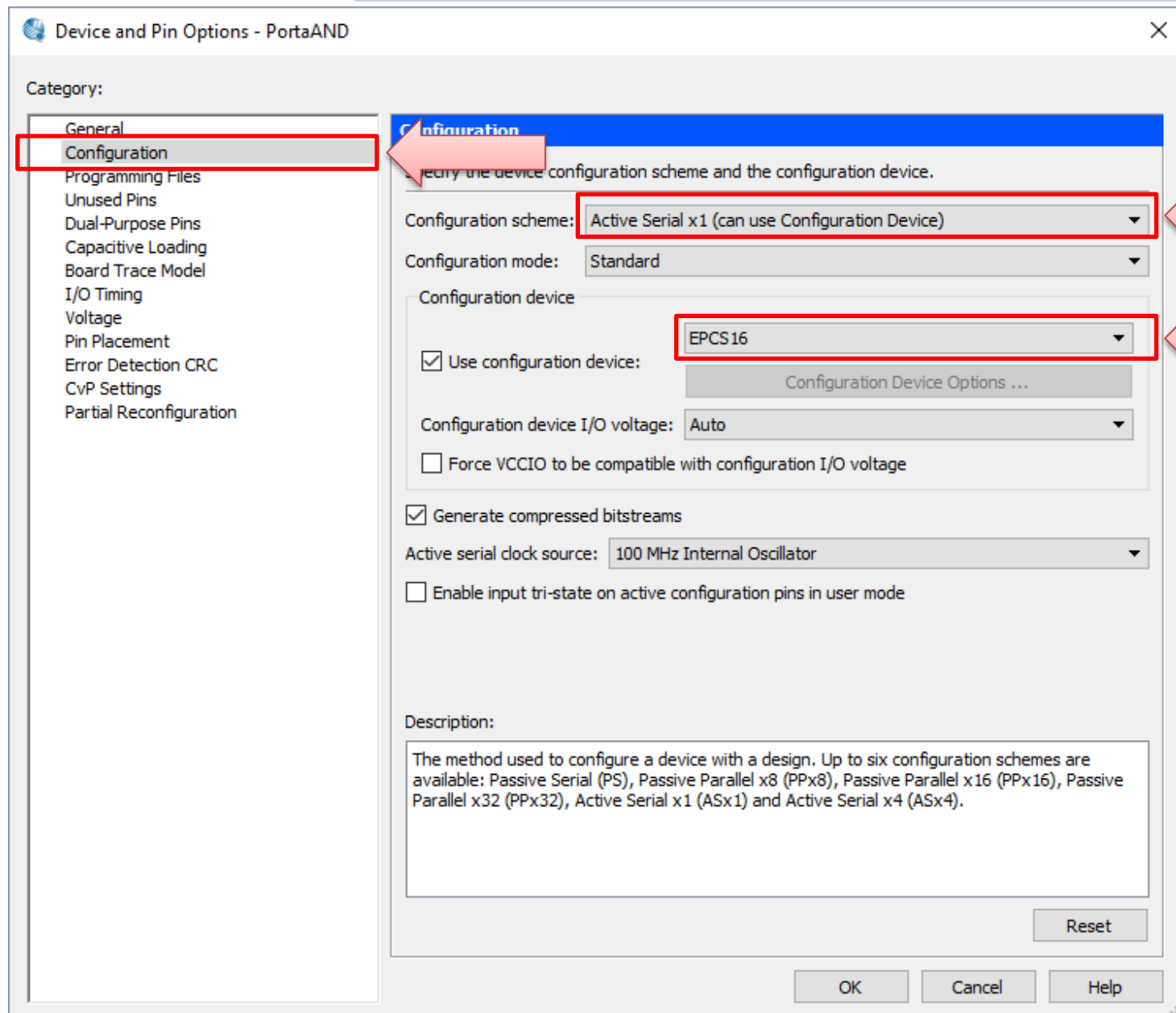
Device and Pin Options... 

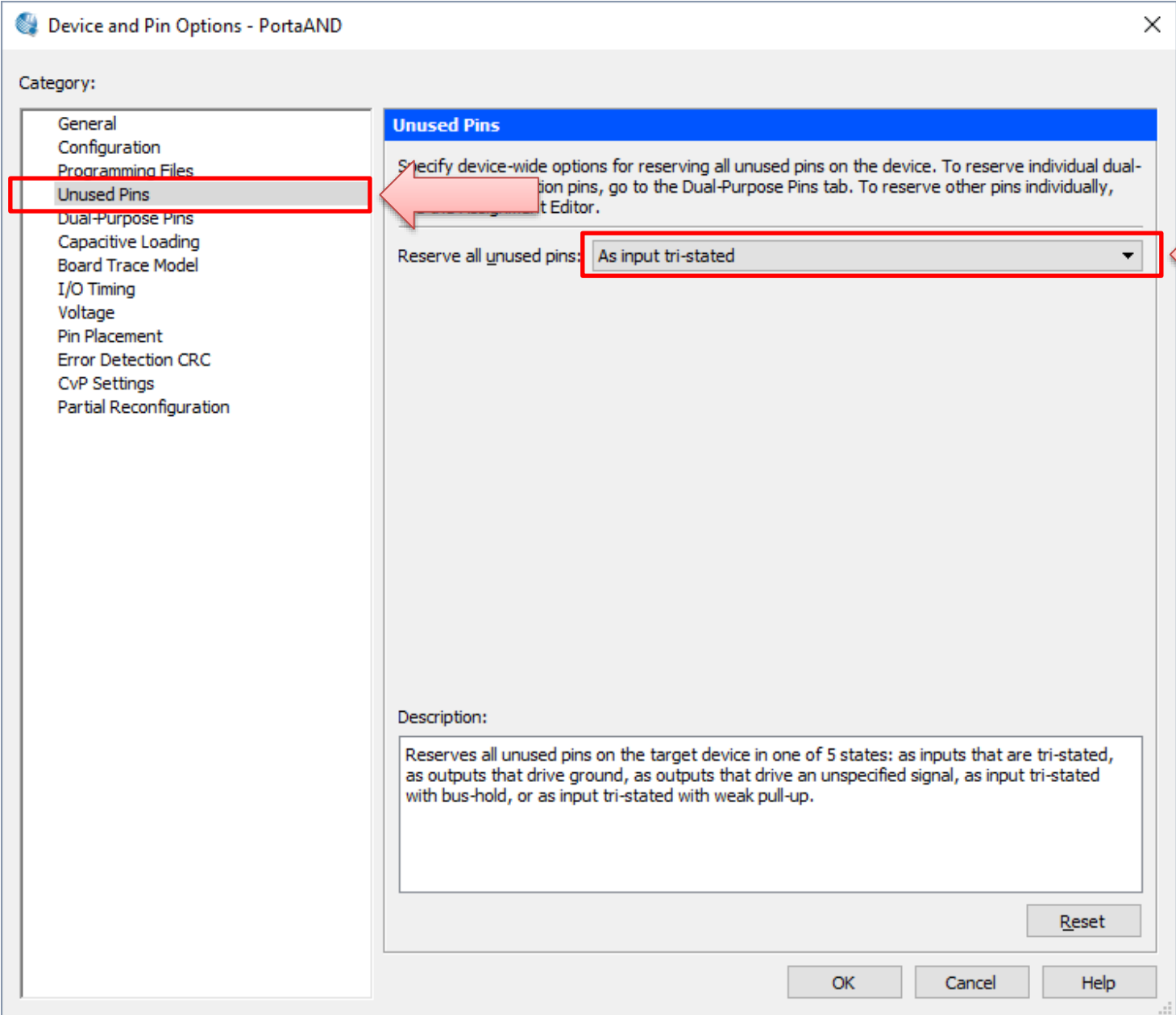
Available devices:

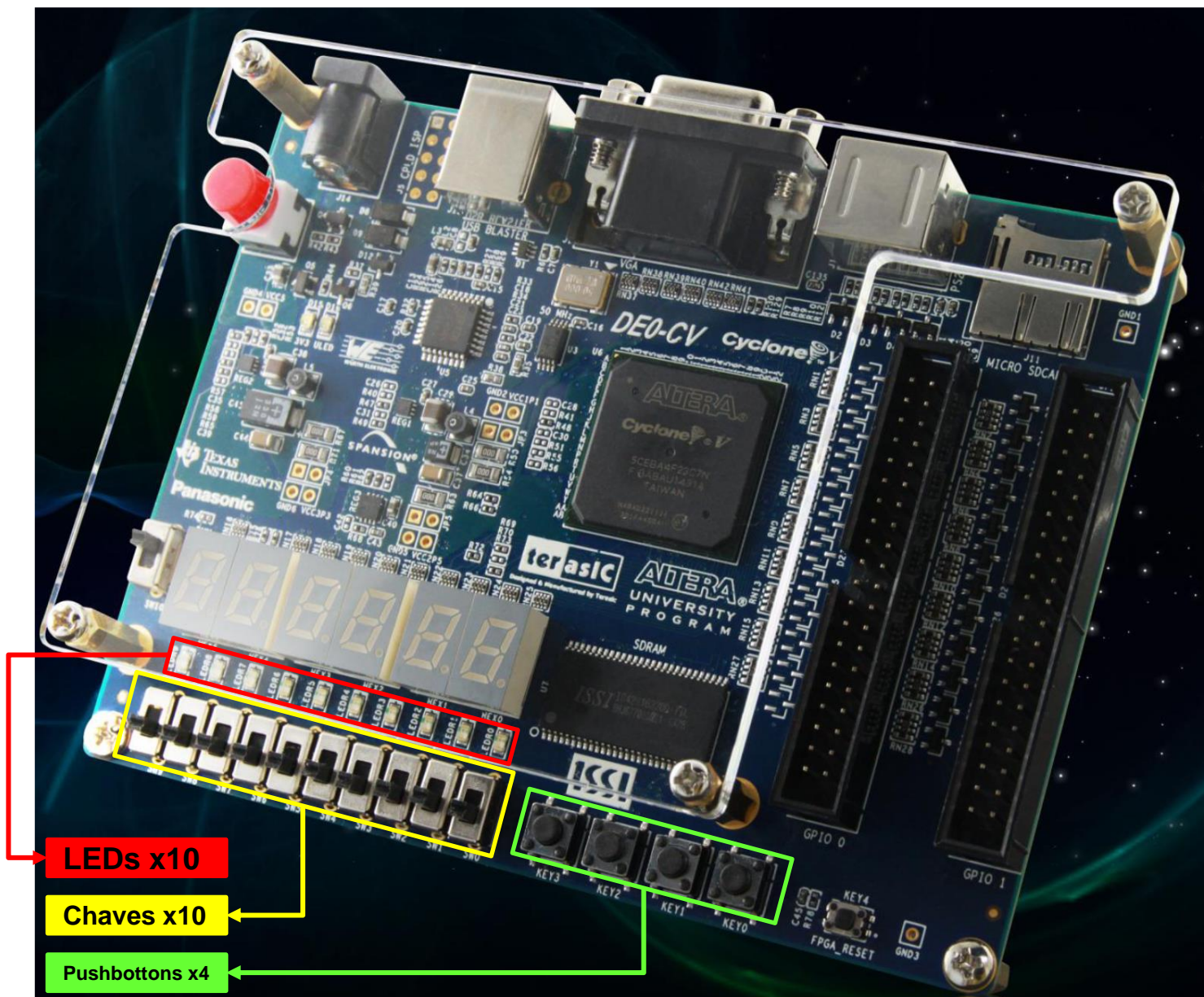
Name	Core Voltage	ALMs	User I/Os	GXB Channel PMA	GXB Channel PCS	PCIe I ^
5CEBA2U15C6	1.1V	9430	176	0	0	0
5CEBA2U15C7	1.1V	9430	176	0	0	0
5CEBA2U15C8	1.1V	9430	176	0	0	0
5CEBA2U15I7	1.1V	9430	176	0	0	0
5CEBA2U19C7	1.1V	9430	224	0	0	0
5CEBA2U19C8	1.1V	9430	224	0	0	0
5CEBA4F17A7	1.1V	18480	128	0	0	0
5CEBA4F17C6	1.1V	18480	128	0	0	0
5CEBA4F17C7	1.1V	18480	128	0	0	0
5CEBA4F17C8	1.1V	18480	128	0	0	0
5CEBA4F17I7	1.1V	18480	128	0	0	0
5CEBA4F23C7	1.1V	18480	224	0	0	0

Migration Devices... 0 migration devices selected

OK Cancel Help







FileEditViewProjectAssignmentsProcessingToolsWindowHelp

Project Navigator

Entity  
Cyclone V: SCEBA4F23C7  
PortaAND

Tasks  
Flow: Compilation  
Task  
Compile Design  
Analysis & Synthesis  
Fitter (Place & Route)  
Assembler (Generate programming file)  
TimeQuest Timing Analysis  
EDA Netlist Writer  
Program Device (Open Programmer)

Start Processing  
Start Compilation  
Analyze Current File  
Start  
Update Memory Initialization File  
Compilation Report  
Dynamic Synthesis Report  
PowerPlay Power Analyzer Tool  
SSN Analyzer Tool  
Receive Compilation Status Notifications

AND2  
inst  
INPUT VCC  
INPUT VCC  
OUTPUT  
Y

IP Catalog  
Installed IP  
Project Directory  
Library  
Basic Functions  
DSP  
Interface Protocols  
Memory Interfaces and C  
Processors and Peripherals  
Search for Partner IP

TypeIDMessage

FileEditViewProjectAssignmentsProcessingToolsWindowHelp

PortaAND

Project Navigator

Entity

Cyclone V: 5CEBA4F23C7

PortaAND

HierarchyFilesDesign UI

Tasks

Flow: CompilationCustomize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming file)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

Run Simulation Tool

Launch Simulation Library Compiler

Launch Design Space Explorer II

TimeQuest Timing Analyzer

Advisors

Chip Planner

Design Partition Planner

Netlist Viewers

SignalTap II Logic Analyzer

In-System Memory Content Editor

Logic Analyzer Interface Editor

In-System Sources and Probes Editor

SignalProbe Pins...

Programmer

JTAG Chain Debugger

Fault Injection Debugger

System Debugging Tools

IP Catalog

Nios II Software Build Tools for Eclipse

Qsys

Tcl Scripts...

Customize...

Options...

License Setup...

Install Devices...

Compilation Report - PortaAND

Summary

StatusSuccessful - Mon Mar 12 16:08:59 2018

Quartus II 64-Bit Version14.1.0 Build 186 12/03/2014 SJ Web Edition

Design NamePortaAND

Level Entity NamePortaAND

FamilyCyclone V

Device5CEBA4F23C7

Design ModelsFinal

Logic utilization (in ALMs)1 / 18,480 (< 1 %)

Logic registers0

Logic pins3 / 224 (1 %)

Logic virtual pins0

Block memory bits0 / 3,153,920 (0 %)

DSP Blocks0 / 66 (0 %)

HSSI RX PCSs0

HSSI TX PCSs0

HSSI TX Serializers0

PLLs0 / 4 (0 %)

DLLs0 / 4 (0 %)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and C

Processors and Periphera

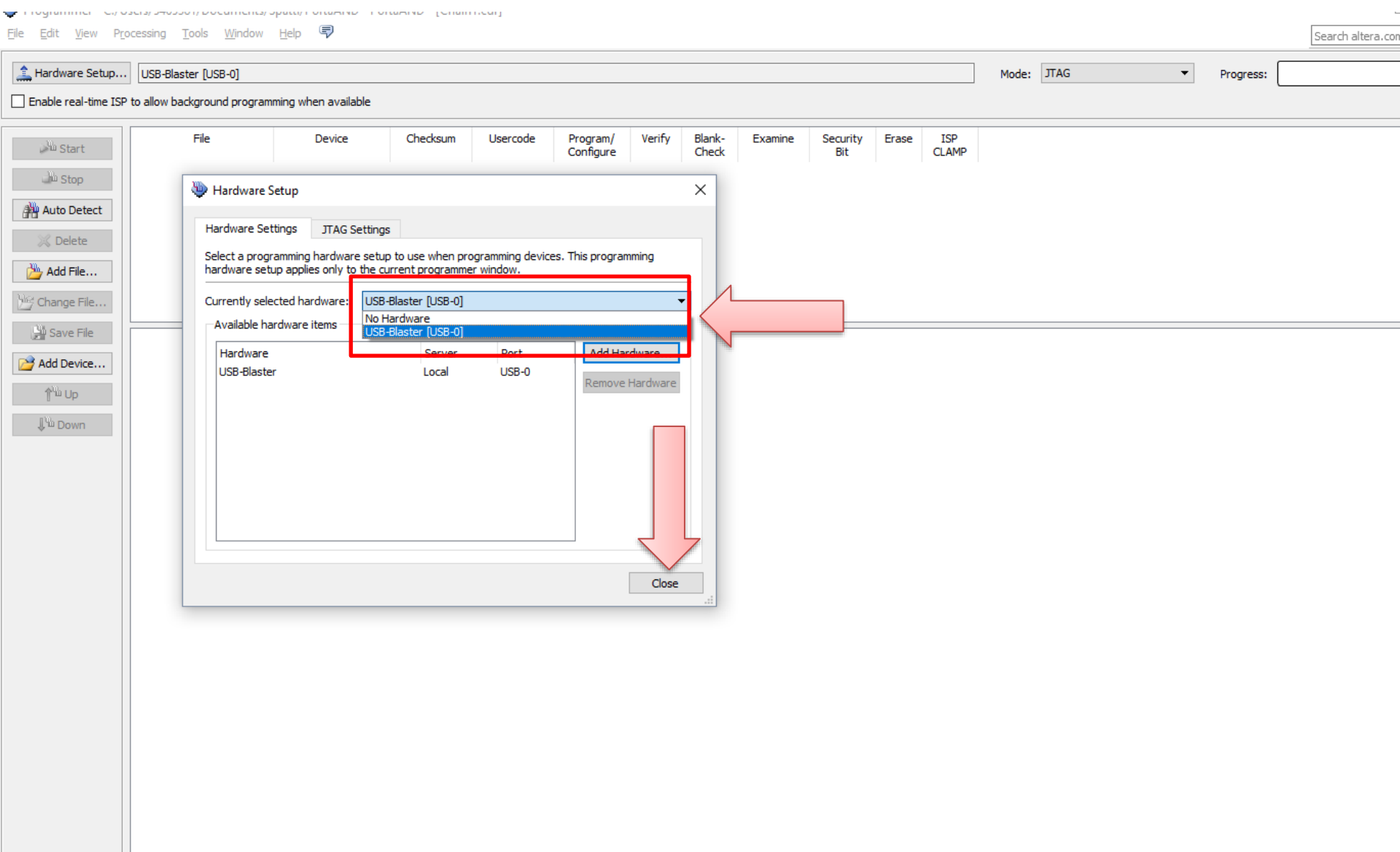
Search for Partner IP

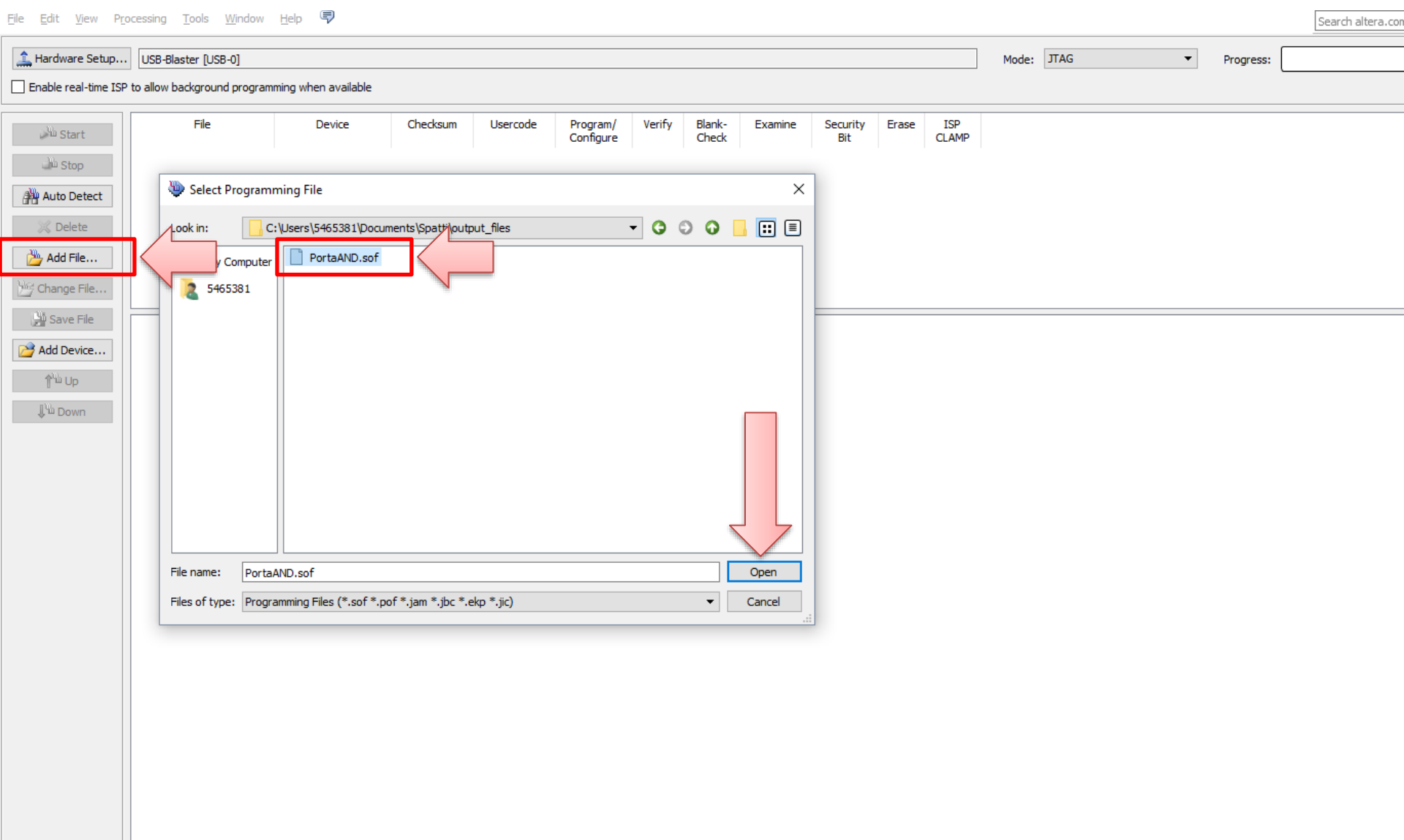
Add...

All

Search>>









File Edit View Processing Tools Window Help

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Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Success)

☐ Enable real-time ISP to allow background programming when available

	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/PortaAND.sof	SCEBA4F23	004DD387	004DD387	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start

Stop

Auto Detect

Delete

Add File...

Change File...

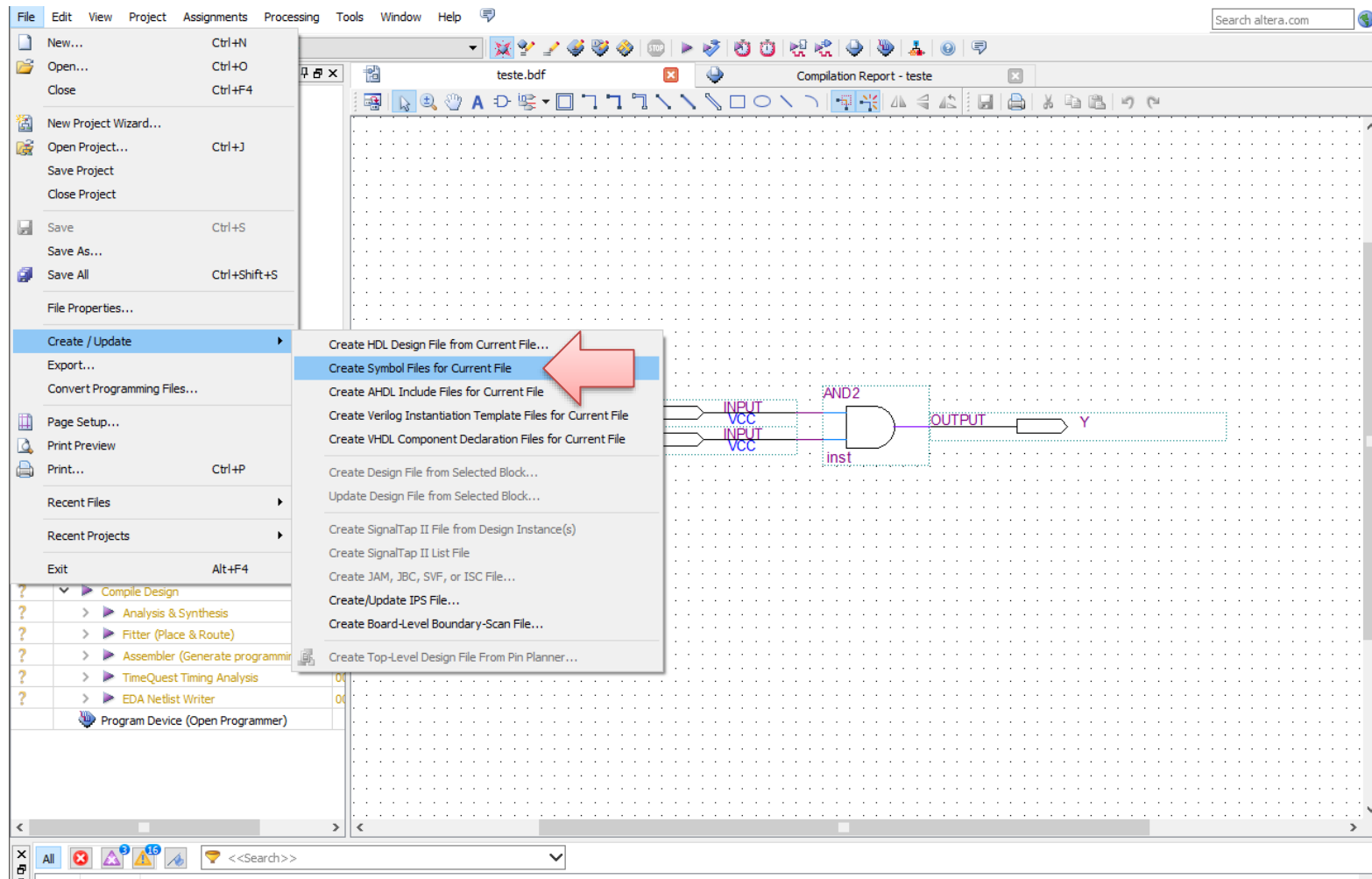
Save File

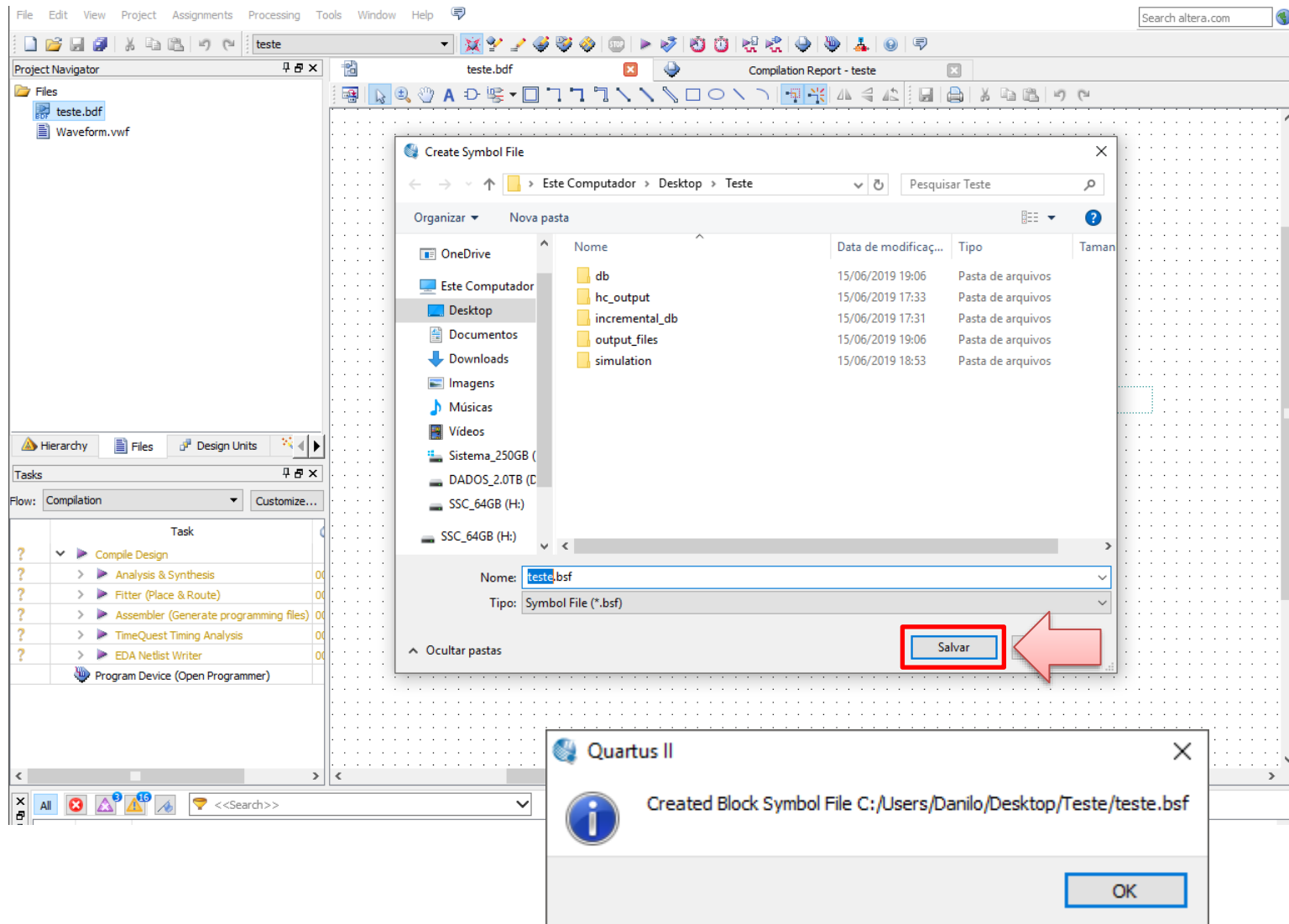
Add Device...

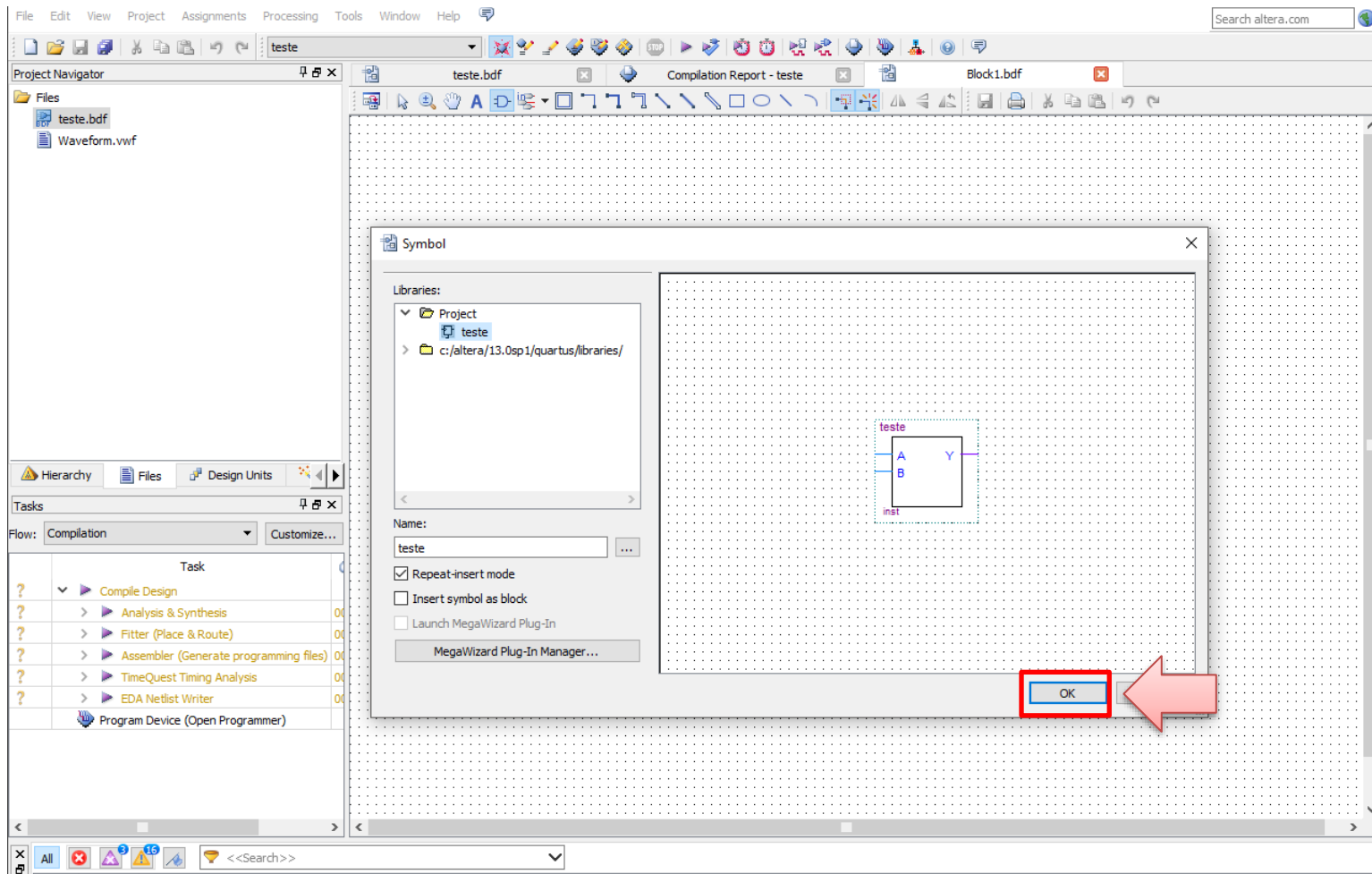
Up

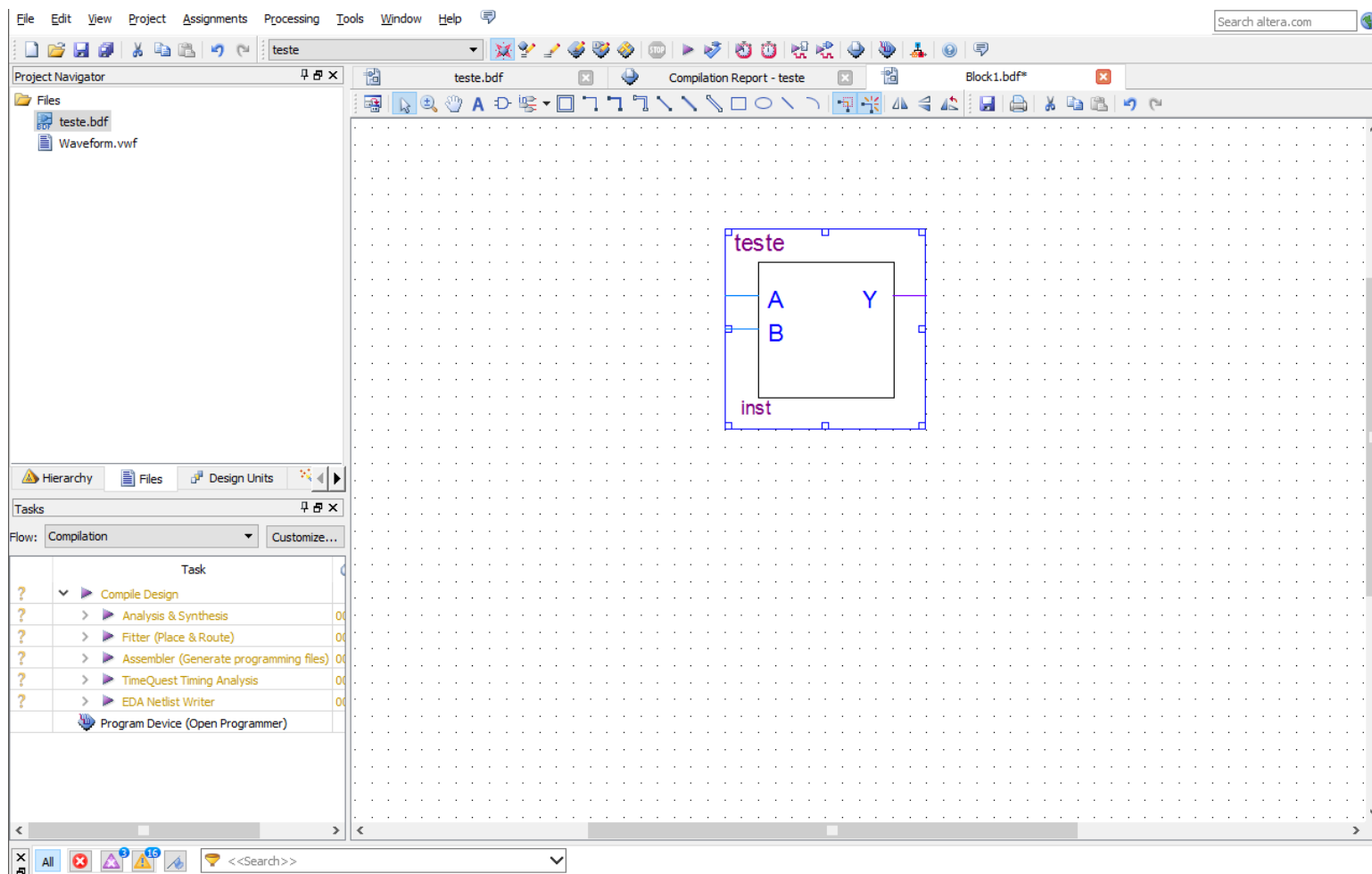
Down

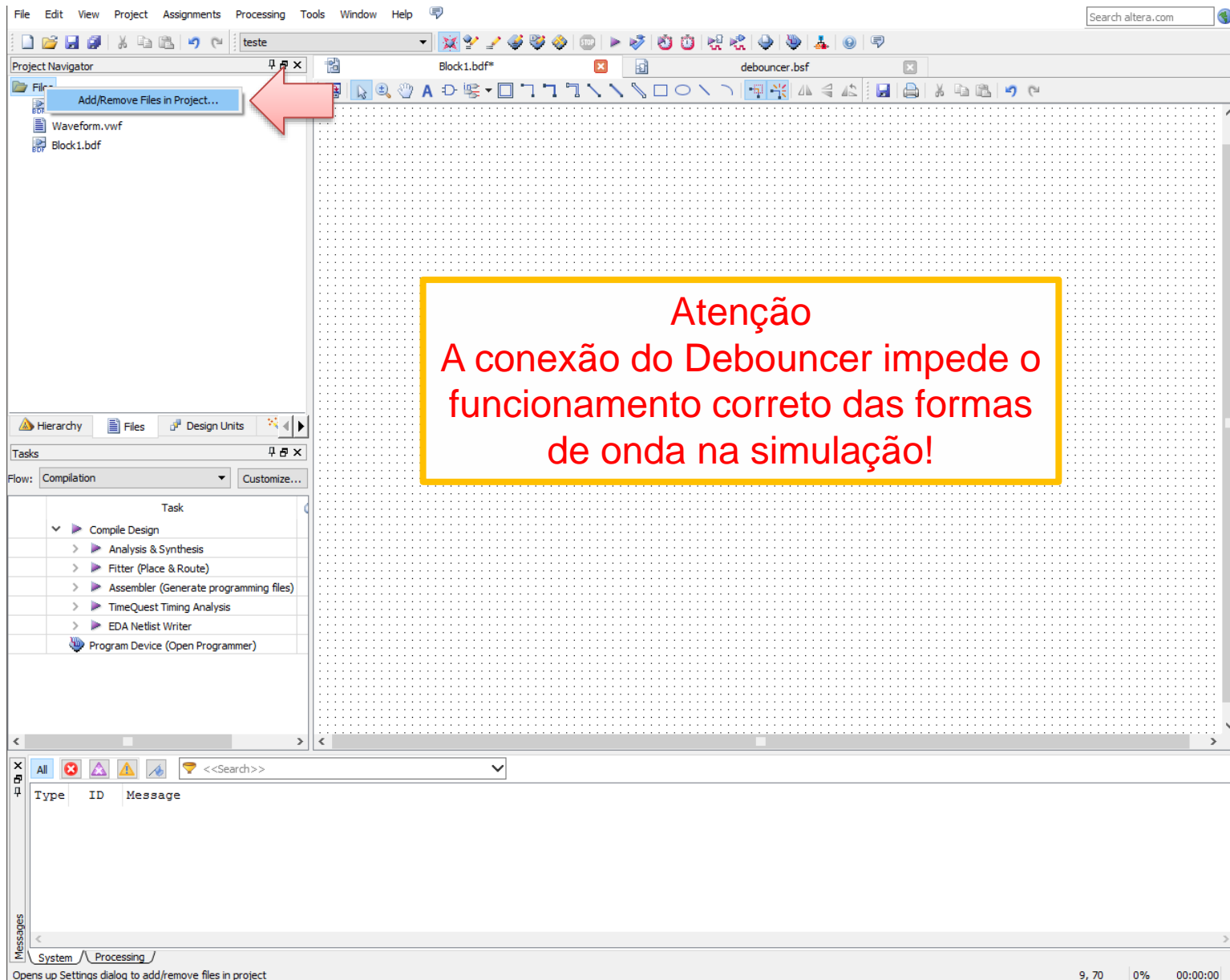
Diagram illustrating the connection of the Altera SCEBA4F23 device to the JTAG interface. The device is connected to the TDI (Test Data In) and TDO (Test Data Out) lines.

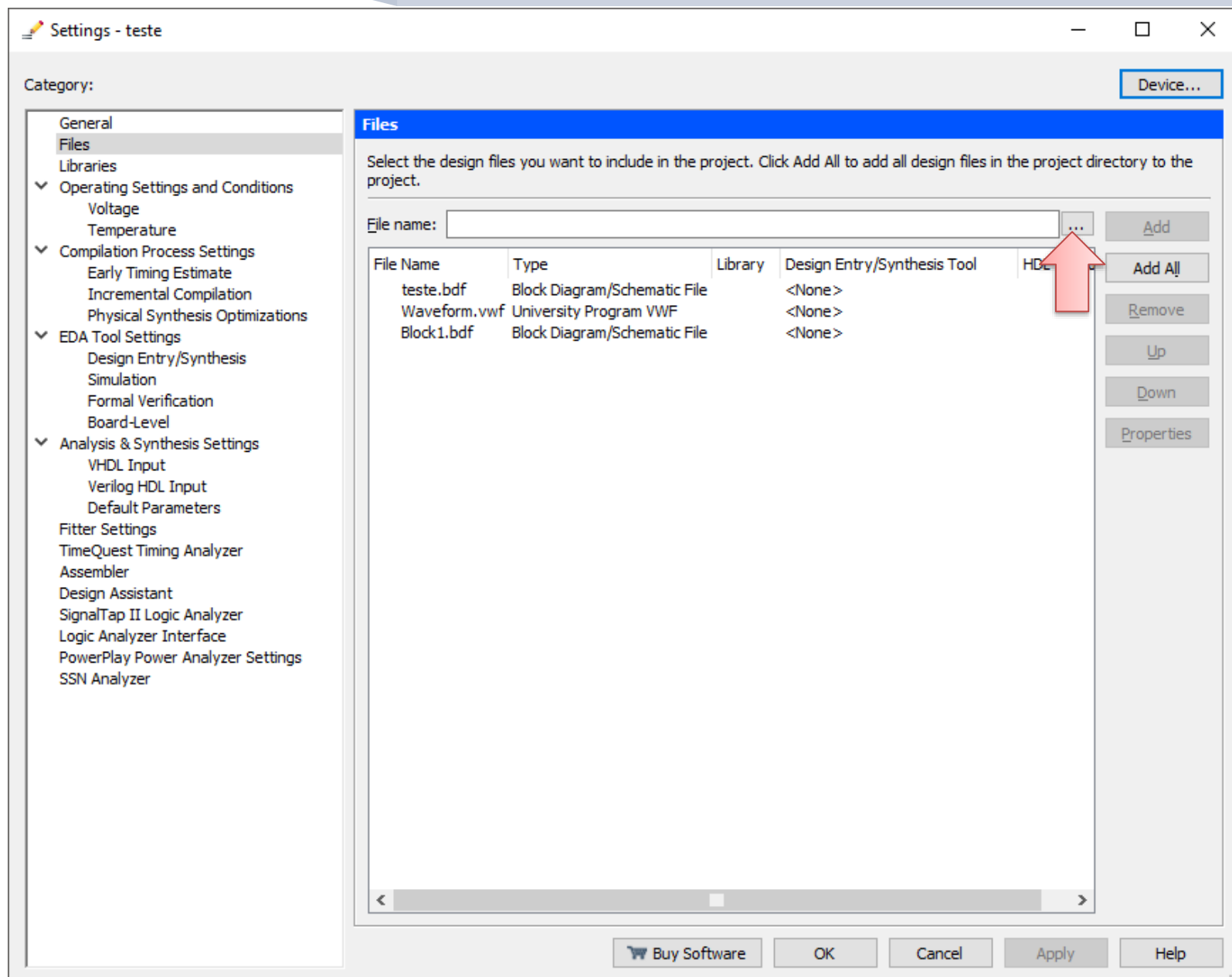


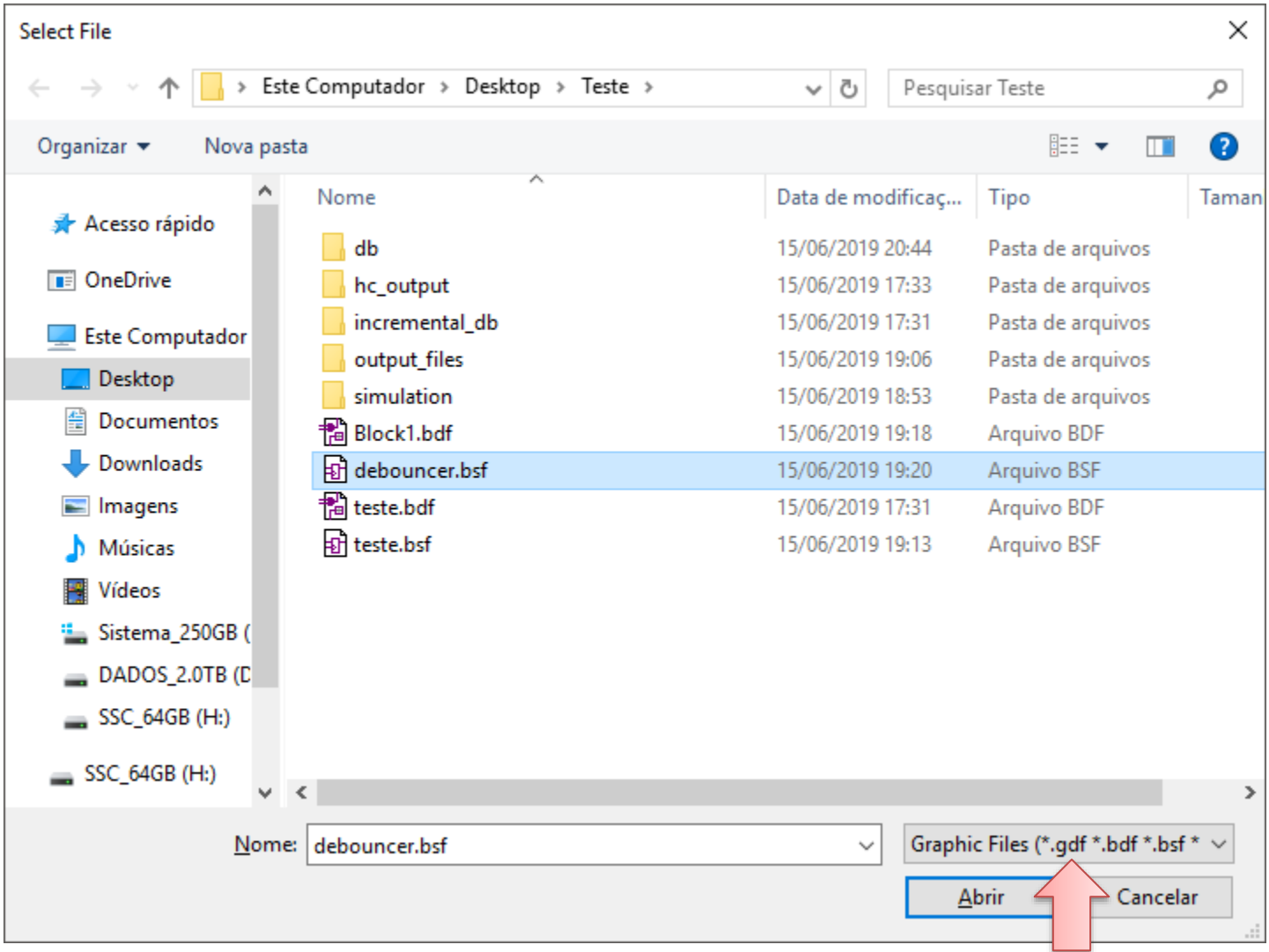




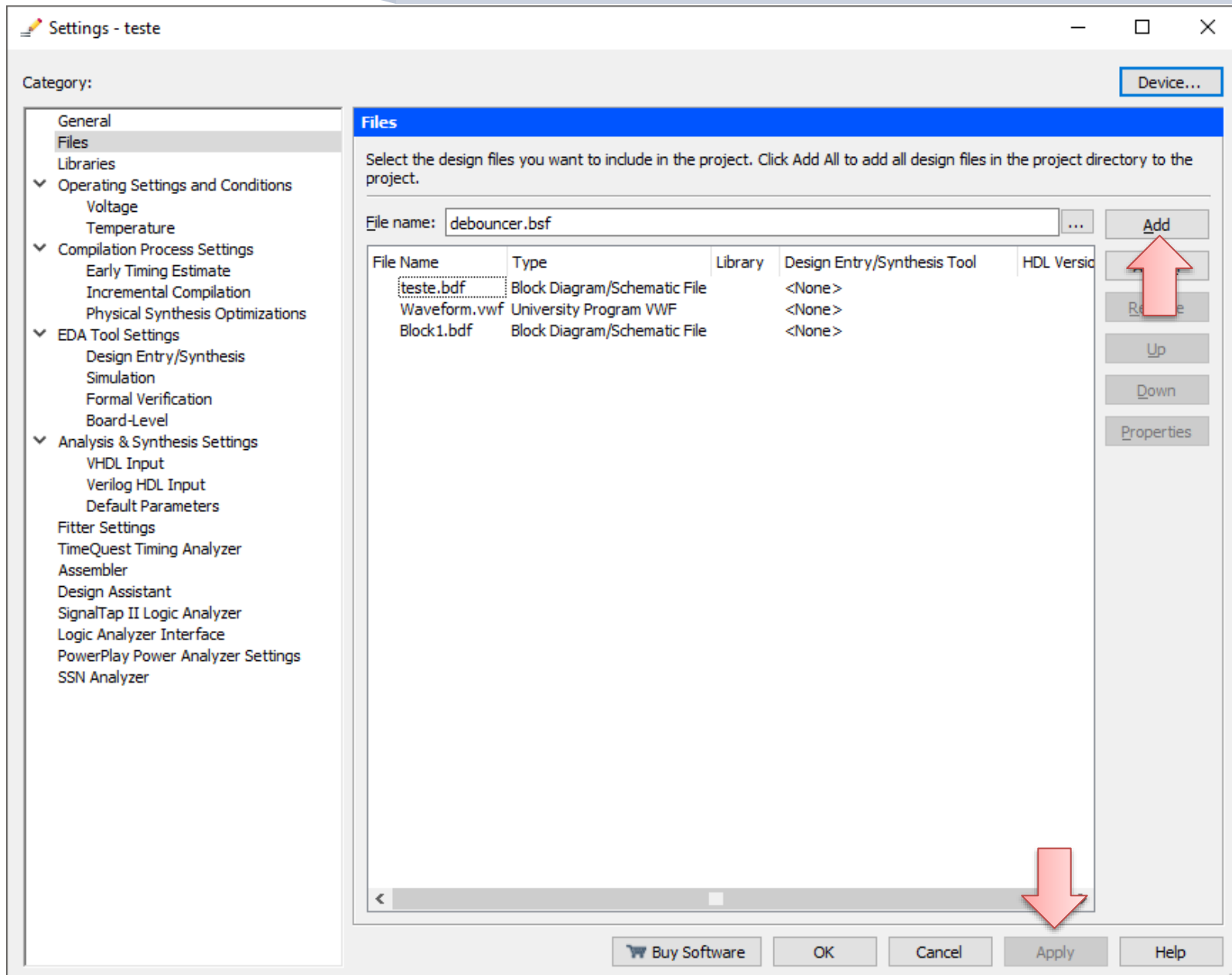


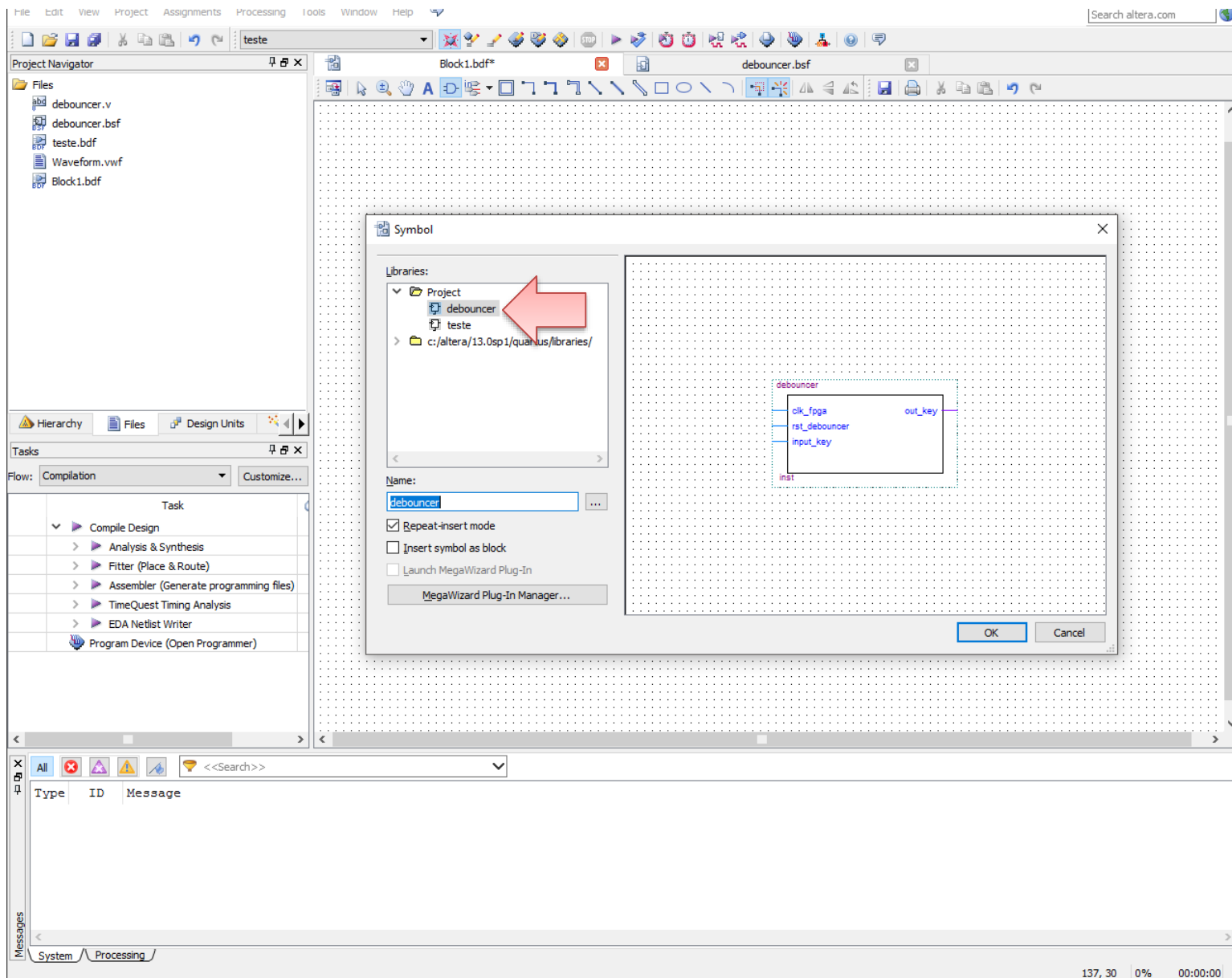


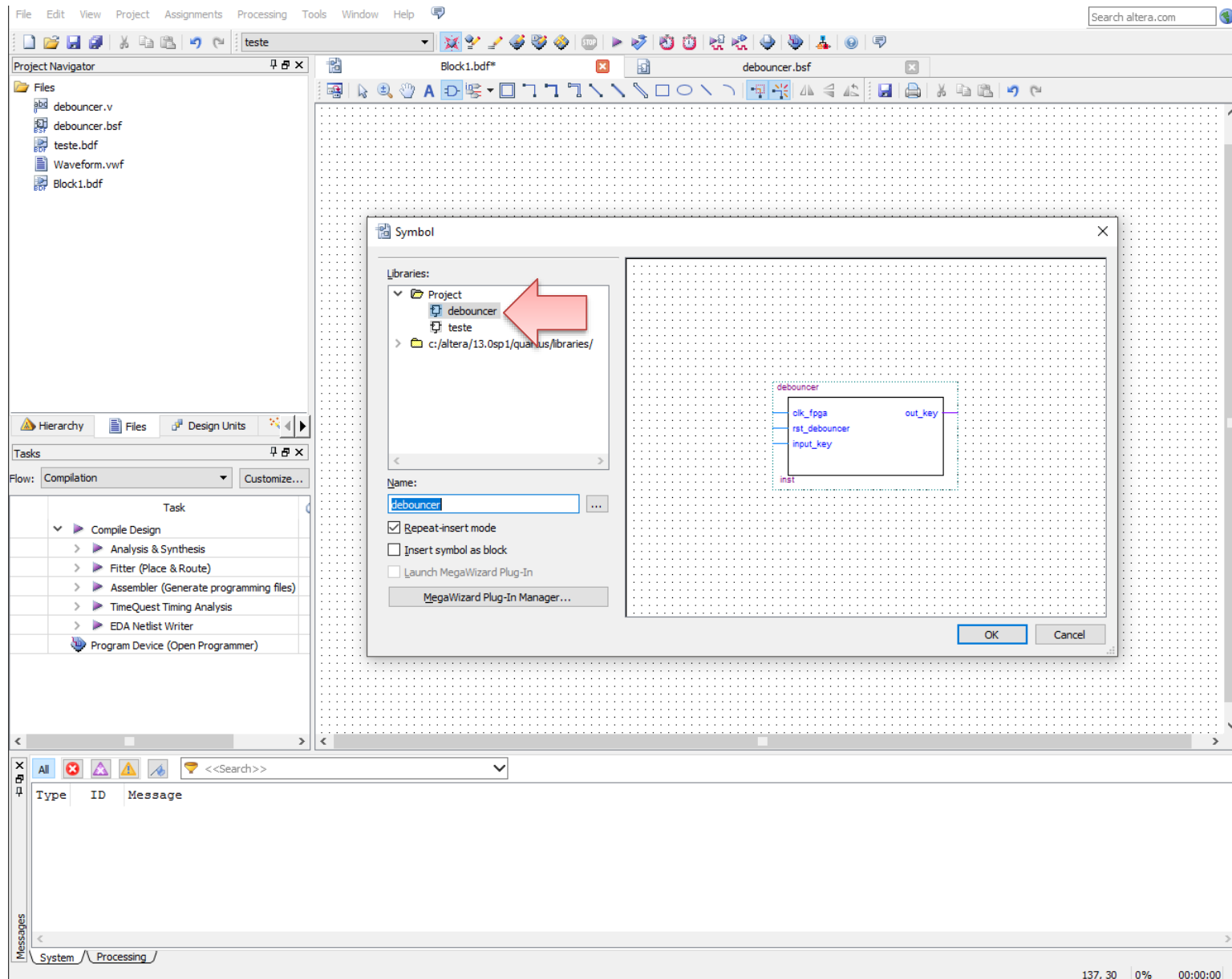












clk\_fpga – clock interno da placa (CLOCK\_50)  
rst\_debouncer – reset do contador do Debouncer  
input\_key – entrada com ruído  
out\_key – saída filtrada

Parameter	Value	Type
DELAY_BITS	16	Signed Integer

debouncer

clk\_fpga  
rst\_debouncer  
input\_key

inst

out\_key

Task

- Complete Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Programmer)

Messages

System Processing

336, 232 0% 00:00:00

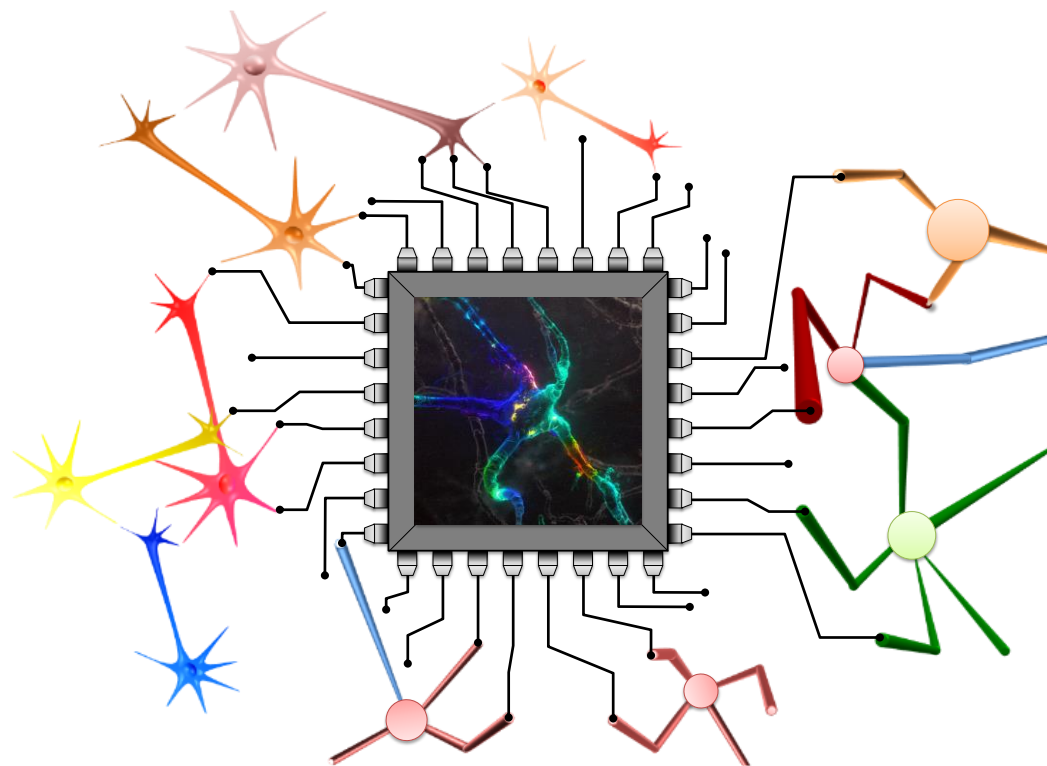
Table 3-6 Pin Assignment of Clock Inputs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>
CLOCK_50	PIN_M9	50 MHz clock input(Bank 3B)
CLOCK2_50	PIN_H13	50 MHz clock input(Bank 7A)
CLOCK3_50	PIN_E10	50 MHz clock input(Bank 8A)
CLOCK4_50	PIN_V15	50 MHz clock input(Bank 4A)

Table 4-5 Pin Assignments for Clock Inputs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
CLOCK_50	PIN_Y2	50 MHz clock input	3.3V
CLOCK2_50	PIN_AG14	50 MHz clock input	3.3V
CLOCK3_50	PIN_AG15	50 MHz clock input	Depending on JP6
SMA_CLKOUT	PIN_AE23	External (SMA) clock output	Depending on JP6
SMA_CLKIN	PIN_AH14	External (SMA) clock input	3.3V

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