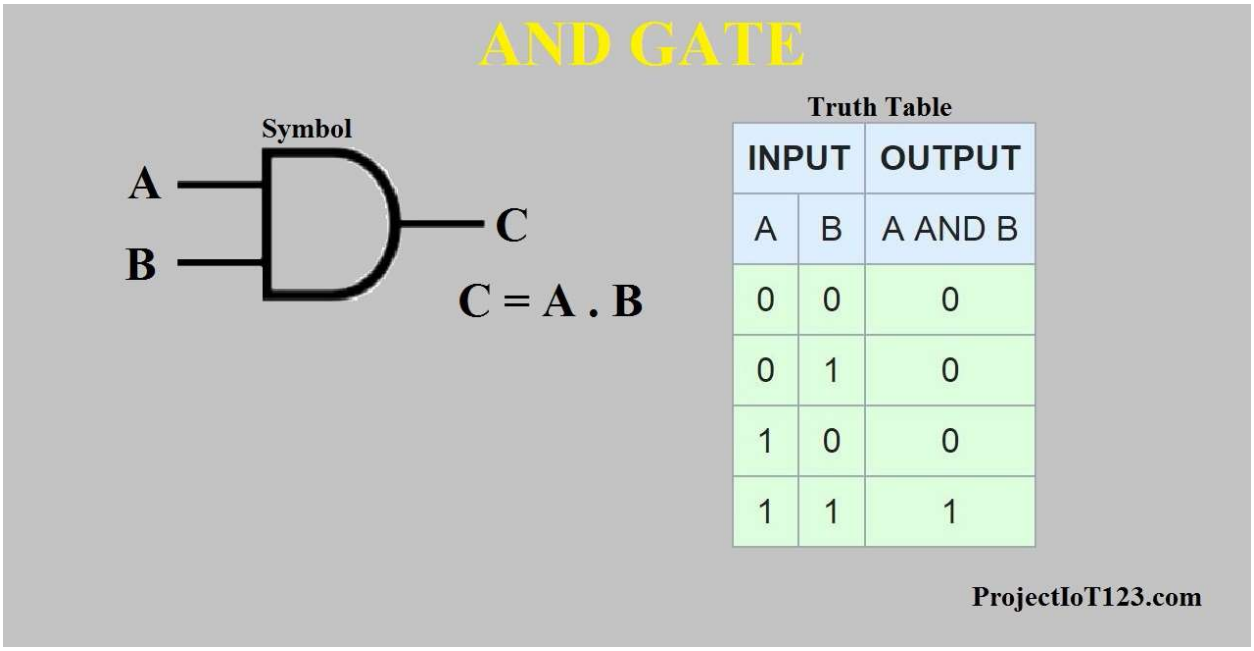


Figure 2.1: AND Gate Logic

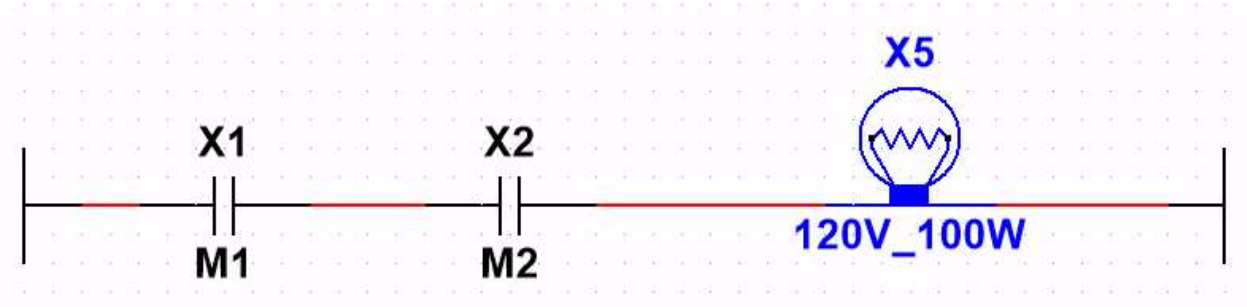
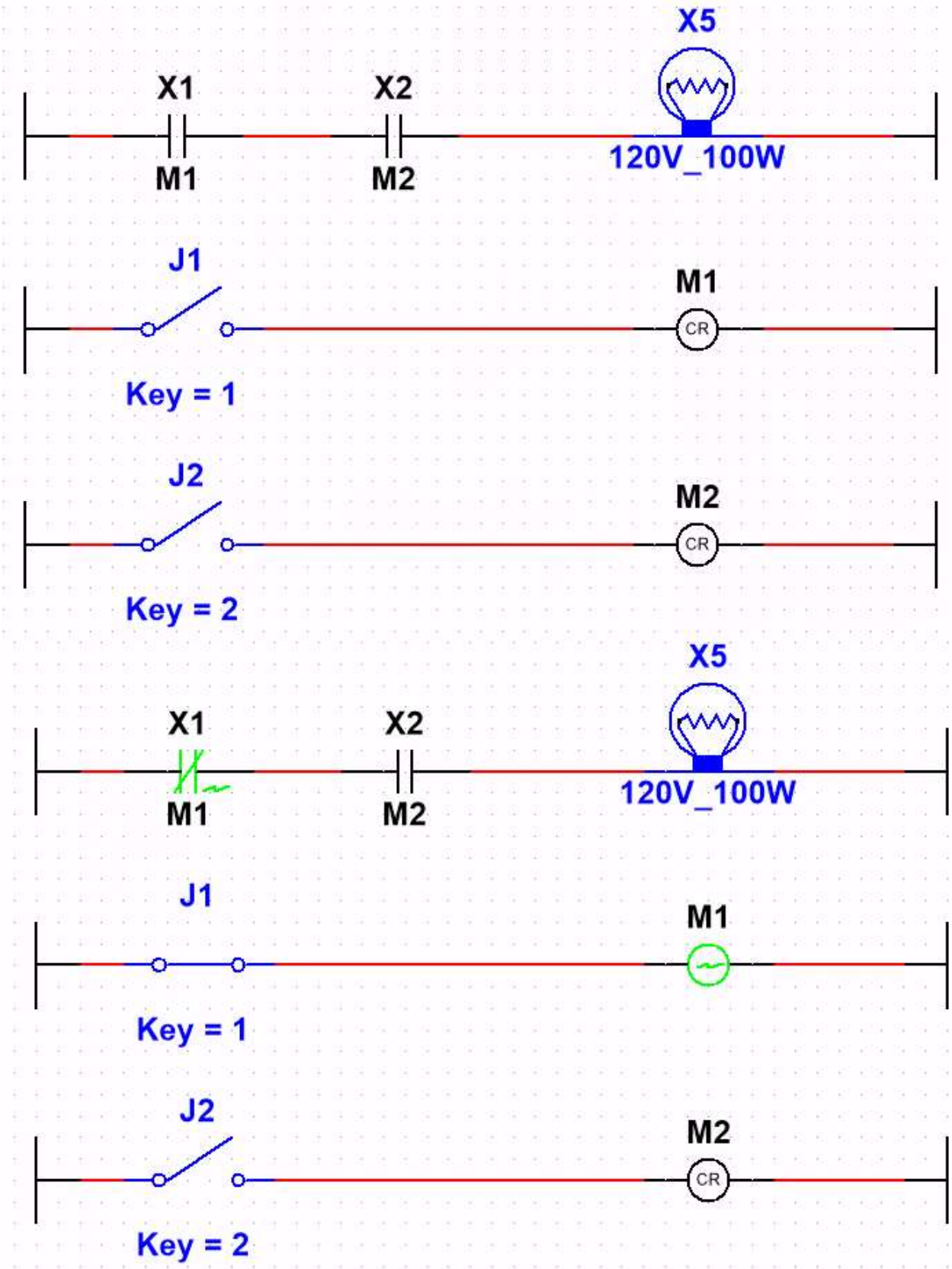


Figure 2.2: AND Gate Ladder Diagram


X5
X1
X2
M1
M2
120V_100W
J1
M1
CR
Key = 1
J2
M2
CR
Key = 2
X5
X1
X2
M1
M2
120V_100W
J1
M1
Key = 1
J2
M2
CR
Key = 2

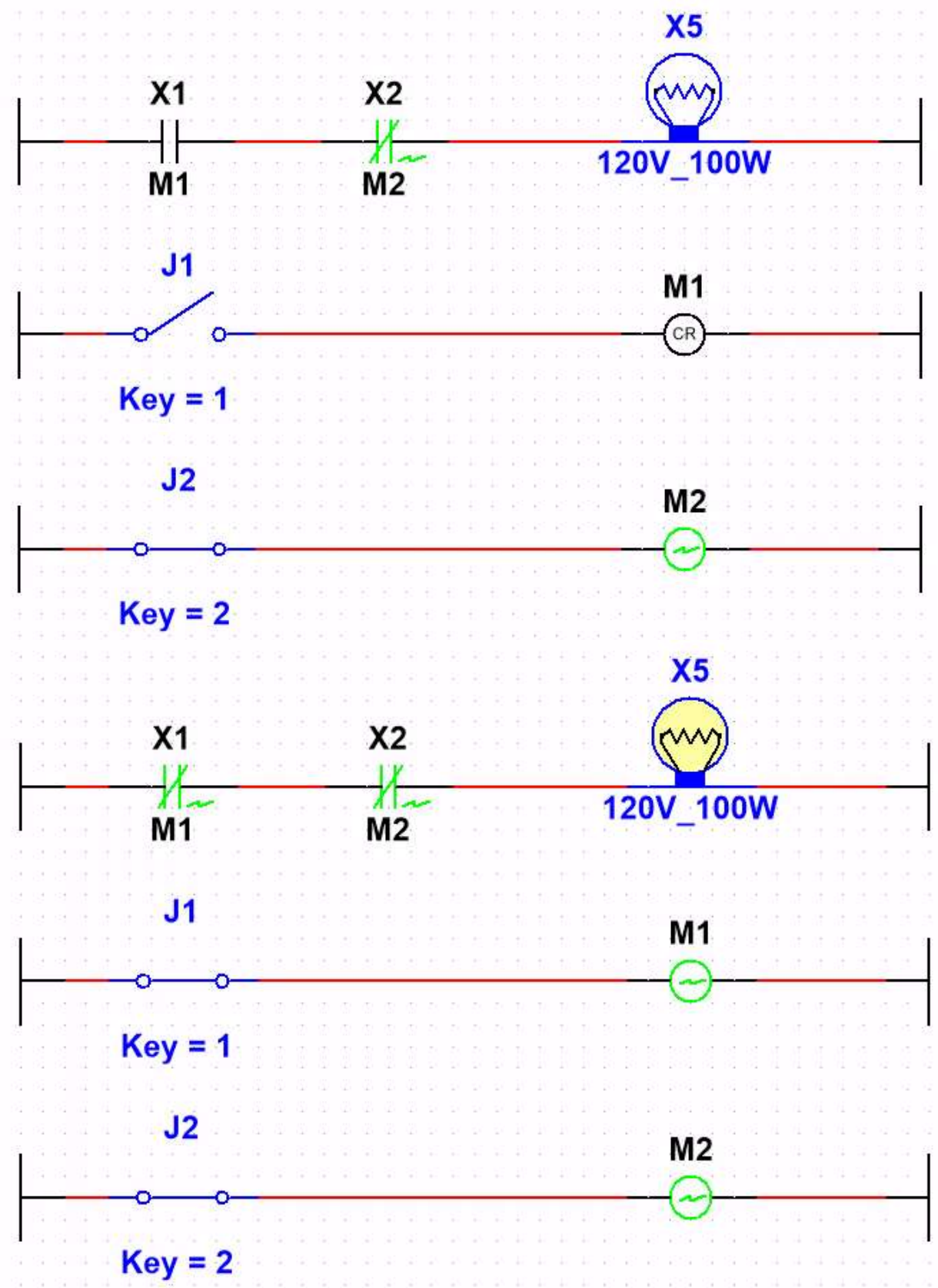


Figure 2.3: AND Gate Outputs

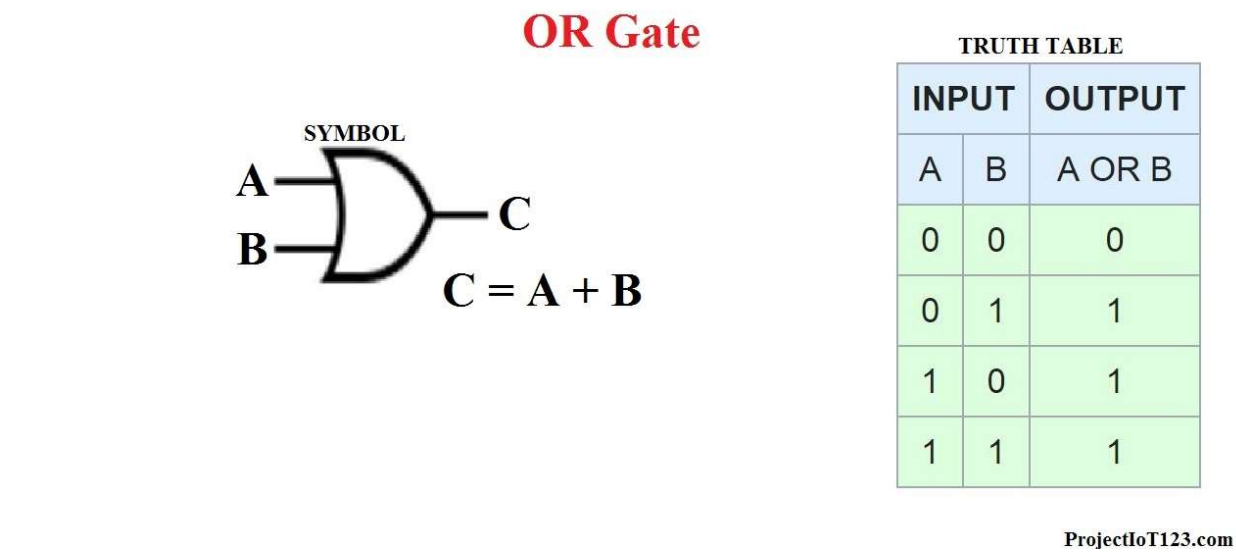


Figure 2.4: OR Gate Logic

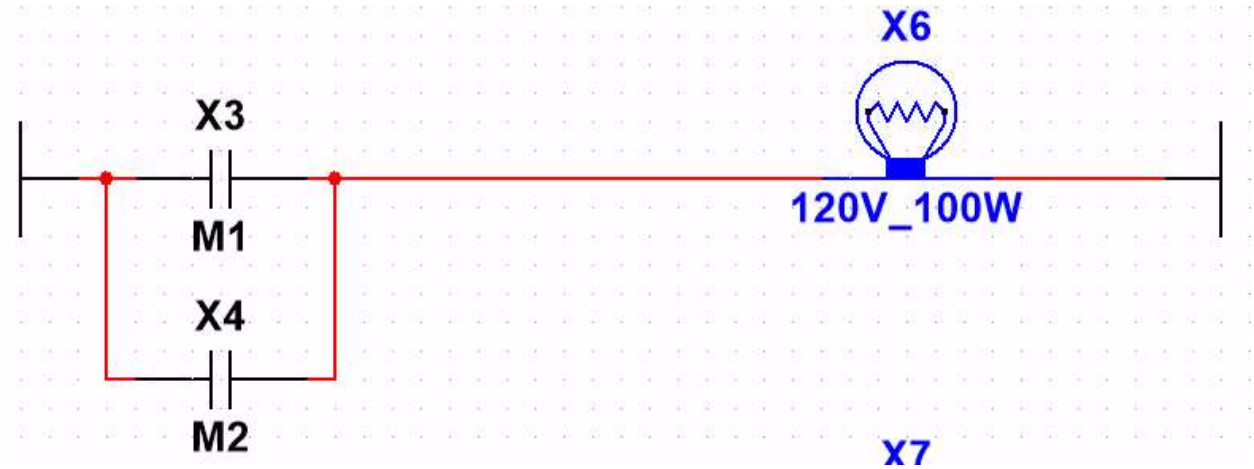
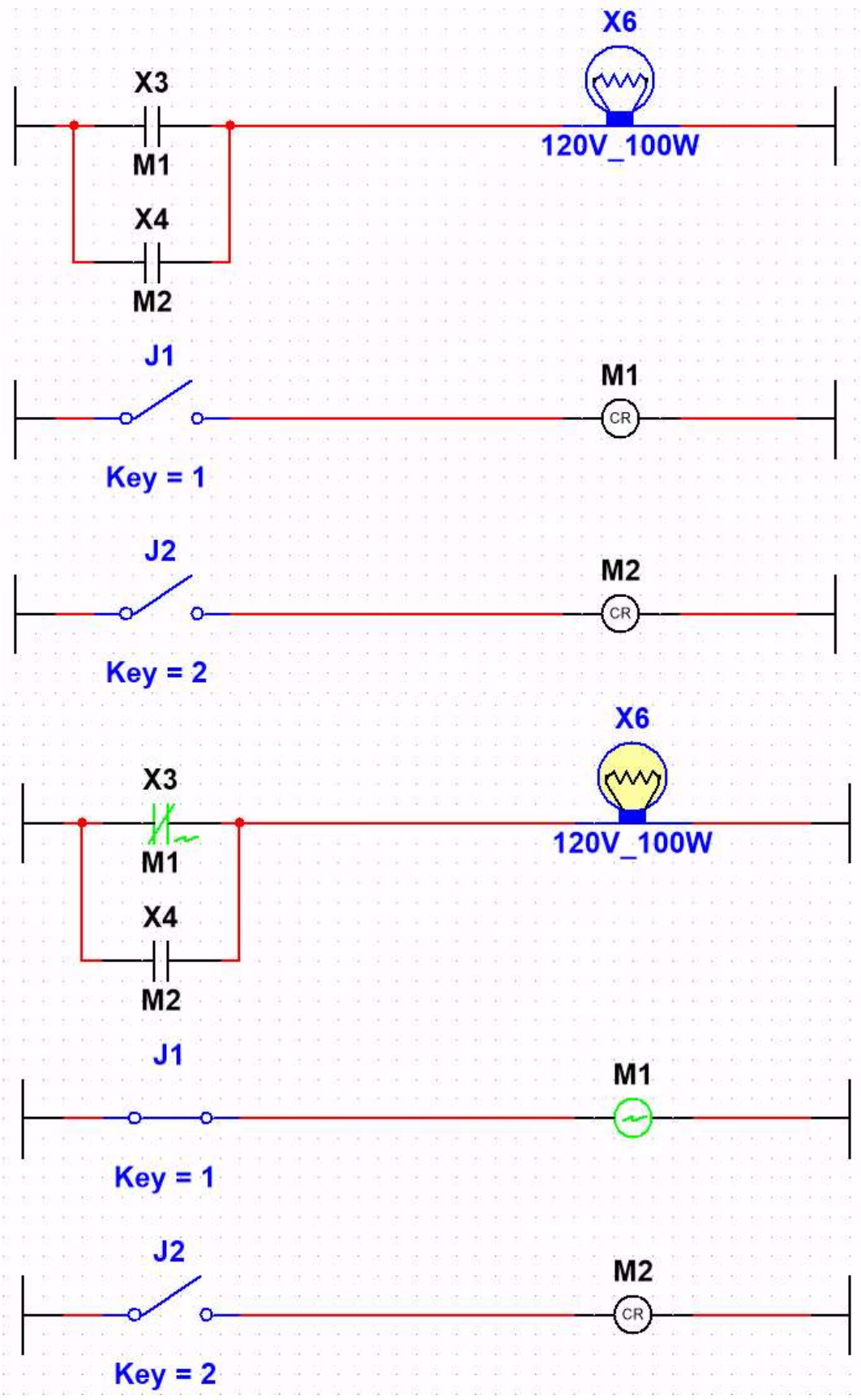


Figure 2.5: OR Gate Ladder Diagram


X6
X3
120V_100W
M1
X4
M2
J1
M1
CR
Key = 1
J2
M2
CR
Key = 2
X6
X3
120V_100W
M1
X4
M2
J1
M1
Key = 1
J2
M2
CR
Key = 2

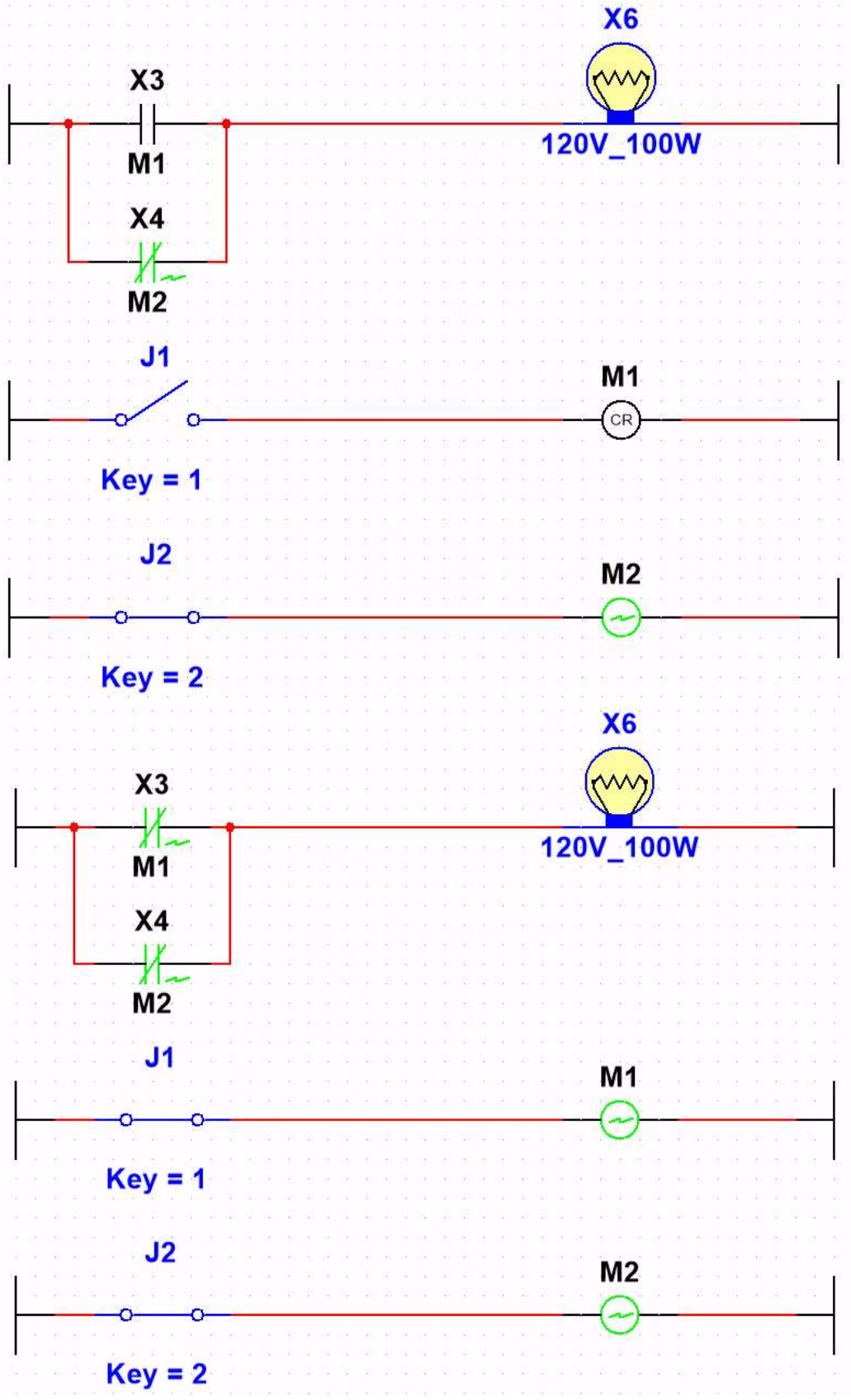
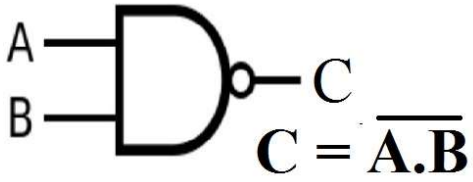


Figure 2.6: OR Gate Outputs

NAND GATE



Truth Table

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

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Figure 2.7: NAND Gate Logic

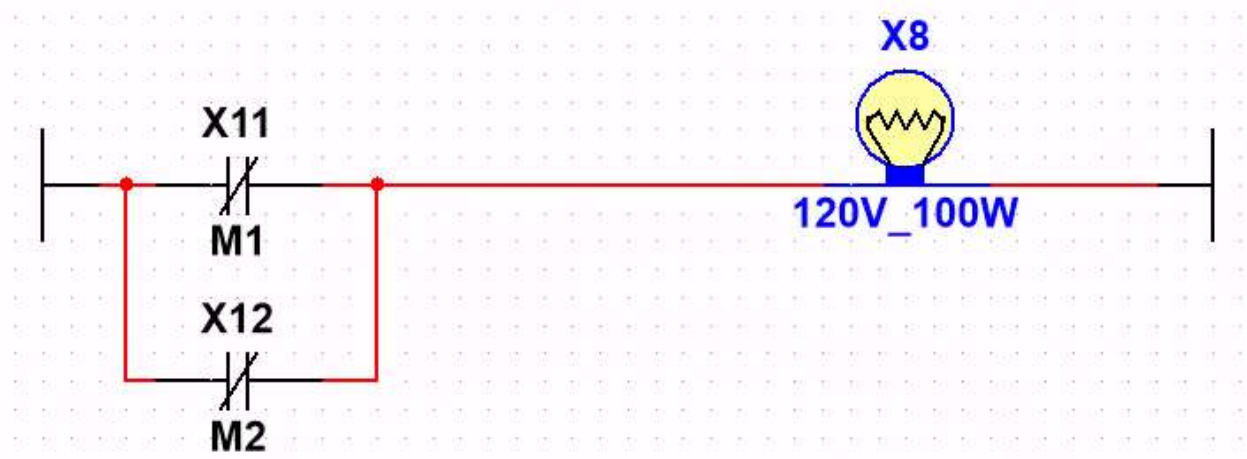
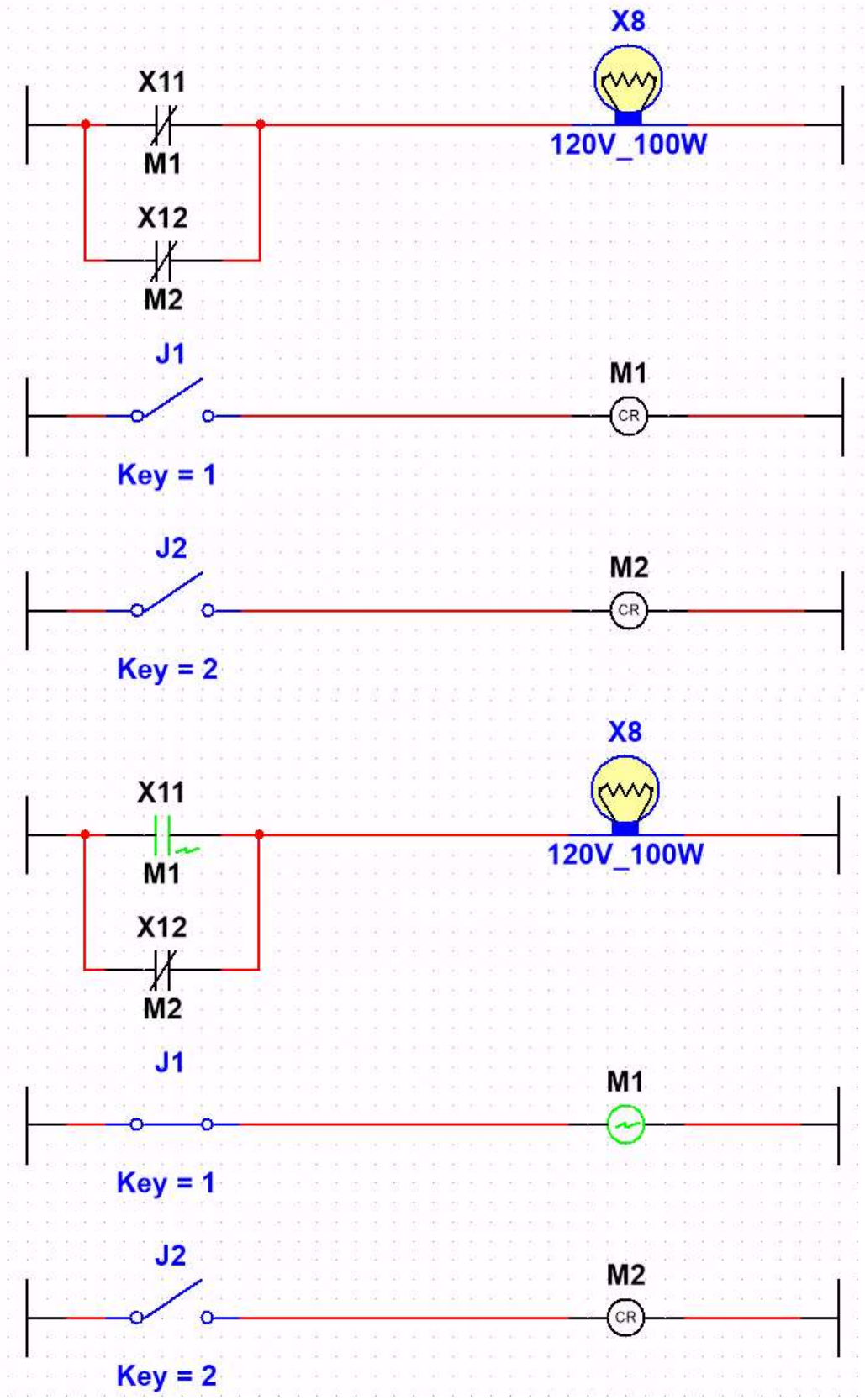


Figure 2.8: NAND Gate Ladder Diagram


X8
X11
M1
120V_100W
X12
M2
J1
M1
CR
Key = 1
J2
M2
CR
Key = 2
X8
X11
M1
120V_100W
X12
M2
J1
M1
Key = 1
J2
M2
CR
Key = 2

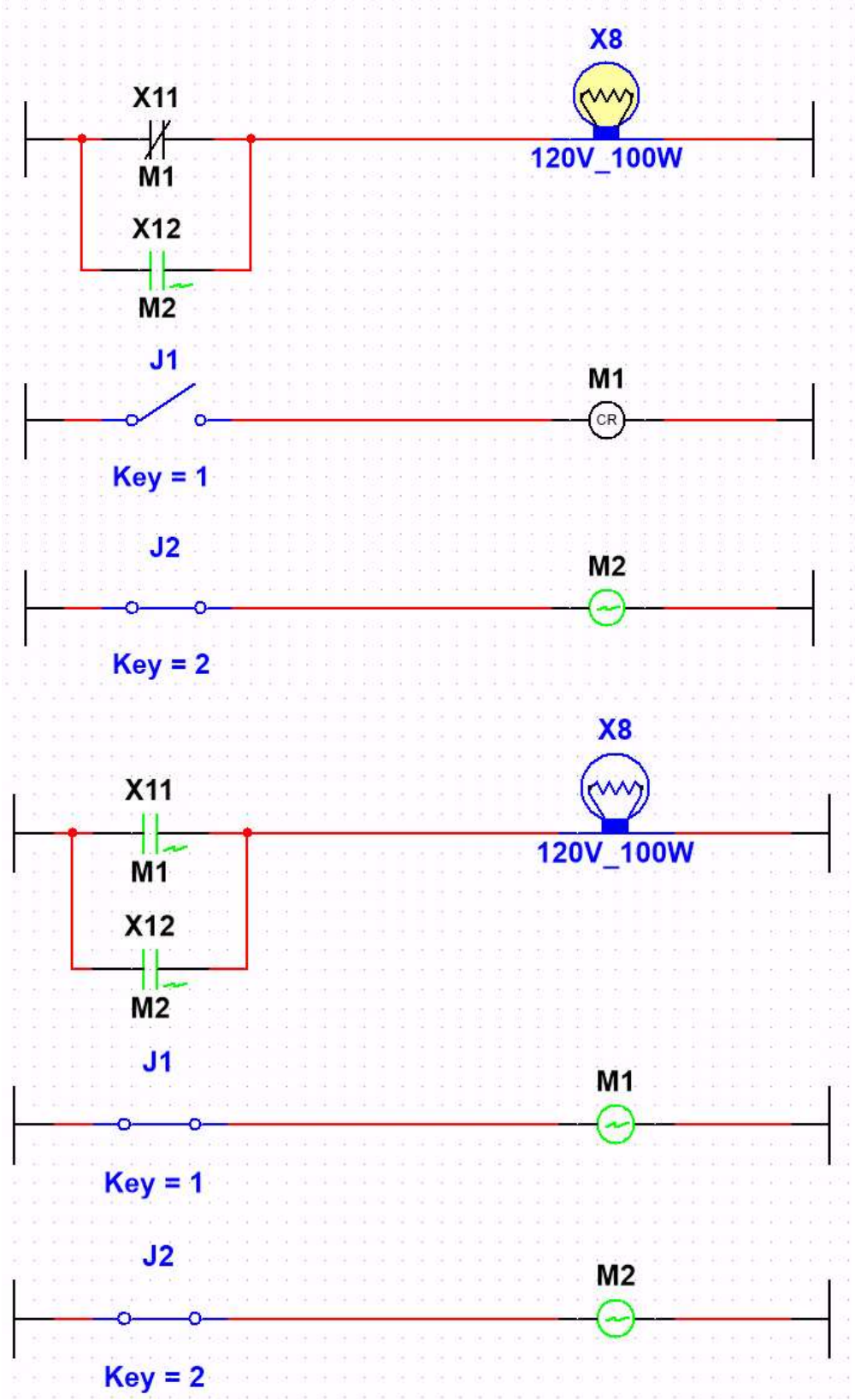
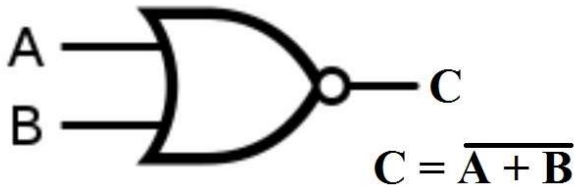


Figure 2.9: NAND Gate Outputs

NOR GATE



TRUTH TABLE

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

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Figure 2.10: NOR Gate Logic

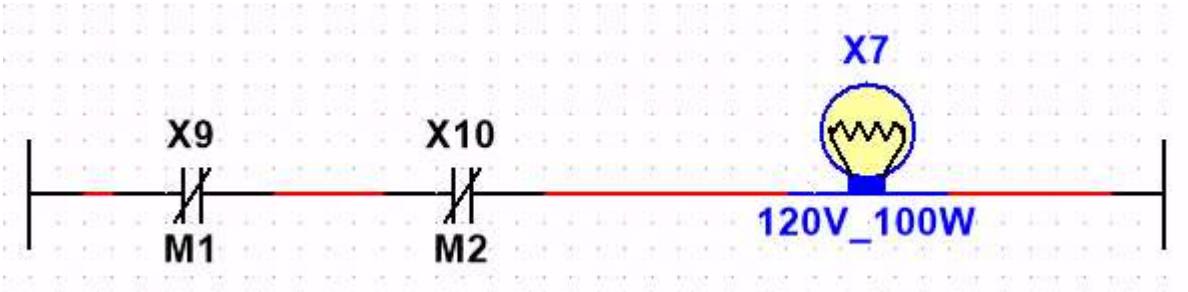
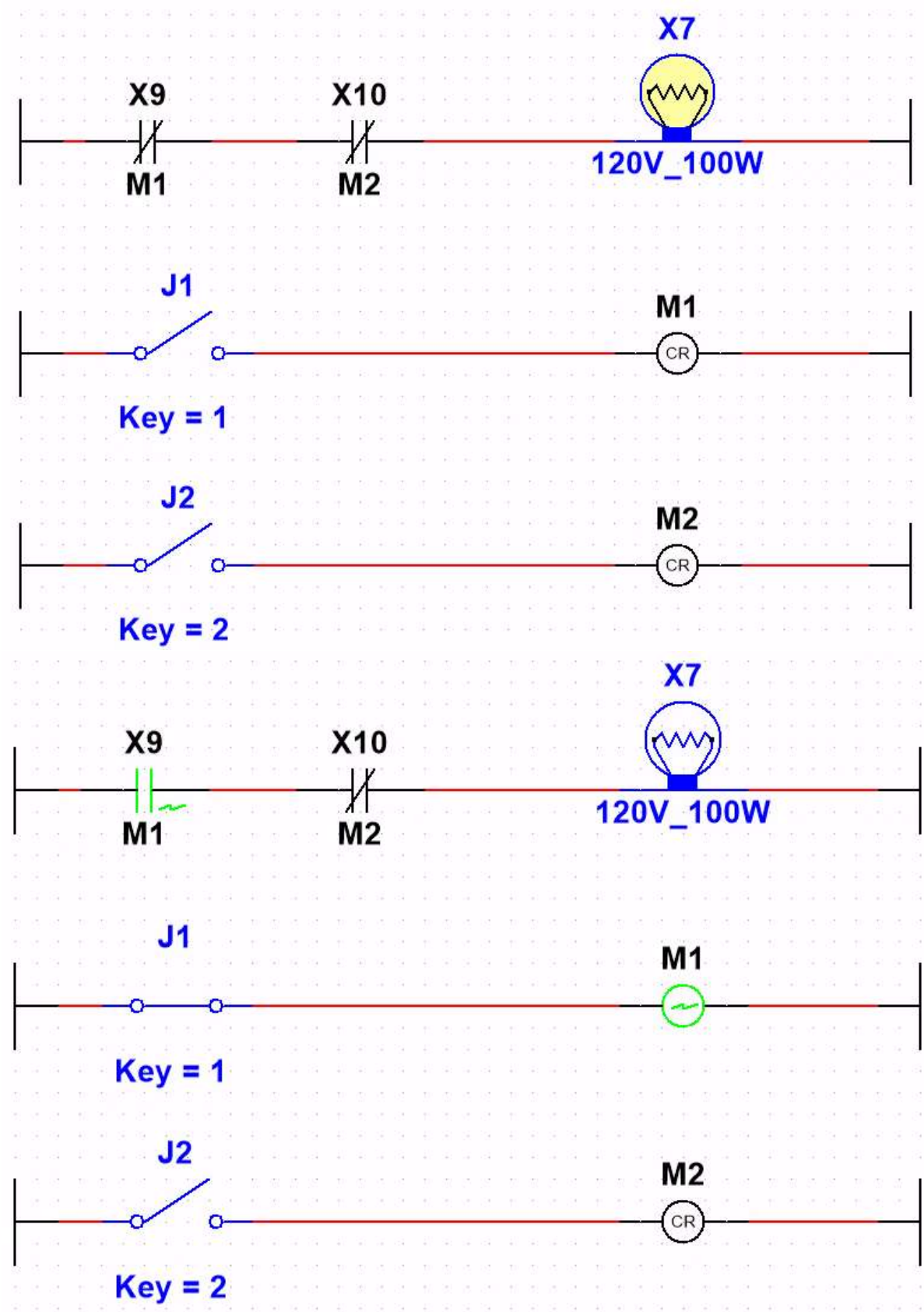


Figure 2.11: NOR Gate Ladder Diagram


X7
X9
X10
M1
M2
120V_100W
J1
M1
CR
Key = 1
J2
M2
CR
Key = 2
X7
X9
X10
M1
M2
120V_100W
J1
M1
Key = 1
J2
M2
CR
Key = 2

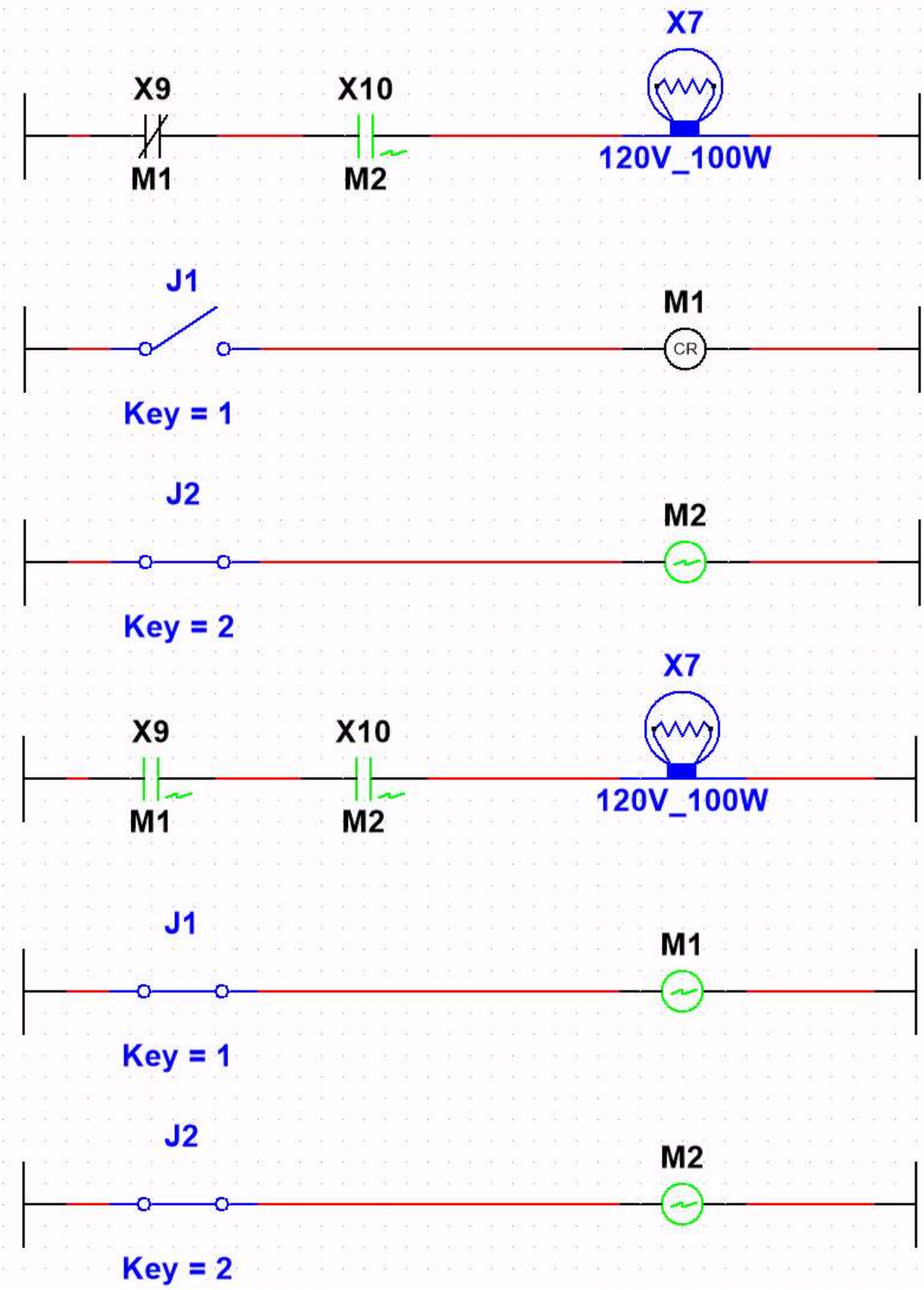


Figure 2.12: NOR Gate Outputs