For problems 6.1 through 6.3: Suppose the propagation delay of an 8-bit adder is 0.8ns, adder/subtractor is 1.1ns, 2-to-1 mux is 0.3ns, and 4-to-1 mux is 0.6ns. Also, assume register setup time (), clock-to-q (), and clock-skew () are all 0.05ns. (15 points)

6.1 Calculate the required maximum clock frequency for each of the following data paths:

a. Single-cycle data path in Fig. 6.2.

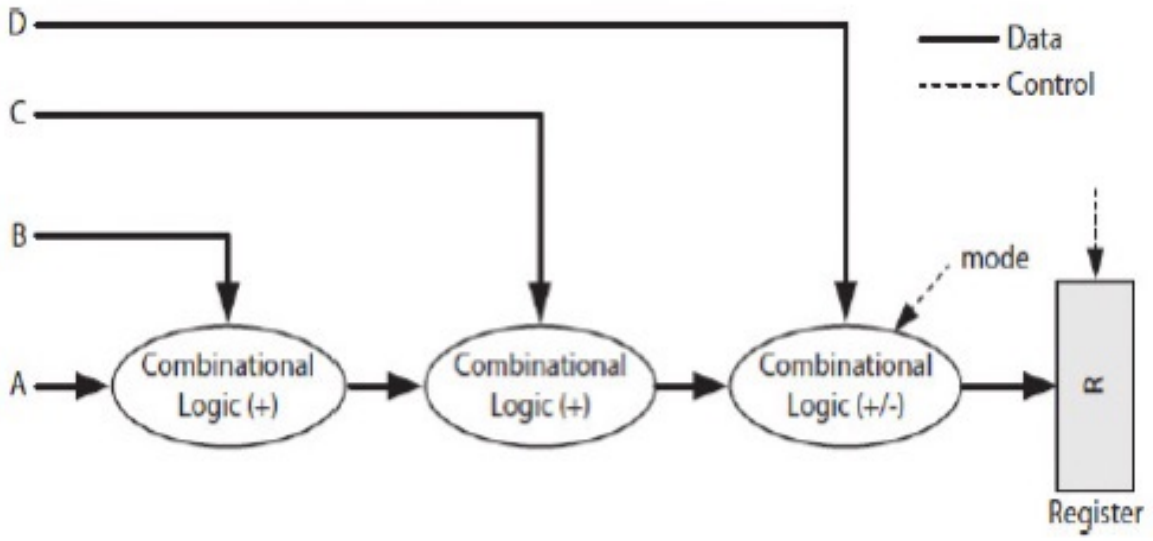

FIGURE 6.2 A single-cycle two-function data path that computes either $A + B + C + D$ or $A + B + C - D$ in one clock cycle.

$f \leq \frac{1}{\tau}$ cycles/second or Hertz (4.2 equation)

$\tau \geq 2\Delta_{ADD} + \Delta_{ADD/SUB} + \tau_{st} + \tau_{cq} + \tau_{cs}$ (6.1 equation)

$\tau \geq 2(0.8\text{ ns}) + (1.1\text{ ns}) + (0.05\text{ ns}) + (0.05\text{ ns}) + (0.05\text{ ns})$

$f \leq \frac{1}{\tau} = 350877193 \Rightarrow \boxed{f \leq 350.877\text{ MHz}}$

For problems 6.1 through 6.3: Suppose the propagation delay of an 8-bit adder is 0.8ns, adder/subtractor is 1.1ns, 2-to-1 mux is 0.3ns, and 4-to-1 mux is 0.6ns. Also, assume register setup time (), clock-to-q (), and clock-skew () are all 0.05ns. (15 points)

6.1 Calculate the required maximum clock frequency for each of the following data paths:

b. Multi-cycle data path in Fig. 6.3.

Cycle 2: $R \leftarrow R + B$
Cycle 3: $R \leftarrow R + C$
Cycle 4: If *mode* == 0 then $R \leftarrow R + D$; otherwise, $R \leftarrow R - D$

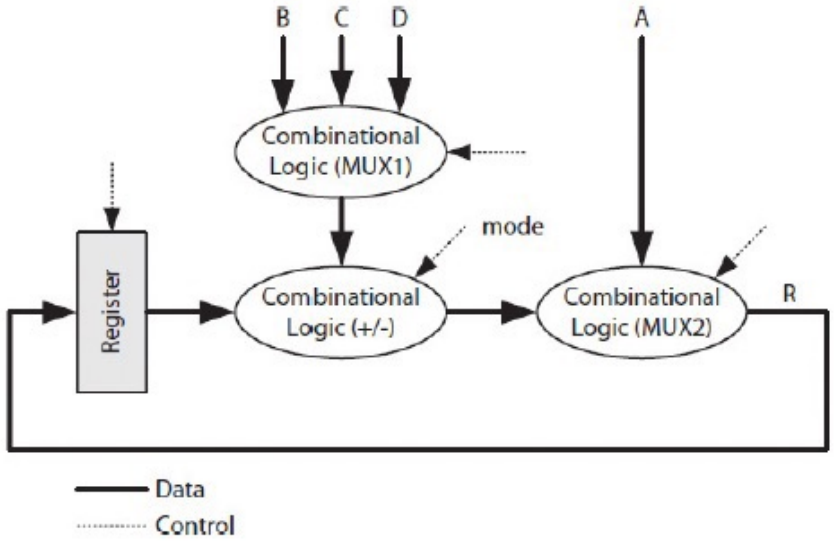

FIGURE 6.3 A multicycle data path requiring four clock cycles to compute $A + B + C + D$ or $A + B + C - D$.

$f \leq \frac{1}{\tau}$ cycles/second or Hertz (4.2 equation)

$\tau \geq \Delta_{mux1} + \Delta_{add/sub} + \Delta_{mux2} + \tau_{st} + \tau_{cq} + \tau_{cs}$ (6.2 equation)

$\tau \geq (0.3\ ns) + (1.1\ ns) + (0.6\ ns) + (0.05\ ns) + (0.05\ ns) + (0.05\ ns)$

$f \leq \frac{1}{\tau} = 465116279.1 \Rightarrow \boxed{f \leq 465.116\ MHz}$

For problems 6.1 through 6.3: Suppose the propagation delay of an 8-bit adder is 0.8ns, adder/subtractor is 1.1ns, 2-to-1 mux is 0.3ns, and 4-to-1 mux is 0.6ns. Also, assume register setup time (), clock-to-q (), and clock-skew () are all 0.05ns. (15 points)

6.1 Calculate the required maximum clock frequency for each of the following data paths:

c. Pipelined data path in Fig. 6.4.

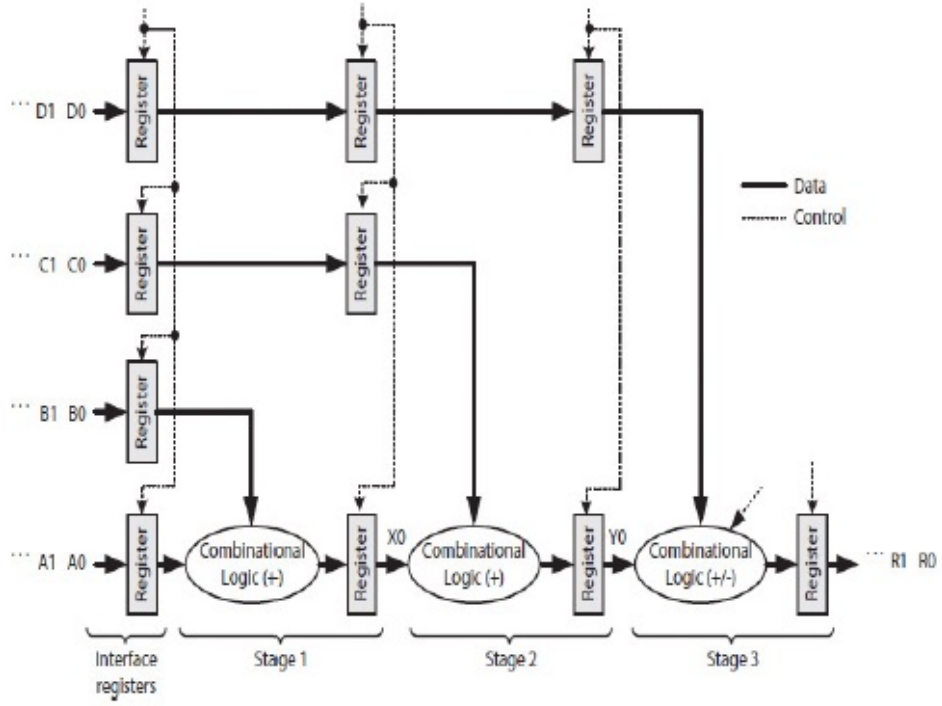

FIGURE 6.4 A two-function pipelined data path computing a stream of quantities $A_i + B_i + C_i \pm D_i$ for $i = 0, 1, 2$, etc.

$f \leq \frac{1}{\tau}$ cycles/second or Hertz (4.2 equation)

$\tau \geq \Delta_{ADD/SUB} + \tau_{st} + \tau_{cq} + \tau_{cs}$ (6.3 equation)

$\tau \geq (1.1\ ns) + (0.05\ ns) + (0.05\ ns) + (0.05\ ns)$

$f \leq \frac{1}{\tau} = 800,000,000 \Rightarrow \boxed{f \leq 800\ MHz}$

6.2 Estimate the speedup between the following data paths when generating N = 1000 quantities $A_i + B_i + C_i \pm D_i$ for i = 0, 1, 2, …, 999. Ignore the data reading and writing delays. (10 points)

a. Problem 6.1a vs. 6.1c

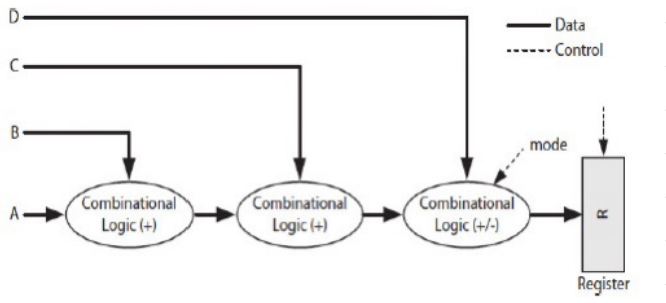

FIGURE 6.2 A single-cycle two-function data path that computes either $A + B + C + D$ or $A + B + C - D$ in one clock cycle.

VS

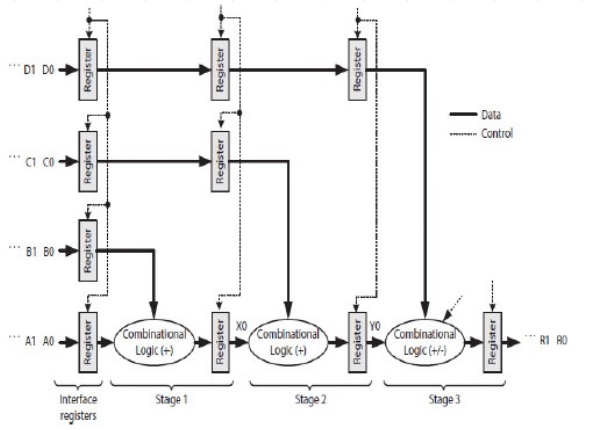

FIGURE 6.4 A two-function pipelined data path computing a stream of quantities $A_i + B_i + C_i \pm D_i$ for $i = 0, 1, 2$, etc.

$$S = \frac{\tau_{single\text{-}cycle}}{\tau_{pipeline}} = \frac{Nk\tau}{k\tau + (N-1)\tau} = \frac{Nk}{k+N-1}$$

(6.6 Equation)

$$= \frac{2(0.8\ ns) + (1.1\ ns) + (0.05\ ns) + (0.05\ ns) + (0.05\ ns)}{(1.1\ ns) + (0.05\ ns) + (0.05\ ns) + (0.05\ ns)}$$

(Using First eq.)

$S = 2.28$ seconds

$$= \frac{(1,000)(3)}{(3) + (1,000-1)}$$

(Using third eq.)

This is the correct answer

$S = 2.994$ seconds