1.6 What is the biggest positive FP number (in Decimal) that can be represented in 16-bit format using 1-bit sign, 4-bit biased exponent, and 11-bit fraction, where bias is 7?

largest floating number has exp value of 1110 and fractional part has all 1's

0 1110 11111111111

Convert 1110 to decimal

$= 1\times2^3 + 1\times2^2 + 1\times2^1 + 0\times2^0$

$= 8 + 4 + 2 + 0$

$= 14$

Calculate Biased Exponent:

$14 - 7 = 7$

IEEE-754 Decimal value is $1.\text{frac} * 2^{\text{Exponent}}$

$= 1.11111111111 * 2^7$

$= 1\times2^0 + 1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4} + 1\times2^{-5} + 1\times2^{-6} + 1\times2^{-7} + 1\times2^{-8}$
$+ 1\times2^{-9} + 1\times2^{-10} + 1\times2^{-11}$

$= 1.999511719$

$\boxed{\text{So } 1.999511719 \times 2^7 \text{ in decimal is } 255.9375}$

1.8 Do the following assuming 16-bit FP numbers with 4-bit bias exponent, bias = 7, and 11-bit fraction.

a) What real number does an FP number with sign = 0, bias exponent = 1 and fraction = 0 represent? (Answer in 4 decimal places)

0	0001	00000000000
Sign	Exponent	Fraction

Bias = 7

so Exponent becomes $1-7=-6$

Unbiased Exponent = Biased Exponent − Bias offset

~~the binary number~~ is

~~1.00000000000~~ [illegible] $\frac{1}{64}$ ~~(in binary)~~

~~so Mantissa~~

~~Mantissa value~~

Find the real number equivalent using the following equation:

$$\text{Real \#} = (-1)^S \times (1+m) \times 2^E$$

S: Sign Bit

m: Mantissa

E: Unbiased Exponent

$$= (-1)^0 \times (1+0) \times 2^{-6}$$

$$= 0.015625$$

$$\boxed{\text{Real \#} = 0.0156}$$

2.4. Proof Demorgan's Theorem $\overline{x+y} = \overline{x}\,\overline{y}$ by creating truth tables for $f = \overline{x+y}$ and $g = \overline{x}\,\overline{y}$.
Are the two truth tables identical?

$f = \overline{x+y}$

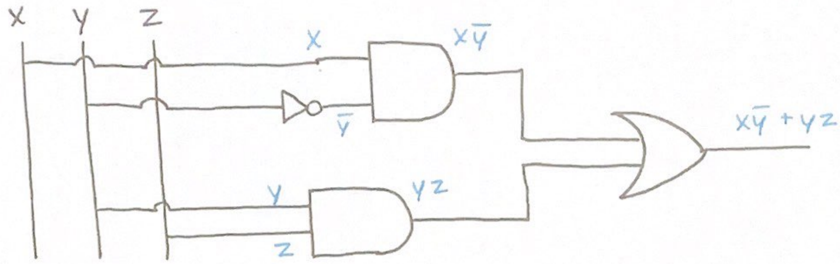
x	y	$x+y$	$\overline{x+y}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

$g = \overline{x}\,\overline{y}$

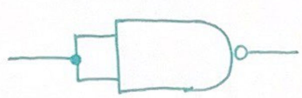
x	y	$\overline{x}$	$\overline{y}$	$\overline{x}\,\overline{y}$
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

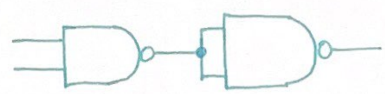
As shown in the last column of each table, we see they match, therefore $\overline{x+y} = \overline{x}\,\overline{y}$

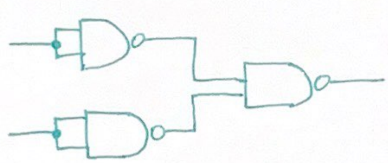
2.5. Draw the circuit schematic for $f = x\bar{y} + yz$ and then convert the schematic to NAND gates using the steps illustrated in the textbook.



We can convert NOT, AND, and OR Gates to NAND using the following configurations

NOT 

AND 

OR 

Now replace each gate with the appropriate configuration