Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, determine the upper bound for its clock frequency. (4 pts)

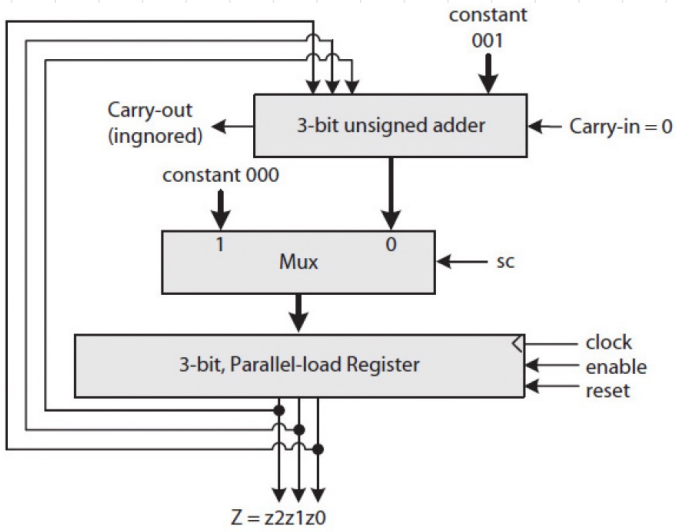


FIGURE 5.31 A synchronously cleared bit-parallel mod-8 up-counter.

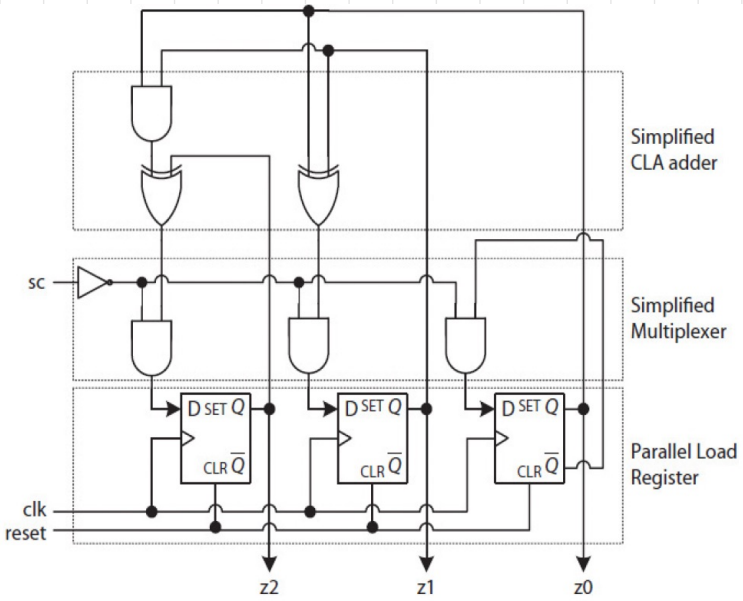


FIGURE 5.32 A synchronously cleared bit-parallel mod-8 up-counter using a simplified CLA adder and a simplified MUX.

The longest path delay for the simplified circuit is:

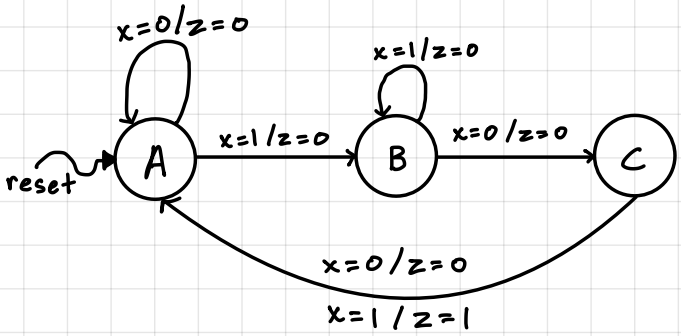
$$\Delta_{AND} + \Delta_{XOR} + \Delta_{AND} = 0.2 + 0.3 + 0.2 = 0.7 \text{ ns}$$

$$T \geq 0.7 + 3(0.1) = 1.0 \text{ ns}$$

$$F \leq 1 \text{ GHz}$$

Problem II: Textbook problem 5.9 assuming the unknown state are ignored (don't care) in the design. (5 pts)

5.9. Design a Mealy sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and draw the circuit schematic similar to the one shown in Fig. 5.16.



A = 00
B = 01
C = 10

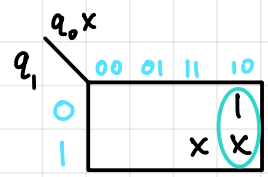
Number of bits = $\text{Log}_2[k]$, where k = # of states

$\log_2(3) = 2$

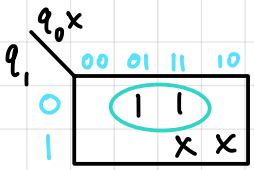
Current State q_1 q_0	Input x	Next State d_1 d_0	Output z
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	1 0	0
0 1	1	0 1	0
1 0	0	0 0	0
1 0	1	0 0	1
1 1	0	x x	x
1 1	1	x x	x

$d_1 = \bar{q}_1 q_0 \bar{x}$ $\quad d_0 = \bar{q}_1 \bar{q}_0 x + \bar{q}_1 q_0 x$

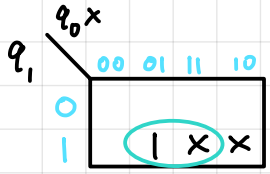
$z = q_1 \bar{q}_0 x$



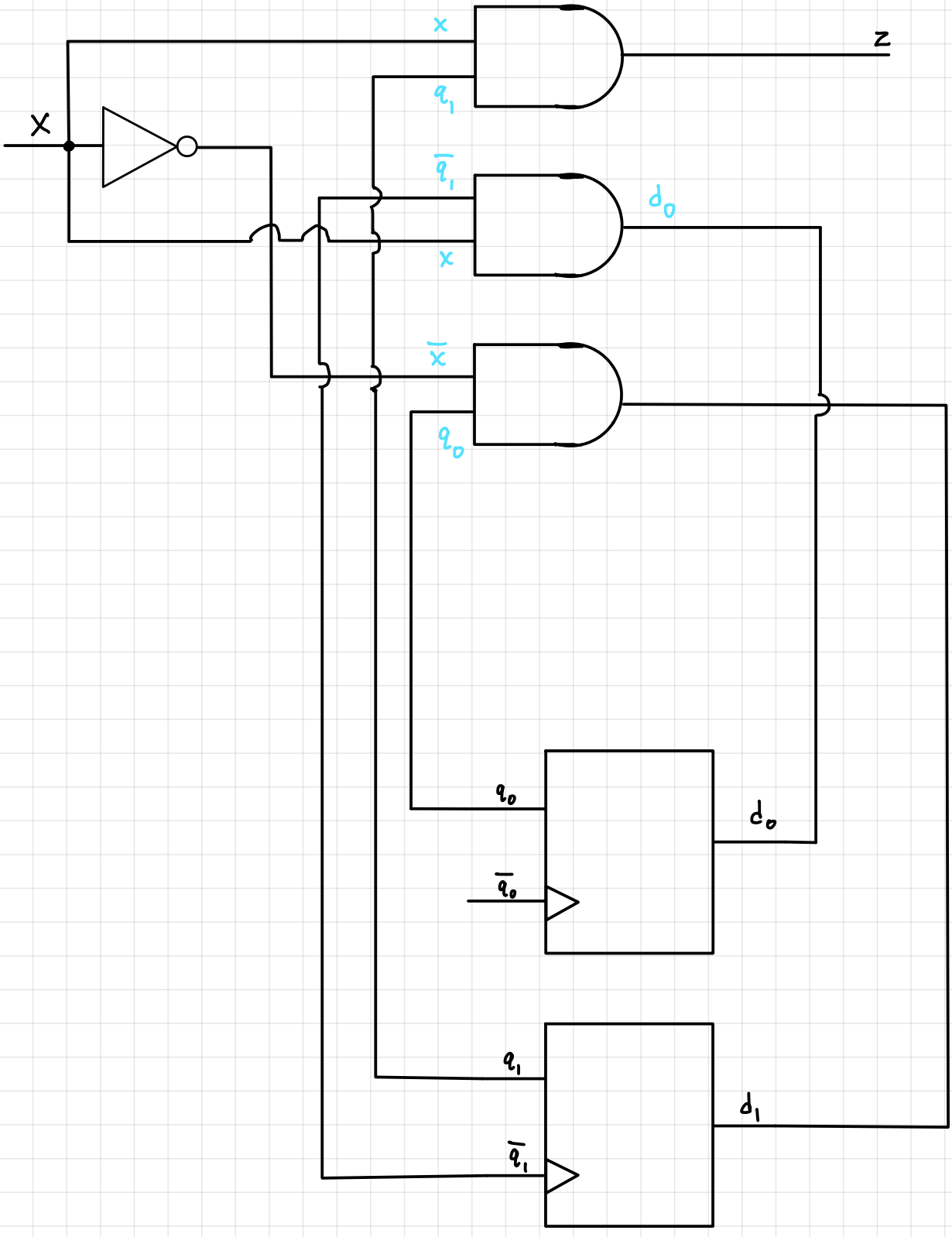
$d_1 = q_0\bar{x}$



$d_0 = \bar{q}_1 x$



$z = q_1 x$



Problem III: Textbook problem 5.11 (only FSD) (3 pts)

5.11. Design a Mealy sequence recognizer that detects the overlapping sequence "1001." Use binary encoded state labels.