5.8. Design a Moore sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and design and draw the circuit schematic similar to the one shown in Fig. 5.16. (4 pts)

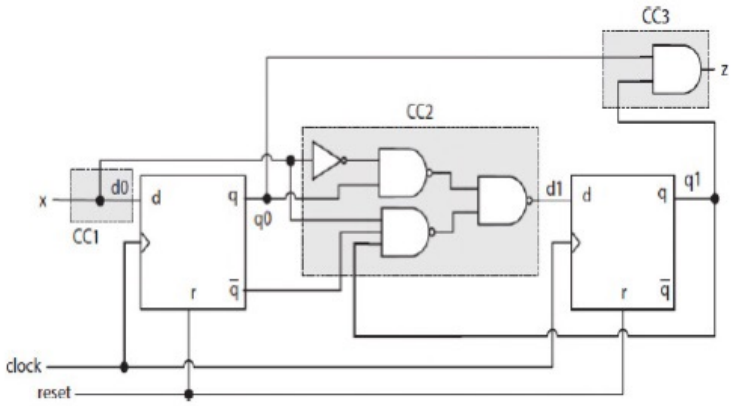
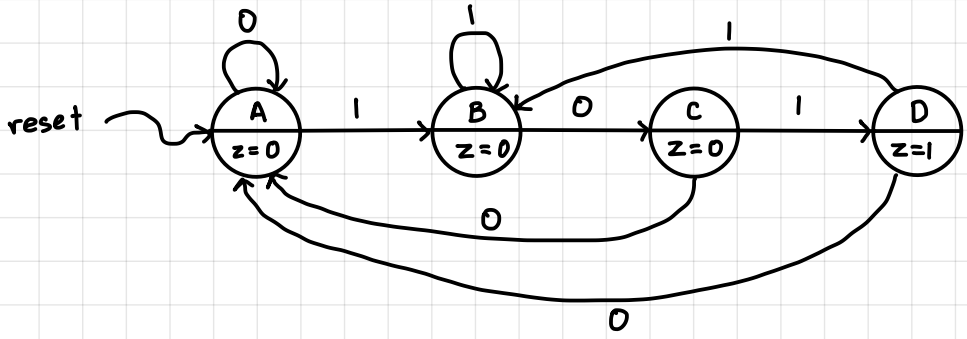


FIGURE 5.16 An alternative and typical layout for the circuit shown in Fig. 5.15.

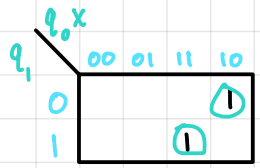


Number of bits = $\text{Log}_2[k]$, where k = # of states

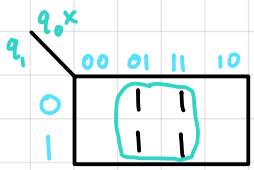
$$\log_2(4) = 2$$

A = 0 0 , B = 0 1, C = 10, D = 11

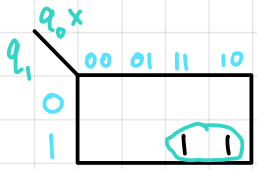
Current State		Input	Next State		Output
q_1	q_0	x	d_1	d_0	z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	1	1



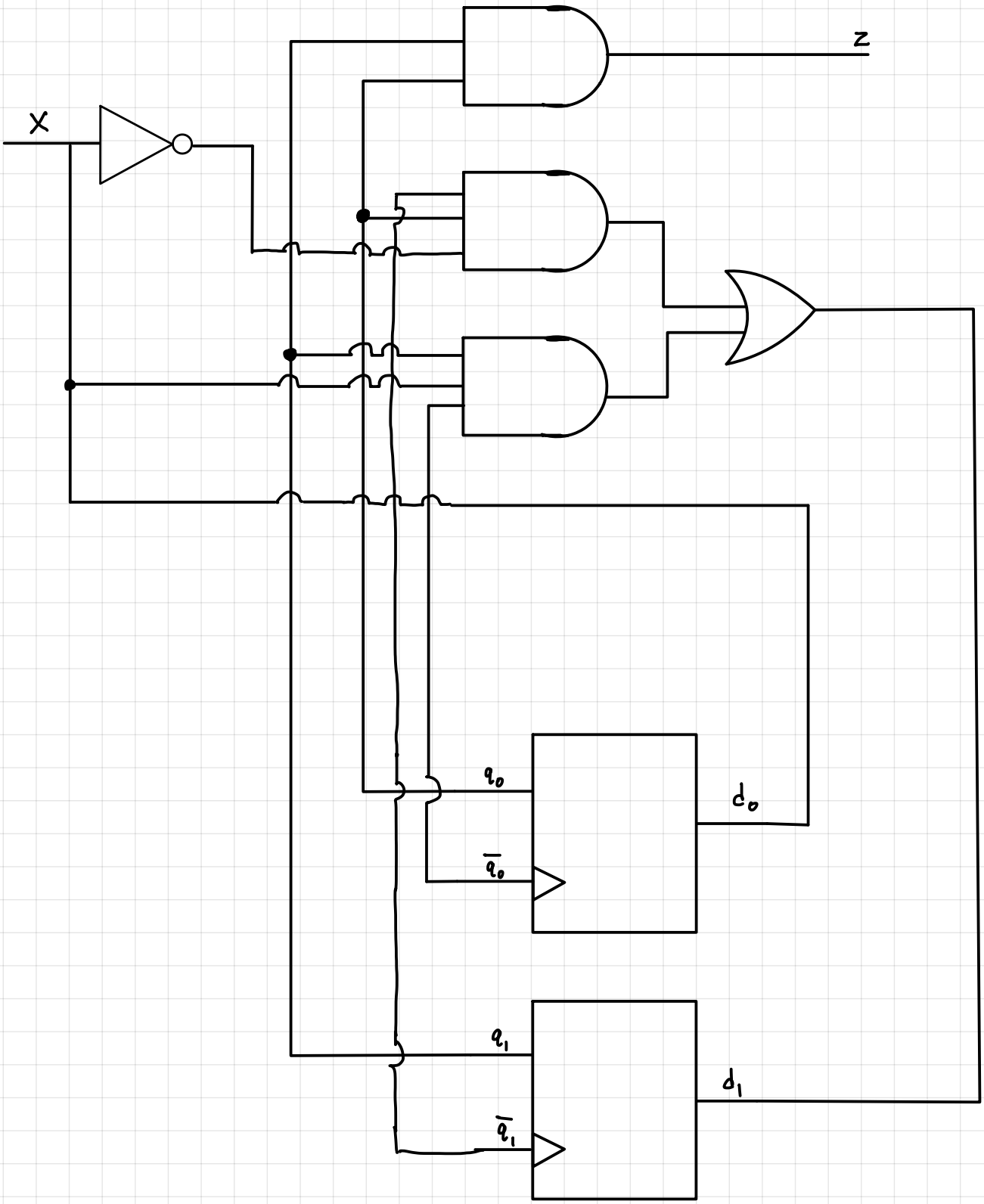
$d_1 = \bar{q}_1 q_0 \bar{x} + q_1 \bar{q}_0 x$



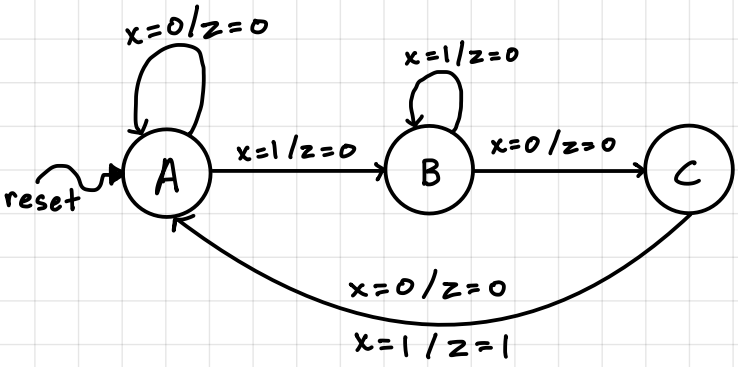
$d_0 = x$



$z = q_1 q_0$


z
x
q_0
$\bar{q}_0$
d_0
q_1
$\bar{q}_1$
d_1

5.9. Design a Mealy sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and draw the circuit schematic similar to the one shown in Fig. 5.16. (4 pts)



A = 00
B = 01
C = 10

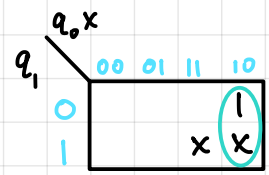
Number of bits = $\text{Log}_2[k]$, where k = # of states

$\log_2(3) = 2$

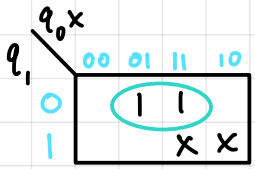
Current State q_1 q_0	Input x	Next State d_1 d_0	Output z
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	1 0	0
0 1	1	0 1	0
1 0	0	0 0	0
1 0	1	0 0	1
1 1	0	x x	x
1 1	1	x x	x

$d_1 = \bar{q}_1 q_0 \bar{x}$ $\quad d_0 = \bar{q}_1 \bar{q}_0 x + \bar{q}_1 q_0 x$

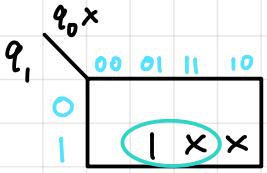
$z = q_1 \bar{q}_0 x$



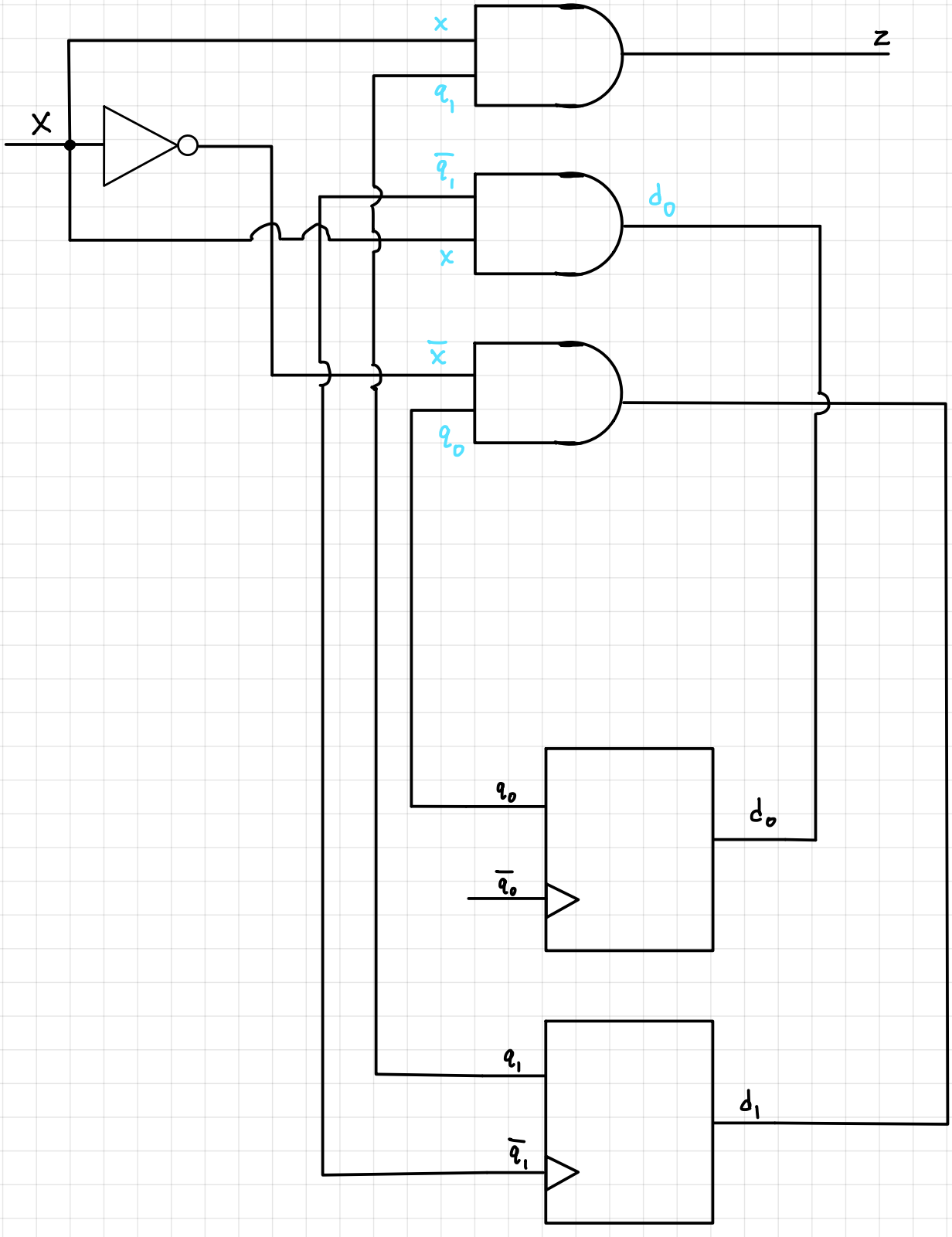
$d_1 = q_0\overline{x}$



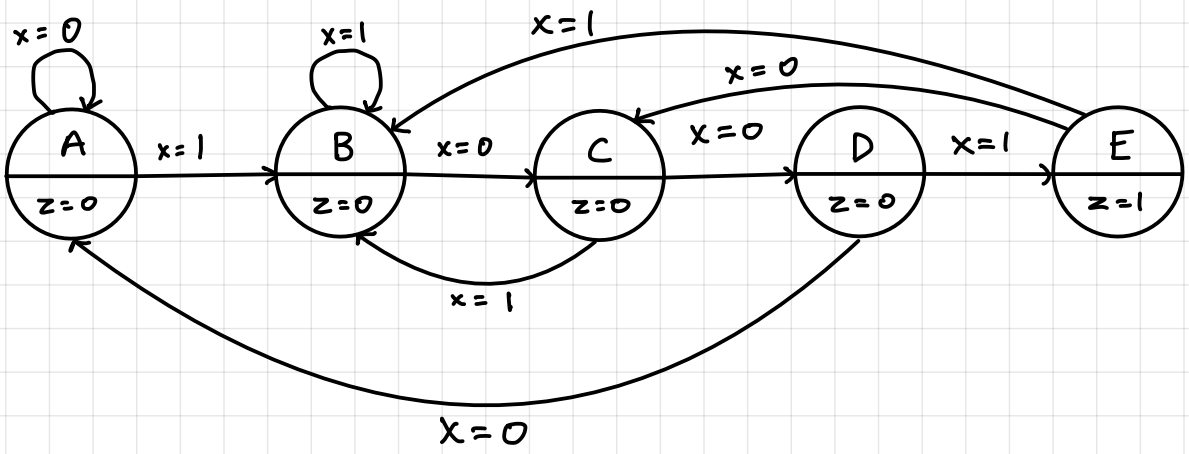
$d_0 = \overline{q}_1 x$



$z = q_1 x$



5.10. Design a Moore sequence recognizer that detects the overlapping sequence "1001." Use binary encoded state labels. . (Step 1. FSD only) (4 pts)



5.11. Design a Mealy sequence recognizer that detects the overlapping sequence "1001." Use binary encoded state labels. .(Step 1. FSD only) (4 pts)