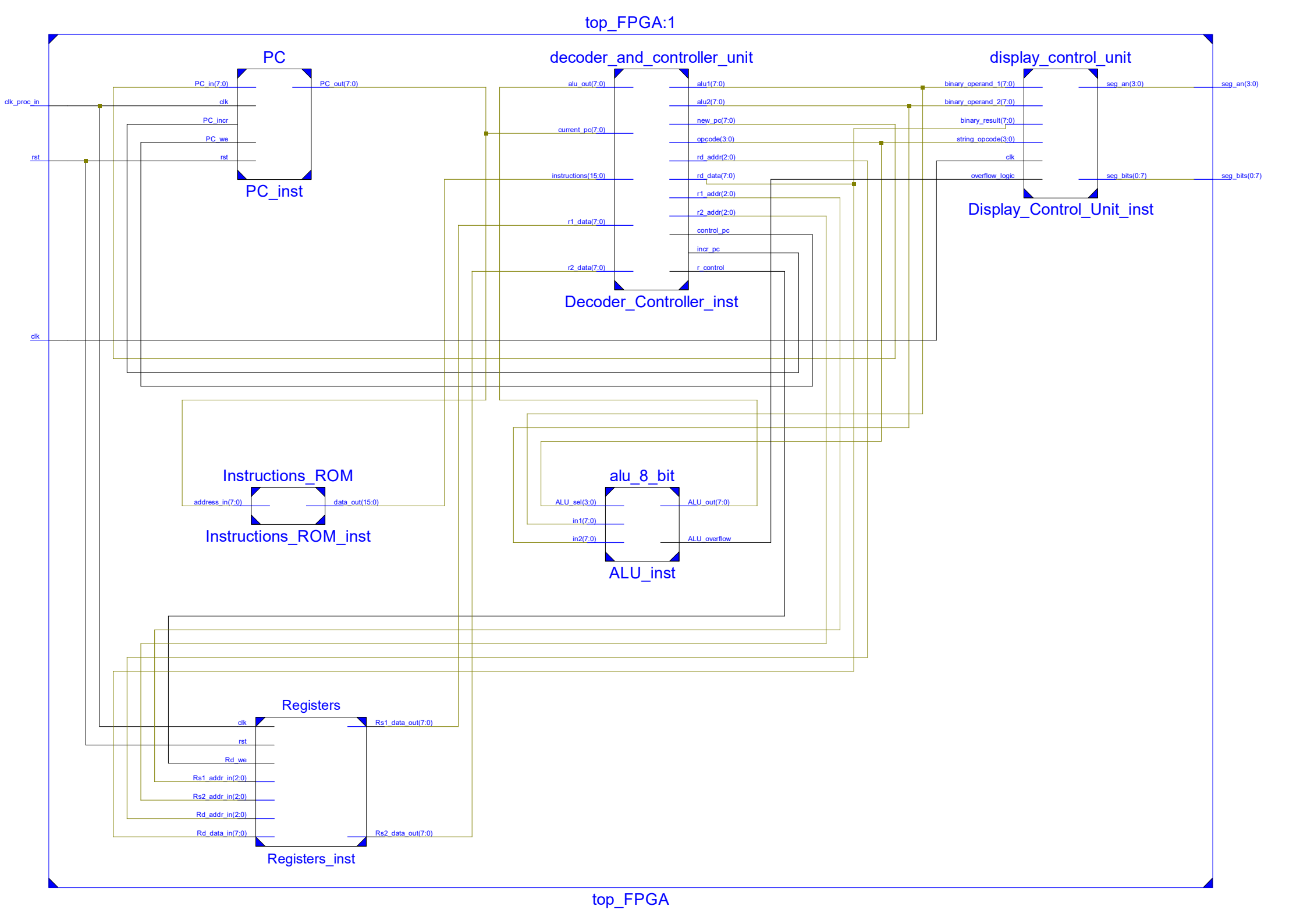
top_FPGA:1
PC
PC_in(7:0)
clk
PC_incr
PC_we
rst
PC_out(7:0)
PC_inst
clk_proc_in
rst
decoder_and_controller_unit
alu_out(7:0)
current_pc(7:0)
instructions(15:0)
r1_data(7:0)
r2_data(7:0)
alu1(7:0)
alu2(7:0)
new_pc(7:0)
opcode(3:0)
rd_addr(2:0)
rd_data(7:0)
r1_addr(2:0)
r2_addr(2:0)
control_pc
incr_pc
r_control
Decoder_Controller_inst
display_control_unit
binary_operand_1(7:0)
binary_operand_2(7:0)
binary_result(7:0)
string_opcode(3:0)
clk
overflow_logic
seg_an(3:0)
seg_bits(0:7)
seg_an(3:0)
seg_bits(0:7)
Display_Control_Unit_inst
clk
Instructions_ROM
address_in(7:0)
data_out(15:0)
Instructions_ROM_inst
alu_8_bit
ALU_sel(3:0)
in1(7:0)
in2(7:0)
ALU_out(7:0)
ALU_overflow
ALU_inst
Registers
clk
rst
Rd_we
Rs1_addr_in(2:0)
Rs2_addr_in(2:0)
Rd_addr_in(2:0)
Rd_data_in(7:0)
Rs1_data_out(7:0)
Rs2_data_out(7:0)
Registers_inst
top_FPGA