top_FPGA Project Status (05/13/2019 - 16:37:30)			
Project File:	Processor.xise	**Parser Errors:**	
Module Name:	top_FPGA	**Implementation State:**	Programming File Generated
Target Device:	xc3s100e-4cp132	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	1 Warning (1 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	117	1,920	6%	
Number of 4 input LUTs	435	1,920	22%	
Number of occupied Slices	277	960	28%	
Number of Slices containing only related logic	277	277	100%	
Number of Slices containing unrelated logic	0	277	0%	
Total Number of 4 input LUTs	476	1,920	24%	
Number used as logic	435			
Number used as a route-thru	41			
Number of bonded IOBs	15	83	18%	
Number of BUFGMUXs	2	24	8%	
Average Fanout of Non-Clock Nets	3.85			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon May 13 16:37:03 2019	0	0	4 Infos (4 new)
Translation Report	Current	Mon May 13 16:37:07 2019	0	0	0
Map Report	Current	Mon May 13 16:37:11 2019	0	0	2 Infos (2 new)
Place and Route Report	Current	Mon May 13 16:37:18 2019	0	1 Warning (1 new)	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Mon May 13 16:37:20 2019	0	0	6 Infos (6 new)
Bitgen Report	Current	Mon May 13 16:37:24 2019	0	0	0

Secondary Reports [-]		
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Out of Date	Mon May 13 15:25:32 2019
WebTalk Report	Current	Mon May 13 16:37:25 2019
WebTalk Log File	Current	Mon May 13 16:37:30 2019

Date Generated: 05/13/2019 - 16:38:02