

A B C D

Layer Stack Legend

Material Thickness Dielectric Material Type Layer Gerber Top Overlay Legend GTO Surface Material Top Solder 0.01mm Solder Resist Solder Mask GTS Top Layer Copper 0.04mm Signal GTL 1.50mm FR-4 Dielectric Copper Bottom Layer 0.04mm GBL Signal -Surface Material Bottom Solder 0.01mm Solder Resist Solder Mask GBS Bottom Overlay GBO Legend

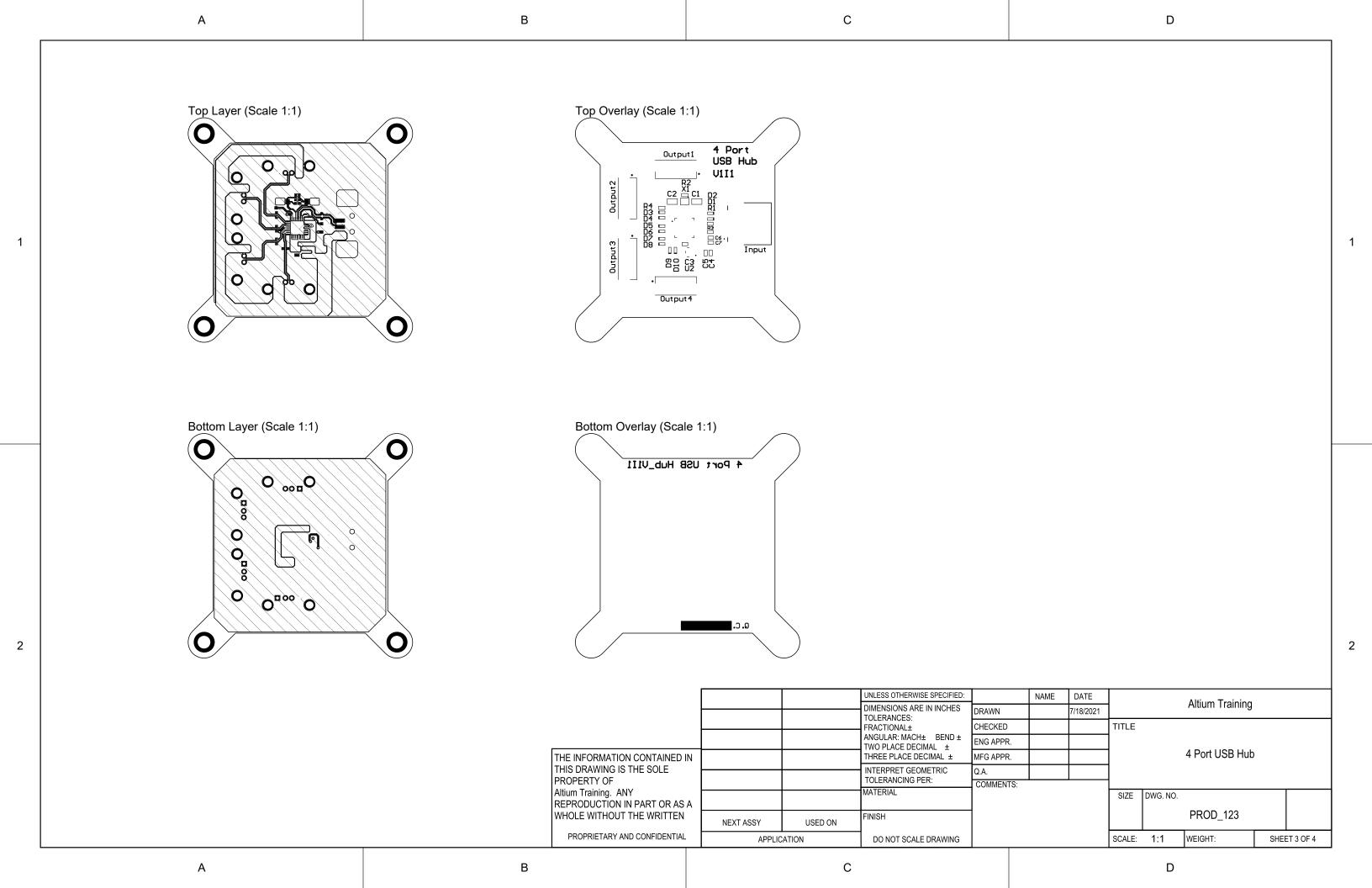
Total thickness: 1.59mm

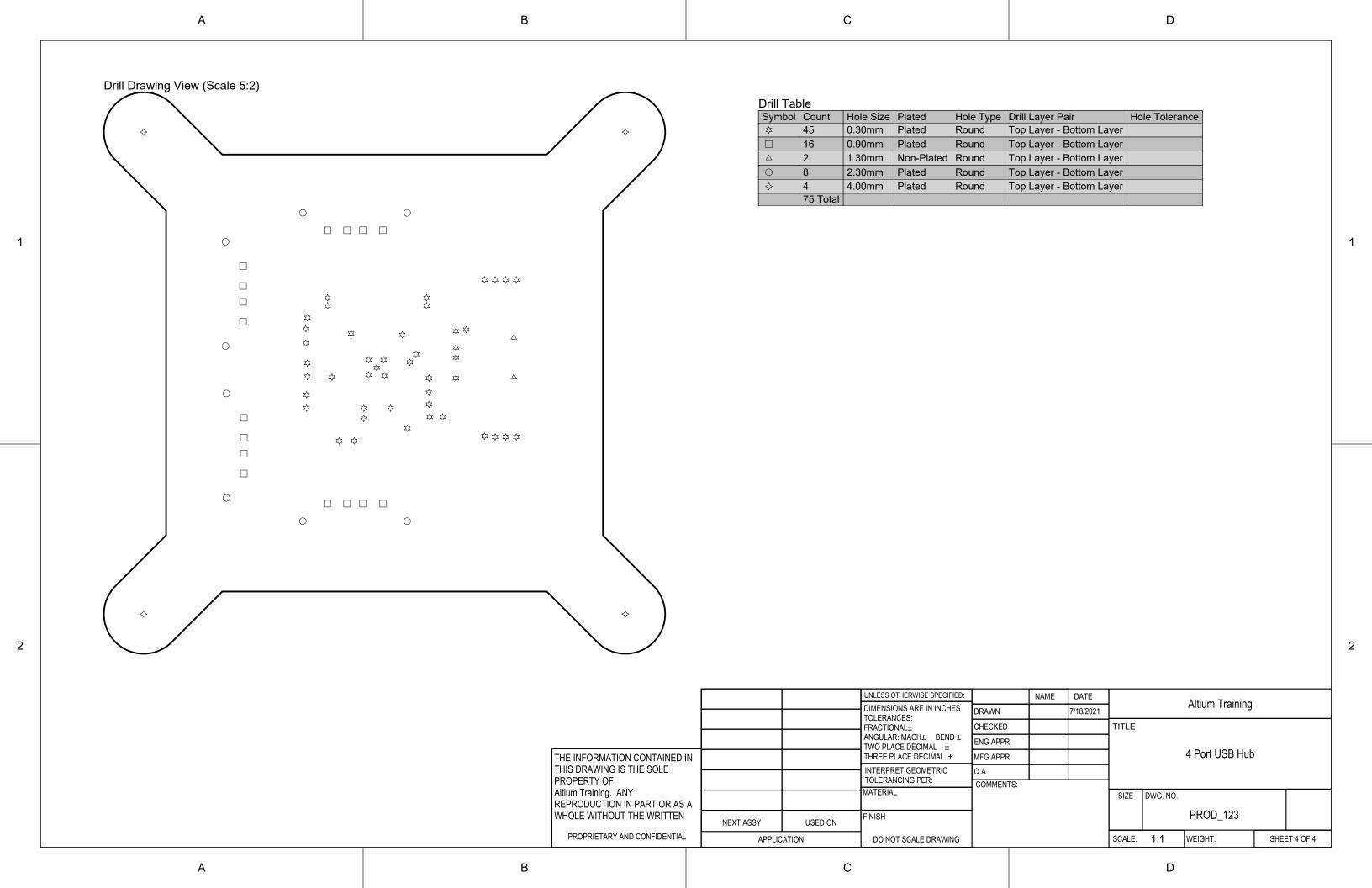
Bill Of Materials

Line #	Designator	Name	Quantity	Manufacturer Part Number
1	C1, C2	18pF,50V	2	C0805C180J5GACTU
2	C3, C7	1uF,6.3V	2	C0402C105K9PACTU
3	C4, C5, C6	4.7uF,6.3V	3	GRM155R60J475ME47 D
4	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10	TVS	10	ESD9B3.3ST5G
5	J1	SMD USB-A	1	USB-A-S-S-B-SM2
6	J2, J3, J4, J5	USB-A	4	KUSBVX-AS1N-B30
7	R1, R3	56K	2	RC0402JR-0756KL
8	R2	1M	1	RC0402FR-071ML
9	R4	12K	1	RC0402JR-0712KL
10	U1	USB2514B-I/M2	1	USB2514B-I/M2
11	U2	MIC5504-3.3YM5-TR	1	MIC5504-3.3YM5-TR
12	X1	24MHz	1	XRCGB24M000F0L00 R0

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			UNLESS OTHERWISE SPECIFIED:		NAME	DATE			Altium Training	
			TOLERANCES: FRACTIONAL± ANGULAR: MACH± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± INTERPRET GEOMETRIC	DRAWN		7/18/2021	- Altium Training			
				CHECKED			TITLE			
				ENG APPR.			4 Port USB Hub			
THE INFORMATION CONTAINED IN				MFG APPR.						
THIS DRAWING IS THE SOLE				Q.A.						
PROPERTY OF			TOLERANCING PER: MATERIAL	COMMENTS:						
Altium Training. ANY REPRODUCTION IN PART OR AS A			IWATERIAL			SIZE	DWG. NO.			
WHOLE WITHOUT THE WRITTEN	NEXT ASSY	USED ON	FINISH						PROD_123	
PROPRIETARY AND CONFIDENTIAL	APPLIC	ATION	DO NOT SCALE DRAWING				SCALE:	1:1	WEIGHT:	SHEET 2 OF

A B C





Electrical Rules Check Report

Class	Document	Message
		Successful Compile for 4-Port_USB_HUB_Project.PrjPcb

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Design Rules Verification Report

Filename: C:\Users\Amit\Documents\AMIT\Github\4-Port_USB_HUB\Design Files\V1I1\4-Po

Warnings 0
Rule Violations 13

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.1mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.1mm) (Max=10mm) (Preferred=0.254mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	4
Hole To Hole Clearance (Gap=0.1mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	4
Silk To Solder Mask (Clearance=0.1mm) (IsPad),(All)	4
Silk to Silk (Clearance=0.1mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	1
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff3_90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff4_90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff90'))	0
Matched Lengths(Tolerance=25.4mm) (Disabled)(InDifferentialPairClass('diff90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff2_90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff90'))	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPairClass('diff1_90'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	13

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)

Hole Size Constraint: (4mm > 2.54mm) Pad Free-1(162.786mm,43.307mm) on Multi-Layer Actual Hole Size = 4mm

Hole Size Constraint: (4mm > 2.54mm) Pad Free-2(223.442mm,43.307mm) on Multi-Layer Actual Hole Size = 4mm

Hole Size Constraint: (4mm > 2.54mm) Pad Free-3(223.442mm,103.964mm) on Multi-Layer Actual Hole Size = 4mm

Hole Size Constraint: (4mm > 2.54mm) Pad Free-4(162.786mm,103.964mm) on Multi-Layer Actual Hole Size = 4mm

Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)

Minimum Solder Mask Sliver Constraint: (0.097mm < 0.1mm) Between Pad U1-1(189.323mm,76.316mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.1mm) Between Pad U1-10(190.138mm,71.501mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.1mm) Between Pad U1-18(194.138mm,71.501mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.1mm) Between Pad U1-27(194.953mm,76.316mm) on Top Layer And Pad

Silk To Solder Mask (Clearance=0.1mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.095mm < 0.1mm) Between Pad C1-1(195.15mm,82.6mm) on Top Layer And Track

Silk To Solder Mask Clearance Constraint: (0.095mm < 0.1mm) Between Pad C1-2(196.9mm,82.6mm) on Top Layer And Track

Silk To Solder Mask Clearance Constraint: (0.095mm < 0.1mm) Between Pad C2-1(189.2mm,82.6mm) on Top Layer And Track

Silk To Solder Mask Clearance Constraint: (0.095mm < 0.1mm) Between Pad C2-2(187.45mm,82.6mm) on Top Layer And Track

Net Antennae (Tolerance=0mm) (All)

Net Antennae: Via (197.1mm,76mm) from Top Layer to Bottom Layer

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