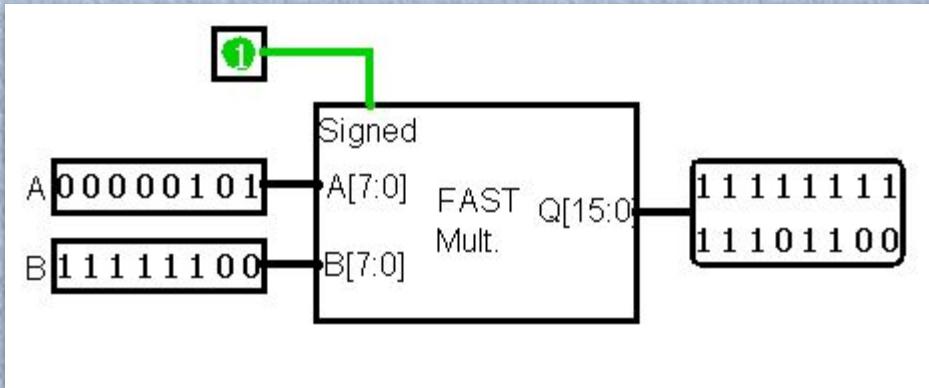


Fast Multiplier



*"This presentation is
brought to you by..."*

Riley Guidry

Alberto Rosas

Dang Tran

All made possible with...



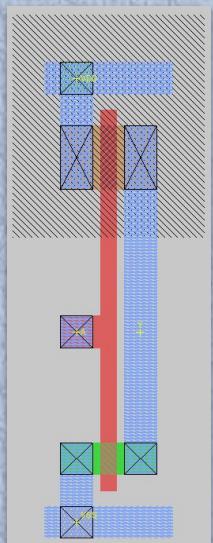
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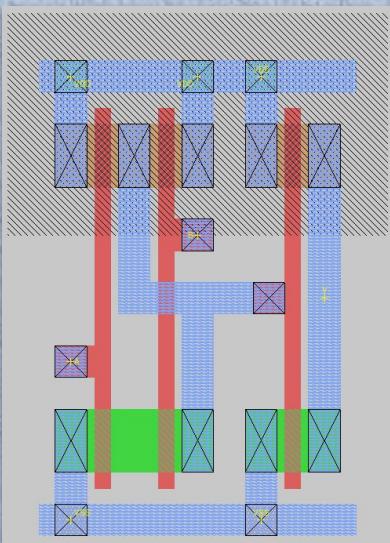
Overview

The fast multiplier utilizes the *Wallace tree* method, a high-speed multiplier architecture that performs fast multiplication of binary numbers. It efficiently reduces the number of partial products and optimizes the addition process using a structured tree-based approach. This results in reduced critical path delay and improved overall performance compared to traditional multiplication algorithms, especially for large operands.

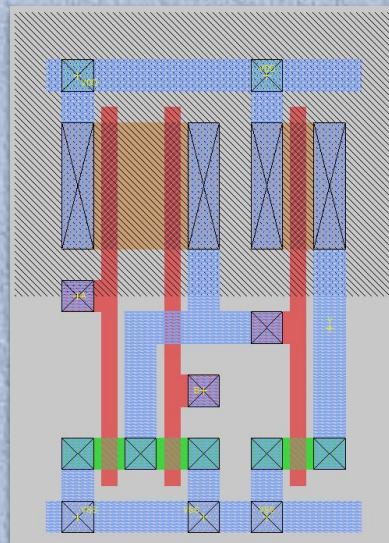
Basic Gates



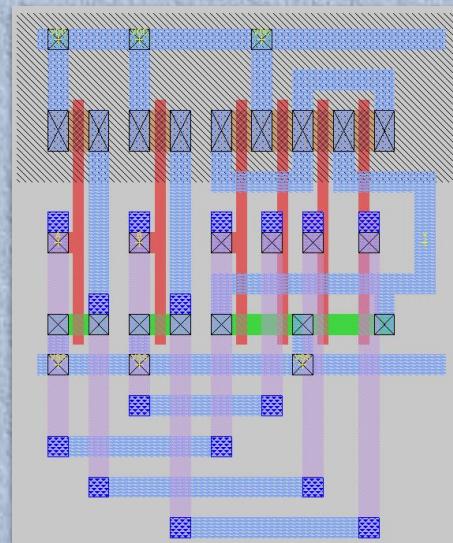
INV



AND-2

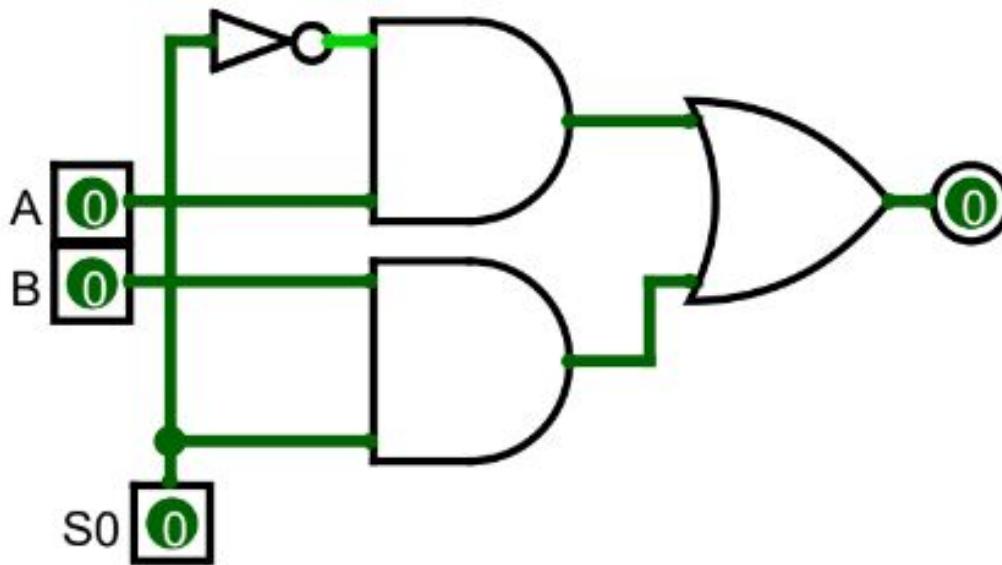


OR-2



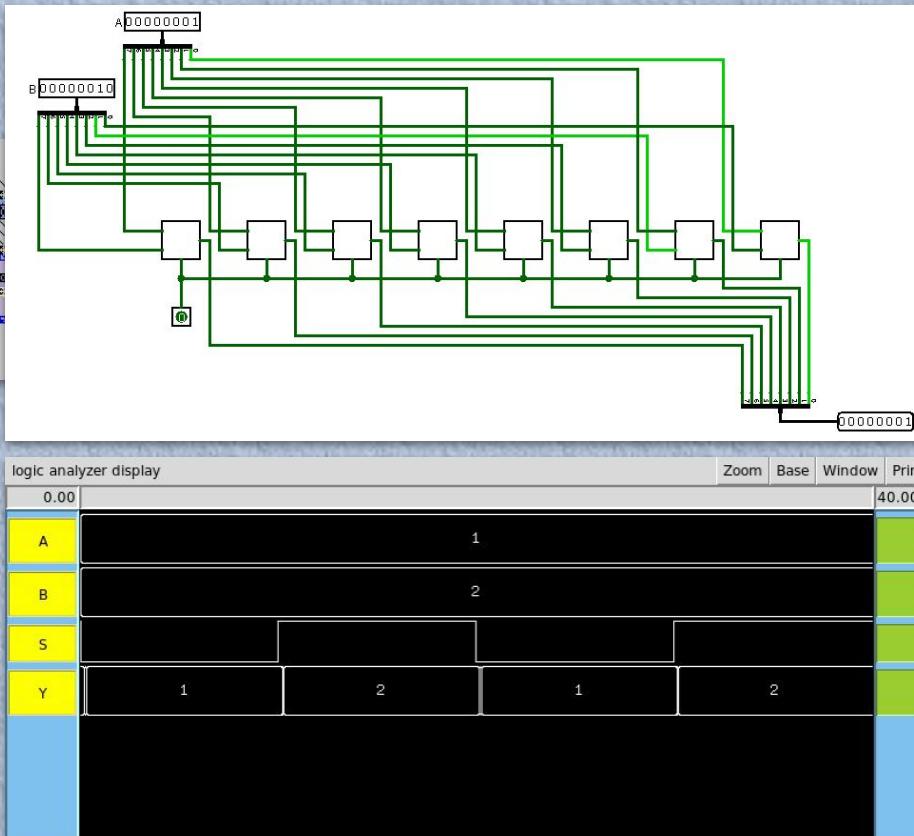
XOR-2

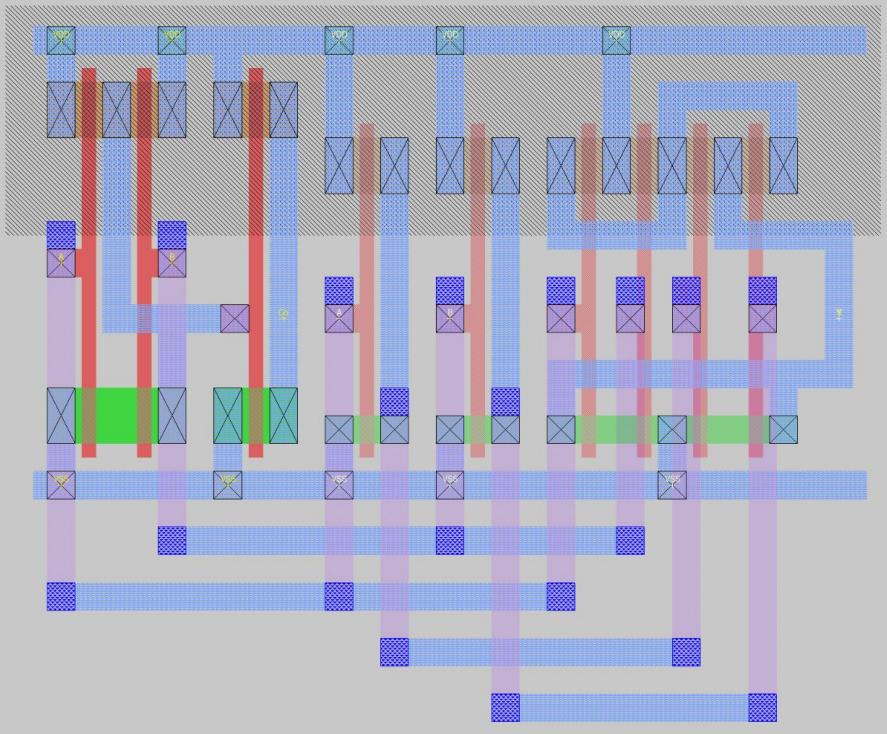
mux2x1



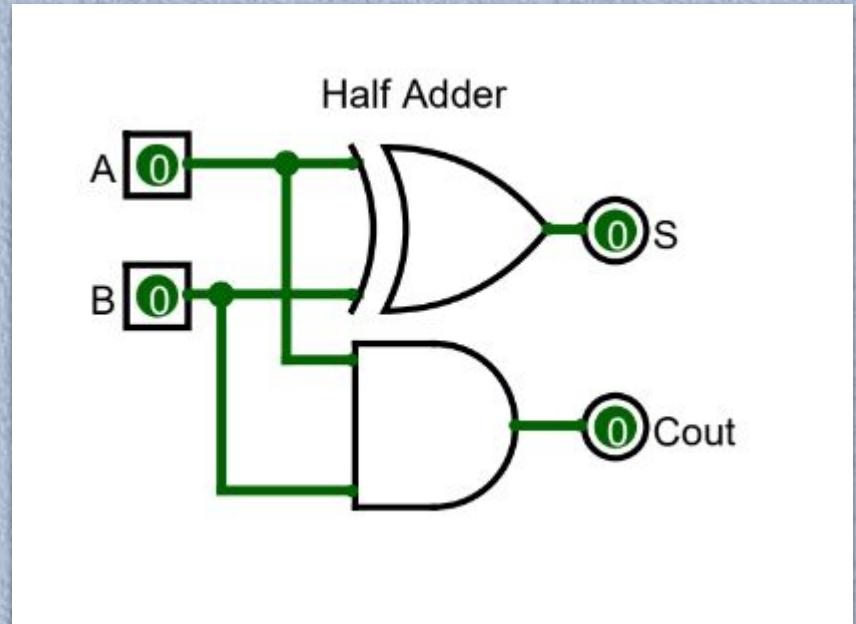
1-bit 2x1 MUX

8-bit 2x1 Multiplexer

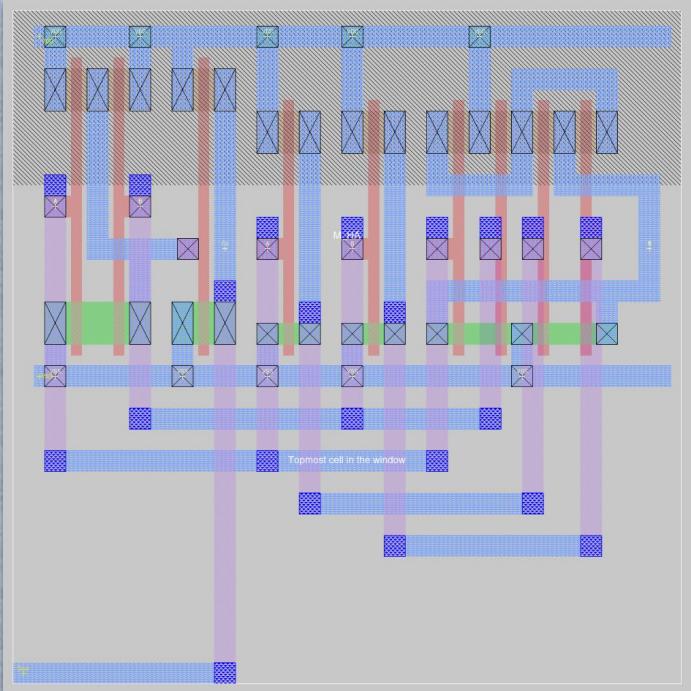




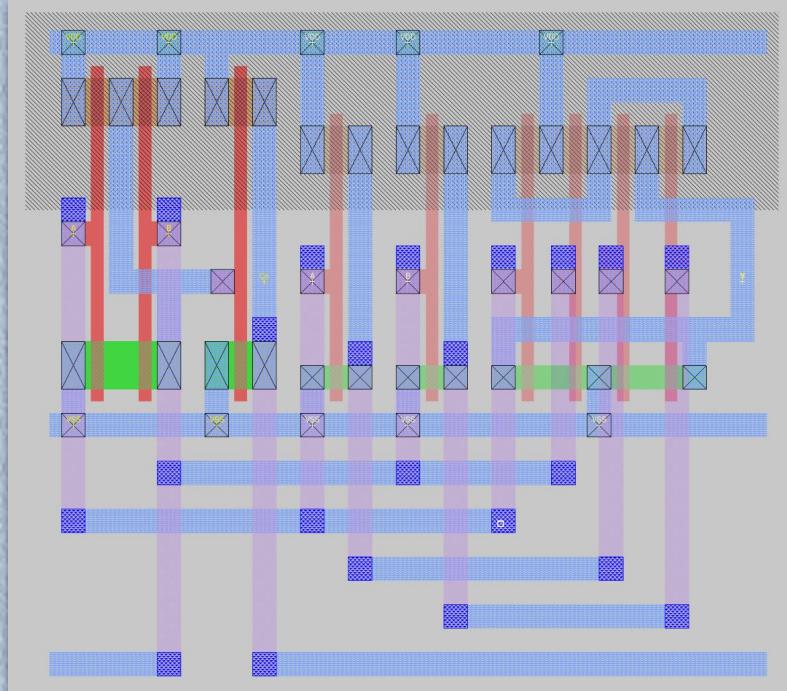
Half Adder



M_HA

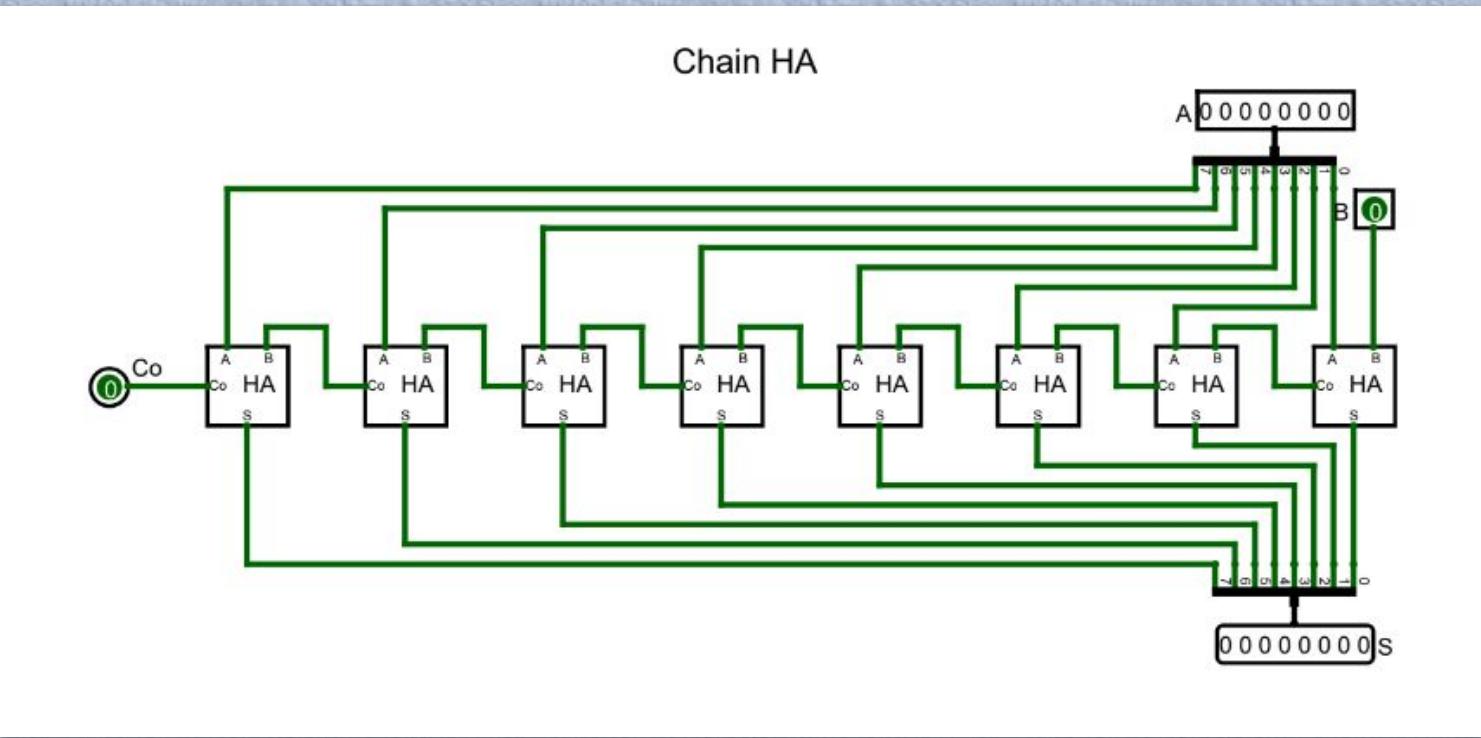


Chain_HA

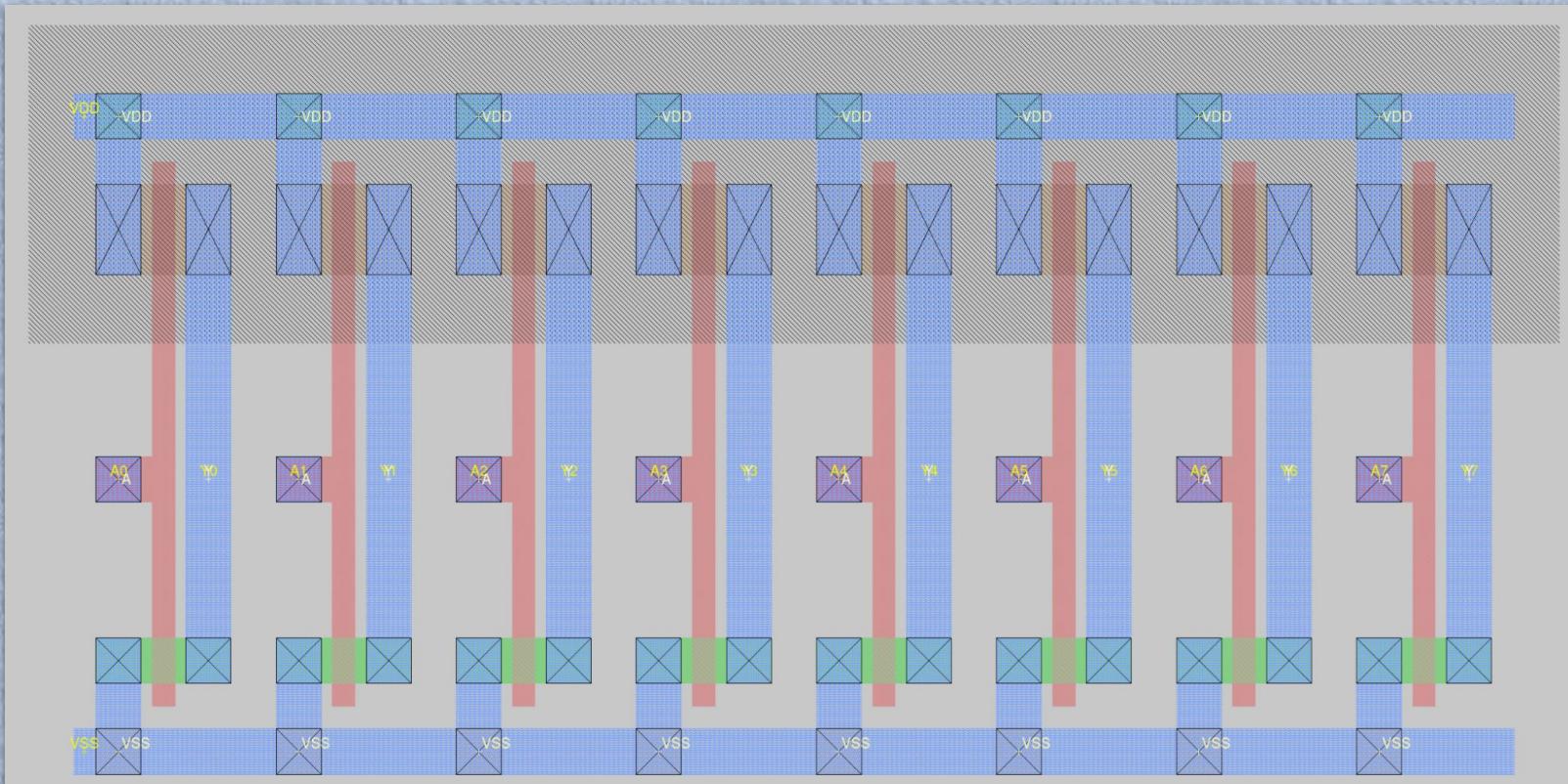


Versions of Half Adder

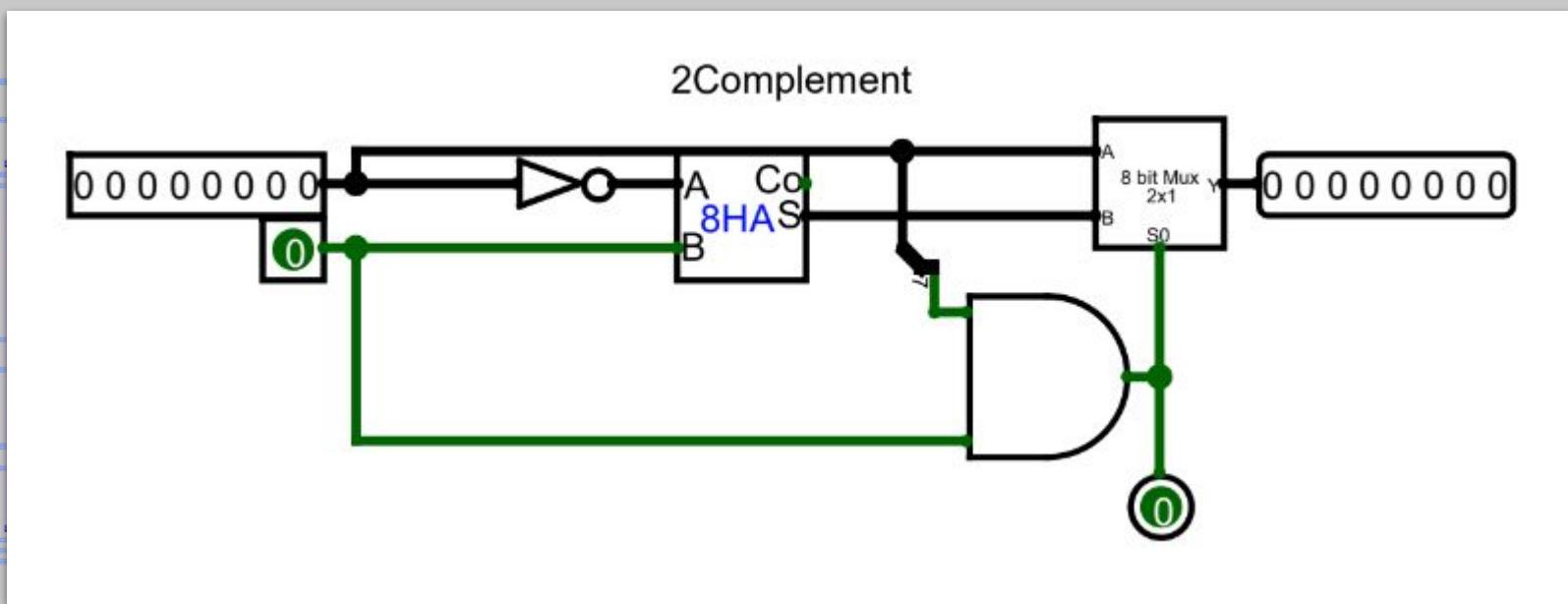
8-bit Adder



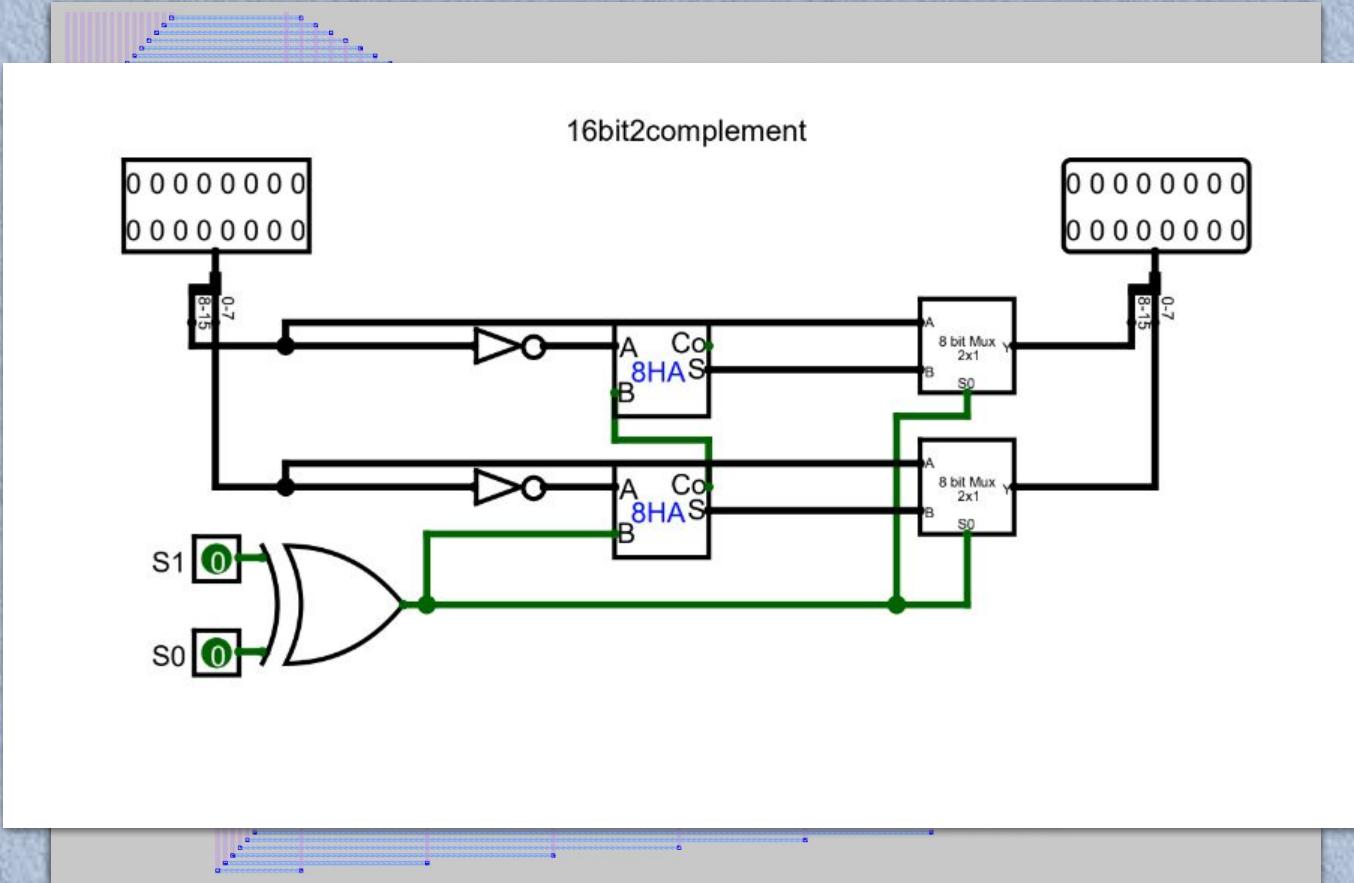
8-bit Inverter



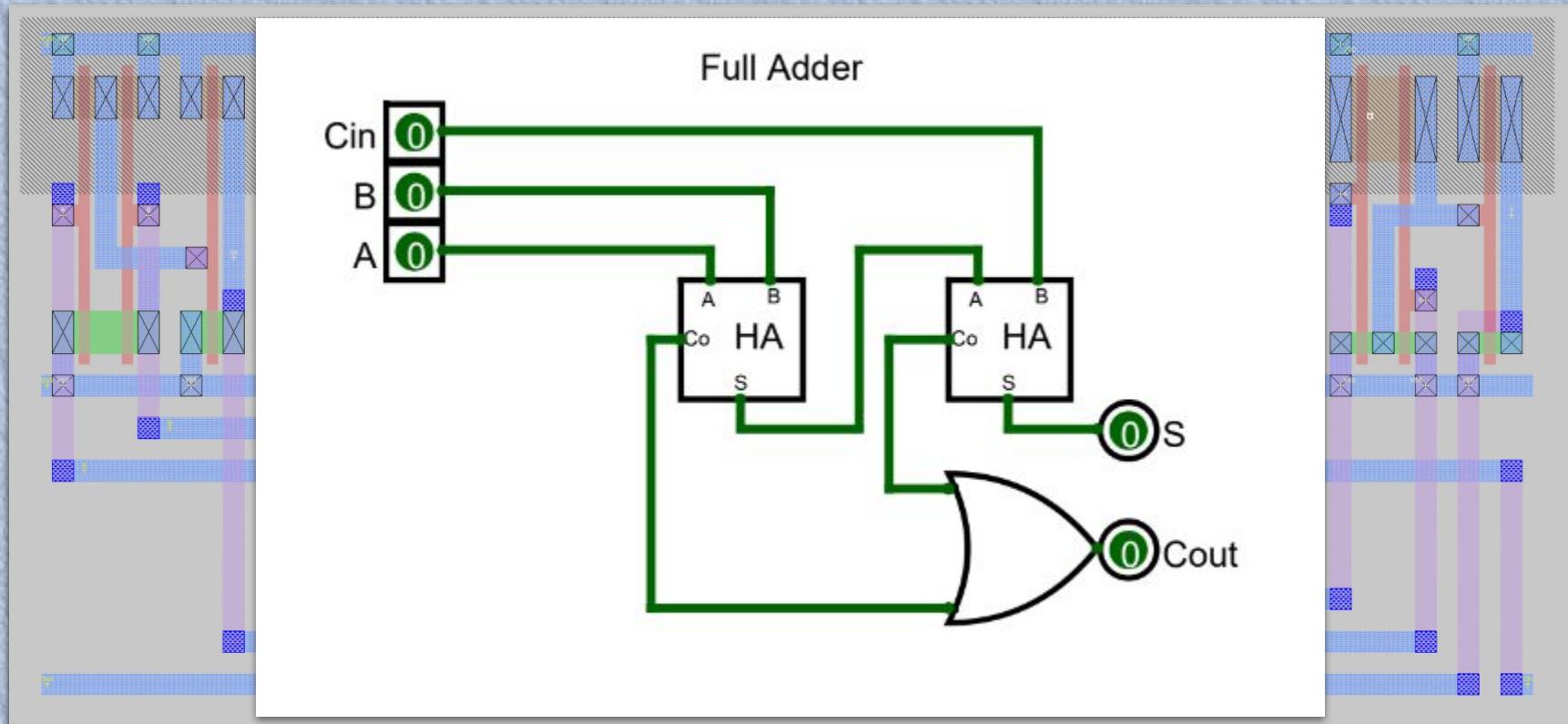
8-bit 2's Complement



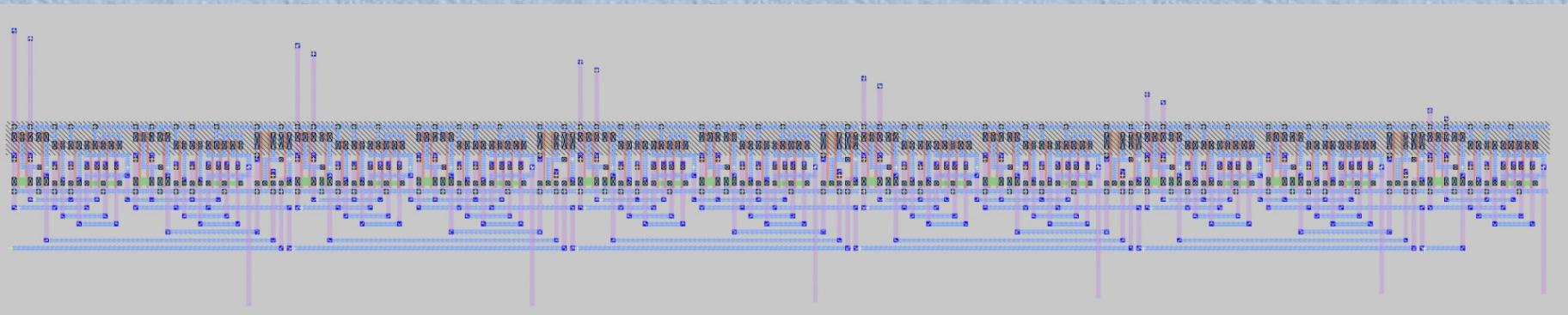
16-bit 2's Complement



Full Adder



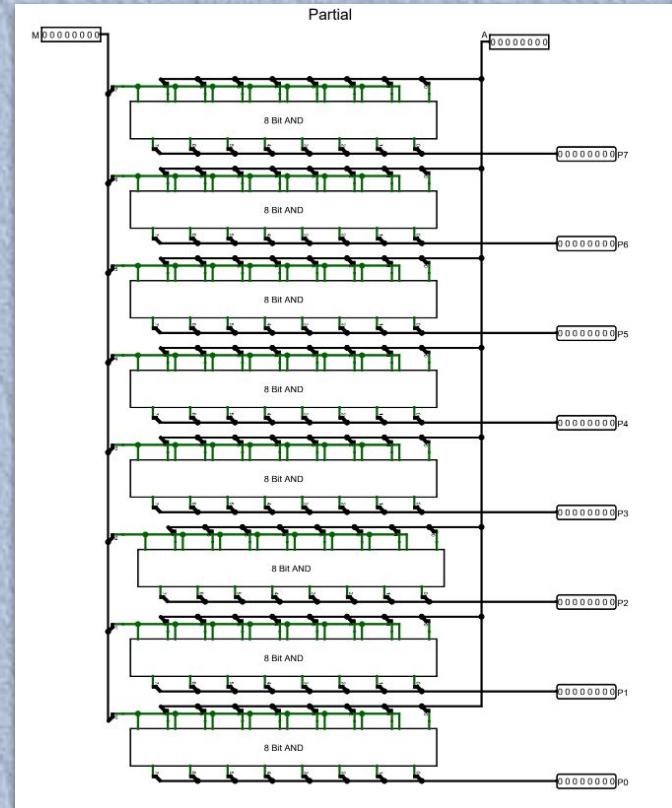
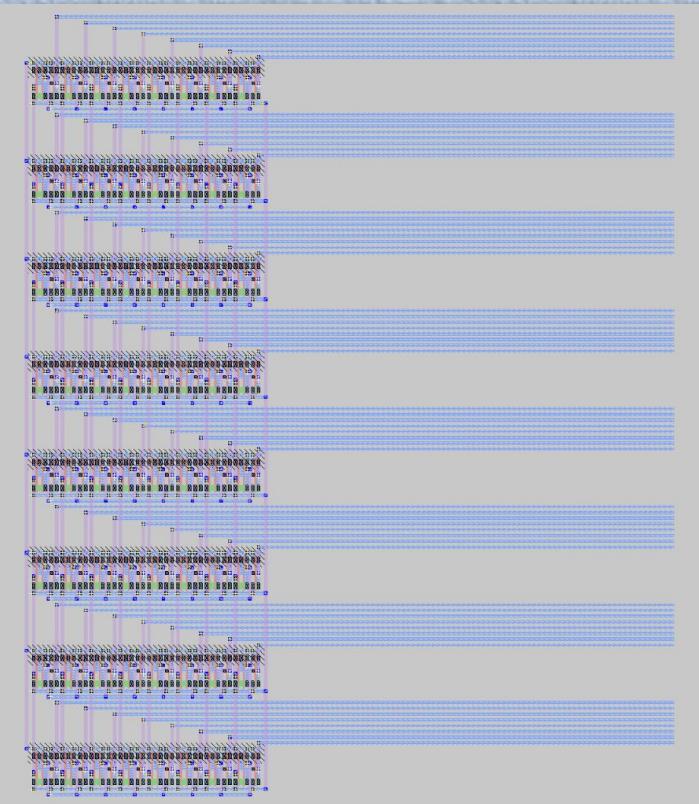
6 Adder



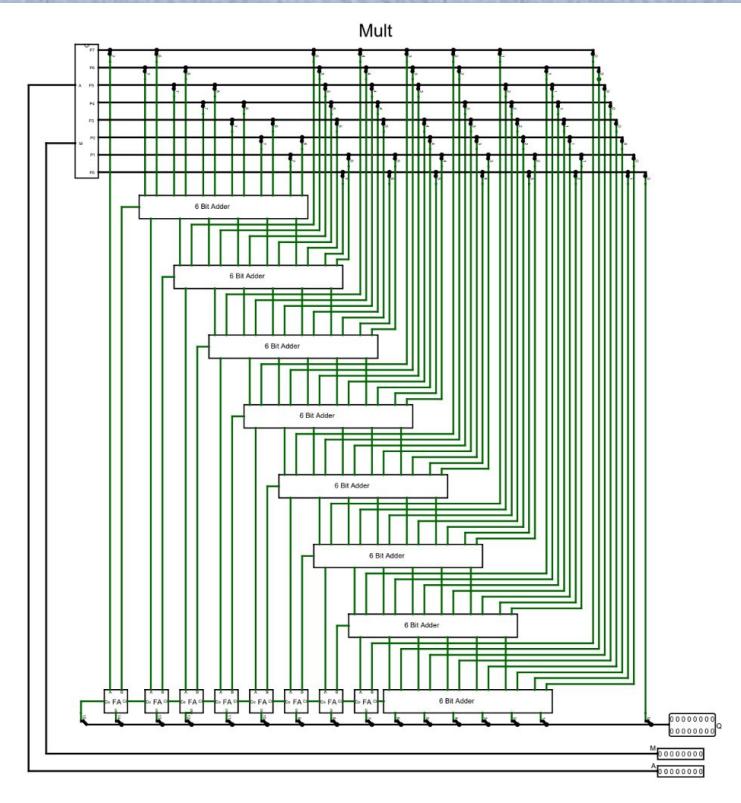
8-bit AND



Partial Product



Multiplier



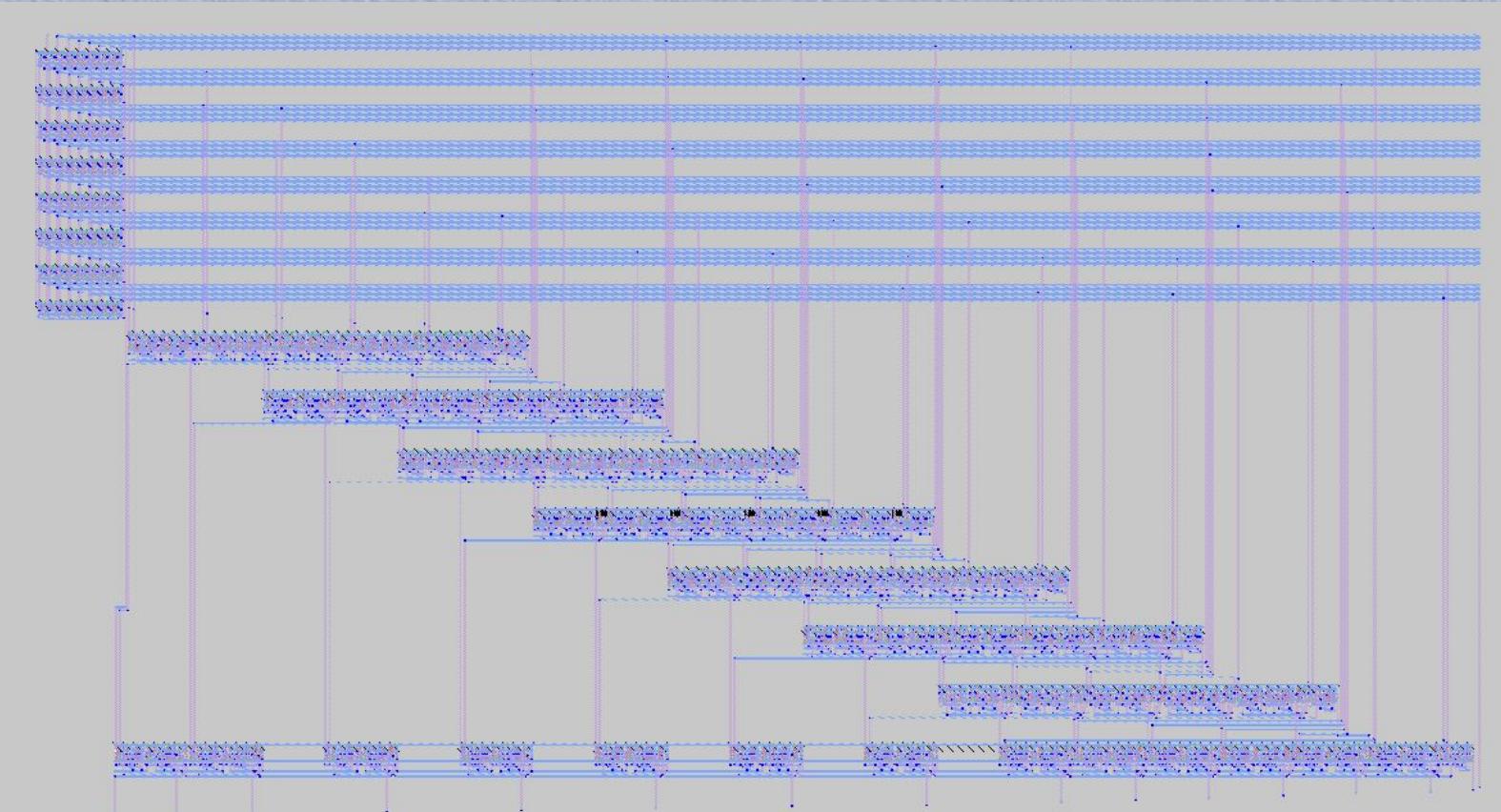
The Wallace tree is made of cascading half and full adders. The AND gates(Partial) are diagrammed in the top left, and their outputs are pulled down into the adder tree according to their “weights.”

$$\text{Weight} = \mathbf{M} + \mathbf{N}$$

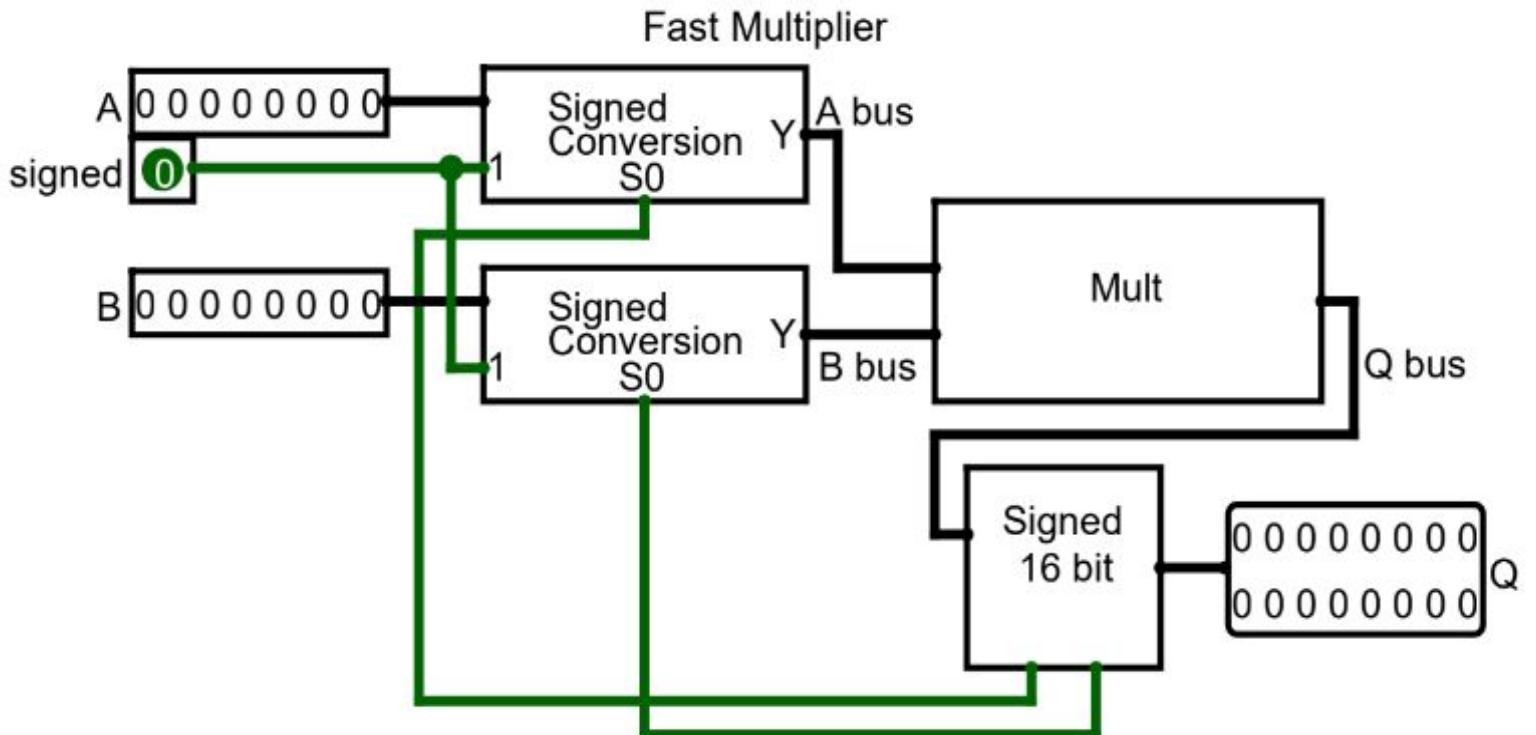
Where M is a position 0-7 for A,
and N is 0-7 for B

$$\begin{aligned}\text{weight}(A[7], B[5]) &= 7 + 5 = 12 \\ \text{weight}(A[2], B[0]) &= 2 + 0 = 2\end{aligned}$$

Multiplier

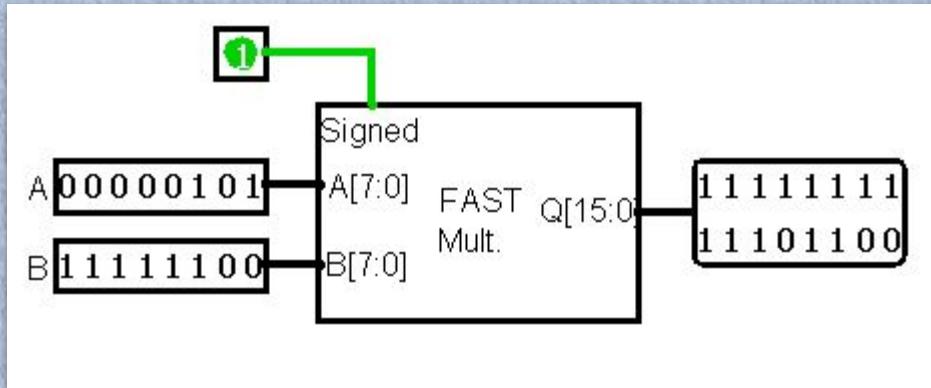


8-bit Fast Multiplier



Parts	Assigned Members
Logisim Schematic	Riley, Alberto
Basic gates	Dang
2x1 MUX	Dang
Half and Full Adder	Alberto
8 and 16 bit 2's Complement	Alberto
Partial Product	Alberto
Multiplier	Riley

Thank you for listening



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Alberto Rosas

Dang Tran

All made possible with...



8-bit Fast Multiplier

