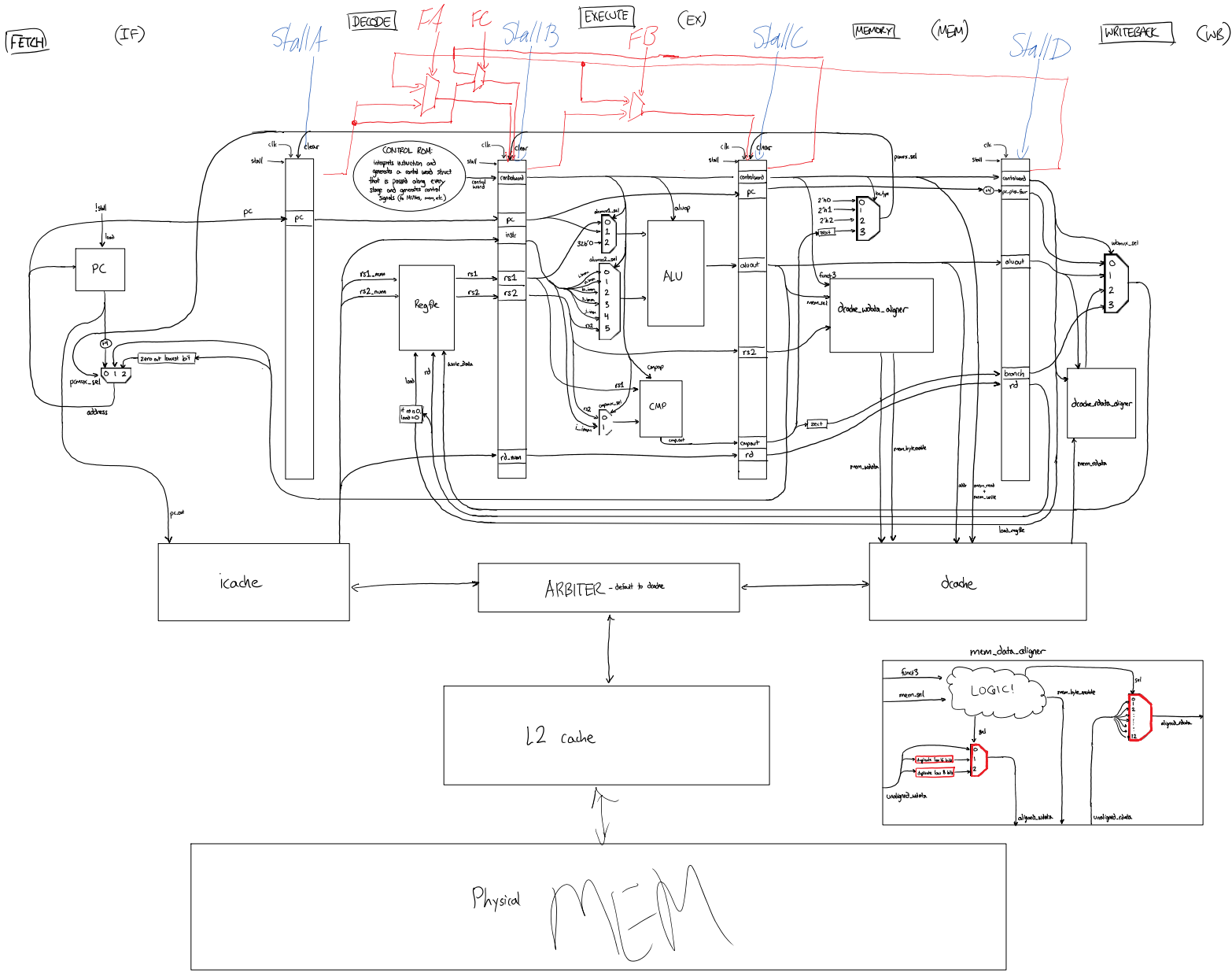

Opcodes: ALU, LX, JALR, SX // ALU means any ALU op, LX means any load, SX means any store

Stall A = [(rd == rs1) + (rd == rs2)] * opcode * mem_resp + StallB + StallC + StallD

StallB = // + StallC + StallD

StallC = // + StallD

StallD = //

Stall = StallA + StallB + StallC + StallD

FA = WB.ctrl.load_regfile && EX.rs == WB.rd && !MEM_is_forwarding

FB = WB.ctrl.load_regfile && MEM.rs == WB.rd

FC = MEM.ctrl.load_regfile && EX.rs == MEM.rd

} Done for rs1 and rs2