



PICO-APL1

PICO-ITX Board

User's Manual 6th Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-APL1	1
● COM + Line-out Cable (optional)	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
18. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.**

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 此产品所标示之环保使用期限, 系指在一般正常使用状况下。</p>						

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
<p>O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.</p> <p>X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.</p> <p>Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only</p>						

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Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	Pico-ITX
CPU	Intel® Atom™ E3900/ Pentium® N4200/ Celeron® N3350 Processor SoC
CPU Frequency	Up to 2.0GHz
Chipset	Intel® Atom™ E3900/ Pentium® N4200/ Celeron® N3350 Processor SoC
Memory Type	204-pin DDR3L SODIMM x 1, DDR3L 1867MHz, Max. 8GB
Max. Memory Capacity	Up to 8GB
BIOS	AMI/SPI
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V AT/ATX (default)
Power Supply Type	AT/ATX (default)
Power Consumption (Typical)	Intel® N3350 Processor, DDR3L 8GB 0.91A@+12V
System Cooling	Heat-spreader/ heatsink optional
Dimension	3.94" x 2.84" (100mm x 72mm)
Gross Weight	0.55 lb (0.25 kg)
Operating Temperature	32 °F~ 140 °F (0°C ~ 60°C),

System

Storage Temperature	-40 °F ~ 176 °F (-40°C ~ 80°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	170,000
Certification	CE,FCC

Display

Chipset	Intel® Atom™ E3900/ Pentium® N4200/ Celeron® N3350 Processor SoC
Resolution	LVDS (18/24bit 2CH) 1920 x 1200 (optional) HDMI 1.4b up to 3840 x 2160 DDI (BIO)
LCD Interface	18/24bit 2CH LVDS

I/O

Storage/SSD	SATA 6.0Gb/s x 1, mSATA or Mini-PCIe by BOM (Full size) x 1
Ethernet	Intel® Gigabit Ethernet i210AT, 10/100/1000Base-TX, RJ-45 x 1
USB Port	USB 3.0 x 2, Rear IO, USB 2.0 x 1
Serial Port	COM1: RS-232 x 1, COM2: RS-232/422/485 x 1 (Ring/ +5V/ +12V)
Audio	Line-out x1
DIO	4-bit (2-in, 2-out)

I/O

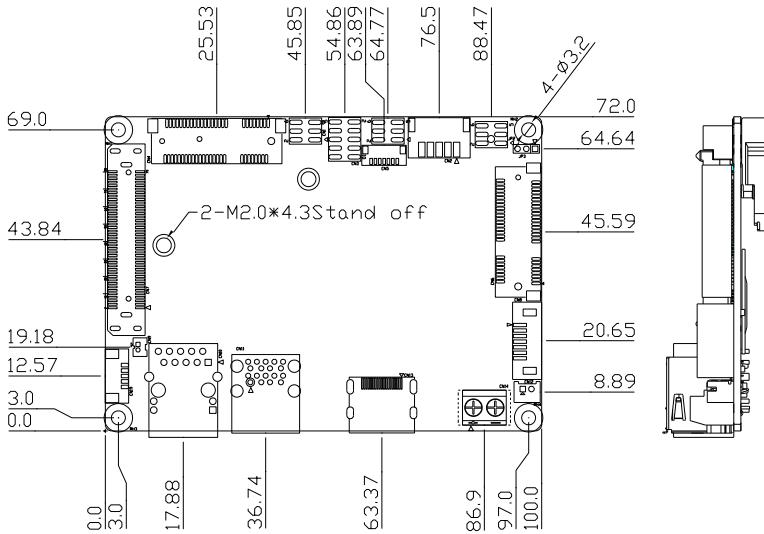
Expansion Slot	Mini Card (Half-size) x 1, BIO (optional) x 1, I2C or SMBus x 1
SIM	—
TPM	—
Touch	—

Chapter 2

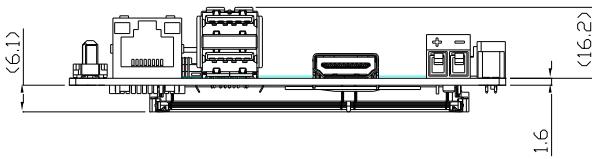
Hardware Information

2.1 Dimensions

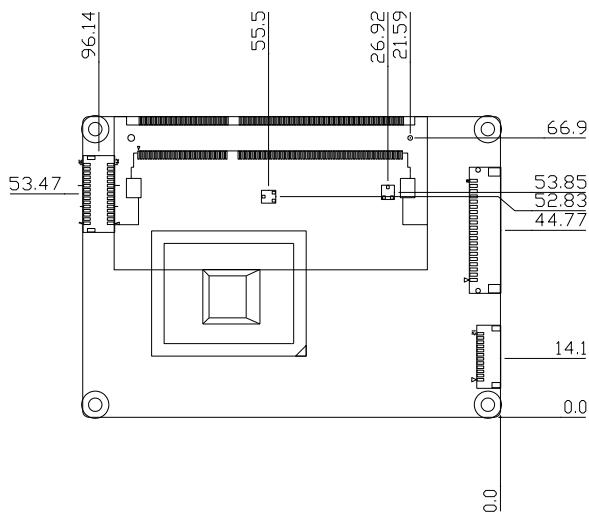
Component Side



Component Side

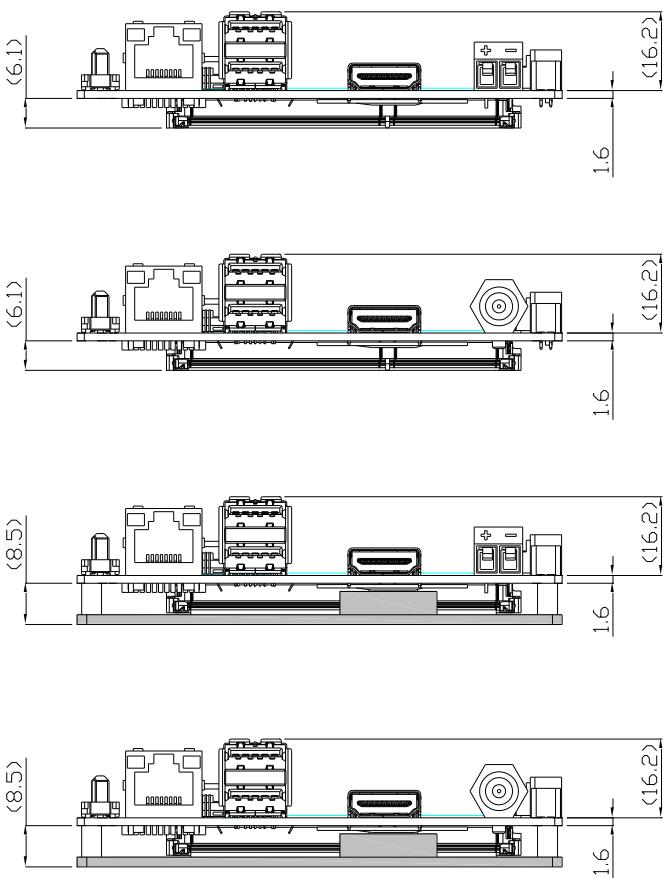


Solder Side



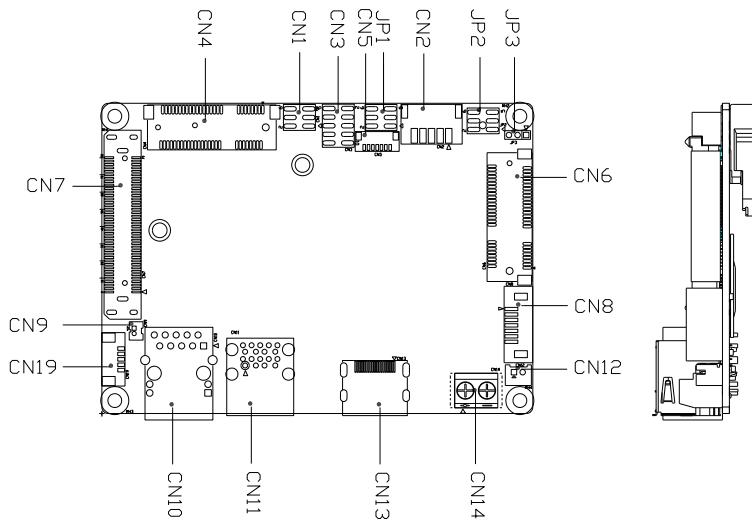
Solder Side

Rear I/O Configuration

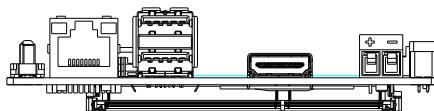


2.2 Jumpers and Connectors

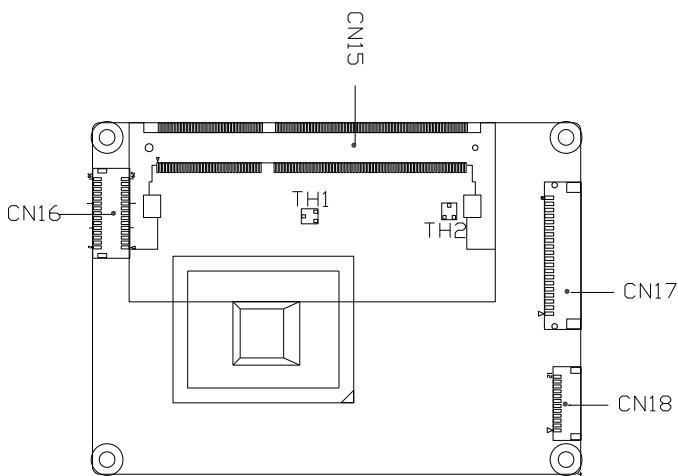
Component Side



Component Side



Solder Side



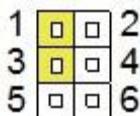
Solder Side

2.3 List of Jumpers

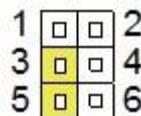
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1(1,3,5)	Clear CMOS Jumper
JP1(2,4,6)	Auto Power Button Enable/Disable Selection
JP2(1,3,5)	LVDS Port Operating Voltage Selection
JP2(2,4,6)	LVDS Port Backlight Inverter Voltage Selection
JP3	LVDS Port Backlight Lightness Control Mode Selection

2.3.1 Clear CMOS Jumper (JP1 1, 3, 5)

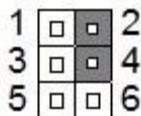


Normal (Default)

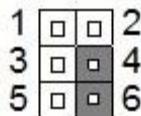


Clear CMOS

2.3.2 Auto Power Button Enable/Disable Selection (JP1 2, 4, 6)

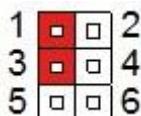


Enable (Default)

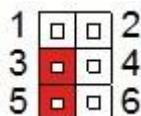


Disable

2.3.3 LVDS Port Operating Voltage Selection (JP2 1,3,5)

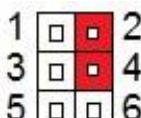


+5V

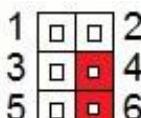


+3.3V (Default)

2.3.4 LVDS Port Backlight Inverter Voltage Selection Selection (JP2 2,4,6)

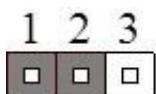


+12V

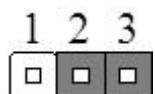


+5V (Default)

2.3.5 LVDS Port Backlight Lightness Control Mode (JP3)



VR Mode (Default)



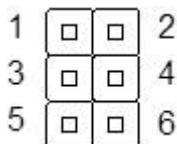
PWM Mode

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

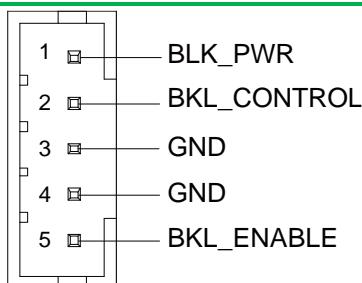
Label	Function
CN1	Digital IO Port
CN2	LVDS Port Inverter / Backlight Connector
CN3	Front Panel
CN4	Mini-Card Slot (Half-Mini Card)
CN5	SPI Programming Header
CN6	Mini-Card Slot (Full-Mini Card)/mSATA (By BOM)
CN7	BIO connector
CN8	SATA Port
CN9	Battery
CN10	LAN (RJ-45) Port
CN11	USB 3.0 Port 1,2
CN12	+5V Output for SATA HDD
CN13	HDMI port
CN14	External +12V Input
CN15	DDR3L SO-DIMM Slot
CN16	LVDS Port
CN17	COM Port 1/2 & line out connector
CN18	LPC Port
CN19	USB 2.0 Port 1

2.4.1 Digital IO Port (CN1)



Pin	Pin Name	Signal Type	Pin Name
1	+5V	PWR	+5V
2	DIO0	I/O	+5V
3	DIO1	I/O	+5V
4	DIO2	I/O	+5V
5	DIO3	I/O	+5V
6	GND	GND	

2.4.2 LVDS Port Inverter / Backlight Connector (CN2)



Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	

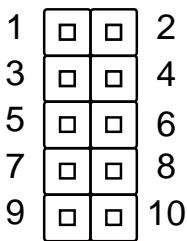
Pin	Pin Name	Signal Type	Signal level
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

※ LVDS/BKL_PWR can be set to +5V or +12V by JP2.

※ LVDS/BKL_CONTROL can be set by JP3.

※ The driving current supports up to 2A.

2.4.3 Front Panel (CN3)



Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

2.4.4 Mini-Card Slot (Half-Mini Card) (CN4)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		

Pin	Pin Name	Signal Type	Signal Level
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.4.5 Mini-Card Slot (Full Mini-Card)/mSATA (by BOM) (CN6)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB/+3.3V	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		

Pin	Pin Name	Signal Type	Signal Level
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-/mSATARX+	DIFF	
24	+3.3VSB/+3.3V	PWR	+3.3V
25	PCIE_RX+/mSATARX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-/mSATATX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+/mSATATX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB/+3.3V	PWR	+3.3V
40	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
41	+3.3VSB/+3.3V	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB/+3.3V	PWR	+3.3V

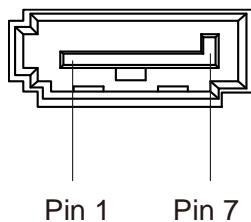
2.4.6 BIO connector (CN7)

Pin	Pin Name	Pin	Pin Name
1	+12VSB	2	GND
3	GND	4	PCIE_TXN0
5	PCIE_RXN0	6	PCIE_TXP0
7	PCIE_RXP0	8	GND
9	GND	10	PCIE_TXN4
11	PCIE_RXN4	12	PCIE_TXP4
13	PCIE_RXP4	14	GND
15	GND	16	PS_ON#
17	DDI0_DDCCLK_3P3	18	DDI0_DDCDATA_3P3
19	+5VSB	20	+5VSB
21	+5VSB	22	+5VSB
23	PCIE_REF_CLK0	24	RESET#
25	PCIE_REF_CLK0#	26	GND
27	GND	28	DDI0_TXN1
29	DDI0_TXN0	30	DDI0_TXP1
31	DDI0_TXP0	32	GND
33	GND	34	DDI0_TXN3
35	DDI0_TXN2	36	DDI0_TXP3
37	DDI0_TXP2	38	GND

Pin	Pin Name	Pin	Pin Name
39	GND	40	BIO_DDI0_HPD
41	DDI0_AUXN	42	GND
43	DDI0_AUXP	44	USB3_TX2_N
45	GND	46	USB3_TX2_P
47	USBN4	48	GND
49	USBP4	50	USB3_RX2_N
51	GND	52	USB3_RX2_P
53	SMB_CLK	54	GND
55	SMB_DATA	56	WAKE#
57	GND	58	USB_OC0#
59	+5V	60	USB_OC1#
61	+5V	62	+5V
63	+5V	64	+5V
65	LPC_AD0	66	LPC_FRAME#
67	LPC_AD1	68	SERIRQ
69	LPC_AD2	70	LPC_DRQ
71	LPC_AD3	72	GPIO0/BIO-POWEROK
73	GND	74	AGND
75	LPC_CLK	76	AUD_LINEOUT_L
77	PME#	78	AUD_LINEOUT_R

Pin	Pin Name	Pin	Pin Name
79	GND	80	GND

2.4.7 SATA Port (CN8)

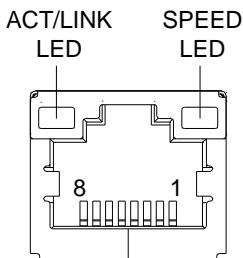


Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX1+	DIFF	
3	SATA_TX1-	DIFF	
4	GND	GND	
5	SATA_RX1-	DIFF	
6	SATA_RX1+	DIFF	
7	GND	GND	

2.4.8 Battery (CN9)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.9 LAN (RJ-45) Port (CN10)

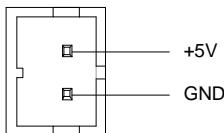


Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.10 USB3.0 Ports 0 and 1 (CN11)

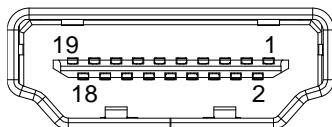
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USBO_SSRX-	DIFF	
6	USBO_SSRX+	DIFF	
7	GND	GND	
8	USBO_SSTX-	DIFF	
9	USBO_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX-	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX-	DIFF	
18	USB1_SSTX+	DIFF	

2.4.11 +5V Output for SATA HDD (CN12)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

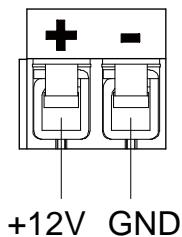
2.4.12 HDMI Port (CN13)



Pin	Pin Name	Signal Type	Signal level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	

Pin	Pin Name	Signal Type	Signal level
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.4.13 External +12V Input (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	

2.4.14 DDR3L SO-DIMM Slot (CN15)

Standard specification

2.4.15 LVDS Port (CN16)

※ LVDS LCD_PWR can be set to +3.3V or +5V by JP2

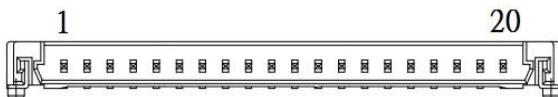
※ The max. driving current is 2A.

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	

7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V

28	GND	GND
29	LVDS_B_CLK-	DIFF
30	LVDS_B_CLK+	DIFF

2.4.16 COM Port 1/2 & line out connector (CN17)



Pin	Pin Name	Signal Type	Signal Level
1	DCDB	IN	
2	DSRB	IN	
3	RXB	IN	
4	RTSB	OUT	±9V
5	TXB	OUT	±9V
6	CTSB	IN	
7	DTRB	OUT	±9V
8	RIB/+5V/+12V	IN/ PWR	+5V/+12V
9	DCDA	IN	
10	DSRA	IN	
11	RXA	IN	
12	RTSA	OUT	±9V
13	TXA	OUT	±9V

Pin	Pin Name	Signal Type	Signal Level
14	CTSA	IN	
15	DTRA	OUT	±9V
16	RIA	IN	
17	GND	GND	
18	AGND	GND	
19	LOUT_R	I/O	
20	LOUT_L	I/O	

2.4.17 COM port2 RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
17	GND	GND	

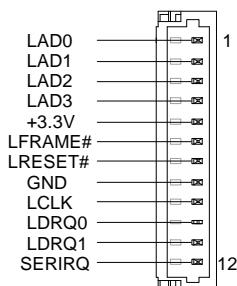
2.4.18 COM port2 RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	$\pm 5V$
2	NC		
3	RS422_TX+	OUT	$\pm 5V$
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
17	GND	GND	

※ COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

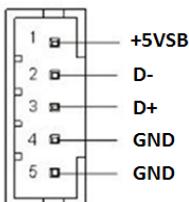
※ COM2 RI/+5V/+12V function can be set by BOM(R248-RI/R256-+12V/R250-+5V)

2.4.19 LPC port2 (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.4.20 USB 2.0 Port 1 (CN19)



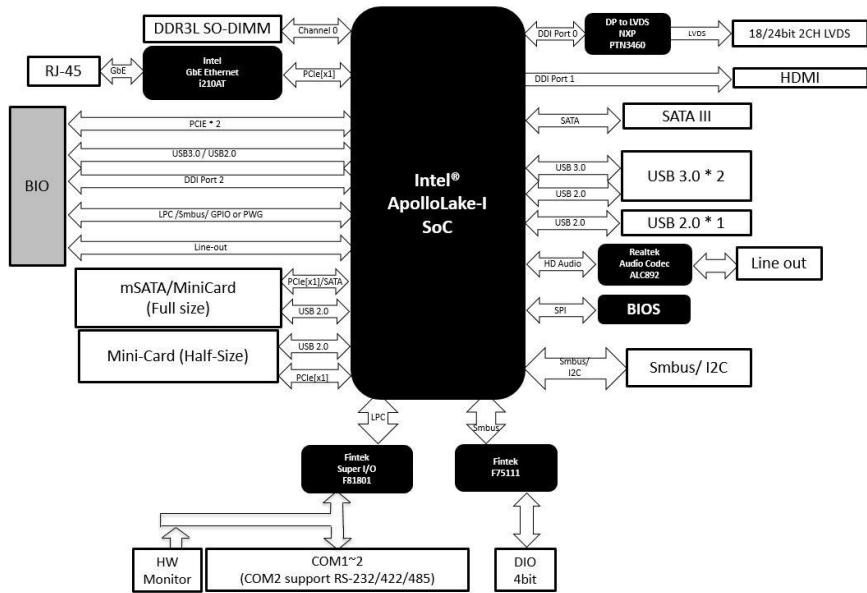
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USBD5-	DIFF	
3	USBD5+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.21 Specifications for I/O Port

I/O	Reference	Signal Name	Rate Output
Digital IO Port	CN1	D0~D3	+5V/(Open drain)
LVDS Port Inverter / Backlight Connector	CN2	VDD	+5V/2A or +12V/2A
Mini-Card Slot	CN4	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
Mini-Card Slot	CN6	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
USB 3.0 Port 1 & 2	CN10	+5VSB	+5VSB/1A (per channel)
+5V Output for SATA HDD	CN12	+5V	+5V/1A

LVDS Port	CN16	VCC	+3.3V/2A or +5V/2A
COM Port 2	CN17	+5V/+12V	+5V/1A or +12V/1A
LPC Port	CN18	+3.3V	+3.3V/0.5A
USB 2.0 Port 1	CN19	+5VSB	+5VSB/0.5A

2.4.22 Function Block



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-APL1 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

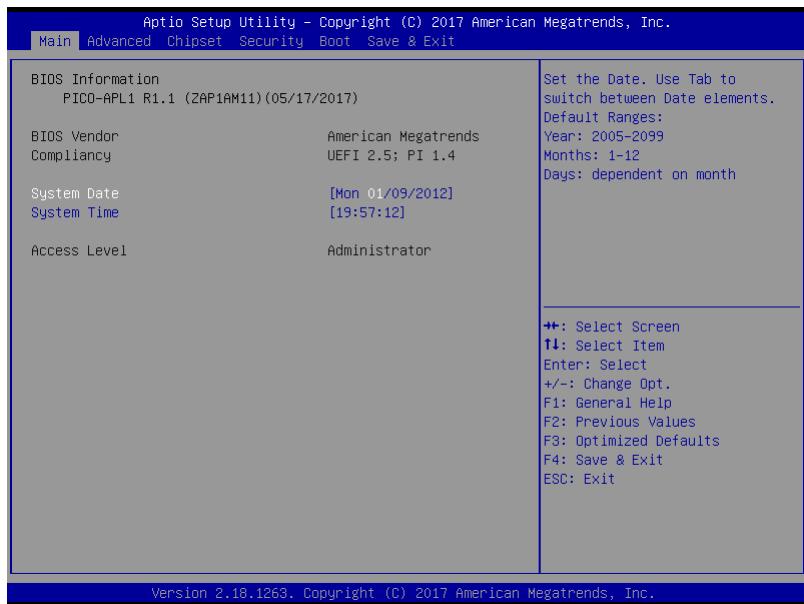
Set setup administrator password.

Save & Exit

Exit system setup after saving the changes.

3.3 Setup Submenu: Main

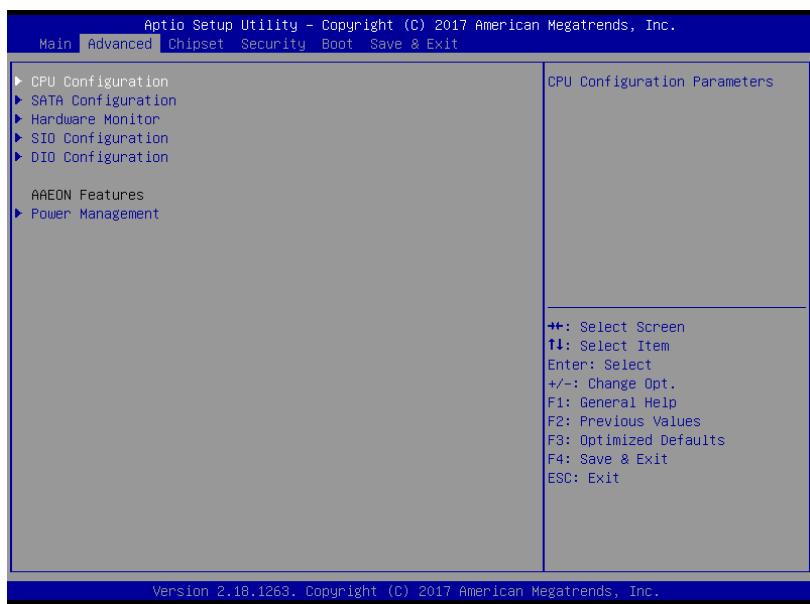
Press "Delete" to enter Setup



Options summary: (*default setting*)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

3.4 Setup Submenu: Advanced

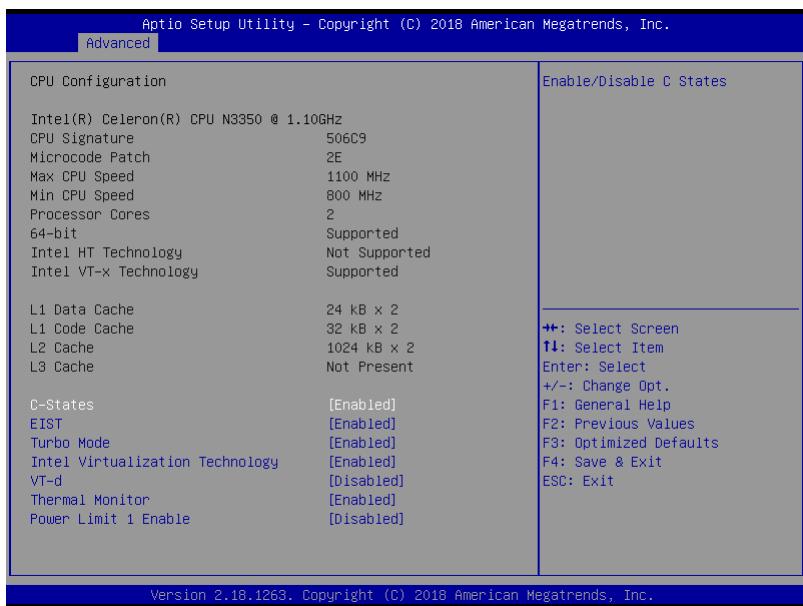


Options summary: (*default setting*)

CPU Configuration		
CPU Configuration Parameters		
SATA Configuration		
SATA Device Configuration		
USB Configuration		
USB Configuration Parameters		
SIO Configuration		
SIO Chip configuration .Enable or Disable SIO Logical Devices, Resources and Features settings, etc.		
Hardware Monitor		

Power Management		
System ACPI/Power Mode/Wake Event Configuration		
Digital IO Port Configuration		
Set Input/Output of digital Port Configuration		

3.4.1 CPU configuration

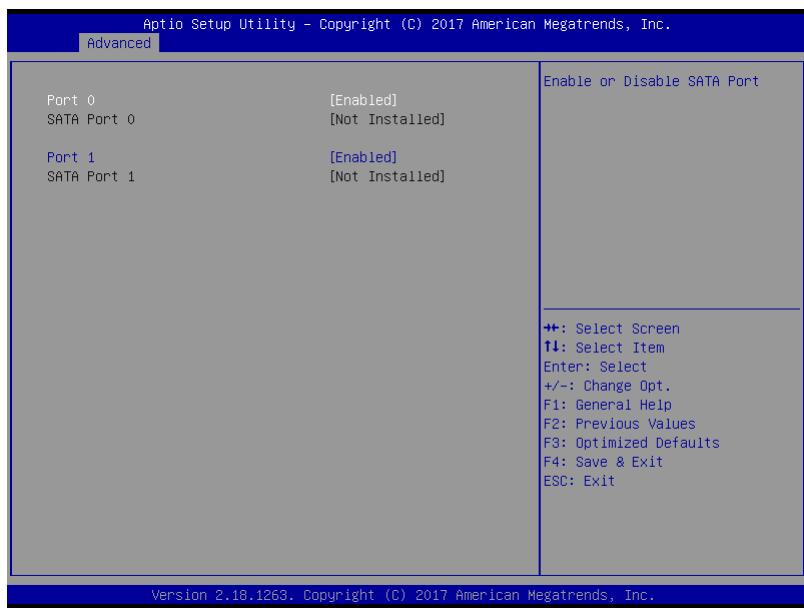


Options summary:

C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU VT-d		
Thermal Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Thermal Monitor		

Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1		

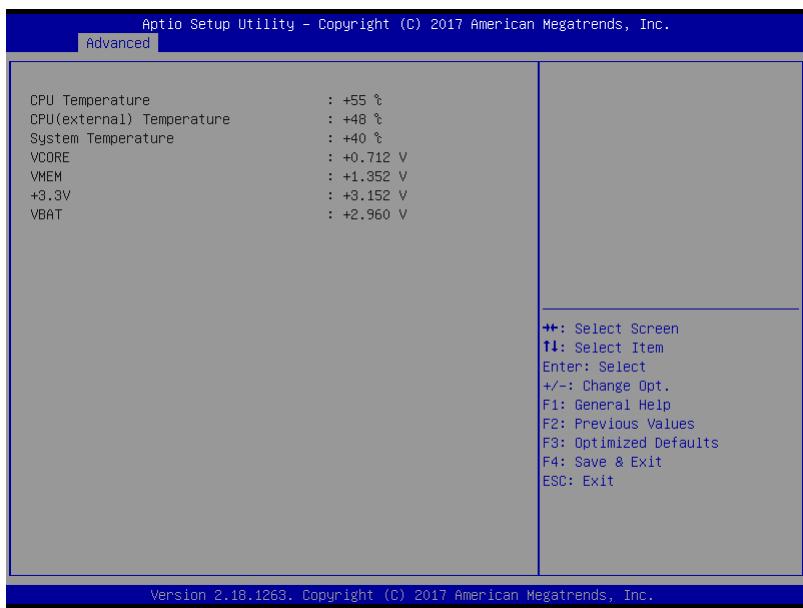
3.4.2 SATA Configuration



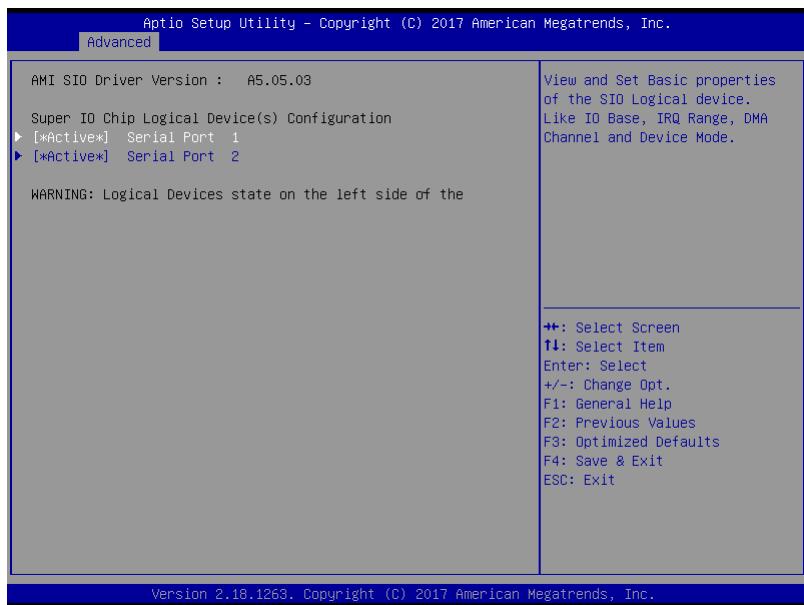
Options summary:

Port 0/1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA port		

3.4.3 Hardware Monitor



3.4.4 SIO Configuration



Options summary: (*default setting*)

Serial Port 1/2 Configuration	
View and Set Basic properties of the SIO Logical device. Like IO Base , IRQ Range , DMA Channel and Device Mode.	

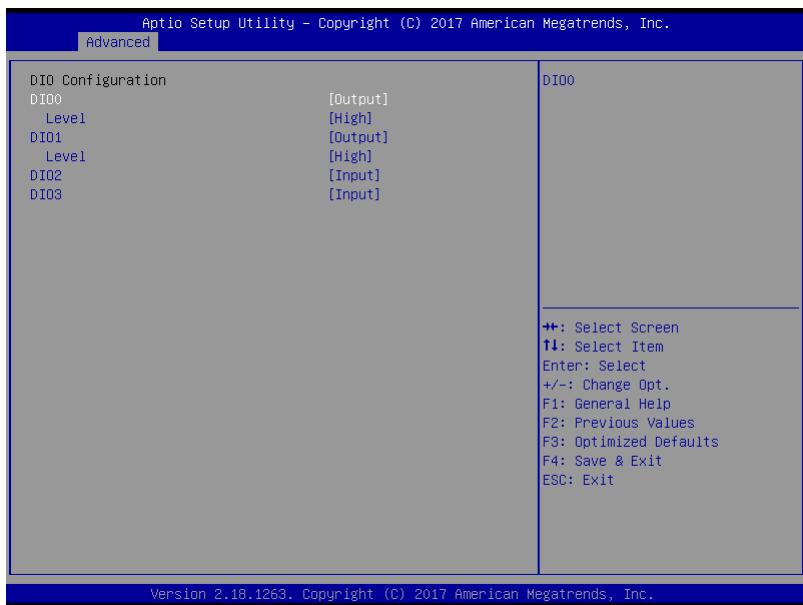
3.4.4.1 Serial Port Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

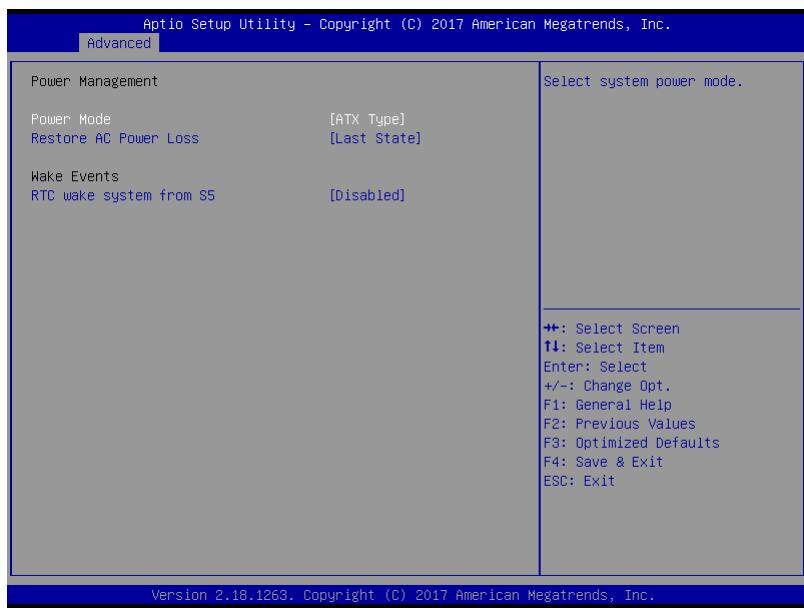
3.4.5 Dio Configuration



Options summary:

DIO *	Output	
	Input	
Set DIO as Input or Output		
Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

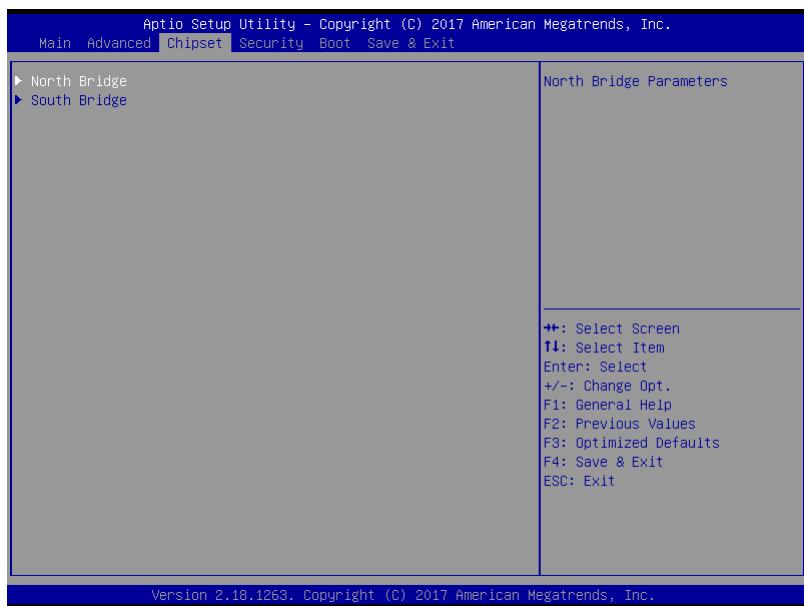
3.4.6 Power Management



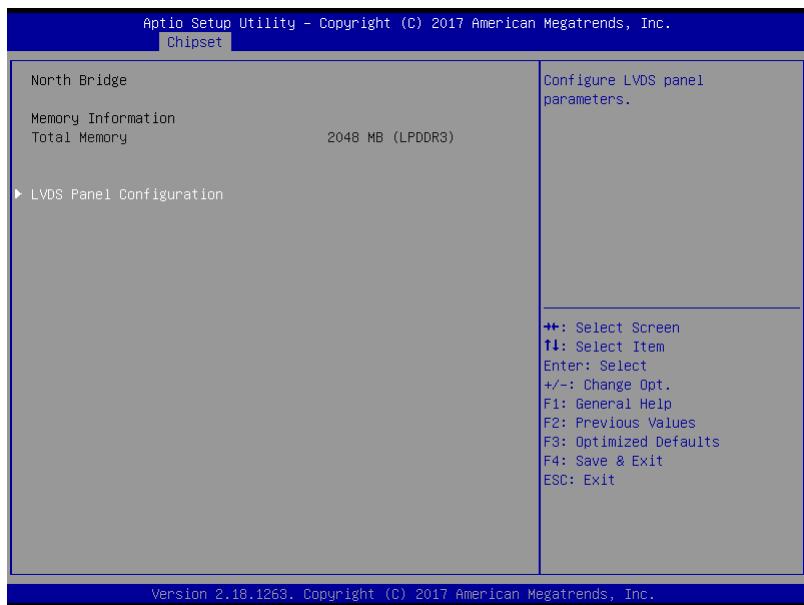
Options summary:

Power Mode	ATX Type AT Type	Optimal Default, Failsafe Default
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
RTC wake		

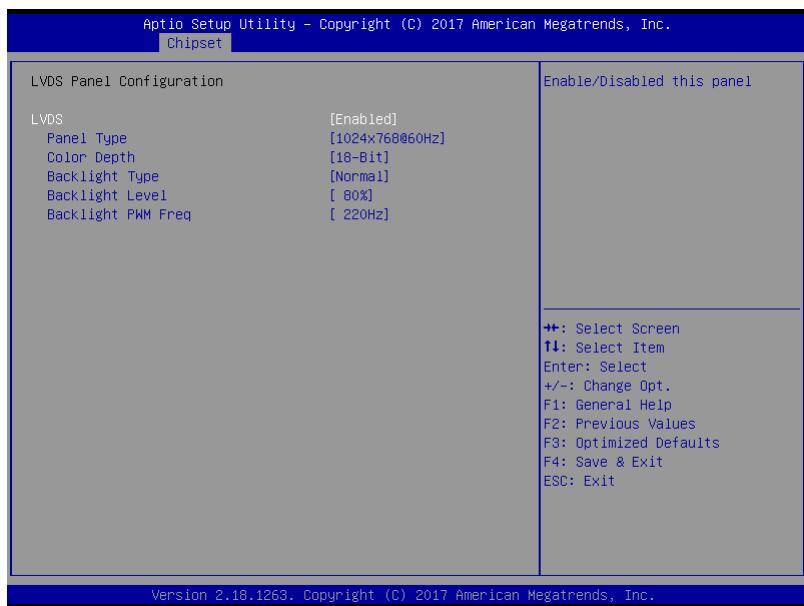
3.4.7 Setup submenu: Chipset



3.4.8 North Bridge



3.5 LVDS Panel Configuration



Options summary:

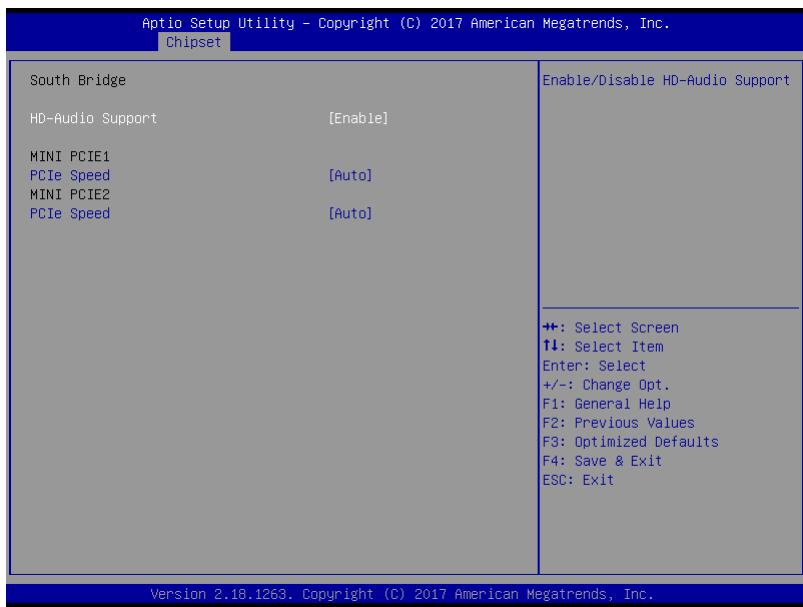
LVDS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled this panel.		
LVDS Panel Type	640X480@60HZ	
	800X480@60HZ	
	800X600@60HZ	
	1024X600@60HZ	
	1024X768@60HZ	Optimal Default, Failsafe Default
	1280X768@60HZ	
	1280X800@60HZ	
	1280X1024@60HZ	

	1366X768@60HZ	
	1440X900@60HZ	
	1600X1200@60HZ	
	1920X1080@60HZ	
	1920X1200@60HZ	

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	Optimal Default, Failsafe Default
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1.1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

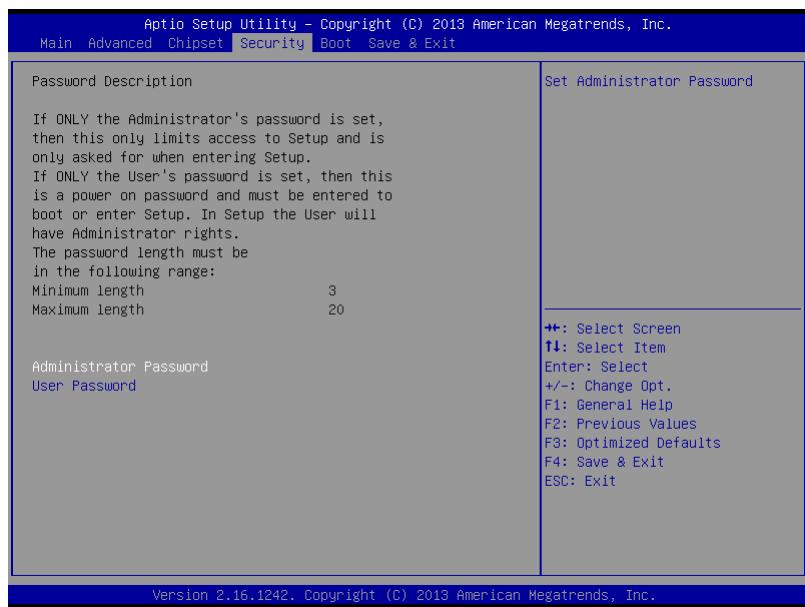
3.5.1 South Bridge



Options summary:

HD-Audio Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled HD audio		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe Speed		

3.5.1.1 Setup submenu: Security



Change User/Supervisor Password

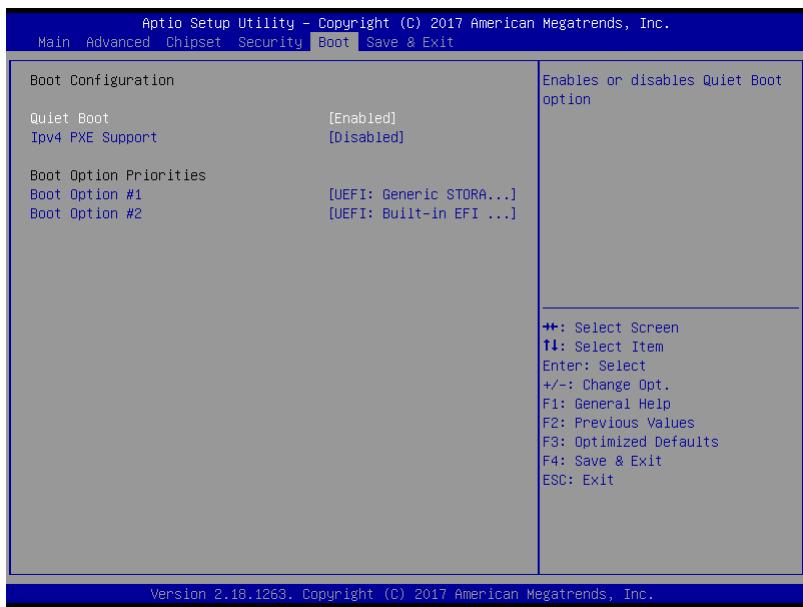
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

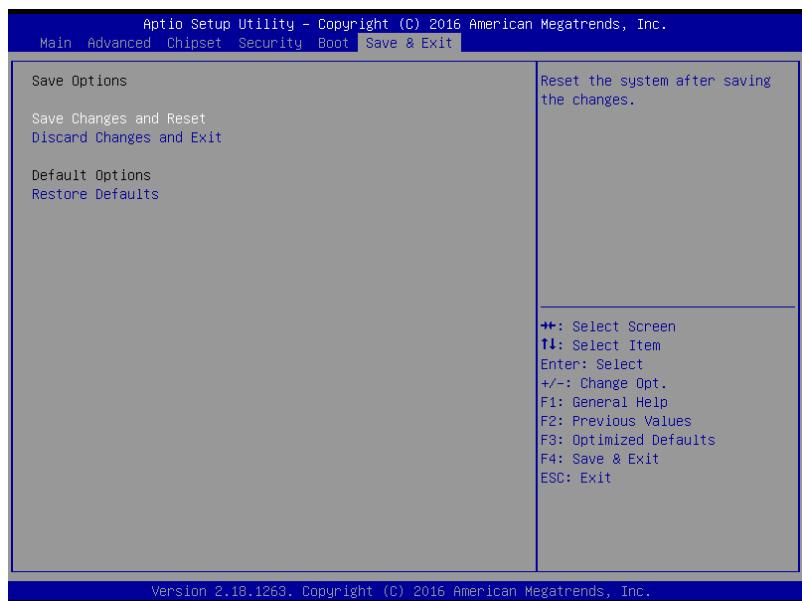
3.5.2 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable showing boot logo.		
Monitor Mwait	Disable	Optimal Default, Failsafe Default
	Enabled	
	Auto	
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.6 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the PICO-APL1 can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/p/pico-itx-boards-pico-apl1#downloads>

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Open the **STEP1 - CHIPSET** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **STEP2 - VGA** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 3 – Install LAN Driver

1. Open the **STEP3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Driver will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - AUDIO** folder and open the **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 5 – Install TXE Driver

1. Open the **STEP5 - TXE** folder and open the **SetupTXE.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 6 – Install FintekSerial_Patch_T4R8 Driver

1. Open the **STEP6-FintekSerial_Patch_T4R8** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 7 – Install GPIO Driver

1. Open the **STEP7 - GPIO** folder and open the **SetupSerialIO.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address

	Default Value	Note
I/O Base Address	0x2E	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7

Table 2 : Watchdog relative register table

Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s <i>Pulse width is must longer than 16ms.</i>
Signal Polarity	0x05	2	0	0: low active 1: high active <i>Must set this bit to 0</i>
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse <i>Must set this bit to 1</i>
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****  
// WDT I/O operation relative definition (Please reference to Table 1)  
#define WDTAddr 0x510 // WDT I/O base address  
Void WDTWriteByte(byte Register, byte Value);  
byte WDT.ReadByte(byte Register);  
Void WDTSetReg(byte Register, byte Bit, byte Val);  
// Watch Dog relative definition (Please reference to Table 2)  
#define DevReg 0x00 // Device configuration register  
    #define WDTRstBit 0x80 // Watchdog WDTRST# (Bit7)  
    #define WDTRstVal 0x80 // Enabled WDTRST#  
#define TimerReg 0x05 // Timer register  
    #define PSWidthBit 0x00 // WDTRST# Pulse width (Bit0:1)  
    #define PSWidthVal 0x01 // 25ms for WDTRST# pulse  
    #define PolarityBit 0x02 // WDTRST# Signal polarity (Bit2)  
    #define PolarityVal 0x00 // Low active for WDTRST#  
    #define UnitBit 0x03 // Unit for timer (Bit3)  
    #define ModeBit 0x04 // WDTRST# mode (Bit4)  
    #define ModeVal 0x01 // 0:level 1: pulse  
    #define EnableBit 0x05 // WDT timer enable (Bit5)  
    #define EnableVal 0x01 // 1: enable  
    #define StatusBit 0x06 // WDT timer status (Bit6)  
#define CounterReg 0x06 // Timer counter register  
*****  
*****  
VOID Main(){  
    // Procedure : AaeonWDTConfig  
    // (byte)Timer : Counter of WDT timer.(0x00~0xFF)  
    // (boolean)Unit : Select time unit(0: second, 1: minute).  
    EnterSIOconfig();  
    SetWDT();  
    AaeonWDTConfig(Counter, Unit);  
    // Procedure : AaeonWDTEnable  
    // This procedure will enable the WDT counting.  
    AaeonWDTEnable();  
    ExitSIOconfig();  
}  
*****
```

```
*****  
// Procedure : AaeonWDTEnable  
VOID EnterSIOconfig (){  
    IOWriteByte (IoConfAddr,0x87);  
    IOWriteByte (IoConfAddr,0x87);  
}  
  
VOID ExitSIOconfig (){  
    IOWriteByte (IoConfAddr,0xAA);  
}  
  
VOID SetWDT ()  
{  
    IOWriteByte (IoConfAddr,0x2B);  
    IOWriteByte(IoConfAddr+1, (IOR.ReadByte(IoConfAddr+1)&0xFC));  
}  
  
// Procedure : AaeonWDTEnable  
VOID AaeonWDTEnable (){  
    WDTEnableDisable(1);  
}  
  
// Procedure : AaeonWDTConfig  
VOID AaeonWDTConfig (byte Counter, BOOLEAN Unit){  
    // Disable WDT counting  
    WDTEnableDisable(0);  
    // Clear Watchdog Timeout Status  
    WDTClearTimeoutStatus();  
    // WDT relative parameter setting  
    WDTParameterSetting(Timer, Unit);  
}  
  
VOID WDTEnableDisable(byte Value){  
    If (Value == 1)  
        WDTSetBit(TimerReg, EnableBit, 1);  
    else  
        WDTSetBit(TimerReg, EnableBit, 0);  
}  
  
VOID WDTParameterSetting(byte Counter, BOOLEAN Unit){  
    // Watchdog Timer counter setting  
    WDTWriteByte(CounterReg, Counter);  
    // WDT counting unit setting
```

```
    WDTSetBit(TimerReg, UnitBit, Unit);
    // WDT output mode set to pulse
    WDTSetBit(TimerReg, ModeBit, ModeVal);
    // WDT output mode set to active low
    WDTSetBit(TimerReg, PolarityBit, PolarityVal);
    // WDT output pulse width is 25ms
    WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
    // Watchdog WDTRST# Enable
    WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus(){
    WDTSetBit(TimerReg, StatusBit, 1);
}
*****
*****
VOID WDTWriteByte(byte Register, byte Value){
    IOWriteByte(WDTAddr+Register, Value);
}

byte WDTReadByte(byte Register){
    return IOReadByte(WDTAddr+Register);
}

VOID WDTSetBit(byte Register, byte Bit, byte Val){
    byte TmpValue;

    TmpValue = WDTReadByte(Register);
    TmpValue &= ~(1 << Bit);
    TmpValue |= Val << Bit;
    WDTWriteByte(Register, TmpValue);
}
*****
*****
```

Appendix B

I/O Information

B.1 I/O Address Map

Input/output (IO)	
	[0000000000000000 - 000000000000006F] PCI Express Root Complex
	[0000000000000020 - 000000000000021] Programmable interrupt controller
	[0000000000000024 - 000000000000025] Programmable interrupt controller
	[0000000000000028 - 000000000000029] Programmable interrupt controller
	[000000000000002C - 00000000000002D] Programmable interrupt controller
	[000000000000002E - 00000000000002F] Motherboard resources
	[0000000000000030 - 000000000000031] Programmable interrupt controller
	[0000000000000034 - 000000000000035] Programmable interrupt controller
	[0000000000000038 - 000000000000039] Programmable interrupt controller
	[000000000000003C - 00000000000003D] Programmable interrupt controller
	[0000000000000040 - 000000000000043] System timer
	[000000000000004E - 00000000000004F] Motherboard resources
	[0000000000000050 - 000000000000053] System timer
	[0000000000000060 - 000000000000060] Standard PS/2 Keyboard
	[0000000000000061 - 000000000000061] Motherboard resources
	[0000000000000063 - 000000000000063] Motherboard resources
	[0000000000000064 - 000000000000064] Standard PS/2 Keyboard
	[0000000000000065 - 000000000000065] Motherboard resources
	[0000000000000067 - 000000000000067] Motherboard resources
	[0000000000000070 - 000000000000070] Motherboard resources
	[0000000000000070 - 000000000000077] System CMOS/real time clock
	[0000000000000078 - 0000000000000CF] PCI Express Root Complex
	[0000000000000080 - 00000000000008F] Motherboard resources
	[0000000000000092 - 000000000000092] Motherboard resources
	[00000000000000A0 - 0000000000000A1] Programmable interrupt controller
	[00000000000000A4 - 0000000000000A5] Programmable interrupt controller
	[00000000000000A8 - 0000000000000A9] Programmable interrupt controller
	[00000000000000AC - 0000000000000AD] Programmable interrupt controller
	[00000000000000B0 - 0000000000000B1] Programmable interrupt controller
	[00000000000000B2 - 0000000000000B3] Motherboard resources
	[00000000000000B4 - 0000000000000B5] Programmable interrupt controller
	[00000000000000B8 - 0000000000000B9] Programmable interrupt controller
	[00000000000000BC - 0000000000000BD] Programmable interrupt controller
	[00000000000002F8 - 0000000000002FF] Communications Port (COM2)
	[00000000000003F8 - 0000000000003FF] Communications Port (COM1)
	[0000000000000400 - 000000000000047F] Motherboard resources
	[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
	[0000000000000500 - 00000000000005FE] Motherboard resources
	[0000000000000680 - 000000000000069F] Motherboard resources
	[0000000000000A00 - 0000000000000A0F] Motherboard resources
	[0000000000000A10 - 0000000000000A1F] Motherboard resources
	[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
	[0000000000000E00 - 000000000000EFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
	[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
	[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
	[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
	[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
	[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller

B.2 Memory Address Map

Memory	
	[00000000000A0000 - 00000000000BFFFF] PCI Express Root Complex
	[00000000000C0000 - 00000000000DFFFF] PCI Express Root Complex
	[00000000000E0000 - 00000000000FFFFF] PCI Express Root Complex
	[0000000007B800001 - 0000000007BFFFFFF] PCI Express Root Complex
	[0000000007C000001 - 0000000007FFFFFF] PCI Express Root Complex
	[00000000080000000 - 0000000008FFFFFFF] Intel(R) HD Graphics
	[00000000080000000 - 000000000CFFFFFFF] PCI Express Root Complex
	[00000000090000000 - 00000000090FFFFFF] Intel(R) HD Graphics
	[00000000091000000 - 000000000910FFFFF] High Definition Audio Controller
	[00000000091100000 - 000000000911FFFFF] Intel(R) i210 Gigabit Network Connection
	[00000000091100000 - 000000000911FFFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
	[00000000091120000 - 00000000091123FFF] Intel(R) i210 Gigabit Network Connection
	[00000000091200000 - 0000000009120FFF] Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
	[00000000091210000 - 00000000091213FFF] High Definition Audio Controller
	[00000000091214000 - 00000000091215FFF] Standard SATA AHCI Controller
	[00000000091218000 - 000000000912180FF] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
	[00000000091219000 - 000000000912197FF] Standard SATA AHCI Controller
	[0000000009121A000 - 0000000009121A0FF] Standard SATA AHCI Controller
	[0000000009121E000 - 0000000009121EFFF] Intel(R) Trusted Execution Engine Interface
	[00000000D0C00000 - 00000000D0C00653] Intel(R) Serial IO GPIO Host Controller - INT3452
	[00000000D0C40000 - 00000000D0C40763] Intel(R) Serial IO GPIO Host Controller - INT3452
	[00000000D0C50000 - 00000000D0C5076B] Intel(R) Serial IO GPIO Host Controller - INT3452
	[00000000D0C70000 - 00000000D0C70673] Intel(R) Serial IO GPIO Host Controller - INT3452
	[00000000E0000000 - 00000000EFFFFFFF] Motherboard resources
	[00000000E0000000 - 00000000EFFFFFFF] PCI Express Root Complex
	[00000000FEA00000 - 00000000FEAFFFFF] Motherboard resources
	[00000000FED00000 - 00000000FED003FF] High precision event timer
	[00000000FED01000 - 00000000FED01FFF] Motherboard resources
	[00000000FED03000 - 00000000FED03FFF] Motherboard resources
	[00000000FED06000 - 00000000FED06FFF] Motherboard resources
	[00000000FED08000 - 00000000FED09FFF] Motherboard resources
	[00000000FED1C000 - 00000000FED1CFFF] Motherboard resources
	[00000000FED80000 - 00000000FEDBFFFF] Motherboard resources
	[00000000FEE00000 - 00000000FEFFFFF] Motherboard resources

B.3 IRQ Mapping Chart

▼ Interrupt request (IRQ)	
	(ISA) 0x00000000 (00) System timer
	(ISA) 0x00000001 (01) Standard PS/2 Keyboard
	(ISA) 0x00000003 (03) Communications Port (COM2)
	(ISA) 0x00000004 (04) Communications Port (COM1)
	(ISA) 0x00000008 (08) High precision event timer
	(ISA) 0x0000000C (12) PS/2 Compatible Mouse
	(ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x00000036 (54) Microsoft ACPI-Compliant System
	(ISA) 0x00000037 (55) Microsoft ACPI-Compliant System
	(ISA) 0x00000038 (56) Microsoft ACPI-Compliant System
	(ISA) 0x00000039 (57) Microsoft ACPI-Compliant System
	(ISA) 0x0000003A (58) Microsoft ACPI-Compliant System
	(ISA) 0x0000003B (59) Microsoft ACPI-Compliant System
	(ISA) 0x0000003C (60) Microsoft ACPI-Compliant System
	(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
	(PCI) 0x00000019 (25) High Definition Audio Controller
	(PCI) 0xFFFFFFF3 (-13) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
	(PCI) 0xFFFFFFF4 (-12) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF5 (-11) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF6 (-10) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF7 (-9) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF8 (-8) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF9 (-7) Intel(R) I210 Gigabit Network Connection
	(PCI) 0xFFFFFFF8A (-6) Intel(R) Trusted Execution Engine Interface
	(PCI) 0xFFFFFFF8B (-5) Intel(R) HD Graphics
	(PCI) 0xFFFFFFF8C (-4) Standard SATA AHCI Controller
	(PCI) 0xFFFFFFF8D (-3) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD6
	(PCI) 0xFFFFFFF8E (-2) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8

Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	Digital IO Port	Molex	51110-0650	N/A	N/A
CN2	LVDS Port Inverter / Backlight Connector	JST	PHR-5	N/A	N/A
CN3	Front Panel Connector	Molex	51110-1050	Front Panel Cable	1701100156
CN7	BIO connector	Hirose	FX18-80S-0.8SV20	N/A	N/A
CN8	SATA Port	Molex	887505318	SATA Cable	1709070500
CN9	Battery	Molex	51021-0200	Battery Cable	175011301C
CN10	LAN Connector	Molex	44915-0001	N/A	N/A
CN12	+5V Output for SATA HDD	JST	PHR-2	SATA power cable	1702150155
CN14	External +12V Input	Molex	19211-0003	Power cable	170204010R
CN16	LVDS Port	JCTC	11002H00-2x15P	LVDS Cable	1704300030

CN17	COM Port 1/2 & line out connector	HRS	DF14-20S-1.25C	COM Port 1/2 & line out cable	1703200153
CN18	LPC Port	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN19	USB Connector	Molex	51021-0500	USB Cable	1700050207

Appendix D

DIO

D1 DIO

The F75111 provides one serial access interface, I2C Bus, to read/write internal registers.

The address of Serial Bus is 0x6E (0110_1110)

The related register for configuring DIO is list as follows:

Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	Reserved	R/W	VSB3V	
5	EN_WDT10	R/W	VSB3V	Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable.
4	Reserved	R/W	VSB3V	
3	Reserved	R/W	VSB3V	
2	Reserved	R/W	VSB3V	
1	SMART_POWR_MANAGEMENT	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

GPIO2x Output Control Register – Index 20h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_OCTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function(default).
6	GP26_OCTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function(default).
5	GP25_OCTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function(default).
4	GP24_OCTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function(default).

GPIO2x Output Data Register – Index 21h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_ODATA	R/W	VSB3V	GPIO 27 output data.
6	GP26_ODATA	R/W	VSB3V	GPIO 26 output data.
5	GP25_ODATA	R/W	VSB3V	GPIO 25 output data.
4	GP24_ODATA	R/W	VSB3V	GPIO 24 output data.

GPIO2x Input Status Register – Index 22h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7	GP27_PSTS	RO	VSB3V	Read the GPIO27 data on the pin.
6	GP26_PSTS	RO	VSB3V	Read the GPIO26 data on the pin.
5	GP25_PSTS	RO	VSB3V	Read the GPIO25 data on the pin.
4	GP24_PSTS	RO	VSB3V	Read the GPIO24 data on the pin.

The following is a sample code for 8 input

```
.MODEL SMALL
.CODE
begin:
    mov cl,01h
    mov al,80h
    call CT_I2CWriteByte
    call Delay5ms

    mov al,00h
    mov cl,20h
    call CT_I2CWriteByte

    mov cl,22h
    call CT_I2CReadByte

;Input : CL - register index
```

```
; CH - device ID  
;Output : AL - Value read  
Ct_I2CReadByte Proc Near  
  
    mov ch,06eh  
  
    mov dx, F040h + 00h ; Host Control Register  
  
    xor al, al ; Clear previous commands  
  
    out dx, al  
  
    call Delay5ms  
  
    mov dx, F040h + 04h ; Transmit Slave Address Register  
  
    inc ch ; Set the slave address and  
  
    mov al, ch ; prepare for a READ command  
  
    out dx, al  
  
    mov dx, F040h + 05h ; Host Command Register  
  
    mov al, cl ; offset to read  
  
    out dx, al  
  
    mov dx, F040h + 06h  
  
  
    xor al, al ; Clear old data  
  
    out dx, al  
  
    mov dx, F040h + 01h ; Host Status Register  
  
    mov al, 07h ; Clear all status bits  
  
    out dx, al  
  
  
    mov dx, F040h + 00h ; Host Control Reegister  
  
    mov al, 12h ; Start a byte access  
  
    out dx, al  
  
    call CT_Clk_SMBus_Ready  
  
    mov dx, F040h + 06h
```

```
in al, dx  
  
ret  
  
Ct_I2CReadByte Endp  
;Input : CL - register index  
; CH - device ID  
; AL - Value to write  
;Output: none
```

```
Ct_I2CWriteByte Proc Near  
mov ch,06eh
```

```
xchg ah, al  
mov dx, F040h + 00h ; Host Control Register  
xor al, al ; Clear previous commands  
out dx, al  
call Delay5ms  
mov dx, F040h + 04h ; Transmit Slave Address Register  
mov al, ch ; Set the slave address and  
out dx, al ; prepare for a WRITE command  
mov dx, F040h + 05h ; Host Command Register  
mov al, cl ; offset to write  
out dx, al  
mov dx, F040h + 06h  
mov al, ah  
out dx, al  
mov dx, F040h + 01h ; Host Status Register  
mov al, 07h ; Clear all status bits
```

```
out dx, al  
mov dx, F040h + 00h ; Host Control Register  
mov al, 12h ; Start a byte access  
out dx, al  
call CT_Clk_SMBus_Ready ;R14  
ret  
Ct_I2CWriteByte Endp  
; Wait until the busy bit clears, indicating that the SMBUS  
; activity has concluded.  
CT_Clk_SMBus_Ready Proc Near  
mov dx, F040h + 01h ; Host Status Register  
Check_I2C_ByteRead_ForBusy:  
in al, dx  
test al, 08h  
jnz Check_I2C_ByteRead_ForBusy  
Check_I2C_ByteRead_ForStatus:  
in al, dx  
test al, 07h ; HSTS[2:0]=All clearable status bits  
jz Check_I2C_ByteRead_ForStatus  
ret  
CT_Clk_SMBus_Ready Endp  
END begin
```

Appendix E

PICO-APL1-SEMI Quick Installation Guide

E.1 Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Description	Remark
1	PICO-APL1	MB
2	Chassis (Major parts)	
3	Bottom Cover of Chassis	
4	Accessory kits (w/ power button)	
5	Driver DVD w/User Manual (in pdf)	
6	QIG (This Doc.)	A0.3

1



2



3



4



5



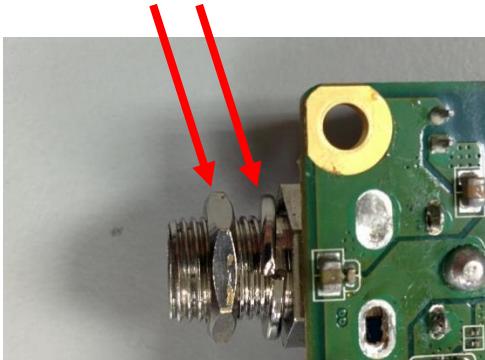
E.2 Assembly procedure

Step 1. Assemble the MB

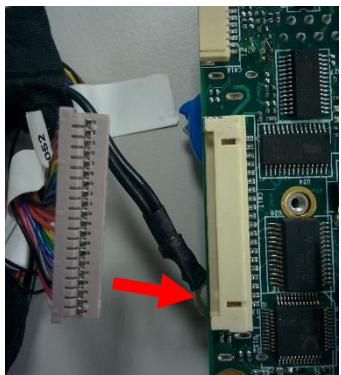
- a. Insert memory into the socket at about 30 degrees. Push it down until it is attached.



- b. Loosen the hexagon shim ring of the DC-Jack on the MB (including a circular shim ring and a hexagonal shim ring).

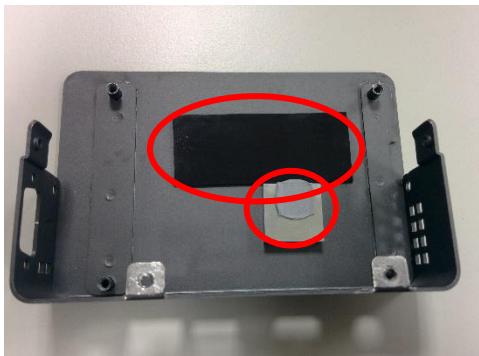


- c. Insert the COM Port 1/2 & line out connector cable until it clicks in (as in the picture below).

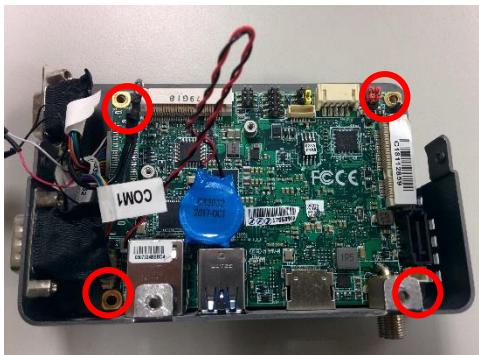


Step 2. Implement MB into the Chassis

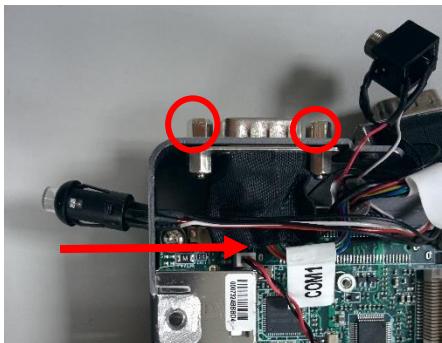
- Remove the protection liner from thermal PAD.



- Install the MB into the chassis, then fasten 4 screws in the corner to the Chassis).



- c. Fasten 2 screws on the side of the chassis for COM Port.
- d. Thread the power button cable from outside to inside of the chassis.



- e. Connect the power button cable to CN3 PIN1,2,3.

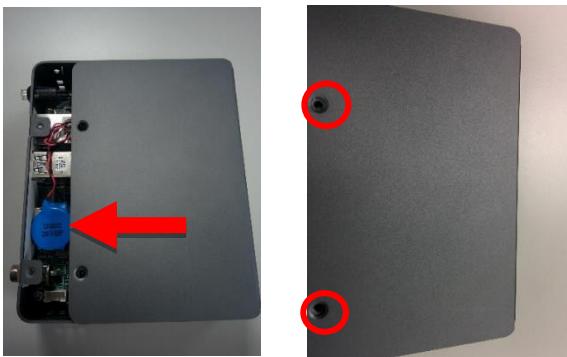


Step 3. Complete the system

- a. Fasten the hexagon shim ring of DC-Jack on MB
- b. Stick the battery to the board



- c. Put the two sides of the chassis together
- d. Fasten the chassis with four flat black screws





Appendix F

PICO-APL1 AI Core Kit Installation Guide

F.1 Product Brief

The AAEON PICO-APL1 AI (artificial intelligence) Core product is bundled with the Intel Movidius Myriad 2 VPU. Before you start to set up the development environment, we suggest you prepare the following items:

- 1 Up to 2G DRAM
- 2 At least 4GB of free storage space connected to the CN8 or CN12 SATA connector for SATA +5V power
- 3 HDMI monitor
- 4 USB keyboard/mouse
- 5 Ubuntu 16.04
- 6 An Internet connection

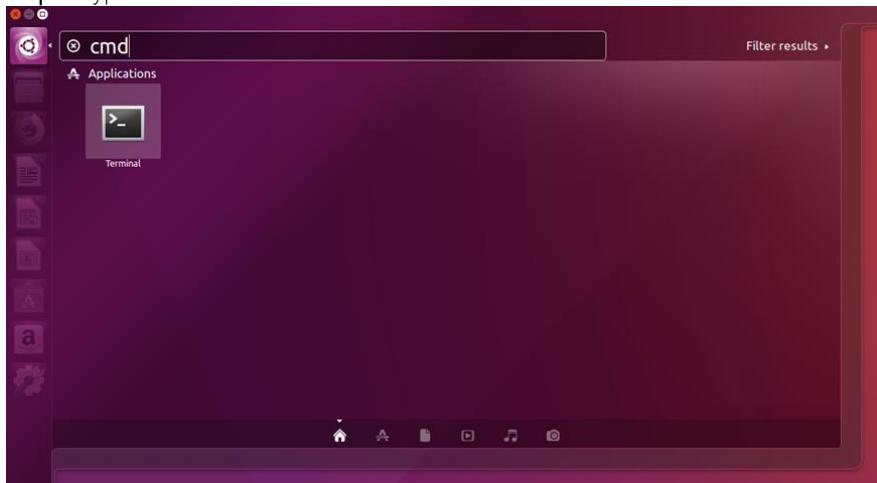
Connect all the above peripherals, then power on and go into CMD (command mode) in Ubuntu.

F.2 Update Ubuntu and Kernel

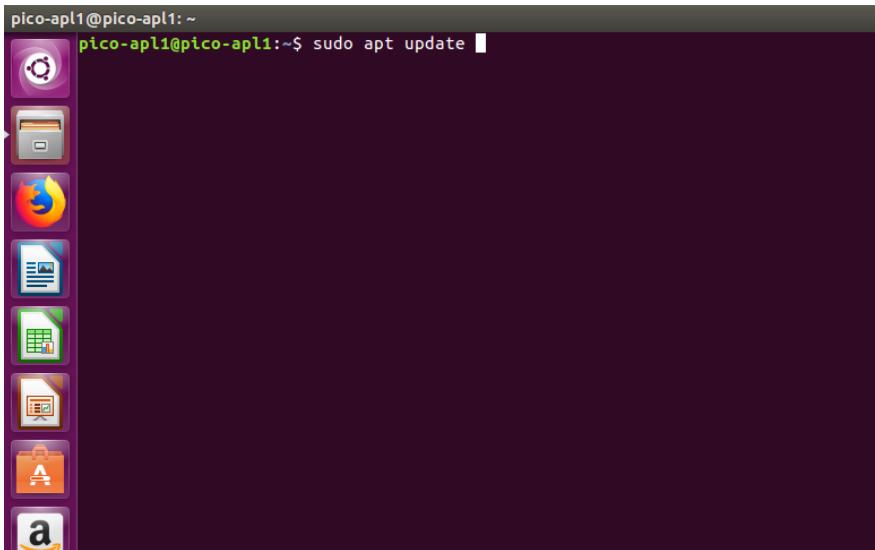
Step 1. To open the terminal, select search



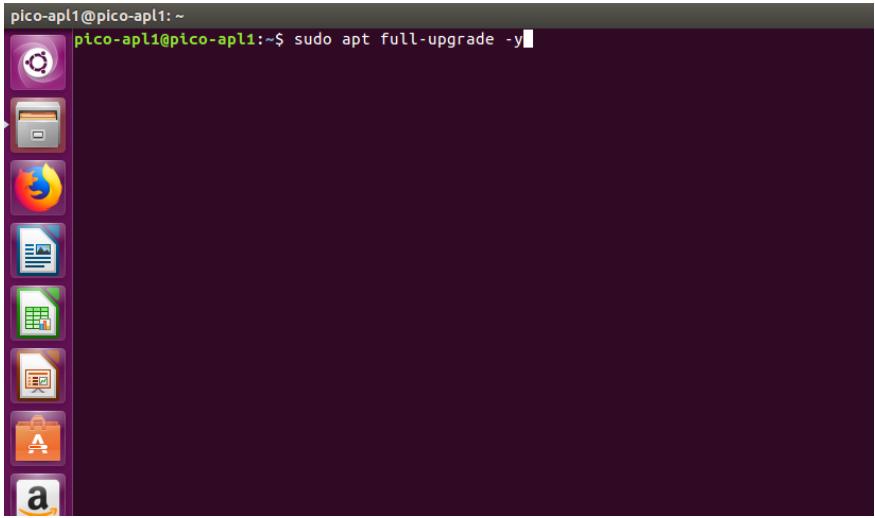
Step 2. Type 'cmd' or 'terminal'



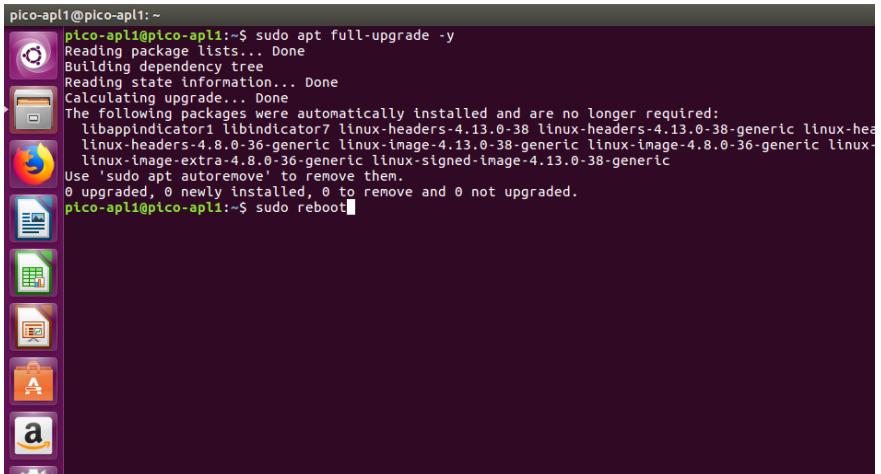
Step 3. Type 'sudo apt update'

A screenshot of the PICO-APL1 desktop environment. On the left is a vertical dock containing icons for the Dash, Home, File Manager, Firefox, LibreOffice Writer, LibreOffice Calc, LibreOffice Impress, LibreOffice Draw, and a folder labeled 'a'. The main window shows a terminal session with the command 'sudo apt update' entered and running.

Step 4. Type 'sudo apt full-upgrade -y'

A screenshot of the PICO-APL1 desktop environment, identical to the previous one but with a different terminal command. The terminal now shows the command 'sudo apt full-upgrade -y' entered and running.

Step 5. Type 'sudo reboot' and the computer will restart



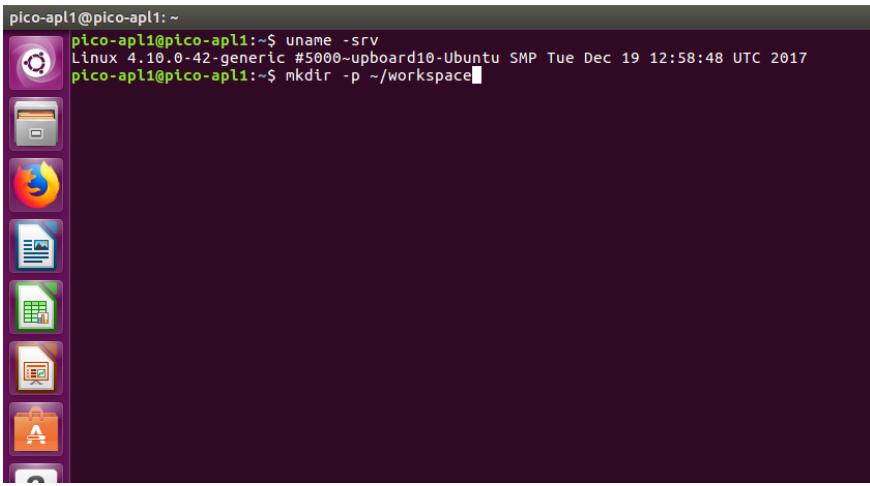
```
pico-apl1@pico-apl1:~$ sudo apt full-upgrade -y
Reading package lists... Done
Building dependency tree
Reading state information... Done
Calculating upgrade... Done
The following packages were automatically installed and are no longer required:
  libappindicator1 libindicator7 linux-headers-4.13.0-38 linux-headers-4.13.0-38-generic linux-headers-4.8.0-36-generic linux-image-4.13.0-38-generic linux-image-4.8.0-36-generic linux-image-extra-4.8.0-36-generic linux-signed-image-4.13.0-38-generic
Use 'sudo apt autoremove' to remove them.
0 upgraded, 0 newly installed, 0 to remove and 0 not upgraded.
pico-apl1@pico-apl1:~$ sudo reboot
```

Step 6. After the restart, open the terminal again

F.3 Install NCSDK

(Please refer to <https://developer.movidius.com/start>)

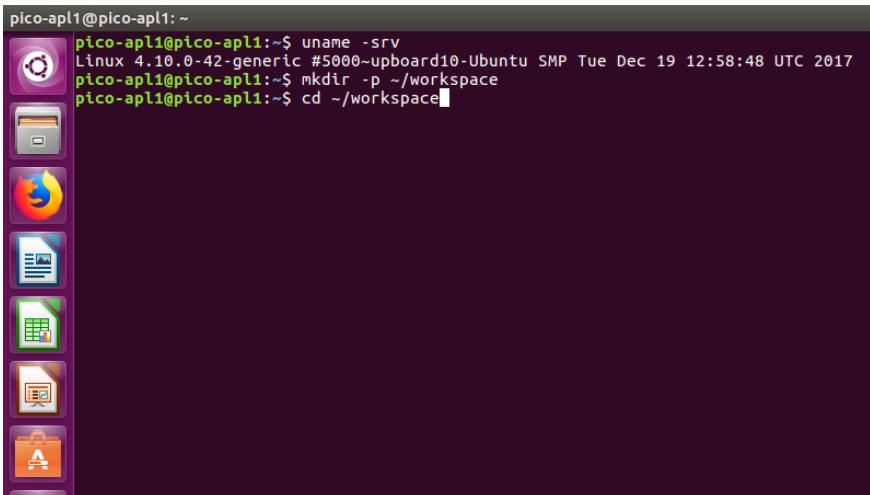
Step 1. Type 'mkdir -p ~/workspace'



```
pico-apl1@pico-apl1:~$ uname -srv
Linux 4.10.0-42-generic #5000-upboard10-Ubuntu SMP Tue Dec 19 12:58:48 UTC 2017
pico-apl1@pico-apl1:~$ mkdir -p ~/workspace
```

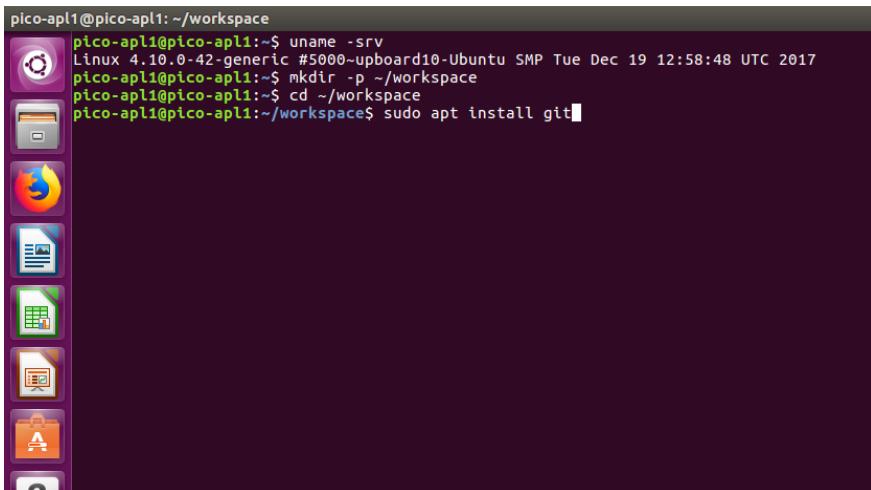
A screenshot of a terminal window titled "PICO-APL1". The window shows a command-line interface with a dark background and light-colored text. The user has run the command "mkdir -p ~/workspace", which creates a new directory in their home folder. The terminal window is surrounded by a purple border, and there are several icons in a dock on the left side.

Step 2. Type 'cd~/workspace'

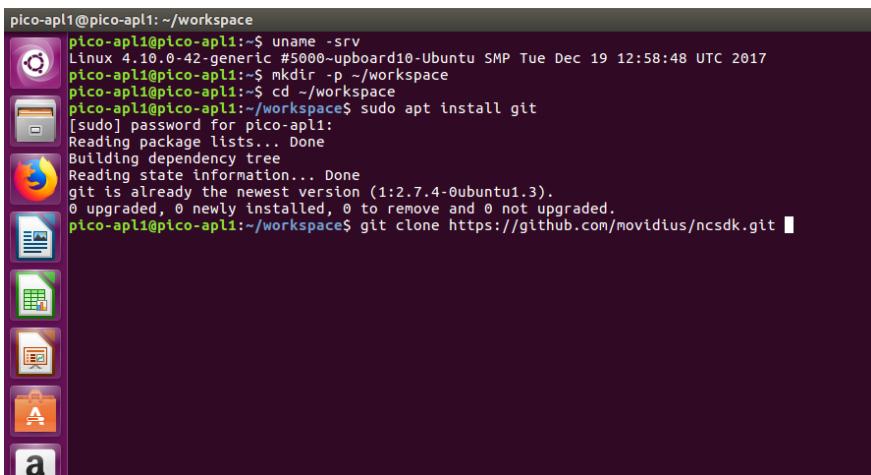


```
pico-apl1@pico-apl1:~$ uname -srv
Linux 4.10.0-42-generic #5000-upboard10-Ubuntu SMP Tue Dec 19 12:58:48 UTC 2017
pico-apl1@pico-apl1:~$ mkdir -p ~/workspace
pico-apl1@pico-apl1:~$ cd ~/workspace
```

This is a continuation of the previous terminal session. The user has run the command "cd ~/workspace", which changes the current working directory to the newly created workspace. The terminal window is surrounded by a purple border, and there are several icons in a dock on the left side.

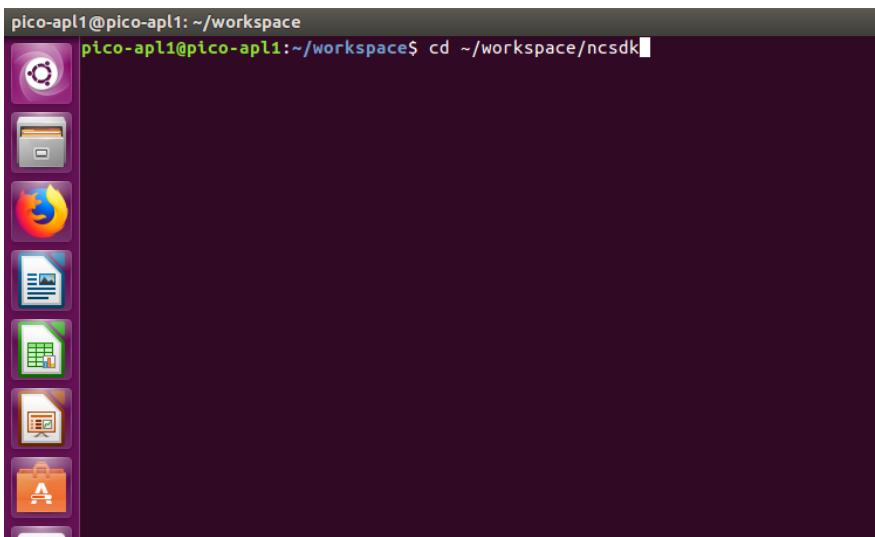
Step 3. Type 'sudo apt install git'

```
pico-apl1@pico-apl1:~/workspace
pico-apl1@pico-apl1:~$ uname -srv
Linux 4.10.0-42-generic #5000-upboard10-Ubuntu SMP Tue Dec 19 12:58:48 UTC 2017
pico-apl1@pico-apl1:~$ mkdir -p ~/workspace
pico-apl1@pico-apl1:~$ cd ~/workspace
pico-apl1@pico-apl1:~/workspace$ sudo apt install git
```

Step 4. Type 'git clone <https://github.com/movidius/ncsdk.git>'

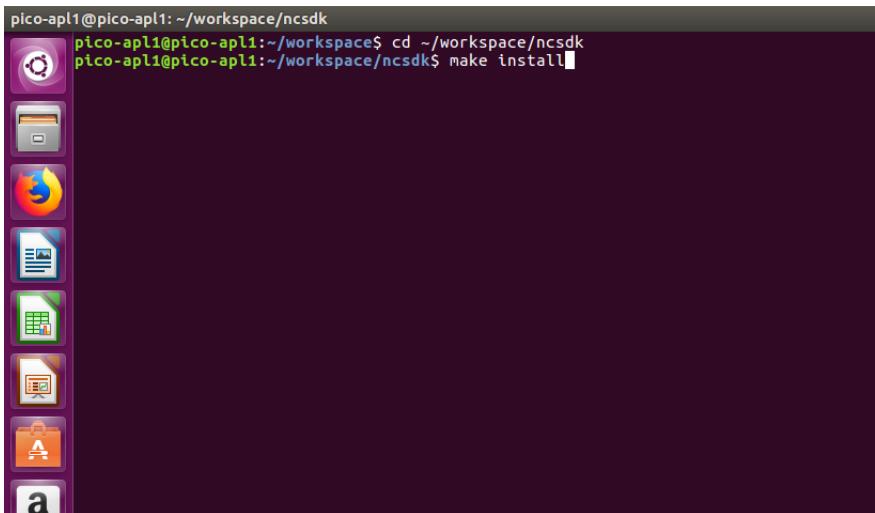
```
pico-apl1@pico-apl1:~/workspace
pico-apl1@pico-apl1:~$ uname -srv
Linux 4.10.0-42-generic #5000-upboard10-Ubuntu SMP Tue Dec 19 12:58:48 UTC 2017
pico-apl1@pico-apl1:~$ mkdir -p ~/workspace
pico-apl1@pico-apl1:~$ cd ~/workspace
pico-apl1@pico-apl1:~/workspace$ sudo apt install git
[sudo] password for pico-apl1:
Reading package lists... Done
Building dependency tree
Reading state information... Done
git is already the newest version (1:2.7.4-0ubuntu1.3).
0 upgraded, 0 newly installed, 0 to remove and 0 not upgraded.
pico-apl1@pico-apl1:~/workspace$ git clone https://github.com/movidius/ncsdk.git
```

Step 5. Type 'cd ~/workspace/ncsdk'



pico-apl1@pico-apl1:~/workspace
pico-apl1@pico-apl1:~/workspace\$ cd ~/workspace/ncsdk

Step 6. Type 'make install'



pico-apl1@pico-apl1:~/workspace/ncsdk
pico-apl1@pico-apl1:~/workspace\$ cd ~/workspace/ncsdk
pico-apl1@pico-apl1:~/workspace\$ make install

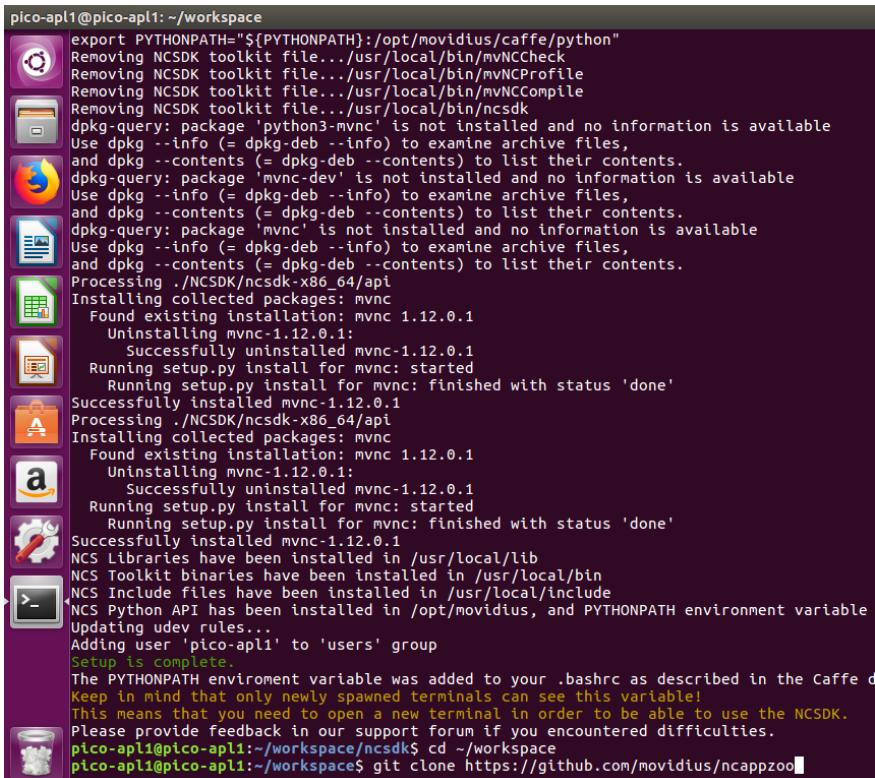
Note: If the installation fails, run 'make install' again.

F.4 Download Movidius Ncappzoo

Step 1. Type 'cd ~/workspace'

```
pico-apl1@pico-apl1:~/workspace/ncsdk
Adding caffe to PYTHONPATH
export PYTHONPATH=$PYTHONPATH:/opt/movidius/caffe/python"
Removing NCSDK toolkit file.../usr/local/bin/mvNCCheck
Removing NCSDK toolkit file.../usr/local/bin/mvNCProfile
Removing NCSDK toolkit file.../usr/local/bin/mvNCCompile
Removing NCSDK toolkit file.../usr/local/bin/ncsdk
dpkg-query: package 'python3-mvnc' is not installed and no information is available
Use dpkg -W (or dpkg --info '(= dpkg-deb -W info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
dpkg-query: package 'mvnc-dev' is not installed and no information is available
Use dpkg -W (or dpkg --info '(= dpkg-deb -W info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
dpkg-query: package 'mvnc' is not installed and no information is available
Use dpkg -W (or dpkg --info '(= dpkg-deb -W info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
Processing ./NCSDK/ncsdk-x86_64/api
Installing collected packages: mvnc
  Found existing installation: mvnc 1.12.0.1
    Uninstalling mvnc-1.12.0.1:
      Successfully uninstalled mvnc-1.12.0.1
    Running setup.py install for mvnc: started
      Running setup.py install for mvnc: finished with status 'done'
Successfully installed mvnc-1.12.0.1
Processing ./NCSDK/ncsdk-x86_64/api
Installing collected packages: mvnc
  Found existing installation: mvnc 1.12.0.1
    Uninstalling mvnc-1.12.0.1:
      Successfully uninstalled mvnc-1.12.0.1
    Running setup.py install for mvnc: started
      Running setup.py install for mvnc: finished with status 'done'
Successfully installed mvnc-1.12.0.1
NCS Libraries have been installed in /usr/local/lib
NCS Toolkit binaries have been installed in /usr/local/bin
NCS Python API has been installed in /opt/movidius, and PYTHONPATH environment variable updated
Updating udev rules...
Adding user 'pico-apl1' to 'users' group
Setup is complete.
The PYTHONPATH environment variable was added to your .bashrc as described in the Caffe documentation.
Keep in mind that only newly spawned terminals can see this variable!
This means that you need to open a new terminal in order to be able to use the NCSDK.
Please provide feedback in our support forum if you encountered difficulties.
pico-apl1@pico-apl1:~/workspace/ncsdk$ cd ~/workspace
```

Step 2. Type 'git clone <https://github.com/movidius/ncappzoo>'



```
pico-apl1@pico-apl1: ~/workspace
export PYTHONPATH="${PYTHONPATH}:/opt/movidius/caffe/python"
Removing NCSDK toolkit file.../usr/local/bin/mvNCCheck
Removing NCSDK toolkit file.../usr/local/bin/mvNCProfile
Removing NCSDK toolkit file.../usr/local/bin/mvNCCompile
Removing NCSDK toolkit file.../usr/local/bin/ncsdk
dpkg-query: package 'python3-mvnc' is not installed and no information is available
Use dpkg --info (= dpkg-deb --info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
dpkg-query: package 'mvnc-dev' is not installed and no information is available
Use dpkg --info (= dpkg-deb --info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
dpkg-query: package 'mvnc' is not installed and no information is available
Use dpkg --info (= dpkg-deb --info) to examine archive files,
and dpkg --contents (= dpkg-deb --contents) to list their contents.
Processing ./NCSDK/ncsdk-x86_64/api
Installing collected packages: mvnc
  Found existing installation: mvnc 1.12.0.1
    Uninstalling mvnc-1.12.0.1:
      Successfully uninstalled mvnc-1.12.0.1
  Running setup.py install for mvnc: started
    Running setup.py install for mvnc: finished with status 'done'
Successfully installed mvnc-1.12.0.1
Processing ./NCSDK/ncsdk-x86_64/api
Installing collected packages: mvnc
  Found existing installation: mvnc 1.12.0.1
    Uninstalling mvnc-1.12.0.1:
      Successfully uninstalled mvnc-1.12.0.1
  Running setup.py install for mvnc: started
    Running setup.py install for mvnc: finished with status 'done'
Successfully installed mvnc-1.12.0.1
NCS Libraries have been installed in /usr/local/lib
NCS Toolkit binaries have been installed in /usr/local/bin
NCS Include files have been installed in /usr/local/include
NCS Python API has been installed in /opt/movidius, and PYTHONPATH environment variable
Updating udev rules...
Adding user 'pico-apl1' to 'users' group
Setup is complete.
The PYTHONPATH environment variable was added to your .bashrc as described in the Caffe documentation.
Keep in mind that only newly spawned terminals can see this variable!
This means that you need to open a new terminal in order to be able to use the NCSDK.
Please provide feedback in our support forum if you encountered difficulties.
pico-apl1@pico-apl1:~/workspace/ncsdk$ cd ~/workspace
pico-apl1@pico-apl1:~/workspace$ git clone https://github.com/movidius/ncappzoo
```

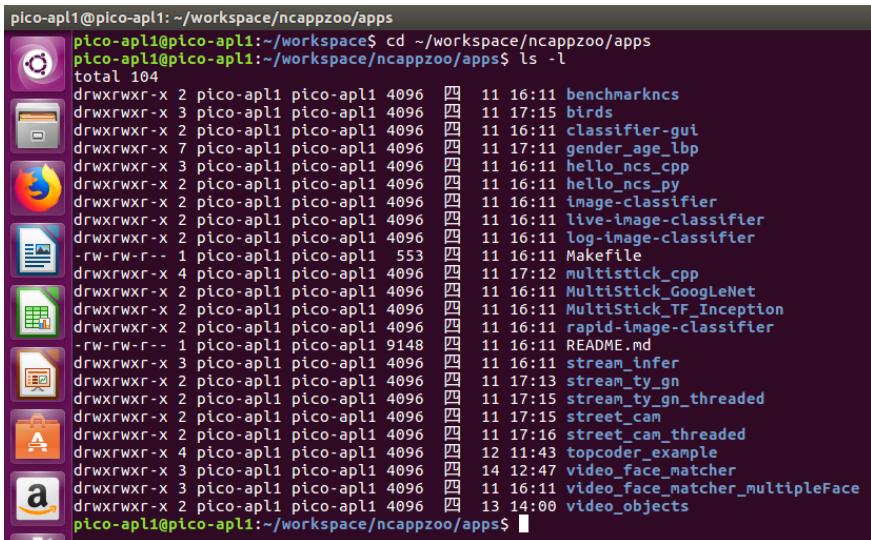
Step 3. Type 'cd ~(workspace/ncappzoo/apps/street_cam && make opencv'

After installing NCSDK, Ncappzoo and OpenCV, you can start running demos.

Step 1. Type 'cd ~/workspace/ncappzoo/apps'

Step 2. Type 'ls -l'

You will see the names of many different folders. Choose one you want.



```
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$ cd ~/workspace/ncappzoo/apps
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$ ls -l
total 104
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 benchmarkncs
drwxrwxr-x 3 pico-apl1 pico-apl1 4096  11 17:15 birds
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 classifier-gui
drwxrwxr-x 7 pico-apl1 pico-apl1 4096  11 17:11 gender_age_lbp
drwxrwxr-x 3 pico-apl1 pico-apl1 4096  11 16:11 hello_ncs_cpp
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 hello_ncs_py
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 image-classifier
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 live-image-classifier
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 log-image-classifier
-rw-rw-r-- 1 pico-apl1 pico-apl1 553   11 16:11 Makefile
drwxrwxr-x 4 pico-apl1 pico-apl1 4096  11 17:12 multistick_cpp
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 Multistick_GoogLeNet
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 MultiStick_TF_Inception
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 16:11 rapid-image-classifier
-rw-rw-r-- 1 pico-apl1 pico-apl1 9148  11 16:11 README.md
drwxrwxr-x 3 pico-apl1 pico-apl1 4096  11 16:11 stream_infer
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 17:13 stream_ty_gn
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 17:15 stream_ty_gn_threaded
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 17:15 street_cam
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  11 17:16 street_cam_threaded
drwxrwxr-x 4 pico-apl1 pico-apl1 4096  12 11:43 topcoder_example
drwxrwxr-x 3 pico-apl1 pico-apl1 4096  14 12:47 video_face_matcher
drwxrwxr-x 3 pico-apl1 pico-apl1 4096  11 16:11 video_face_matcher_multipleFace
drwxrwxr-x 2 pico-apl1 pico-apl1 4096  13 14:00 video_objects
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$
```

Step 3. Type 'cd <folder's name>'

Step 4. Type 'make help'

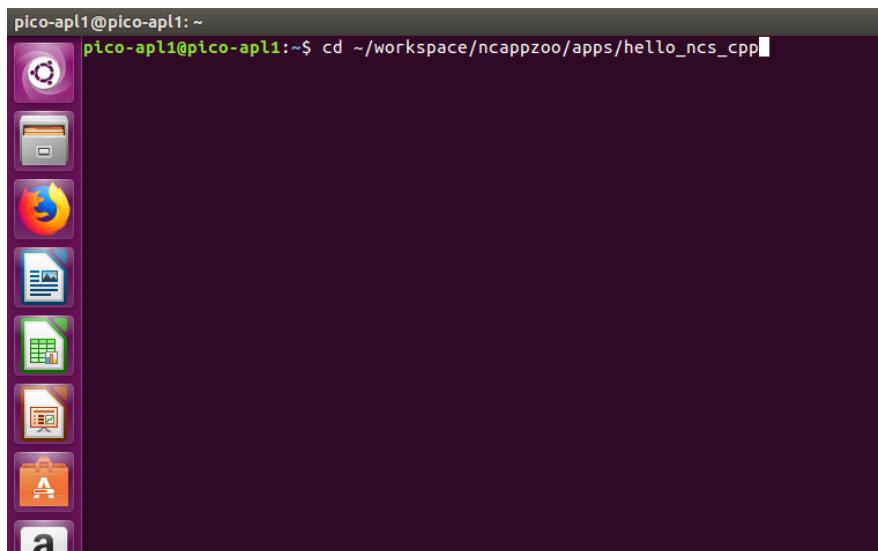
You will see all the commands you can use on each page.

```
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps
pico-apl1@pico-apl1:~/workspace/ncappzoo$ cd ~/workspace/ncappzoo/apps
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$ ls -l
total 104
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 benchmarkncs
drwxrwxr-x 3 pico-apl1 pico-apl1 4096 11 17:15 birds
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 classifier-gui
drwxrwxr-x 7 pico-apl1 pico-apl1 4096 11 17:11 gender_age_lbp
drwxrwxr-x 3 pico-apl1 pico-apl1 4096 11 16:11 hello_ncs_cpp
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 hello_ncs_py
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 image-classifier
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 live-image-classifier
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 log-image-classifier
-rw-rw-r-- 1 pico-apl1 pico-apl1 553 11 16:11 Makefile
drwxrwxr-x 4 pico-apl1 pico-apl1 4096 11 17:12 multistick_cpp
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 MultiStick_GoogLeNet
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 MultiStick_TF_Inception
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 16:11 rapid-image-classifier
-rw-rw-r-- 1 pico-apl1 pico-apl1 9148 11 16:11 README.md
drwxrwxr-x 3 pico-apl1 pico-apl1 4096 11 16:11 stream_infer
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 17:13 stream_ty_gn
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 17:15 stream_ty_gn_threaded
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 17:15 street_cam
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 11 17:16 street_cam_threaded
drwxrwxr-x 4 pico-apl1 pico-apl1 4096 12 11:43 topcoder_example
drwxrwxr-x 3 pico-apl1 pico-apl1 4096 14 12:47 video_face_matcher
drwxrwxr-x 3 pico-apl1 pico-apl1 4096 11 16:11 video_face_matcher_multipleFace
drwxrwxr-x 2 pico-apl1 pico-apl1 4096 13 14:00 video_objects
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$ make help
Possible make targets:
    make help - shows this message
    make all - does make all in each sub directory
    make clean - does make clean in each subdirectory
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps$
```

F.5 Example in Movidius Ncappzoo

*(example: cd ~/workspace/ncappzoo/apps/hello_ncs_cpp && make run)

Step 1. Type 'cd ~/workspace/ncappzoo/apps/hello_ncs_cpp'

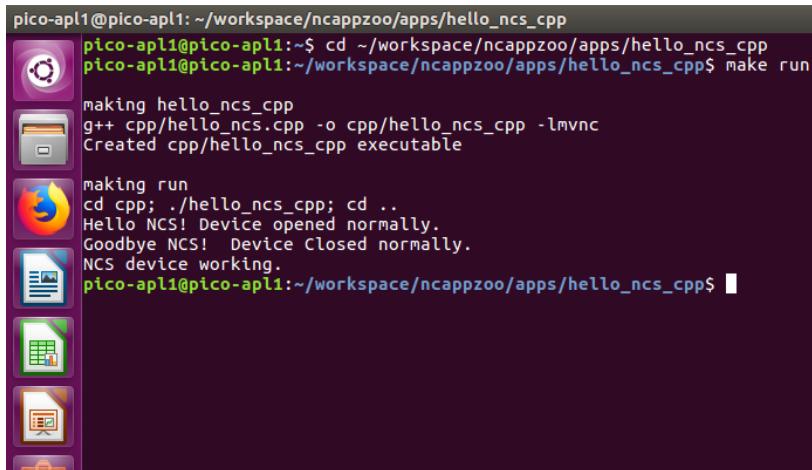


A screenshot of a terminal window on a Linux system. The window title is 'pico-apl1@pico-apl1: ~'. The user has typed the command 'cd ~/workspace/ncappzoo/apps/hello_ncs_cpp' into the terminal. To the left of the terminal window, there is a vertical dock containing icons for various applications, including a terminal icon, a file manager icon, a browser icon, a file viewer icon, a terminal icon, a file viewer icon, a terminal icon, and a file viewer icon.

```
pico-apl1@pico-apl1:~$ cd ~/workspace/ncappzoo/apps/hello_ncs_cpp
```

Step 2. Type 'make help'

You will see all the commands you can use on each page.

Step 3. Type 'make run'

```
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps/hello_ncs_cpp
pico-apl1@pico-apl1:~$ cd ~/workspace/ncappzoo/apps/hello_ncs_cpp
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps/hello_ncs_cpp$ make run
making hello_ncs_cpp
g++ cpp/hello_ncs.cpp -o cpp/hello_ncs_cpp -lmvnc
Created cpp/hello_ncs_cpp executable
making run
cd cpp; ./hello_ncs_cpp; cd ..
Hello NCS! Device opened normally.
Goodbye NCS! Device Closed normally.
NCS device working.
pico-apl1@pico-apl1:~/workspace/ncappzoo/apps/hello_ncs_cpp$ █
```

F.6 Appendix

With some relative directories, for example “video or graphic” relative directories, you need to install “*opencv*” before you can start working.

You can install “*opencv*” in the following directory:

```
cd~ workspace/ncappzo/apps/stree_cam  
make opencv.
```

Other

Some demos might need 2 or more Movidius modules, an Internet connection or a USB Camera. Customers can purchase more USB type Movidius Neural Compute Sticks and plug them in to a USB port.

Good link to check:

<https://developer.movidius.com/start>

<https://github.com/movidius/ncappzoo>

AAEON Accessory:

968C064G52 : 64GB SATA DOM with Power Cable.

PICO-APL1-HSP01: Heat-spreader

PICO-APL1-HSK01: Heat-sink, to be used with Heat-spreader