PICO-KBU4

PICO-KBU4 Single-Board Computer

User's Manual 2nd Ed

Last Updated: February 11, 2019

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-KBU4	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1 - Product Specifications 1

1.1 Specifications 2

Chapter 2 – Hardware Information 5

2.1 Dimensions 6

2.2 Jumpers and Connectors 8

2.3 List of Jumpers 10

2.3.1 LVDS Backlight Lightness Control Mode Selection (JP3) 11

2.3.2 LVDS Operating Voltage Selection (JP4) 11

2.3.3 LVDS Backlight Inverter Voltage Selection (JP4) 11

2.3.4 Clear CMOS Jumper (JP5) 11

2.3.5 Auto Power Button Enable/Disable Selection (JP5) 12

2.4 List of Connectors 13

2.4.1 RTC Battery Connector (CN1) 14

2.4.2 HDMI (CN2) 14

2.4.3 LVDS Inverter / Backlight Connector (CN4) 16

2.4.4 LVDS Port (CN5) 17

2.4.5 LAN (RJ-45) Port1 (CN6) 19

2.4.6 LAN (RJ-45) Port2 (CN7) 20

2.4.7 Digital IO Port (CN9) 21

2.4.8 USB 2.0 Port 1/2 (CN10) 22

2.4.9 USB 2.0/3.0 Port 3 Port 3/4 (CN11) 23

2.4.10 External +12V Input (CN14) 24

2.4.11 Front Panel Port (CN15) 25

2.4.12 COM Port1/ COM Port2 (CN16) 26

2.4.13 BIO Bank1 Connector (CN17) 28

2.4.14 LPC Port (CN19) 33

2.4.15 SATA Port (CN20) 34
2.4.16 +5V Output for SATA HDD (CN21) 35
2.4.17 M.2 (Key B) Connector (CN26) 35
2.4.18 Smart FAN Connector (CN27) 39
2.4.19 M.2 (Key E) Connector (CN30) 39
2.4.20 DDR4 SO-DIMM Slot (DIMM1) 42
2.5 Function Block 43
2.6 Assembly Options 44
Chapter 3 - AMI BIOS Setup 46
3.1 System Test and Initialization 47
3.2 AMI BIOS Setup 48
3.3 Setup Submenu: Main 49
3.4 Setup Submenu: Advanced 50
3.4.1 CPU configuration 51
3.4.2 SATA Configuration 53
3.4.3 Hardware Monitor 54
3.4.3.1 CPU Smart Fan Mode Configuration 55
3.4.4 SIO Configuration 56
3.4.4.1 Serial Port Configuration 57
3.4.5 USB Configuration 58
3.4.6 Digital IO Port Configuration 59
3.4.7 Power management 60
3.4.8 Firmware Update Configuration 61
3.5 Setup submenu: Chipset 62
3.5.1 System Agent (SA) Configuration 63
3.5.1.1 Graphics Configuration 64
3.5.1.1.1 LVDS Panel Configuration 65
3.5.2 PCH-IO Configuration 67

3.6 Setup submenu: Security....68
3.7 Setup submenu: Boot....69
3.7.1 BBS Priorities....70
3.8 Setup submenu: Exit....71
Chapter 4 – Drivers Installation....72
4.1 Driver Download/Installation....73
Appendix A - Watchdog Timer Programming....75
A.1 Watchdog Timer Registers....76
A.2 Watchdog Sample Program....77
Appendix B - I/O Information....80
B.1 I/O Address Map....81
B.2 Memory Address Map....82
B.3 IRQ Mapping Chart....83
Appendix C – Mating Connectors....84
C.1 List of Mating Connectors and Cables....85
Appendix D – DIO....87
D.1 DIO....88

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Pico-ITX
CPU	7th Generation Intel® Core™ i processor U series, Intel® i7-7600U, i5-7300U, i3-7100U series & Celeron® 3965U (optional)
CPU Frequency	Up to 3.9/2.8 GHz
Chipset	7th Generation Intel® Core™ i processor U series, Intel® i7-7600U, i5-7300U, i3-7100U series & Celeron® 3965U (optional)
Memory Type	DDR4 1866/2133MHz SODIMM x 1, Max. 16 GB
Max. Memory Capacity	Up to 16 GB
BIOS	AMI/SPI
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V AT/ATX (default)
Power Supply Type	AT/ATX (default)
Power Consumption (Typical)	i7-7600@DDR4 16GB, 12V@2.3A
System Cooling	Heat-spreader, heatsink & cooler (Smart FAN) optional
Dimension	3.94" x 2.84" (100mm x 72mm)

System

Gross Weight	0,55 lb (0.25 Kg)
Operating Temperature	32˚F ~ 140˚F (0˚C ~ 60˚C)
Storage Temperature	-40˚F ~ 176˚F (-40˚C ~ 80˚C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	163,000
Certification	CE, FCC

Display

Chipset	7th Generation Intel® Core™ i processor U series, Intel® i7-7600U, i5-7300U, i3-7100U series & Celeron® 3965U (Optional)
Resolution	LVDS (18/24-bit 2CH) 1920 x 1200 HDMI 1.4b up to 4096 x 2304 (4K) DDI (BIO)
LCD Interface	18/24-bit 2CH LVDS

I/O

Storage/SSD	SATA 6.0 Gb/s x 1, M.2 B-key (2242)
Ethernet	Realtek 8111G Gigabit Ethernet 10/100/1000Base-TX, RJ-45 x 2
USB Port	USB 3.0 x 2 Rear I/O, USB 2.0 x 2 Pin header
Serial Port	COM1: RS-232 x 1, COM2: RS-232/422/485 x 1 (Ring/ +5V/ +12V)
Audio	Line-out x1

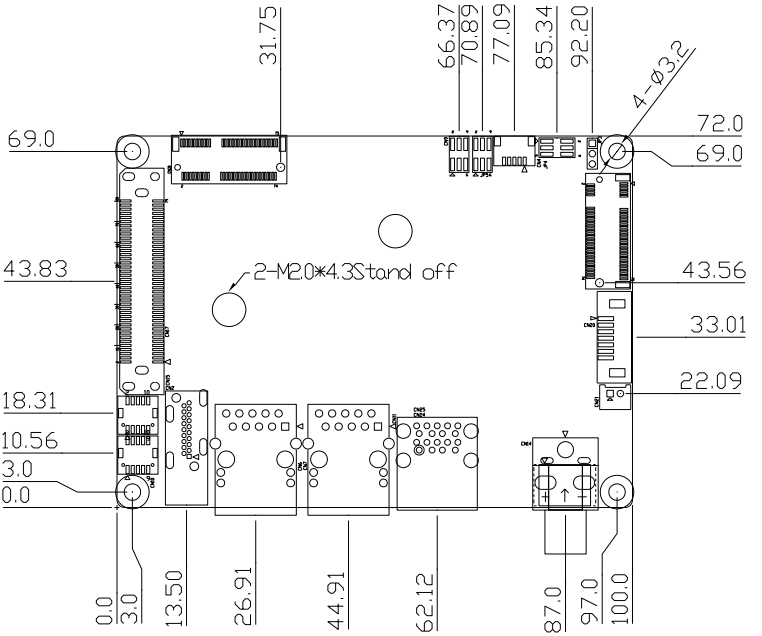
I/O	
DIO	4-bit (2-in, 2-out)
Expansion Slot	M.2 E-Key (2230), BIO (optional), I2C x 1 or Smbus x 1
SIM	—
TPM	—
Touch	—

Chapter 2

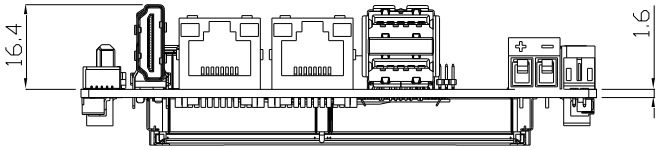
Hardware Information

2.1 Dimensions

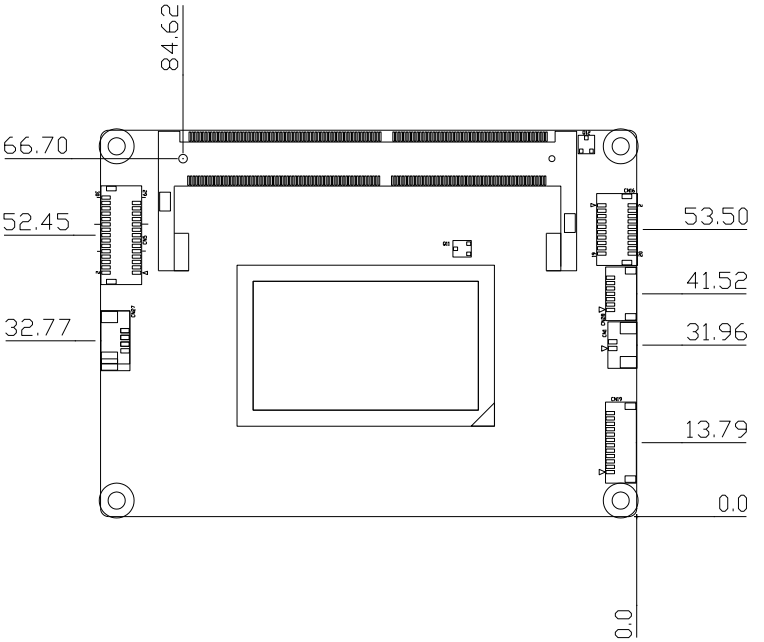
Component Side



Component Side



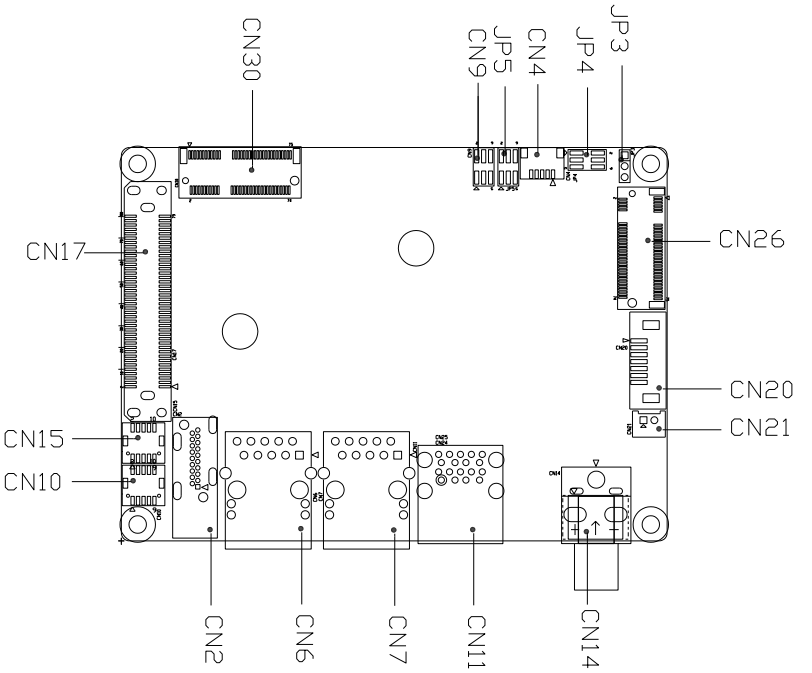
Solder Side



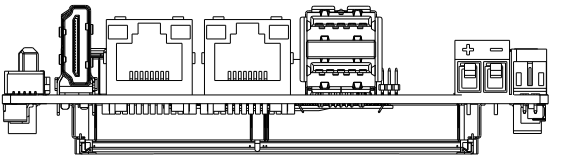
Solder Side

2.2 Jumpers and Connectors

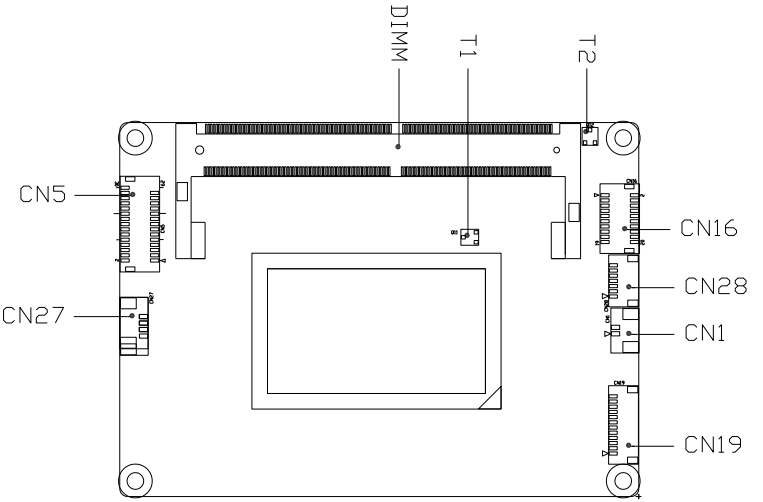
Component Side



Component Side



Solder Side



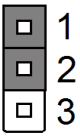
Solder Side

2.3 List of Jumpers

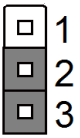
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP3	LVDS Backlight Lightness Control Mode Selection
JP4	LVDS Operating Voltage Selection LVDS Backlight Inverter Voltage Selection
JP5	Clear CMOS Jumper Auto Power Button Enable/Disable Selection

2.3.1 LVDS Backlight Lightness Control Mode Selection (JP3)

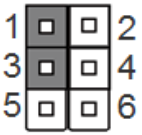


VR Mode(Default)

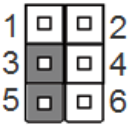


PWM Mode

2.3.2 LVDS Operating Voltage Selection (JP4)

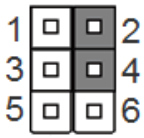


+5V

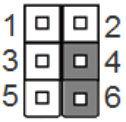


+3.3V (Default)

2.3.3 LVDS Backlight Inverter Voltage Selection (JP4)

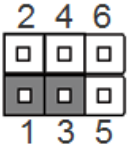


+12V (Default)

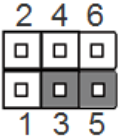


+5V

2.3.4 Clear CMOS Jumper (JP5)

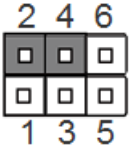


Normal (Default)

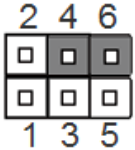


Clear CMOS

2.3.5 Auto Power Button Enable/Disable Selection (JP5)



Enable Auto Power Button (Default)



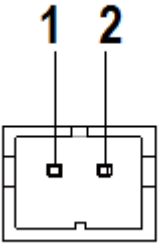
Disable Auto Power Button

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

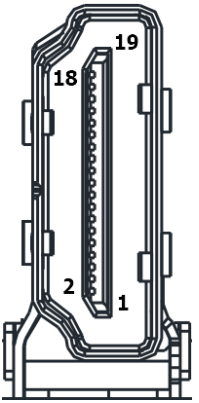
Label	Function
CN1	RTC Battery Connector
CN2	HDMI
CN4	LVDS Inverter / Backlight Connector
CN5	LVDS Port
CN6	LAN (RJ-45) Port1
CN7	LAN (RJ-45) Port2
CN9	Digital IO Port
CN10	USB 2.0 Port 1/2
CN11	USB 2.0/3.0 Port 3 Port 0/1
CN14	External +12V Input
CN15	Front Panel
CN16	COM Port1/ COM Port2
CN17	BIO Bank1 Connector
CN19	LPC Port
CN20	SATA Port
CN21	+5V Output for SATA HDD
CN26	M.2 (Key B) Connector
CN27	Smart FAN Connector
CN30	M.2 (Key E) Connector
DIMM1	DDR4 SO-DIMM Slot

2.4.1 RTC Battery Connector (CN1)



Pin	Pin Name	Signal Type	Pin Name
1	GND	GND	GND
2	+3.3V	PWR	+3.3V

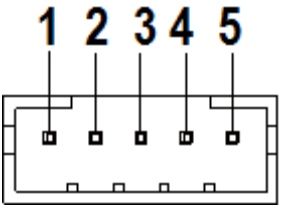
2.4.2 HDMI (CN2)



Pin	Pin Name	Signal Type	Signal level
1	HDMI_TX2+	DIFF	
2	GND	GND	GND
3	HDMI_TX2-	DIFF	

Pin	Pin Name	Signal Type	Signal level
4	HDMI_TX1+	DIFF	
5	GND	GND	GND
6	HDMI_TX1-	DIFF	
7	HDMI_TX0+	DIFF	
8	GND	GND	GND
9	HDMI_TX0-	DIFF	
10	HDMI_CLK+	DIFF	
11	GND	GND	GND
12	HDMI_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	GND
18	+5V	PWR	+5V
19	HDMI_HPD		

2.4.3 LVDS Inverter / Backlight Connector (CN4)



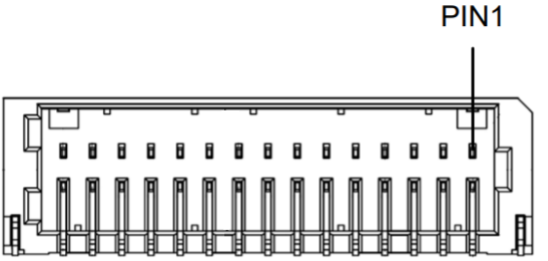
Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	GND
4	GND	GND	GND
5	BKL_ENABLE	OUT	+3.3V

※ LVDS/BKL_PWR can be set to +5V or +12V by JP4.

※ LVDS/BKL_CONTROL can be set by JP3.

※ The driving current supports up to 1A.

2.4.4 LVDS Port (CN5)



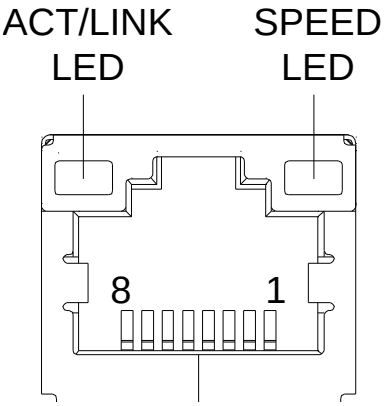
※ LVDS LCD_PWR can be set to +3.3V or +5V by JP4.

※ The max. driving current is 1A.

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	GND
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	GND
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V

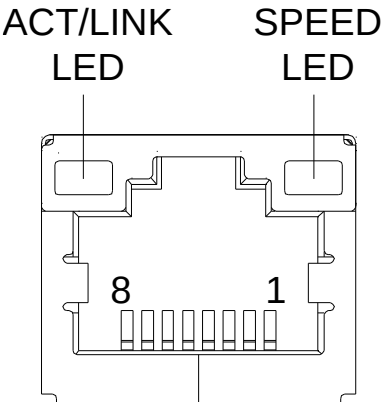
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	GND
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.4.5 LAN (RJ-45) Port1 (CN6)



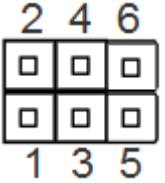
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.6 LAN (RJ-45) Port2 (CN7)



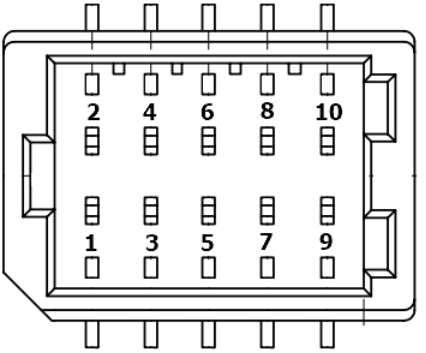
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.7 Digital IO Port (CN9)



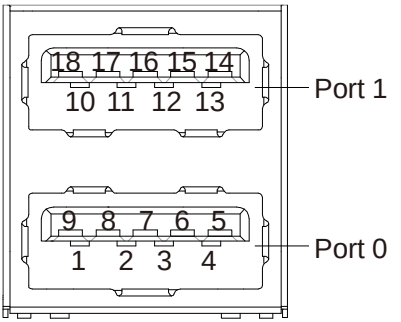
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	DIO_0	IN/OUT	
3	DIO_1	IN/OUT	
4	DIO_2	IN/OUT	
5	DIO_3	IN/OUT	
6	GND	GND	GND

2.4.8 USB 2.0 Port 1/2 (CN10)



Pin	Pin Name	Signal Type	Signal Level
1	+V5SB	PWR	+5V
2	+V5SB	PWR	+5V
3	USB1_D-	DIFF	
4	USB2_D-	DIFF	
5	USB1_D+	DIFF	
6	USB2_D+	DIFF	
7	GND	GND	GND
8	GND	GND	GND
9	GND	GND	GND
10	GND	GND	GND

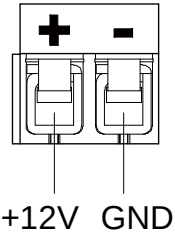
2.4.9 USB 2.0/3.0 Port 3 Port 3/4 (CN11)



Pin	Pin Name	Signal Type	Signal Level
1	+V5SB	PWR	+5V
2	USB3_D-	DIFF	
3	USB3_D+	DIFF	
4	GND	GND	GND
5	USB3_SSRX−	DIFF	
6	USB3_SSRX+	DIFF	
7	GND	GND	GND
8	USB3_SSTX−	DIFF	
9	USB3_SSTX+	DIFF	
10	+V5SB	PWR	+5V
11	USB4_D-	DIFF	
12	USB4_D+	DIFF	
13	GND	GND	GND
14	USB4_SSRX−	DIFF	
15	USB4_SSRX+	DIFF	
16	GND	GND	GND
17	USB4_SSTX−	DIFF	

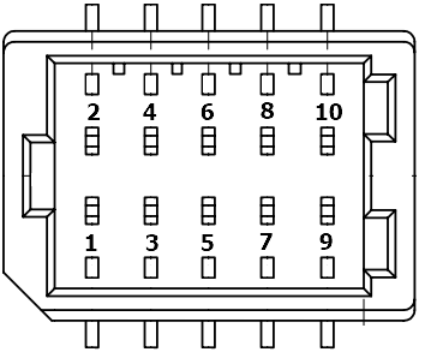
18	USB4_SSTX+	DIFF

2.4.10External +12V Input (CN14)



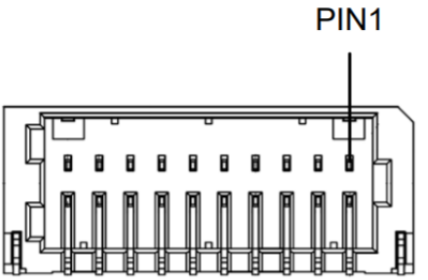
Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	GND

2.4.11 Front Panel Port (CN15)



Pin	Pin Name	Signal Type	Signal level
1	GND	GND	GND
2	EXT_PWRBTN#	IN	
3	SATA_LED-	OUT	
4	SATA_LED+	OUT	
5	BUZZER-	OUT	
6	BUZZER+	OUT	
7	GND	GND	GND
8	PWR_LED+	OUT	
9	GND	GND	GND
10	HWRST#	IN	

2.4.12COM Port1/ COM Port2 (CN16)



Pin	Pin Name	Signal Type	Signal Level
1	LOUT_L	OUT	
2	LOUT_R	OUT	
3	GND	GND	GND
4	AGND	GND	GND
5	DCDA	IN	
6	DCDB	IN	
7	RXA	IN	
8	RXB	IN	
9	TXA	OUT	±9V
10	TXB	OUT	±9V
11	DTRA	OUT	±9V
12	DTRB	OUT	±9V
13	DSRA	IN	
14	DSRB	IN	
15	RTSA	OUT	±9V
16	RTSB	OUT	±9V

17	CTSA	IN	
18	CTSB	IN	
19	RIA/+5V/+12V	IN/ PWR	+5V/+12V
20	RIB/+5V/+12V	IN/ PWR	+5V/+12V

COM Port 2 RS-422			
Pin	Pin Name	Signal Type	Signal Level
3	GND	GND	GND
6	RS422_TX-	OUT	±5V
8	RS422_TX+	OUT	±5V
10	RS422_RX+	IN	
12	RS422_RX-	IN	

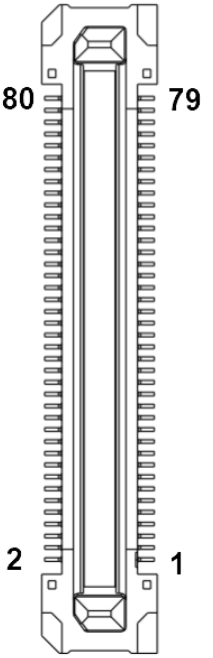
COM Port 2 RS-485			
Pin	Pin Name	Signal Type	Signal Level
3	GND	GND	GND
6	RS485_D-	I/O	±5V
8	RS485_D+	I/O	±5V

※ COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

※ COM2 RI/+5V/+12V function can be set by

BOM(R317-RI/R316-+12V/R318-+5V)

2.4.13BIO Bank1 Connector (CN17)



Pin	Pin Name		Signal Type	Signal Level
1	+12V	PWR	+12V	
2	GND	GND	GND	
3	GND	GND	GND	
4	PCIE9_TXN	DIFF		
5	PCIE9_RXN	DIFF		
6	PCIE9_TXP	DIFF		
7	PCIE9_RXP	DIFF		
8	GND	GND	GND	

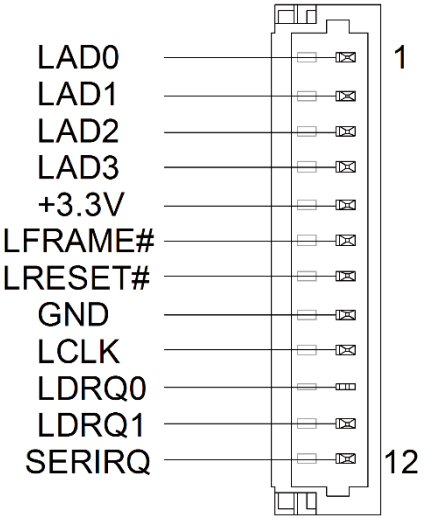
Pin	Pin Name		Signal Type	Signal Level
9	GND	GND	GND	
10	PCIE10_TXN	DIFF		
11	PCIE10_RXN	DIFF		
12	PCIE10_TXP	DIFF		
13	PCIE10_RXP	DIFF		
14	GND	GND	GND	
15	GND	GND	GND	
16	PS_ON#	OUT		
17	DDI1_CTRL_CLK	OUT		
18	DDI1_CTRL_DATA	IN/OUT		
19	+V5A	PWR	+5V	
20	+V5A	PWR	+5V	
21	+V5A	PWR	+5V	
22	+V5A	PWR	+5V	
23	CLK_PCIE_P4	DIFF		
24	BUF_PLT_RST#	OUT		
25	CLK_PCIE_N4	DIFF		
26	GND	GND	GND	
27	GND	GND	GND	
28	DDI1_LANE1_DN	OUT		

Pin	Pin Name		Signal Type	Signal Level
29	DDI1_LANE0_DN	OUT		
30	DDI1_LANE1_DP	OUT		
31	DDI1_LANE0_DP	OUT		
32	GND	GND	GND	
33	GND	GND	GND	
34	DDI1_LANE3_DN	OUT		
35	DDI1_LANE2_DN	OUT		
36	DDI1_LANE3_DP	OUT		
37	DDI1_LANE2_DP	OUT		
38	GND	GND	GND	
39	GND	GND	GND	
40	DDI1_HPD	OUT		
41	DDI1_AUX_DN	OUT		
42	GND	GND	GND	
43	DDI1_AUX_DP	OUT		
44	USB3_4_TXN	IN/OUT		
45	GND	GND	GND	
46	USB3_4_TXP	IN/OUT		
47	USB2N_4	IN/OUT		
48	GND	GND	GND	

Pin	Pin Name		Signal Type	Signal Level
49	USB2P_4	IN/OUT		
50	USB3_4_RXN	IN/OUT		
51	GND	GND	GND	
52	USB3_4_RXP	IN/OUT		
53	SMB_CLK	OUT	+3.3V	
54	GND	GND	GND	
55	SMB_DATA	IN/OUT	+3.3V	
56	PCIE_WAKE#	IN		
57	GND	GND	GND	
58	USB2_OC3#	IN		
59	+V5S	PWR	+5V	
60	USB2_OC3#	IN		
61	+V5S	PWR	+5V	
62	+V5S	PWR	+5V	
63	+V5S	PWR	+5V	
64	+V5S	PWR	+5V	
65	LPC_AD0	IN/OUT		
66	LPC_FRAME#	OUT		
67	LPC_AD1	IN/OUT		
68	INT_SERIRQ	IN/OUT		

Pin	Pin Name		Signal Type	Signal Level
69	LPC_AD2	IN/OUT		
70	NC	NC		
71	LPC_AD3	IN/OUT		
72	BIO_PWR_OK	IN		
73	GND	GND	GND	
74	AUD_GND	GND	GND	
75	LPC_CLK_BIO	OUT		
76	LOUT_L	OUT		
77	PME#	OUT		
78	LOUT_R	OUT		
79	GND	GND	GND	
80	GND	GND	GND	

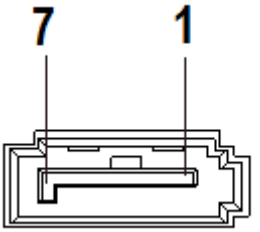
2.4.14LPC Port (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	IN/OUT	+3.3V
2	LAD1	IN/OUT	+3.3V
3	LAD2	IN/OUT	+3.3V
4	LAD3	IN/OUT	+3.3V
5	+V3.3S	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	GND
9	LCLK	OUT	
10	SMB_DATA/ I2C_SDA	IN/OUT	

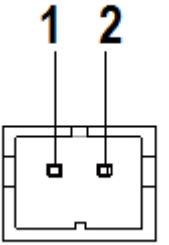
11	SMB_CLK/ I2C_CLK	OUT	
12	SMB_ALERT/ INT_SERIRQ	IN	+3.3V

2.4.15SATA Port (CN20)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.16+5V Output for SATA HDD (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V5S	PWR	+5V

2.4.17M.2 (Key B) Connector (CN26)

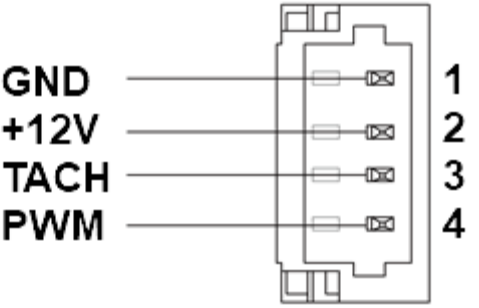
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V3.3S	PWR	+3.3V
3	GND	GND	GND
4	+V3.3S	PWR	+3.3V
5	GND	GND	GND
6	NC	NC	
7	USB2P_10	IN/OUT	
8	W_DISABLE0#	OUT	
9	USB2N_10	IN/OUT	
10	SSD_LED#	IN	
11	GND	GND	GND

20	NC	NC	
21	GND	GND	GND
22	NC	NC	
23	NC	NC	
24	NC	NC	
25	NC	NC	
26	NC	NC	
27	GND	GND	GND
28	NC	NC	
29	PCIE11_RXN	DIFF	
30	NC	NC	
31	PCIE11_RXP	DIFF	
32	NC	NC	
33	GND	GND	GND
34	NC	NC	
35	PCIE11_TXN	DIFF	
36	NC	NC	
37	PCIE11_TXP	DIFF	
38	NC	NC	
39	GND	GND	GND
40	NC	NC	
41	SATA2_RXP	DIFF	

42	NC	NC	
43	SATA2_RXN	DIFF	
44	NC	NC	
45	GND	GND	GND
46	NC	NC	
47	SATA2_TXN	DIFF	
48	NC	NC	
49	SATA2_TXP	DIFF	
50	BUF_PLT_RST#	OUT	
51	GND	GND	GND
52	PCIE_CLK_REQ3#	IN	
53	PCIE3_CLKN	DIFF	
54	PCIE_WAKE#	IN	
55	PCIE3_CLKP	DIFF	
56	NC	NC	
57	GND	GND	GND
58	NC	NC	
59	NC	NC	
60	NC	NC	
61	NC	NC	
62	NC	NC	
63	NC	NC	

64	NC	NC	
65	NC	NC	
66	NC	NC	
67	NC	NC	
68	NC	NC	
69	GND	GND	GND
70	+V3.3S	PWR	+3.3V
71	GND	GND	GND
72	+V3.3S	PWR	+3.3V
73	GND	GND	GND
74	+V3.3S	PWR	+3.3V
75	NC	NC	

2.4.18Smart FAN Connector (CN27)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V3.3S	PWR	+12V
3	TACH	IN	
4	PWM	OUT	

2.4.19M.2 (Key E) Connector (CN30)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V3.3A	PWR	+3.3V
3	USB2P_5	IN/OUT	
4	+V3.3A	PWR	+3.3V
5	USB2N_5	IN/OUT	
6	NC	NC	
7	GND	GND	GND

8	NC	NC	
9	NC	NC	
10	NC	NC	
11	NC	NC	
12	NC	NC	
13	NC	NC	
14	NC	NC	
15	NC	NC	
16	NC	NC	
17	NC	NC	
18	NC	NC	
19	NC	NC	
20	NC	NC	
21	NC	NC	
22	NC	NC	
23	NC	NC	
32	NC	NC	
33	GND	GND	GND
34	NC	NC	
35	PCIE1_TXP	DIFF	
36	NC	NC	
37	PCIE1_TXN	DIFF	

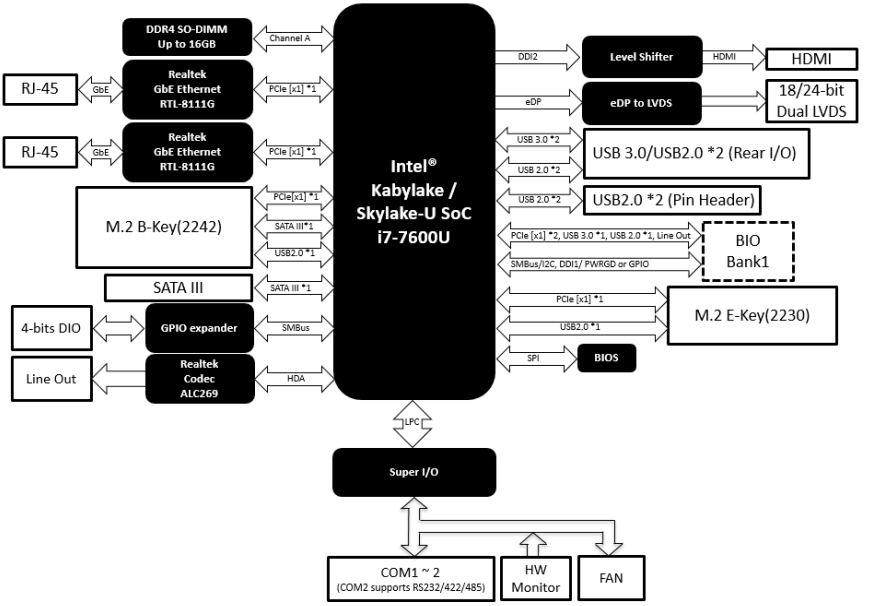
38	NC	NC	
39	GND	GND	GND
40	NC	NC	
41	PCIE1_RXP	DIFF	
42	NC	NC	
43	PCIE1_RXN	DIFF	
44	NC	NC	
45	GND	GND	GND
46	NC	NC	
47	PCIE1_CLKP	DIFF	
48	NC	NC	
49	PCIE1_CLKN	DIFF	
50	NC	NC	
51	GND	GND	GND
52	BUF_PLT_RST#	OUT	
53	PCIE_CLK_REQ1#	IN	
54	W_DISABLE1#	OUT	
55	PCIE_WAKE#	IN	
56	W_DISABLE2#	OUT	
57	GND	GND	GND
58	NC	NC	
59	NC	NC	

60	NC	NC	
61	NC	NC	
62	NC	NC	
63	GND	GND	GND
64	NC	NC	
65	NC	NC	
66	NC	NC	
67	NC	NC	
68	NC	NC	
69	GND	GND	GND
70	NC	NC	
71	NC	NC	
72	+V3.3S	PWR	+3.3V
73	NC	NC	
74	+V3.3S	PWR	+3.3V
75	GND	GND	GND

2.4.20 DDR4 SO-DIMM Slot (DIMM1)

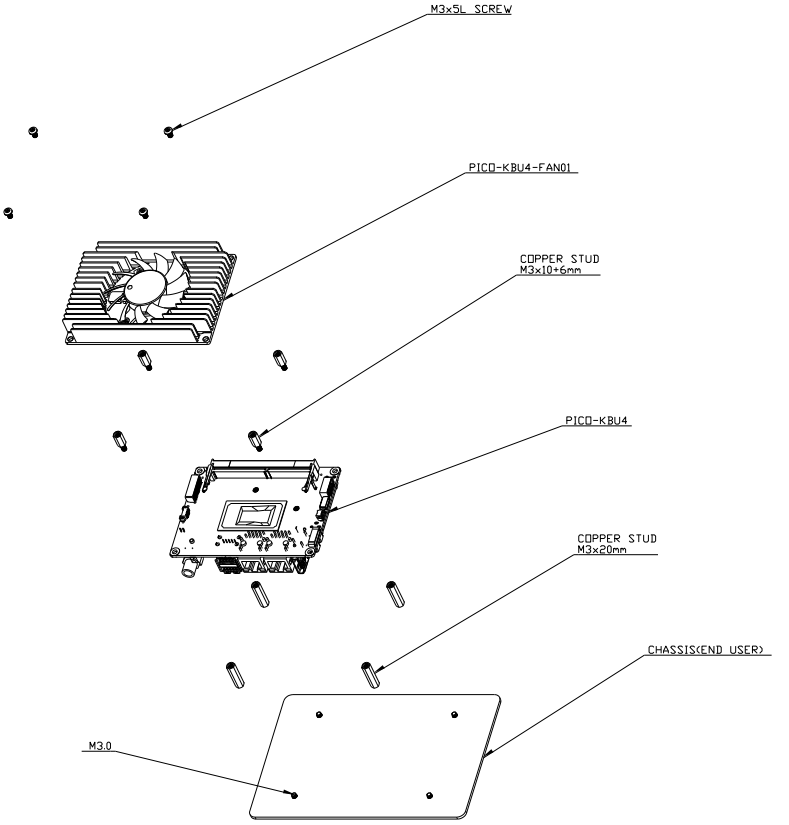
Standard specification

2.5 Function Block

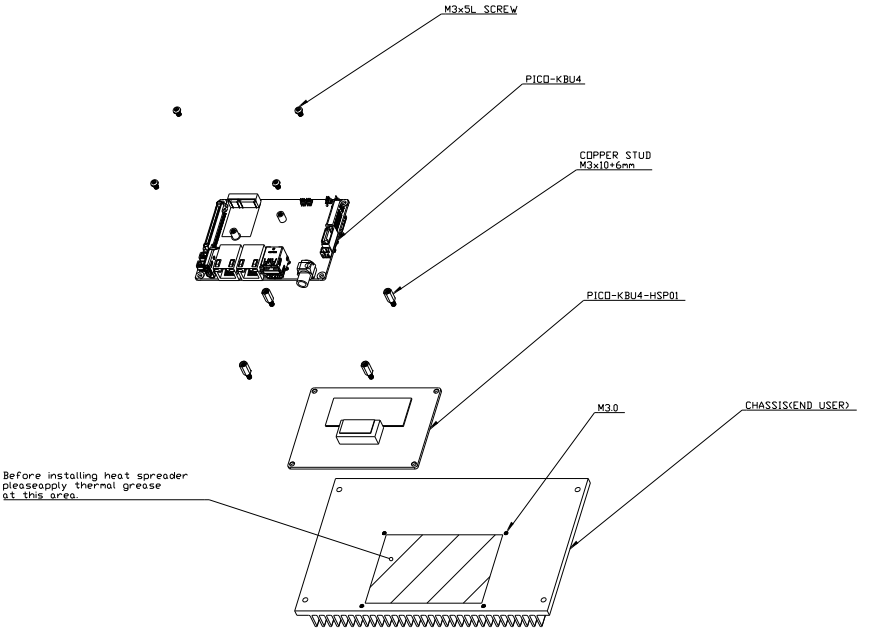


2.6 Assembly Options

Option1 (Part Number：PICO-KBU4-FAN01)



Option2(Part Number：PICO-KBU4-HSK01)



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-APL1 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

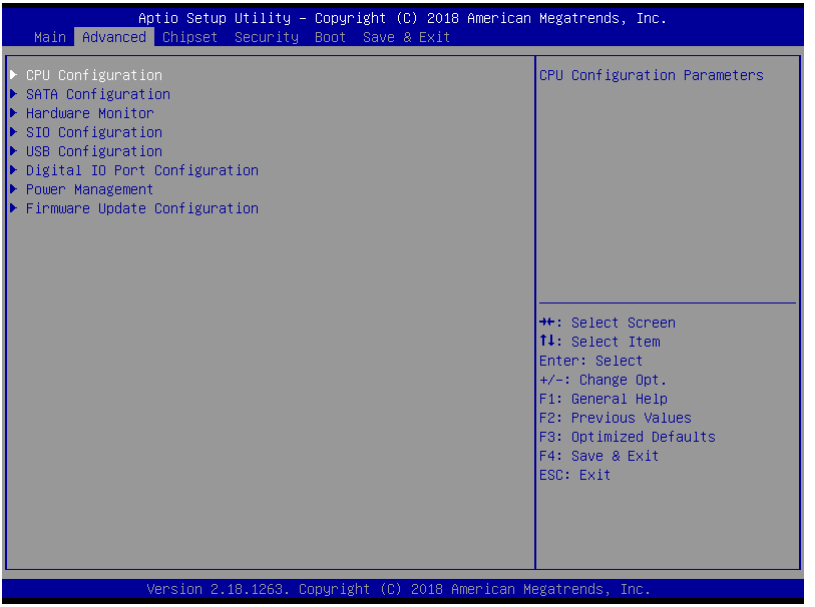
Set setup administrator password.

Save & Exit

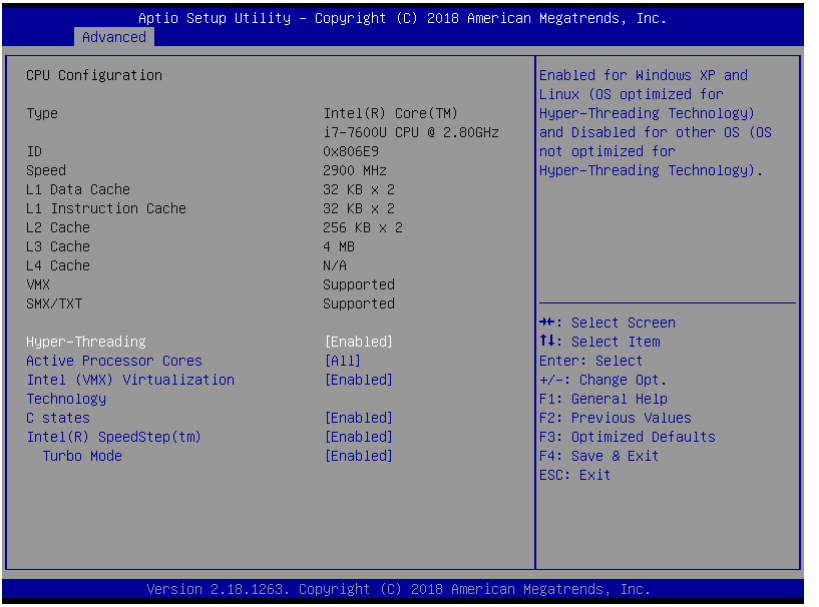
Exit system setup after saving the changes.

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



3.4.1 CPU configuration

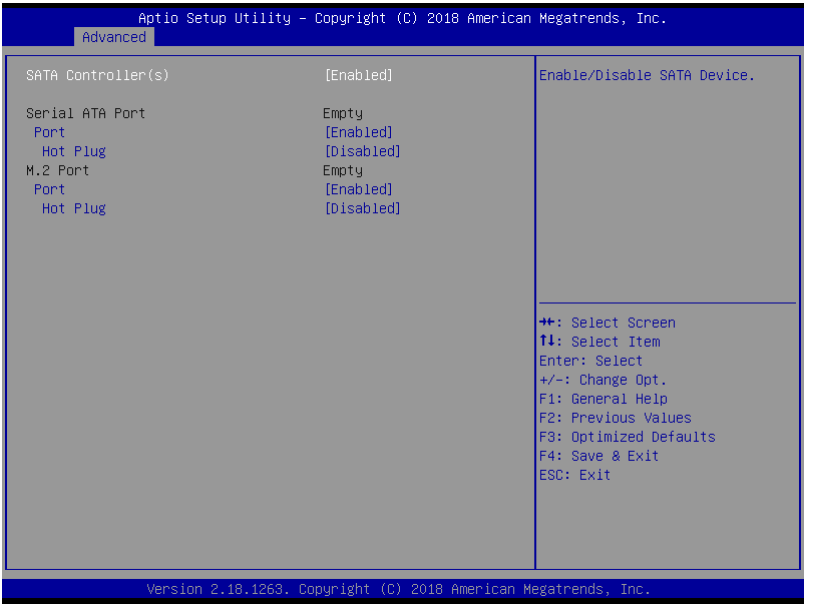


Options summary:

Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable for Linux and Disabled for other OS.		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
CPU C states	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CPU power Management. Allows CPU to go to C states when it's not 100% utilized.		
Intel® SpeedStep™	Disabled	

	Enabled	Optimal Default, Failsafe Default
Allows more then two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor turbo mode. AUTO means enabled, unless max turbo ratio is bigger than 16 – SKL A0 W/A		

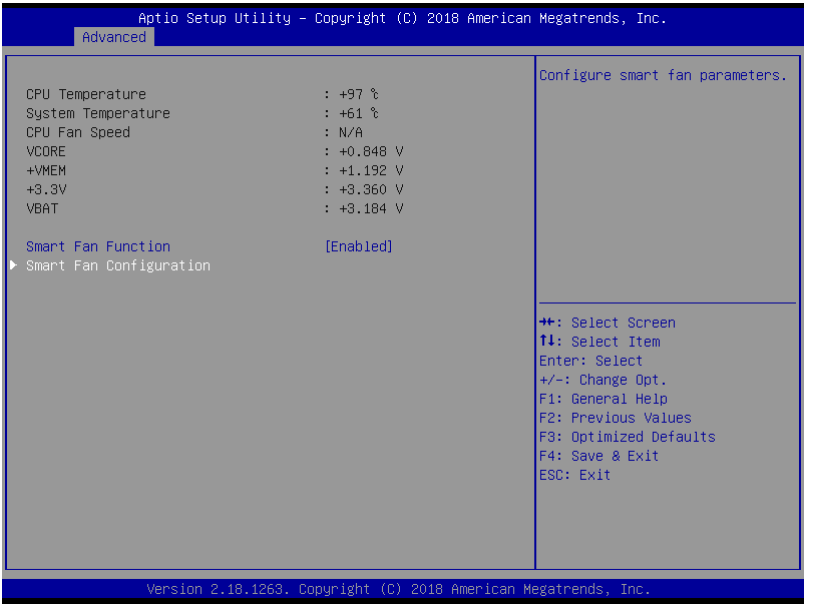
3.4.2 SATA Configuration



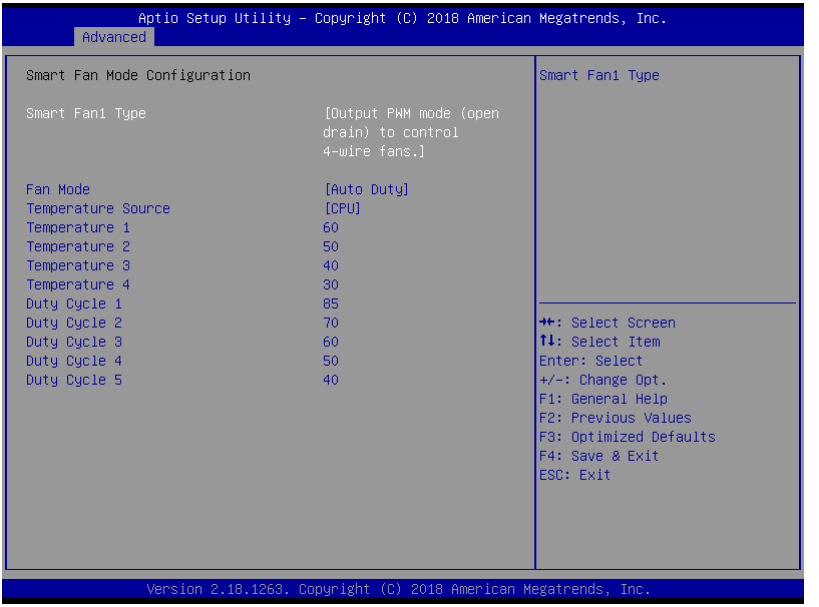
Options summary:

SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable SATA Device.		
Port X	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.3 Hardware Monitor



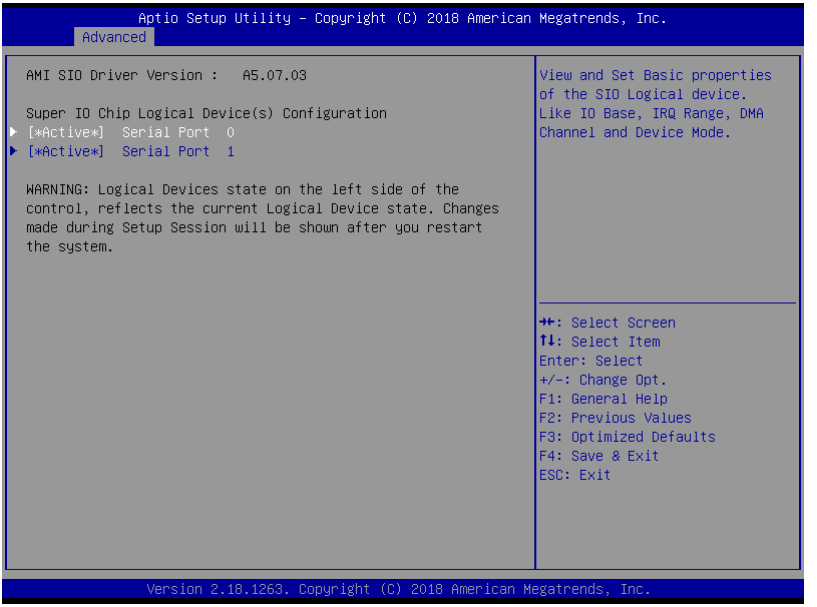
3.4.3.1 CPU Smart Fan Mode Configuration



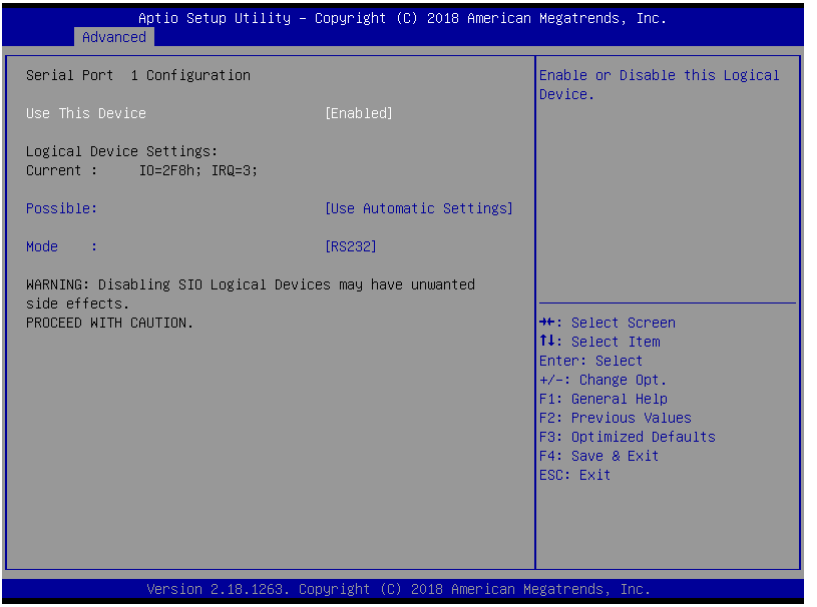
Options summary:

Smart Fan1 Type	Use linear fan application circuit.	
	Output PWM mode (open drain) to control 4-wire fans.	Optimal Default, Failsafe Default
Smart fan type		
Fan Mode	Manual Duty	
	Auto Duty	Optimal Default, Failsafe Default
Smart fan mode		
Temperature Source	CPU	Optimal Default, Failsafe Default
Select the monitored temperature source for this fan.		

3.4.4 SIO Configuration



3.4.4.1 Serial Port Configuration



Options summary:

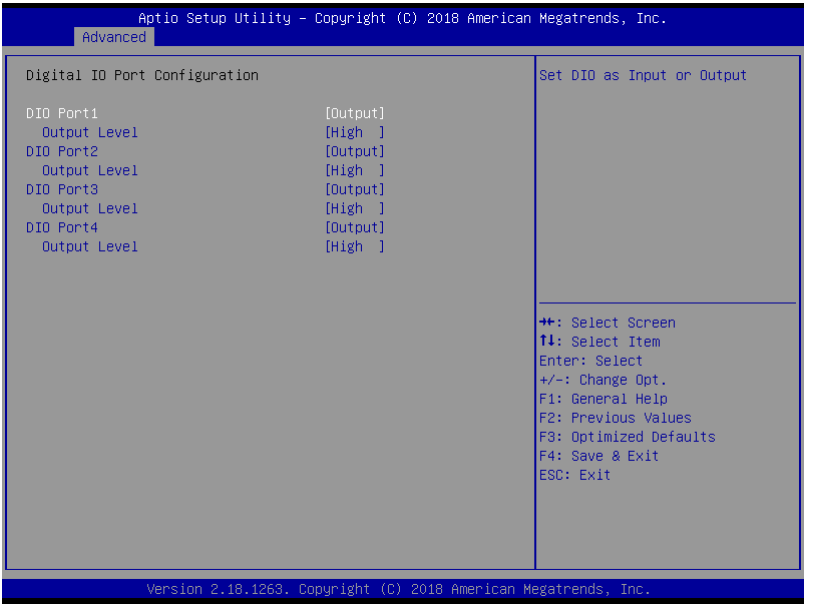
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422;	
	RS485	
UART 232/422/485 selection		

3.4.5 USB Configuration

Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		
USB Port 0/1 function routing	FCH USB port 8/9	Optimal Default, Failsafe Default
	FCH USB port 0/1	

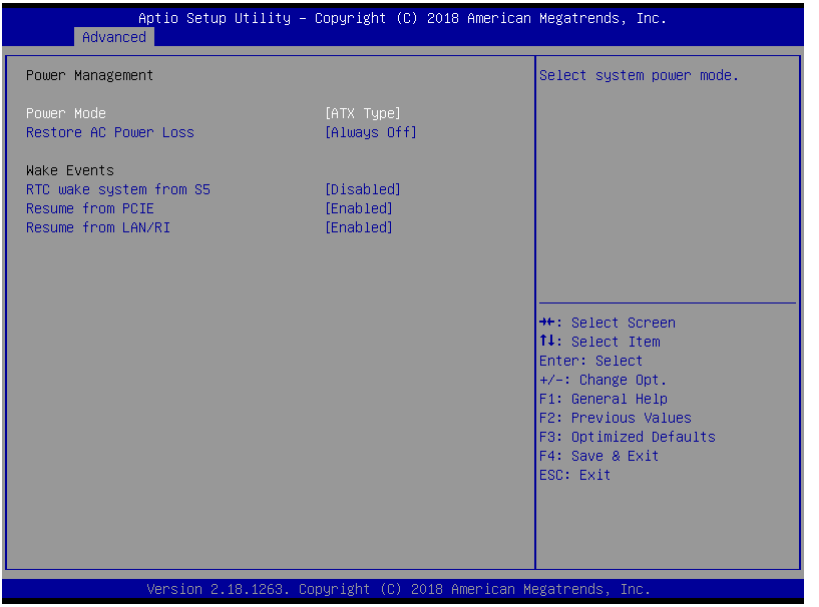
3.4.6 Digital IO Port Configuration



Options summary:

DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

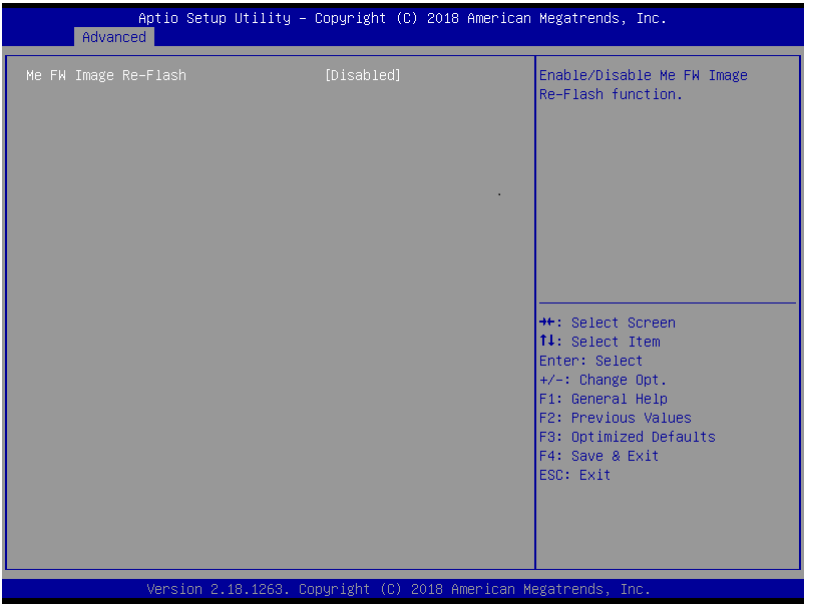
3.4.7 Power management



Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore on Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		
Resume from PCIE	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable resume from PCIE		
Resume form LAN/RI	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable resume from PCIE		

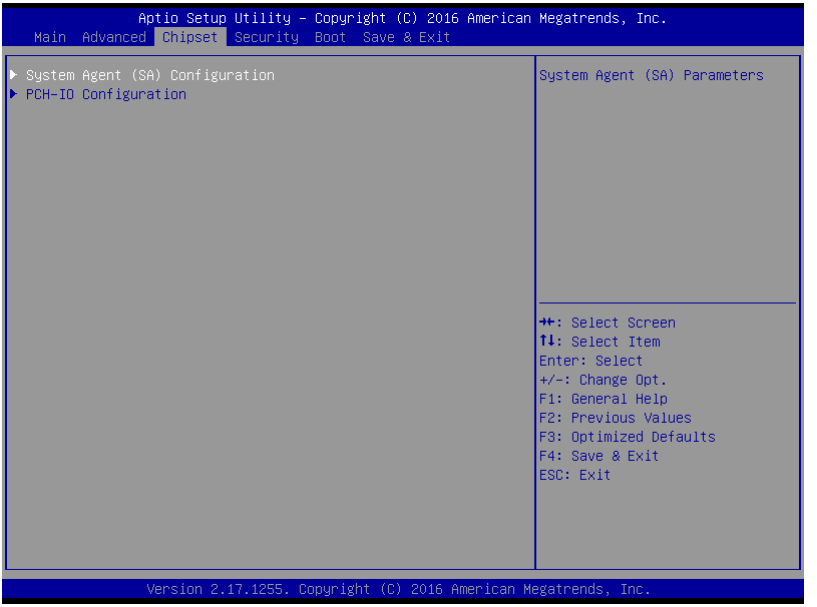
3.4.8 Firmware Update Configuration



Options summary:

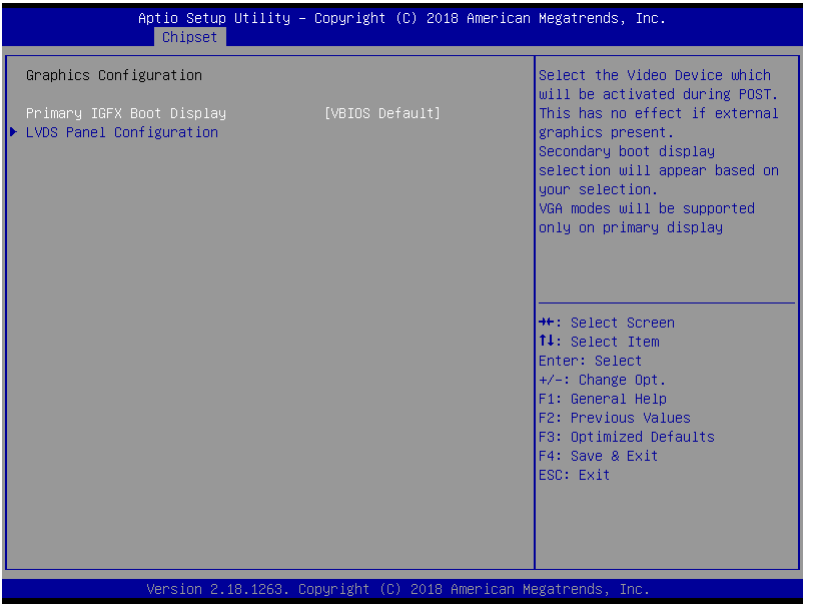
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		

3.5 Setup submenu: Chipset



3.5.1 System Agent (SA) Configuration

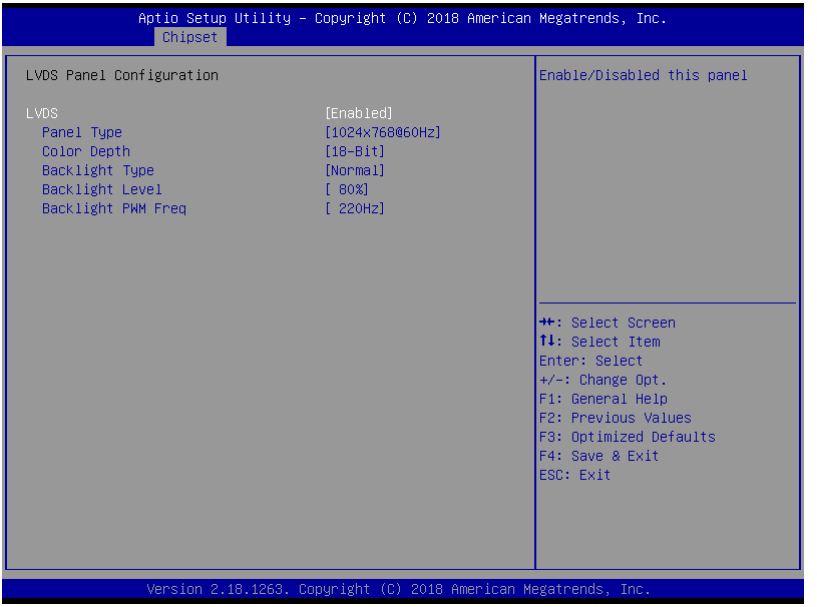
3.5.1.1 Graphics Configuration



Options summary:

Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	HDMI	
	LVDS	
Select the Video Device which will be activated during POST. This has no effect if external graphic present. Secondary boot display selection will appear based on your selection.		

3.5.1.1.1 LVDS Panel Configuration



Options summary:

LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled this panel.		
LVDS Panel Type	640x480,18bit,60Hz	Optimal Default, Failsafe Default
	800x480,18bit,60Hz	
	800x600,18bit,60Hz	
	1024x600,18bit,60Hz	
	1024x768,18bit,60Hz	
	1024x768,24bit,60Hz	
	1280x768,24bit,60Hz	
	1280x1024,48bit,60Hz	
	1366x768,24bit,60Hz	
	1440x900,48bit,60Hz	
	1600x1200,48bit,60Hz	
	1920x1080,48bit,60Hz	
	1920x1200,48bit,60Hz	

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

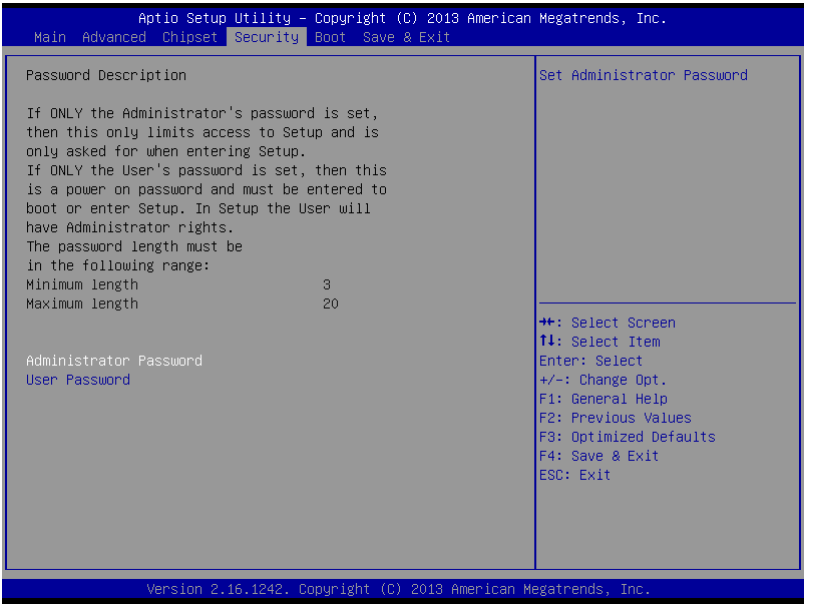
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	Optimal Default, Failsafe Default
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.5.2 PCH-IO Configuration

Options summary:

HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise.		
PCI Express Root Port 1	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable PCI Express Root Port 1		
PCIe Lane* Gen Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Select PCI Express port speed.		

3.6 Setup submenu: Security



Change User/Supervisor Password

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

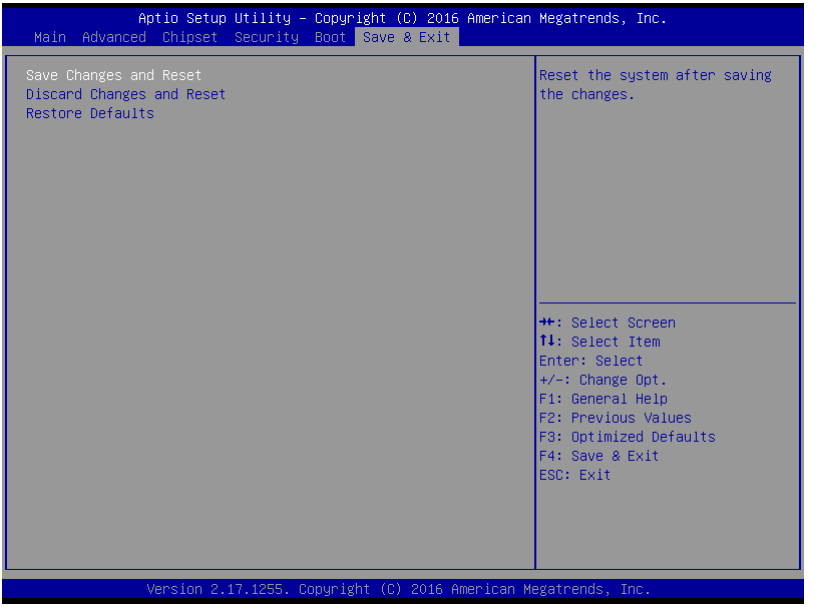
3.7 Setup submenu: Boot

Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable showing boot logo.		
Launch PXE OpROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROm		

3.7.1 BBS Priorities

3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the PICO-KBU4 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/pico-itx-boards-pico-kbu4#downloads

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Open the **STEP1 - CHIPSET** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **STEP2 - Graphic** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 3 – Install LAN Driver

1. Open the **STEP3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Driver will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - Audio** folder and select your OS
2. Open the Setup.exe file
3. Follow the instructions
4. Driver will be installed automatically

Step 5 – Install Serial Port Driver (Optional)

1. Open the **STEP5 – Serial Port Driver** folder and select your OS
2. Open the .exe file
3. Follow the instructions
4. Driver will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0x2E	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s *Pulse width is must longer then 16ms.*
Signal Polarity	0x05	2	0	0: low active 1: high active *Must set this bit to 0*
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse *Must set this bit to 1*
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg         0x00   // Device configuration register
     #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
     #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
     #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
     #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
     #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
     #define   PolarityVal    0x00     // Low active for WDTRST#
     #define   UnitBit        0x03     // Unit for timer (Bit3)
     #define   ModeBit        0x04     // WDTRST# mode (Bit4)
     #define   ModeVal        0x01     // 0:level 1: pulse
     #define   EnableBit      0x05     // WDT timer enable (Bit5)
     #define   EnableVal      0x01     // 1: enable
     #define   StatusBit      0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*************************************************************************

*************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        EnterSIOconfig();
        SetWDT();
        AaeonWDTConfig(Counter, Unit);
        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
        ExitSIOconfig();
}
*************************************************************************
```

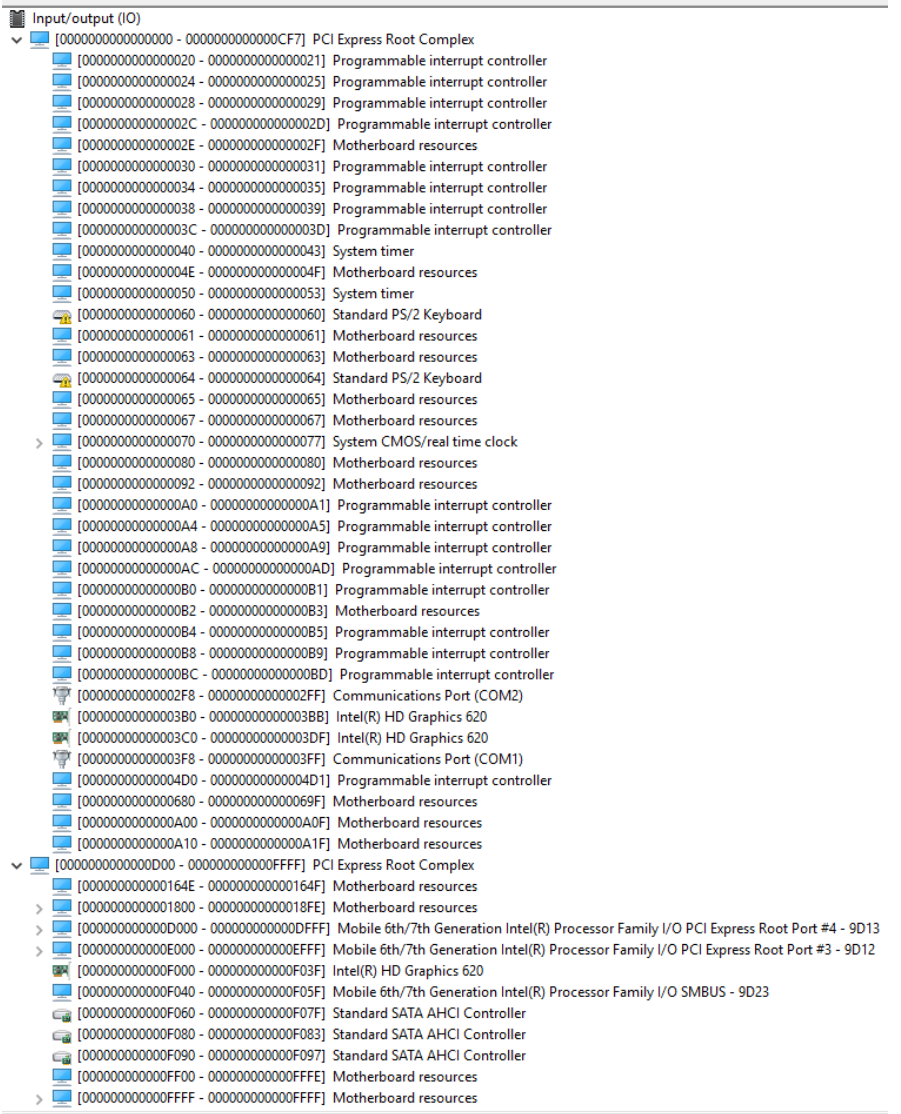
```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    EnterSIOconfig ()
        IOWriteByte (IoConfAddr,0x87);
        IOWriteByte (IoConfAddr,0x87);
}

VOID    ExitSIOconfig ()
        IOWriteByte (IoConfAddr,0xAA);
}

VOID    SetWDT ()
        IOWriteByte (IoConfAddr,0x2B);
        IOWriteByte(IoConfAddr+1, (IOReadByte(IoConfAddr+1)&0xFC));
}

// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ()
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit)
        // Disable WDT counting
        WDTEnableDisable(0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value)
        If (Value == 1)
            WDTSetBit(TimerReg, EnableBit, 1);
        else
            WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit)
        // Watchdog Timer counter setting
        WDTWriteByte(CounterReg, Counter);
       // WDT counting unit setting
```

```
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
         // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
VOID   WDTWriteByte(byte Register, byte Value){
        IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
        return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
        byte TmpValue;

        TmpValue = WDTReadByte(Register);
        TmpValue &= ~(1 << Bit);
        TmpValue |= Val << Bit;
        WDTWriteByte(Register, TmpValue);
}

*****************************************************************************
```

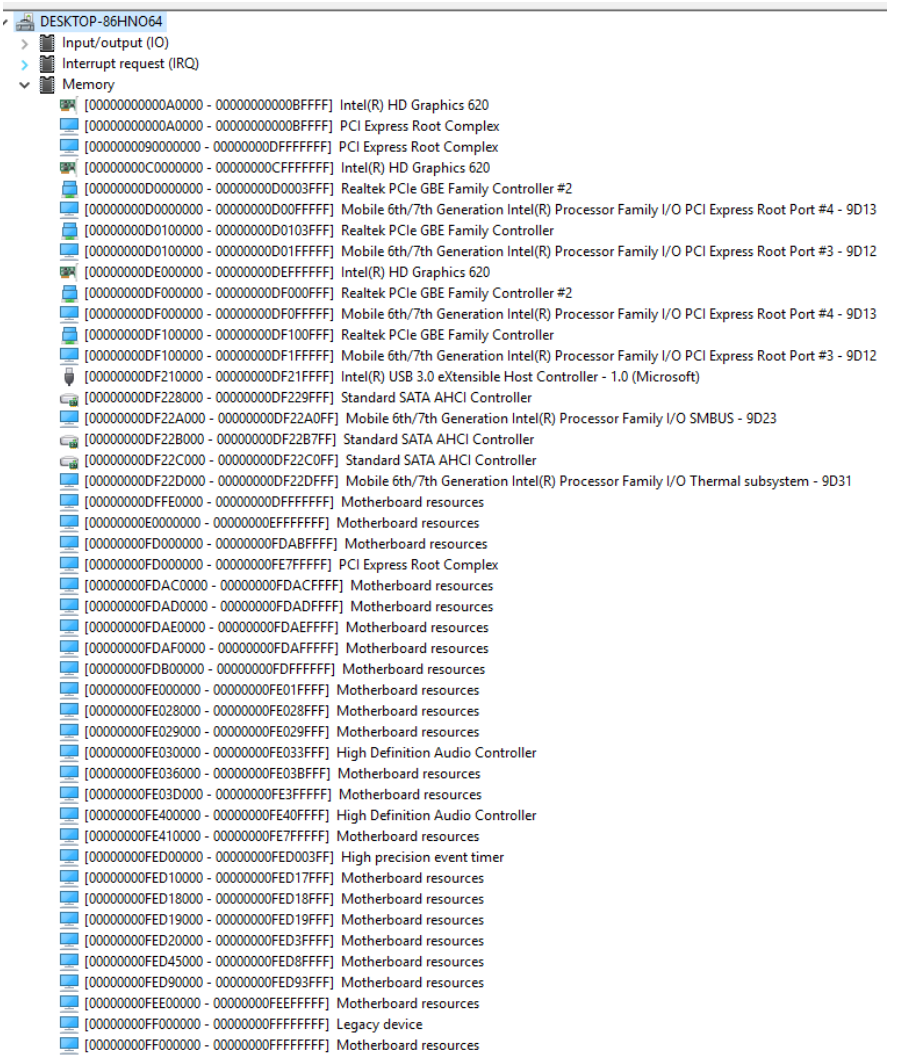
Appendix B

I/O Information

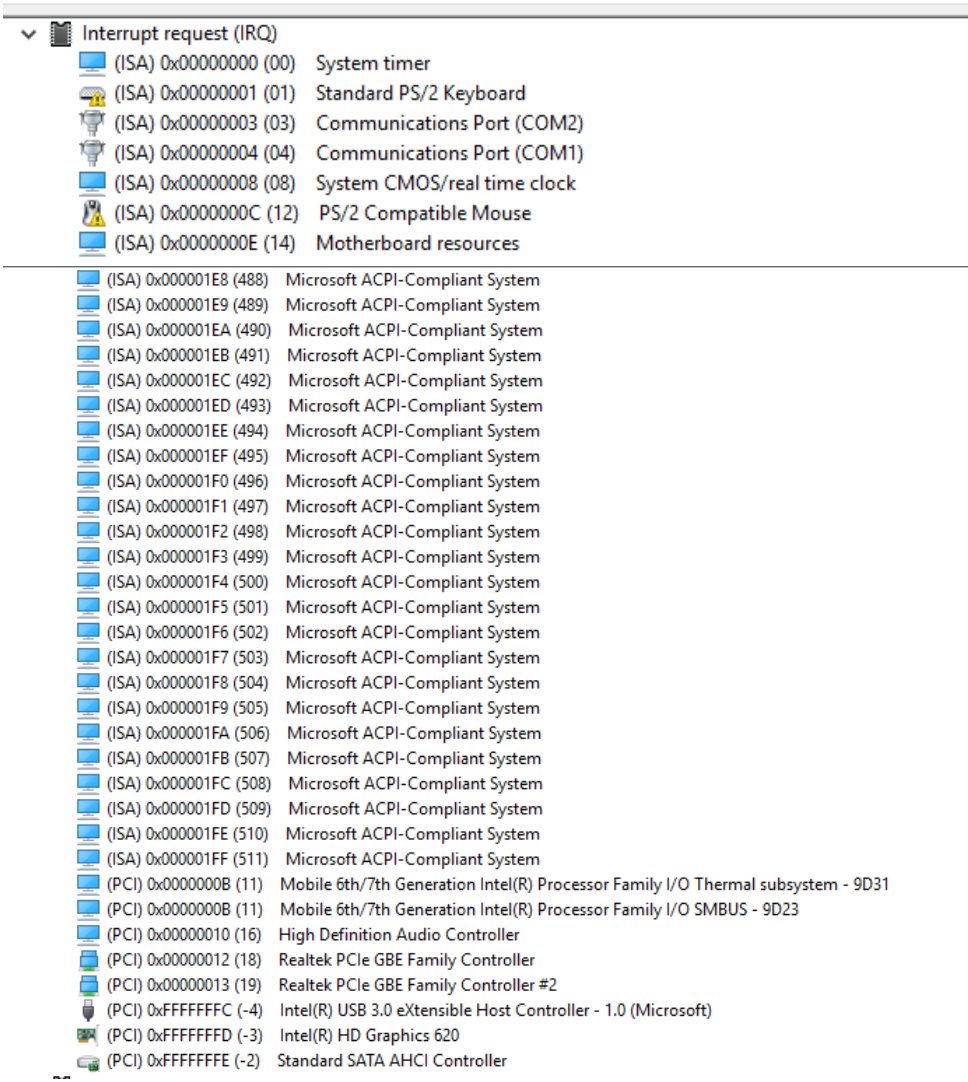
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	Battery	Molex	51021-0200	Battery Cable	175011301C
CN2	HDMI	Molex	88768-9900	NA	NA
CN4	LVDS Port Inverter / Backlight Connector	JST	SHR-05V-S-B	LVDS Inverter Cable	1709050203
CN5	LVDS Port	JCTC	11002H00-2x15P	LVDS Cable	1704300030
CN6	LAN Connector	Molex	44915-0001	NA	NA
CN7	LAN Connector	Molex	44915-0001	NA	NA
CN9	Digital IO Port	Molex	78120-0607	NA	NA
CN10	USB 2.0 Connector	JCTC	11002H00-2x5P	USB Cable	170010010D
CN11	USB 3.0 Connector	Wurth Electronics	710-692112030100	NA	NA
CN14	External +12V Input	Molex	19211-0003	Power Cable	170204010R
CN15	Front Panel Connector	JCTC	11002H00-2x5P	Front Panel Cable	1709100108
CN16	COM Port 1/2 & line out Connector	JCTC	11002H00-2x10P	COM Port Cable	1701200101
CN17	BIO Connector	Hirose	FX18-80S-0.8SV20	NA	NA
CN19	LPC Port	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN20	SATA Port	Molex	887505318	NA	NA

CN21	+5V Output for SATA HDD	JST	PHR-2	SATA power Cable	1702150155
CN23	DC Jack(Optional)	HUANG JI	5525C257-3T00-R1-7.5	Power Cable	1702041004
CN27	FAN Connector	Molex	51021-0400	NA	NA

Appendix D

DIO

D.1 DIO

The F75111 provides one serial access interface, I2C Bus, to read/write internal registers. The address of Serial Bus is 0x6E (0110_1110)

The related register for configuring DIO is list as follows:

Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	Reserved	R/W	VSB3V	
5	EN_WDT10	R/W	VSB3V	Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable.
4	Reserved	R/W	VSB3V	
3	Reserved	R/W	VSB3V	
2	Reserved	R/W	VSB3V	
1	SMART_POWR_MANAGEMENT	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

GPIO2x Output Control Register – Index 20h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_OCTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function(default).
6	GP26_OCTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function(default).
5	GP25_OCTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function(default).
4	GP24_OCTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function(default).

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GPIO2x Output Data Register – Index 21h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_ODATA	R/W	VSB3V	GPIO 27 output data.
6	GP26_ODATA	R/W	VSB3V	GPIO 26 output data.
5	GP25_ODATA	R/W	VSB3V	GPIO 25 output data.
4	GP24_ODATA	R/W	VSB3V	GPIO 24 output data.

GPIO2x Input Status Register – Index 22h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7	GP27_PSTS	RO	VSB3V	Read the GPIO27 data on the pin.
6	GP26_PSTS	RO	VSB3V	Read the GPIO26 data on the pin.
5	GP25_PSTS	RO	VSB3V	Read the GPIO25 data on the pin.
4	GP24_PSTS	RO	VSB3V	Read the GPIO24 data on the pin.

The following is a sample code for 8 input

```
.MODEL SMALL
.CODE
begin:
mov cl,01h
mov al,80h
call CT_I2CWriteByte
call Delay5ms

        mov al,00h
mov cl,20h
call CT_I2CWriteByte

mov cl,22h
call CT_I2CReadByte

;Input : CL - register index
```

```
; CH - device ID
;Output : AL - Value read
Ct_I2CReadByte Proc Near
mov ch,06eh
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
inc ch ; Set the slave address and
mov al, ch ; prepare for a READ command
out dx, al
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to read
out dx, al
mov dx, F040h + 06h

xor al, al ; Clear old data
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
out dx, al

mov dx, F040h + 00h ; Host Control Reegister
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready
mov dx, F040h + 06h
```

```
in al, dx

ret
Ct_I2CReadByte Endp
;Input : CL - register index
; CH - device ID
; AL - Value to write
;Output: none

Ct_I2CWriteByte Proc Near
mov ch,06eh

xchg ah, al
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
mov al, ch ; Set the slave address and
out dx, al ; prepare for a WRITE command
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to write
out dx, al
mov dx, F040h + 06h
mov al, ah
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
```

```
out dx, al
mov dx, F040h + 00h ; Host Control Register
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready ;R14
ret
Ct_I2CWriteByte Endp
; Wait until the busy bit clears, indicating that the SMBUS
; activity has concluded.
CT_Chk_SMBus_Ready Proc Near
mov dx, F040h + 01h ; Host Status Register
Check_I2C_ByteRead_ForBusy:
in al, dx
test al, 08h
jnz Check_I2C_ByteRead_ForBusy
Check_I2C_ByteRead_ForStatus:
in al, dx
test al, 07h ; HSTS[2:0]=All clearable status bits
jz Check_I2C_ByteRead_ForStatus
ret
CT_Chk_SMBus_Ready Endp
END begin
```