Lab 6 Report

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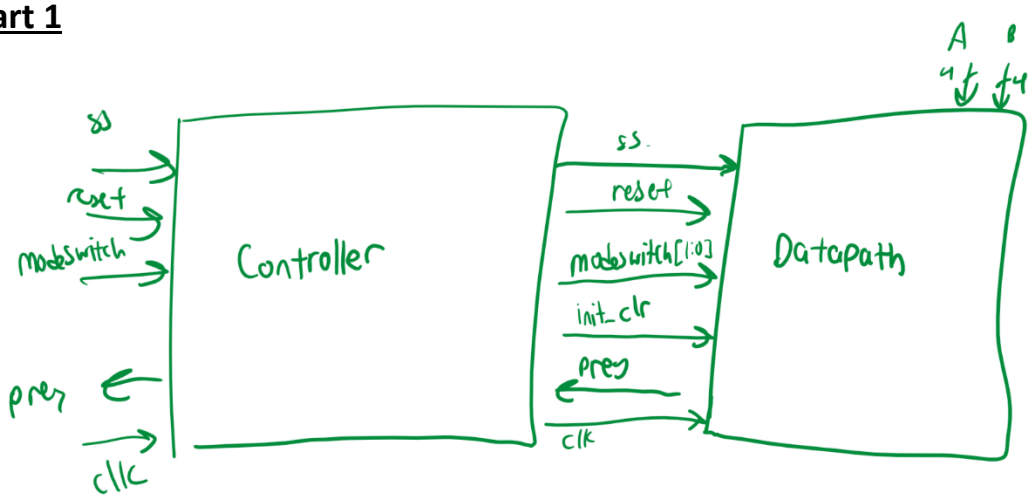
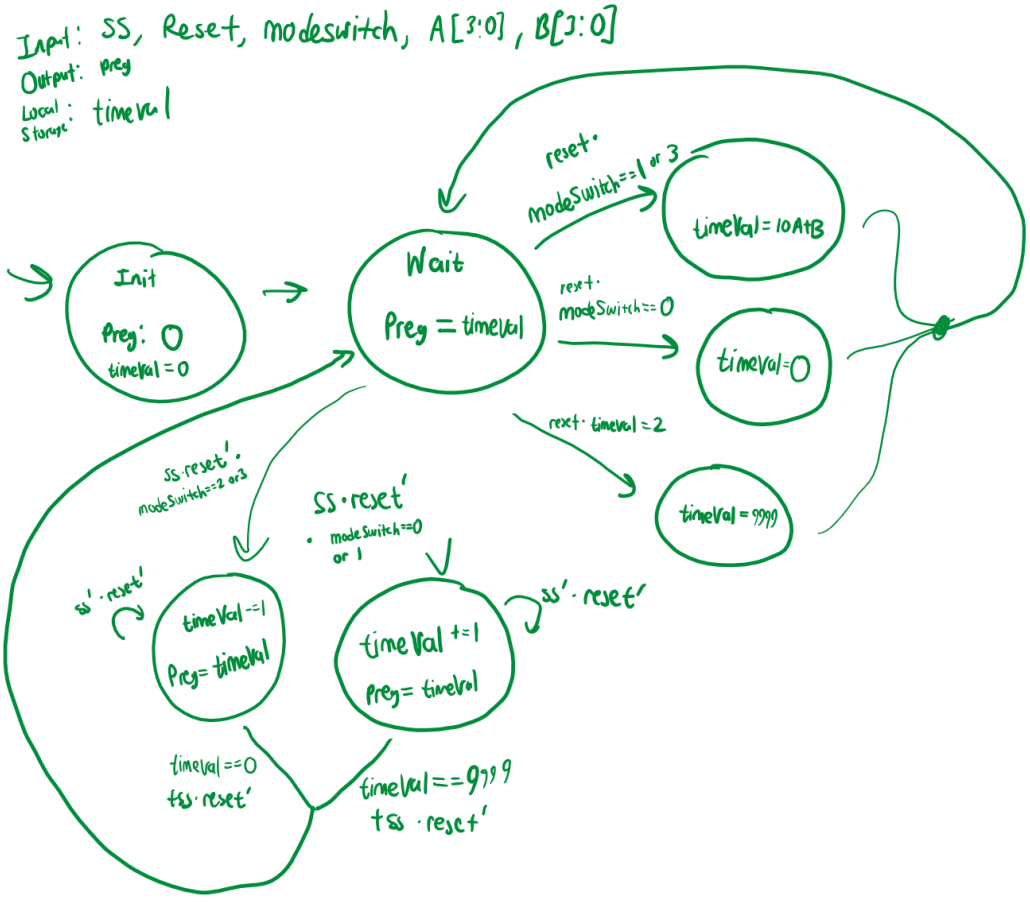
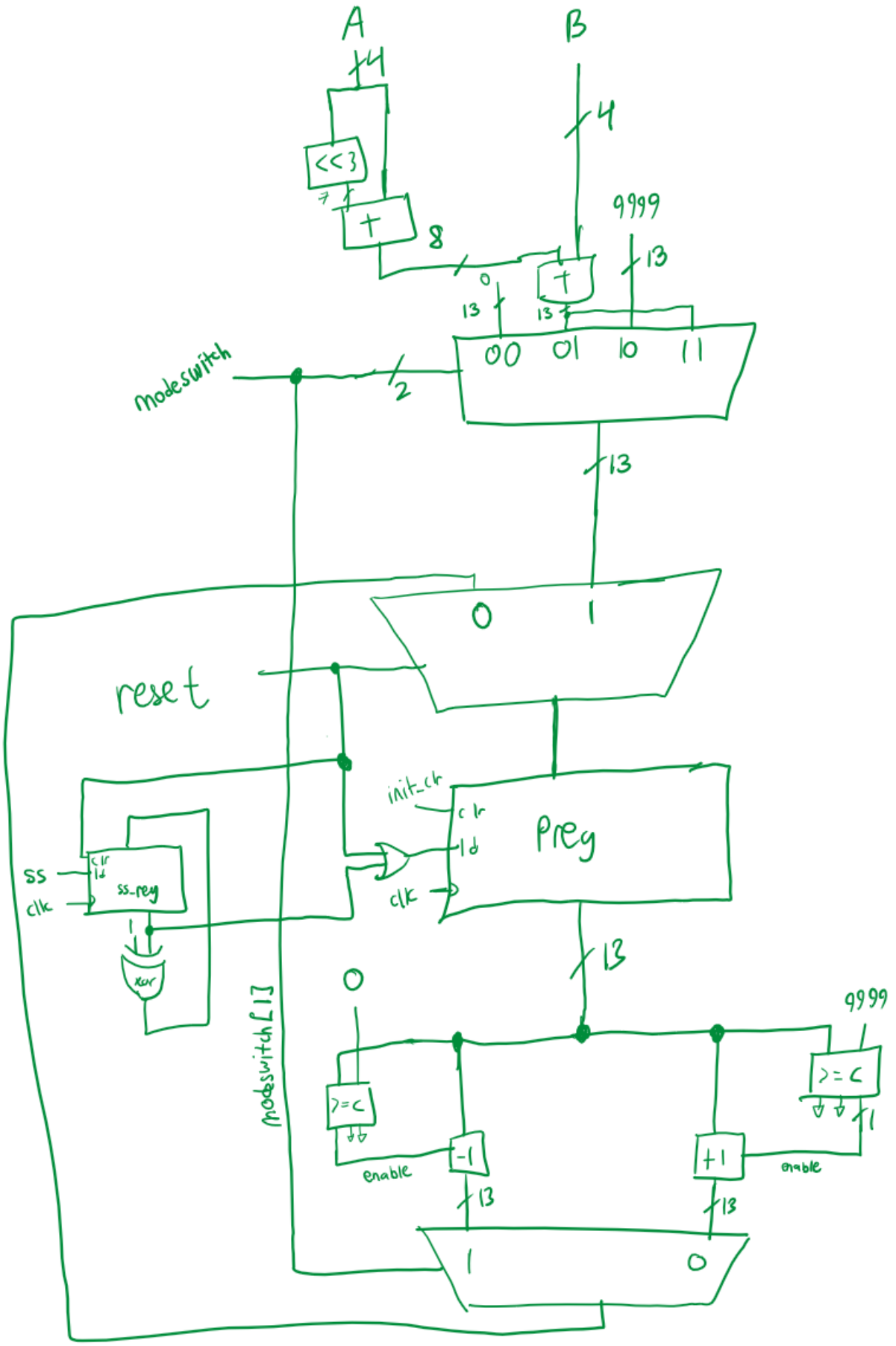
Section: MW 11 – 12:30

Part 1






A
B
4
4
<<3
+
8
9999
13
+
0
13
13
00
01
10
11
modeswitch
2
13
0
1
reset
init_clr
clr
ld
Preg
clk
ss
clk
clr
ld
ss_reg
1
xor
13
modeswitch[1]
0
9999
>=C
>=C
1
-1
+1
enable
enable
13
13
1
0


init_ clr = 1
Init
Preg: 0
timeVal = 0
init_clr=0
Wait
Preg = timeVal
reset·
modeSwitch==1 or 3
init_clr=0
timeVal = 10AtB
reset·
modeSwitch==0
init_clr=0
timeVal=0
reset· timeVal = 2
init_clr=0
timeVal = 9999
ss·reset'·
modeSwitch=2 or3
ss·reset'
· modeSwitch==0
or 1
ss'·reset'
timeVal -=1
Preg= timeVal
init_clr
=0
timeVal +=1
Preg= timeVal
ss'·reset'
init_clr =0
timeVal==0
tss·reset'
timeVal==9999
tss·reset'

Part 2

Verilog:

```
`timescale 1ns / 1ps

module Modes(
    input clk,
    input reset,
    input ss,
    input [1:0] modeSwitch,
    input [3:0] A, B,
    output wire [3:0] an,
    output wire [0:0] dp,
    output wire [6:0] sseg

);

    reg [13:0] timeVal = 0;
    reg [1:0] state = 0;
    reg [1:0] next_state = 0;
    reg [1:0] modeState = 0;

    wire [6:0] in0, in1, in2, in3;

    hexto7segment c1 (.x(timeVal/1000 % 10), .r(in3));
    hexto7segment c2 (.x(timeVal/100 % 10), .r(in2));
    hexto7segment c3 (.x(timeVal/10 % 10), .r(in1));
    hexto7segment c4 (.x(timeVal % 10), .r(in0));

    wire slow_clk1;
    wire slow_clk2;

    reg [3:0] Aval = 0;
    reg [3:0] Bval = 0;

    clkdiv cl1(clk, reset, slow_clk1);
    clkdiv2 cl2(clk, reset, slow_clk2);

    time_mux_state_machine c6(
        .clk (slow_clk1),
        .reset (reset),
        .in0 (in0),
        .in1 (in1),
```

```
    .in2 (in2),
    .in3 (in3),
    .an (an),
    .sseg (sseg),
    .dp(dp));

always @(posedge slow_clk2 or posedge reset) begin
    if (reset) begin
        state <= 2'b00;
        next_state <= 2'b00;
        if (modeSwitch == 2'b00)
            timeVal <= 13'b0;
        else if (modeSwitch == 2'b01 || modeSwitch == 2'b11) begin
            if (8*A[3] + 4*A[2] + 2*A[1] + A[0] <= 9)
                Aval = 8*A[3] + 4*A[2] + 2*A[1] + A[0];
            if (8*B[3] + 4*B[2] + 2*B[1] + B[0] <= 9)
                Bval = 8*B[3] + 4*B[2] + 2*B[1] + B[0];
            timeVal <= 10*(Aval) + Bval;
        end
        else if (modeSwitch == 2'b10)
            timeVal <= 9999;
    end
    else begin
        case (state)
            2'b00   : begin
                if (modeSwitch == 2'b00 || modeSwitch == 2'b01) begin
                if (ss * (timeVal < 9999))
                    next_state = 2'b01;
                else
                    next_state = 2'b00;
                end

                else if (modeSwitch == 2'b10 || modeSwitch == 2'b11) begin
                if (ss * (timeVal > 0))
                    next_state = 2'b01;
                else
                    next_state = 2'b00;
                end

                end
            2'b01   : begin
                if (modeSwitch == 2'b00 || modeSwitch == 2'b01) begin
                timeVal = timeVal + 1;
                if (!ss * (timeVal < 9999))
```

```
                next_state = 2'b01;
            else
                next_state = 2'b00;
            end

            else if (modeSwitch == 2'b10 || modeSwitch == 2'b11) begin
            timeVal = timeVal - 1;
            if (!ss * (timeVal > 0))
                next_state = 2'b01;
            else
                next_state = 2'b00;
            end

            end

          default : begin
                next_state = 2'b00 ;
                state = 2'b00;
            end
        endcase
        state <= next_state;
      end
    end

endmodule
```

Constraints:

```
set_property PACKAGE_PIN W5 [get_ports clk]
        set_property IOSTANDARD LVCMOS33 [get_ports clk]
        create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

#7 segment display
set_property PACKAGE_PIN W7 [get_ports {sseg[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[0]}]
set_property PACKAGE_PIN W6 [get_ports {sseg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[1]}]
set_property PACKAGE_PIN U8 [get_ports {sseg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[2]}]
set_property PACKAGE_PIN V8 [get_ports {sseg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[3]}]
set_property PACKAGE_PIN U5 [get_ports {sseg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[4]}]
set_property PACKAGE_PIN V5 [get_ports {sseg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[5]}]
set_property PACKAGE_PIN U7 [get_ports {sseg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sseg[6]}]

set_property PACKAGE_PIN U2 [get_ports {an[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]

set_property PACKAGE_PIN V7 [get_ports dp]
        set_property IOSTANDARD LVCMOS33 [get_ports dp]



#Buttons
set_property PACKAGE_PIN U18 [get_ports reset]
        set_property IOSTANDARD LVCMOS33 [get_ports reset]
set_property PACKAGE_PIN T18 [get_ports ss]
        set_property IOSTANDARD LVCMOS33 [get_ports ss]

#Mode
set_property PACKAGE_PIN R2 [get_ports {modeSwitch[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {modeSwitch[1]}]
set_property PACKAGE_PIN T1 [get_ports {modeSwitch[0]}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {modeSwitch[0]}]

## Switches
## Connects pin V17 (SW0 on the board) to input a in our gate module
set_property PACKAGE_PIN V17 [get_ports {B[0]}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
## Connects pin V16 (SW1 on the board) to input b in our gate module
set_property PACKAGE_PIN V16 [get_ports {B[1]}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property PACKAGE_PIN W16 [get_ports {B[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property PACKAGE_PIN W17 [get_ports {B[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]

set_property PACKAGE_PIN W15 [get_ports {A[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property PACKAGE_PIN V15 [get_ports {A[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W14 [get_ports {A[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W13 [get_ports {A[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
```