High Performance and Low Power ONOFIC Approach for VLSI CMOS Circuits Design

A

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Submitted

By

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CERTIFICATE

This is to certify that the project work entitled "**High Performance and Low Power ONOFIC Approach for VLSI CMOS Circuits Design** " done by **A. Akshay Raj Singh** bearing Reg.No. 17BD1A0463, student of **Electronics and Communication Engineering Department**, is a record of bonafide work carried out by him. This project is done as a partial fulfillment of obtaining **Bachelor of Technology** Degree to be awarded by **JNTUH, Hyderabad.**

The matter embodied in this project report has not been submitted to any other university for the award of any other degree.

Head of the Department

Prof. Mr.Anthony

Contents

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Abstract

Improving high performance with reduced power consumption and chip area are the main constraint for designing VLSI CMOS circuits. In this paper, high performance and low power ONOFIC approach for VLSI CMOS circuits have been implemented. The proposed method reduces the power dissipation and improves the speed of a VLSI circuit design. Mostly the concentrated part in deep sub micron regime is the power dissipation. Many techniques have been proposed for reducing leakage current in deep sub micron but with some limitations they are not suitable for actual requirements. The proposed On/Off Logic (ONOFIC) serves the needs for deep sub micron with its reduced power dissipation and increased performance in VLSI circuits. Thus, the proposed ONOFIC approach results have been compared with LECTOR technique and observed that the proposed technique shows the improved performance and reduced power dissipation. The tool used for implementing the design is "CADENCE design tools".

CHAPTER-1

1.1 INTRODUCTION.

CADENCE design tool:

The Cadence tool kit consist of several programs for different applications such as schematic drawing, layout, verification, and simulation. These applications can be used on various computer platforms. The open architecture also allows for integration of tools from other vendors or of own design. The integration of all this tools is done by a program called Design Framework II (DFW). The DFW-application is the cornerstone in the Cadence environment. It provides a common user interface and a common data base to the tools used. This makes it possible to switch between different applications without having to convert the data base.

- Layer definitions: Conductors, contacts, transistors ...
- Design rules: minimum size, distance to objects ...
- Display: Colours and patterns to use on the screen.
- Electrical properties: resistance, capacitance .

The technology files are usually supplied by the silicon vendor, that is to fabricate the design, along with some libraries of standard cells and IO pads that can be used by the designer. Such a collection is called a Design Kit.

The design flow:

CREATE THE DESIGN ⇨ ANALYZE ⇨ CREATE LAYOUT ⇨ VERIFICATION

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transitor symbols, and maybe other components such as resistors and capacitances, and wires connecting them. From the schematic view the symbol view is created (almost

automatically) so that the cell can be used on a higher level in the hierarchy.

The step Analyze the design includes functional verification (simulation) of the design on a schematic level.

The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colours. All the cells and blocks used have the size they will have on the final chip.

The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.
When a command is performed, from a form or a menu, the system is executing functions written in the SKILL language. SKILL is developed by Cadence and is based on Lisp. The Cadence tools are using SKILL for internal communication and for the tool-design communication. SKILL is also accessible for the designers. Commands can be written in the CIWwindow or placed in command files for execution. it can be used for simple tasks like executing a command or building more complex functions to perform various tasks.

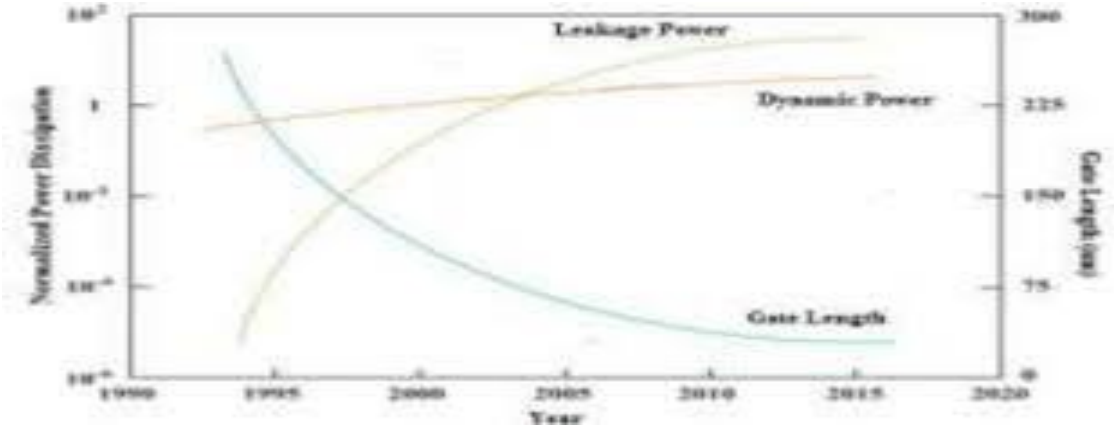


Fig. 1. Trends of Recent Power Dissipation

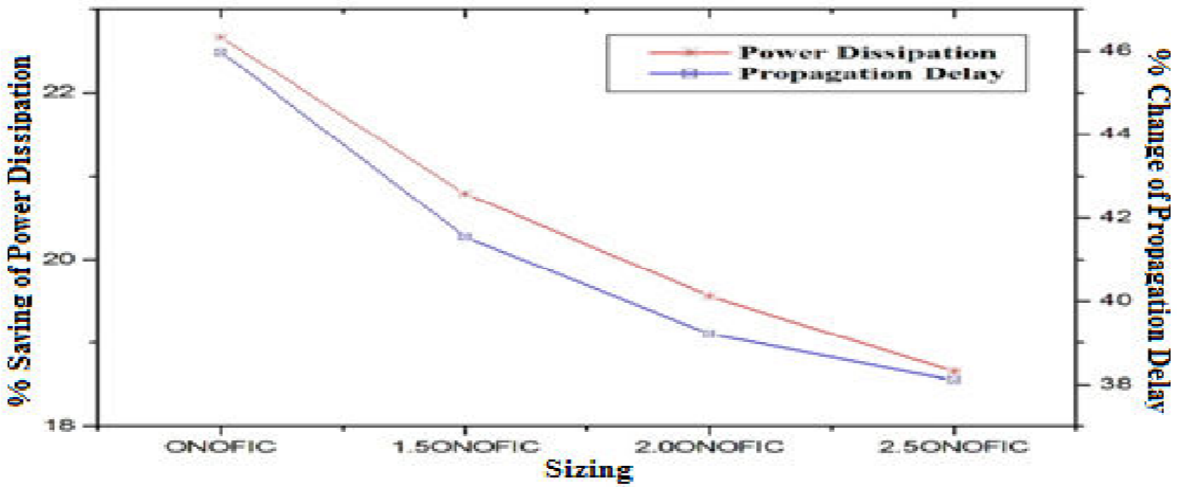


Fig. 2 . Leakage Reduction ONOFIC Approach for deep submicron VLSI circuit design

The design of low power circuits mainly focus on performance, power dissipation and chip area. The concentrated part in VLSI CMOS circuits is deep sub micron regime. The constraint in deep sub micron is to reduce the device dimensions leads to decrease in chip area. Supply voltage plays an important role in electronic devices to control the power consumption. By reducing supply voltage and threshold voltage we can retains the performance. Introducing new lower level technologies in integrated circuits leads to increase in power dissipation. As the technology scaling down the leakage power dissipation goes up. Several technologies have been implemented to reducing the leakage power dissipation.As the technology scaling down the leakage power dissipation goes up. Several technologies have been implemented to reducing the leakage power dissipation here “onofic” means On Off logic .

A perfect designer concentrates mostly for efficient techniques for leakage current reduction in deep sub micron regime. For

designing high performance and low power CMOS circuits a new method is implemented in this paper which is On/Off logic (ONOFIC) approach.

An extended ONOFIC approach called alternate ONOFIC is used to further reducing the leakage current of the logic circuits. It uses two ONOFIC blocks one at the side of pull-up network and another at the side of pull-down network. These two ONOFIC blocks are dual in nature and giving the logic low or logic high leakage reduction in alternate cycle of the input signal combinations. For any output stable level only one of the ONOFIC block is turn-on and other one should be in turn-off state.

*1.2-Literature Survey:

The below given literature survey is from an article i.e a base paper of **S Dhar , M . Pattanaik and P. Rajaram, "Advancement in nanoscale CMOS device design en route to ultra-low-power applications", VLSI Design, Vol. 2011"** which says

In recent years, the demand for power sensitive designs has grown significantly due to the fast growth of battery-operated portable applications. As the technology scaling continues unabated, subthreshold device design has gained a lot of attention due to the low-power and ultra-low-power consumption in various applications. Design of low-power high-performance submicron and deep submicron CMOS devices and circuits is a big challenge. Short-channel effect is a major challenge for scaling the gate length down and below 0.1 μm. Detailed review and potential solutions for prolonging CMOS as the leading information technology proposed by various researchers in the past two decades are presented in this paper. This paper attempts to categorize the challenges and solutions for

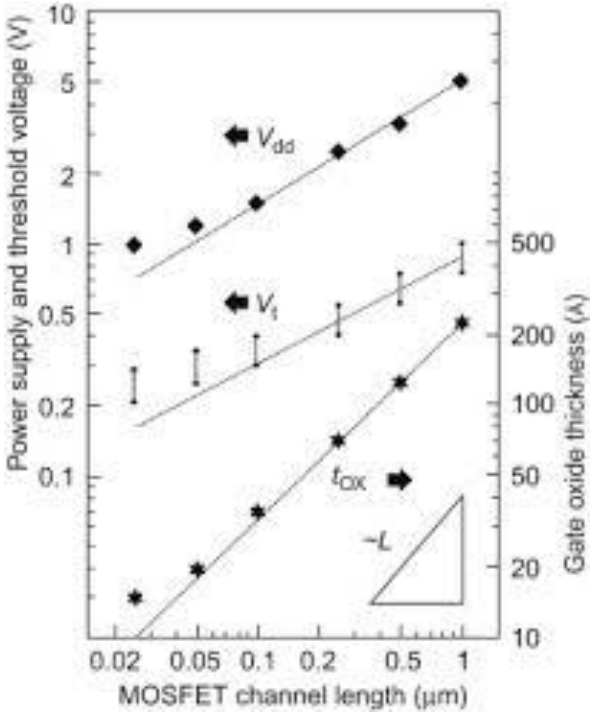
low-power and low-voltage application and thus provides a roadmap for device designers working in the submicron and deep submicron region of CMOS devices separately.

Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has been the major device for integrated circuits over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET-based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions. A lot of research has gone into device design over the last thirty years, but the evolution of process technologies brings new obstacles as well as new opportunities to device designers. Continuous CMOS scaling has been the main driving factor of silicon technology advancement to improve the performance. Design of low-power high-performance CMOS devices and circuits is a big challenge. The process parameters in low power design are channel length, oxide thickness, threshold voltage, and doping concentration in the channel. As the technology is scaled down, process parameter variations have become severe problem for low-power design. The low-power design technique should be such that it is less sensitive to the process parameter variations. As technology scales down, the variations of these process parameters are expected to be significant in future generations. As a result, the yield of the circuit will be less. The variation of leakage power and delay in the transistors on a given die are different for different low-power design techniques. The role of threshold voltage (Vth) and subthreshold swing (S) has become increasingly important with VLSI applications emphasizing on low-voltage, low-power, and high-speed design. Short-channel effect is a major challenge for scaling the gate length down and below 0.1 μm. The dependence of Vth on channel length is stronger as compared to other factors that also cause Vth fluctuation at small

device dimension such as random dopant distribution [1]. The gate oxide thickness in recent process technologies has approached the limit when direct tunneling starts to play a significant role in both off-state and on-state MOSFET transistor operation modes. This phenomenon, in addition to subthreshold leakage, results in a dramatic total standby leakage power dissipation. Thus, better design strategies to control the total leakage power are necessary. It is well known that gate tunneling currents are highly sensitive to the voltage variation across the gate oxide. Supply voltage attenuation can give significant reduction in gate leakage power consumption. Circuit design techniques to mitigate the impact of gate leakage would be much less efficient than the use of high-k material since gate leakage is a stronger function of process-induced oxide thickness fluctuation as compared to change in Vdd and threshold voltage. In addition to the gate-oxide scaling issue, higher doping concentrations would degrade subthreshold swing (S). Furthermore, Vdd scaling necessitates threshold voltage (Vth) reduction, which exponentially increases IOFF. IOFF reduction is critical where chips are often in standby mode of operation, and even during active operation, acceptable IOFF is required since leakage power consumption is rapidly increasing at a much faster rate compared to dynamic power . Few front ends of line challenges faced by transistors in the deep submicron and ultradeep submicron region include diminishing Vgs−Vth, larger Vth/Vdd, thin junctions drive dopant levels to saturation, dopant loss and statistical dopant fluctuation on small geometry devices increase device variability, and increase in channel doping concentration to control DIBL reduces carrier mobility while increasing body effect, gate oxide scaling slowing as it approaches the monolayer thickness of SiO_2 .

Subthreshold design is an inevitable choice in the semiconductor roadmap for achieving ultra-low-power consumption. In order to

achieve optimal performance, device, circuit, and architectural level optimizations specific to the subthreshold operation need to be applied. Due to the high sensitivity of the subthreshold circuits to process variations, it is imperative to use innovative design techniques to improve circuit robustness. Enhanced channel mobility due to applied strain to the channel is a major contributor to meeting the MOSFET performance requirements. In order to successfully scale ICs to meet performance, leakage current, and other requirements, numerous major processes and material innovations, such as high-k dielectric, metal gate electrodes, elevated source/drain, and doping techniques, need to be implemented. Dealing with fluctuations, statistical process variations, impact of quantum effects, line edge roughness, and variation in the ultra thin body width needs to be understood for better deep submicron performance especially for low-power applications.



*1.3-Thesis Organisation:

After studying in detail about the on-off logic we have organized the whole procedure into some different section or chapters which are divided into divisions, when comes to first chapter it briefly describes about the on/off (onofic) approach . Second chapter describes about the NAND gate logic , the on/off functioning of the Nmos and Pmos & even in this part the truth table is been verified & the connection of nand gate are been shown with the help of some simple figures .Third chapter takes to the detailed vision of on/off logic (onofic) how the cmos is been accumulated into the nand gate to work as onofic & it also comes across how the onofic logic is been applied to nand which has pullup network and pulldown network. When comes to Fourth chapter it describes about the working ,functioning & use of Virtuoso tool in detail.Fifth chapter is all about the results which are been executed with the tool & also we get the o/p of Schematic,Testbench,OutputWaveforms.The last division is all about Conclusion and References.

CHAPTER-2

*2.1 Designing and verifying NAND gate.

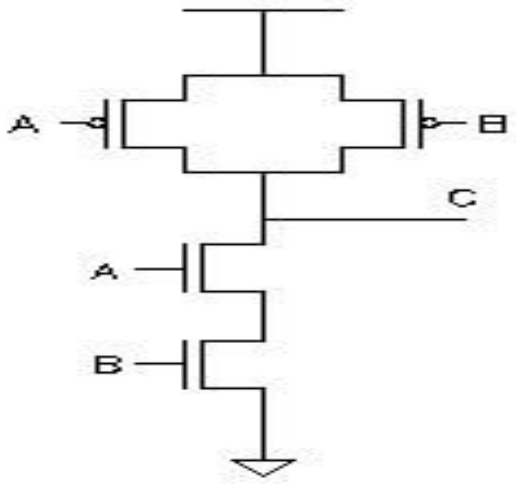
In this chapter the designing , connecting, using of pmos and nmos ,symbol creation and simulation is been done
At first to start with the process we have to launch virtuoso and the create a library and enter to the cellview and then select a preferred gpdk in this case used is gpdk180 and the in the cell view we have to go to analog lib and select the pmos for the pullup network and nmos for the pulldown network and also the voltage source as Vdd and ground to be as Voss .Now by giving the key word as ‘w’ we could connect the select transistors here in the case of and gate the pros drains are been connected to each other and the sources are given to the voltage source(DVD) and the body of these pros is been given to DVD when comes to the nmos similarly these are connect in a horizontal form and the drain of first nmos is connected to the source of second nmos and the junction where these both are been connected is been given as an output and the source of nmos2 is given to the gnd (Vss) and now the gates of pmos 1,2 &nmos 1&2 are been given as an input - A,B ; output-Y
These inputs and outputs of these design are been given through a pin (p) and the labels are also given for some complicated connections.

As we are done with this process we save the schematic and then run it which shows us the warnings(G) if any else we head towards the designing of the symbol where we have to just go to create and give the correct input & output pins and also top and bottom pins as(Vdd,Vss)

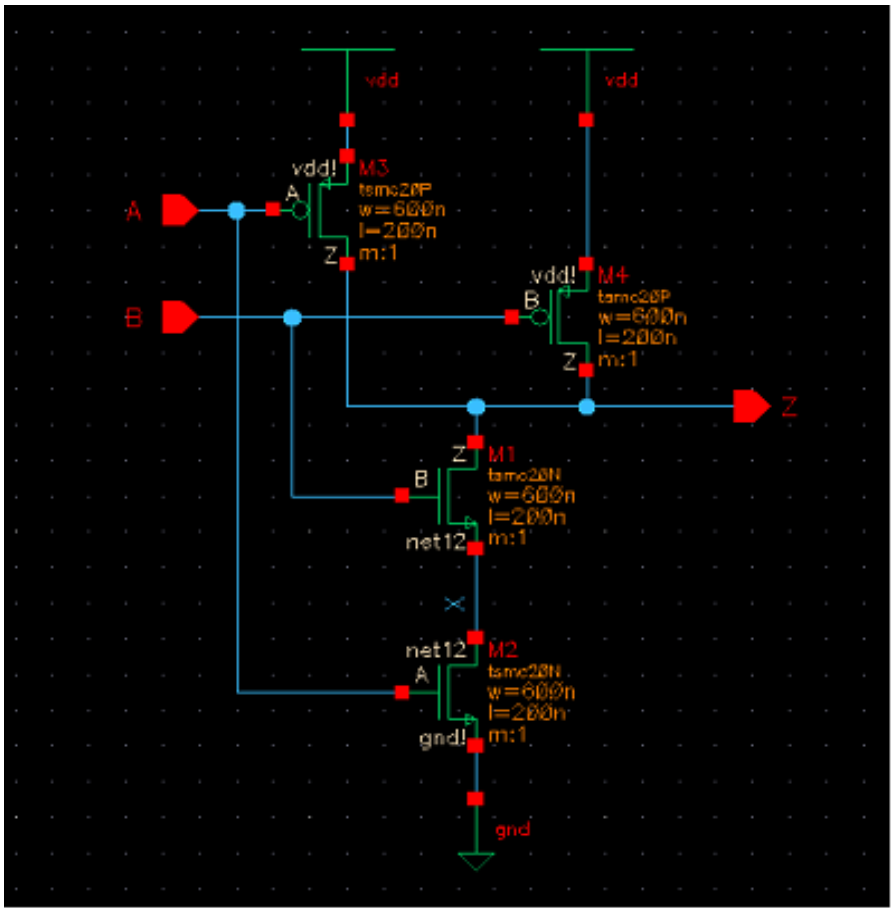
Now the next step is to create the testbench as we have to take a new file and create a testbench from the symbol created then connect the Vpulse which is to extracted from the analog lib and thesw vpulse are to be connected for both the inputs with a dcvoltage(1.8v) and timeperiod (2u,4u,……) and connect vdc to the top pin which is vdd and even give it the dc voltage and connect and the negative halves to vss and connect vss to gnd

Now launch through ADE-L and select the outputs on the design to be plotted then move to the analyses through which we choose trans and give time period and set it to moderate and at last we go to simulation and then Netlist and Run after some while we get the wave forms through which we could verify the truth table of nand gate.

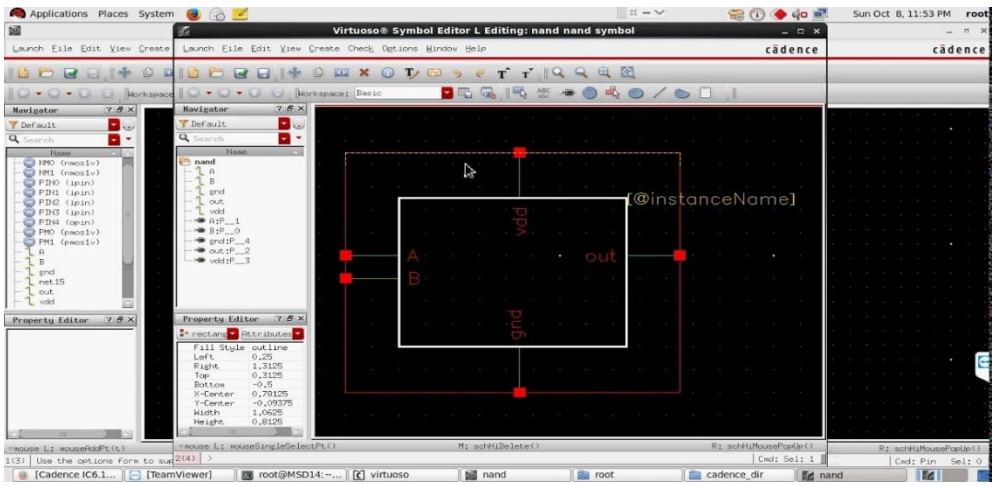
Given below is the schematic ,Design & Symbol for a NAND gate.



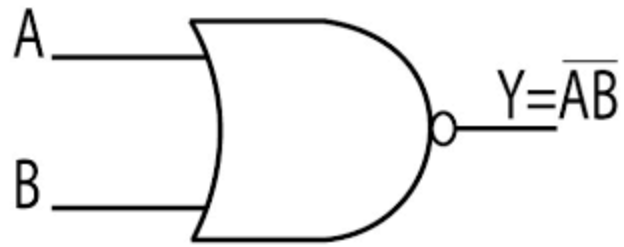
NAND



- Layout for a NAND gate



- Symbol for a NAND gate



A	B	A **NAND** B
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for NAND GATE

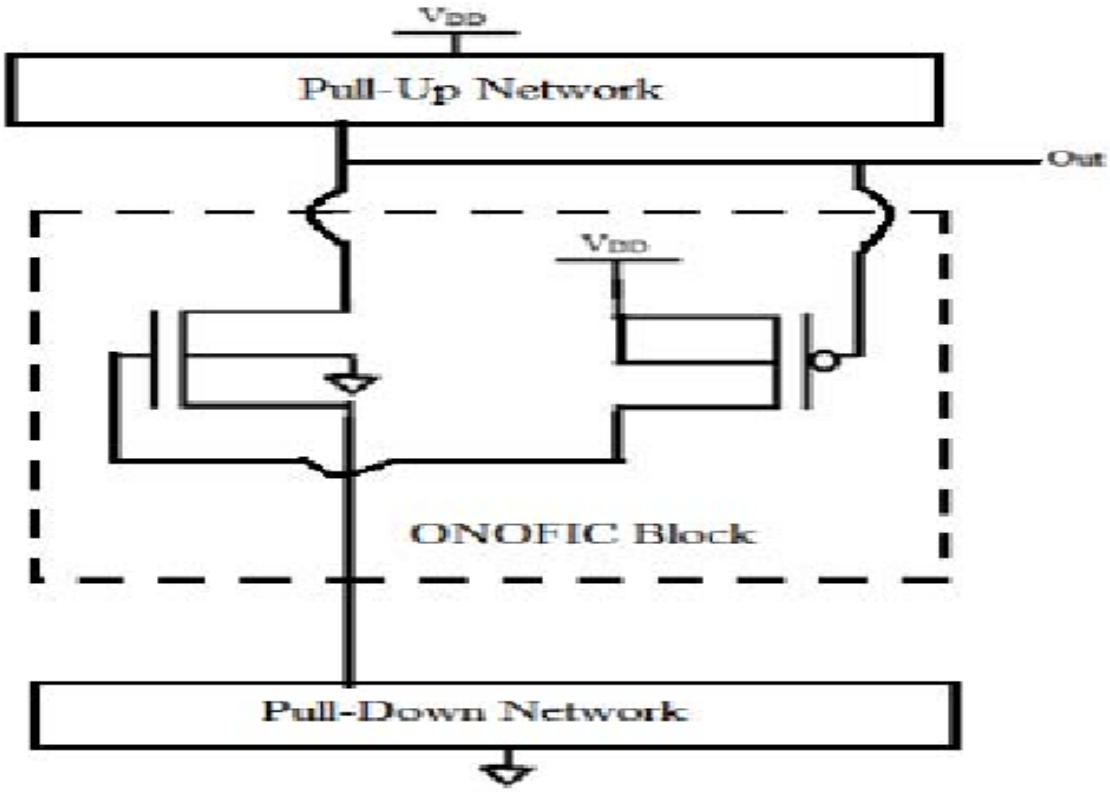
CHAPTER-3

* 3.1 PROPOSED ONOFIC APPROACH

The proposed On/Off logic (ONOFIC) approach reduces the leakage current and leakage power with simple and single threshold voltage circuit level approach. The ONOFIC approach efficiently reduces the leakage current in both active and standby mode of logic circuit. It introduced the extra logic between pull-up and pull-down networks for leakage reduction. This additional introduced logic circuit is called as On/Off logic (ONOFIC) circuit. The ONOFIC logic circuit contains one PMOS and one NMOS transistor. The connection of ONOFIC transistors is as shown in Fig. 2. Due to maintaining on or off condition for any output logic level this circuit is called as ONOFIC. This logic directly affects the power dissipation and propagation delay of the logic circuit. ONOFIC circuit uses the logic of force stacking for controlling the leakage current by providing the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state. In ONOFIC block the operation of NMOS transistor is controlled by a PMOS transistor. Depending on the output logic ONOFIC NMOS or PMOS transistors must be in cut-off or in linear mode

In ONOFIC block, the drain of PMOS transistor is connected to the gate of NMOS transistor and the output is connected to the gate of PMOS transistor. The drain of the pull-down network is connected to the source of NMOS transistor and PMOS source terminal is connected to VDD of the circuit. The NMOS transistor drain is connected to the output of the circuit and the substrate of NMOS transistor is connected to the ground while the substrate of PMOS transistor is connected to the VDD. The ONOFIC CMOS inverter logic is explained in Table I. The main concept of this technique is the property of on/off. The both ONOFIC transistors are in linear region when ONOFIC logic is in on condition while both transistors are in cut-off mode if ONOFIC logic is in off state. This reduces the leakage current at

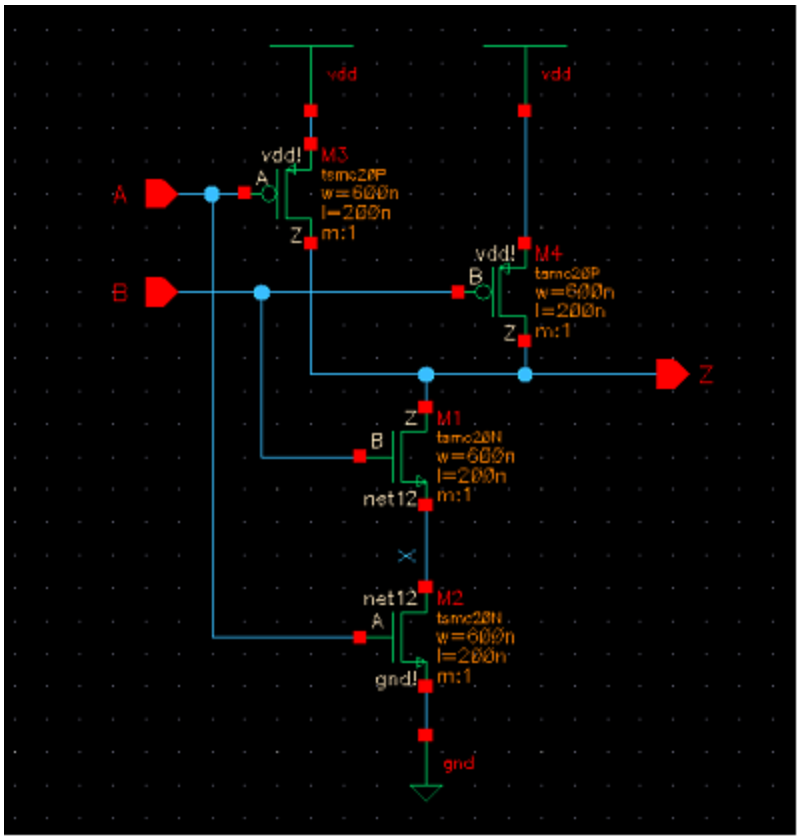
both active and standby mode with accurate logic level at the output. The good conducting path is obtained by turning on the ONOFIC block and it acts as a good resistance to control the leakage current when it is in off state.



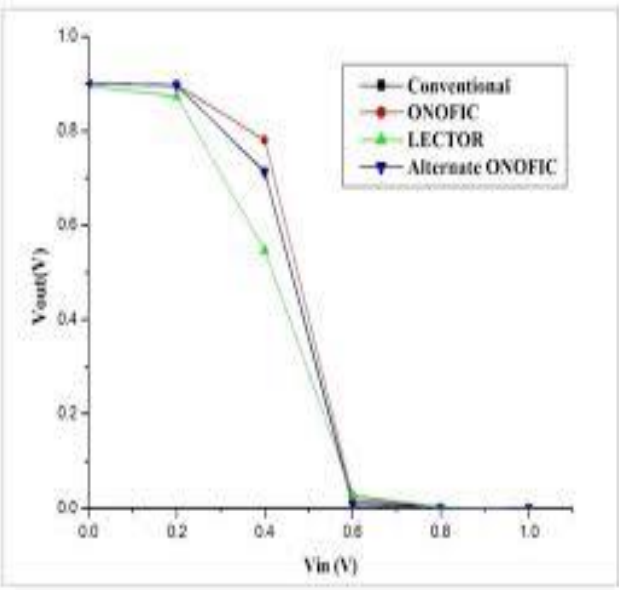
Schematic of ONOFIC logic

Input level	Pros	Onofic pmos	Onofic nmos	nmos
Logic low	ON	OFF	OFF	OFF
Logic high	OFF	OFF	OFF	ON

THE TRANSISTOR OPERATION OFAN ONOFIC CMOS INVERTER.



ONOFIC Approach NAND gate Circuit diagram



CMOS inverter DC characteristic

when compared to the other controller circuits the ONOFIC technique uses the same threshold voltage throughout the entire block which can improve the performance of the logic circuits. From the literature survey the LECTOR technique is also used a same threshold voltage throughout the circuit block. The above Fig. shows the DC characteristic of three techniques conventional, LECTOR and ONOFIC CMOS inverters. From the schematic Fig. we observed that the DC characteristics of conventional and ONOFIC inverter is similar to each other with large slope when compared to LECTOR CMOS inverter has low slope. Hence, when compared to LECTOR technique ONOFIC technique has less propagation delay and high voltage swing. The output waveforms shown in above Fig are of conventional; LECTOR and ONOFIC CMOS inverter at 32 nm technology shows the reduced leakage power obtained by ONOFIC approach. The slope of the CMOS inverter circuit with any input combination is given as Equation (1)

, Slope = ðVout/ðVin = ð(IoutRout)/ðVin; (1)

Iout = k/2 (VT)2 e(Vin-Vth)/VT (1- e-Vout/VT); (2)

Here k is device process parameter, VT is voltage temperature. Where Vth is device threshold voltage and which depends on doping densities of the material with material's quality factor, the flat voltage and charge storing capacitances. From the Equations (1) and (2) observed that the large slope is occurred due to large Iout current which leads to large static power dissipation and hence LECTOR technique has low static power dissipation when compared to conventional and ONOFIC approach. Equation (3) gives the propagation delay,

tp = (RoutΔVout)/Iout; (3)

Where, Rout is the sum of loads of resistive and capacitive of the CMOS circuit. ONOFIC and conventional circuits have less propagation delay when compared to LECTOR technique due to large Iout as observed from Equation (3). Due to less propagation delay the output values obtained quicker when input combination applied. The concept of stacking provides the ONOFIC circuit for controlling leakage current with maximum resistance when it is in off state and minimum resistance when it is in on state. In ONOFIC block, the operation of NMOS transistor is controlled by the PMOS

transistor. ONOFIC NMOS transistor mode is depends upon the output logic. The minimum propagation delay is obtained due to fast performance of turning-off and turning on of a PMOS transistor when compared to other techniques.

CHAPTER-4

REVIEW OF SOFTWARE MODULES

This chapter contains the basic information about the proposed system software modules. The following sections are covered in this chapter.

1. Virtuoso S-Edit
2. Virtuoso L-Edit
3. Assuraa

Each software explanation and the purpose of the software can be explained as follows:

4.1 VIRTUOSO S-EDIT:

Virtuoso Schematic Writer.

You will make a schematic and an image for a static CMOS inverter

- Embed cases into your plan
- Associate cases together utilizing wires
- Change case properties - Add pins to your outline
- Make and alter an image cellview
- Check and spare your outline

Making AnotherCellview

• To make another cell see, tap on Record - › New - › Cellview (you can do this in either the icfb window or the Library Administrator). A window shows up and select instructional exercise for the Library Name field, and sort in inverter for the Cell Name. The View Name ought to be schematic and the Apparatus field ought to be Writer Schematic. Snap alright when done.

• another window named Virtuoso Schematic Altering: instructional exercise inverter schematic ought to show up. This is the schematic window or cellview. Note that the last parts of the window name relate to the library (instructional exercise) and the cellview (inverter) that you are at present dealing with. • Investigate the order menu to finish everything and the symbols on the left. Tapping on the best (drop down) menu will uncover more charge choices. On the off chance that there is a bolt to one side of the

charge choice in the drop down menu, it implies that there are more choices under it. Tap on the order choice to uncover more alternatives

• By certain charge alternatives, there are a few letters beside it. These are bindkeys (or all the more usually known as hot-keys) that summon the order utilizing straightforward key presses. They will wind up plainly convenient when you get more acquainted with the schematic editorial manager and the bindkeys.

• The symbols on the left compare to a few most much of the time utilized charges, for example, include occurrence, change case properties, include wire, zoom in, zoom out, fix, erase and so on. By setting the mouse cursor over the symbol, the name of the symbol shows up.

• A fly up menu shows up when you put the cursor on any unfilled part of the schematic and press the center mouse catch.

• The correct mouse catch rehashes the last executed order.

Drawing a Schematic for a CMOS Inverter

Presently you are prepared to draw the schematic of a CMOS inverter as appeared underneath in the delineation. From the figure, you can see that the inverter comprises of two transistors (one

n-sort and one ptype), Vdd and Ground. These are known as occasions.

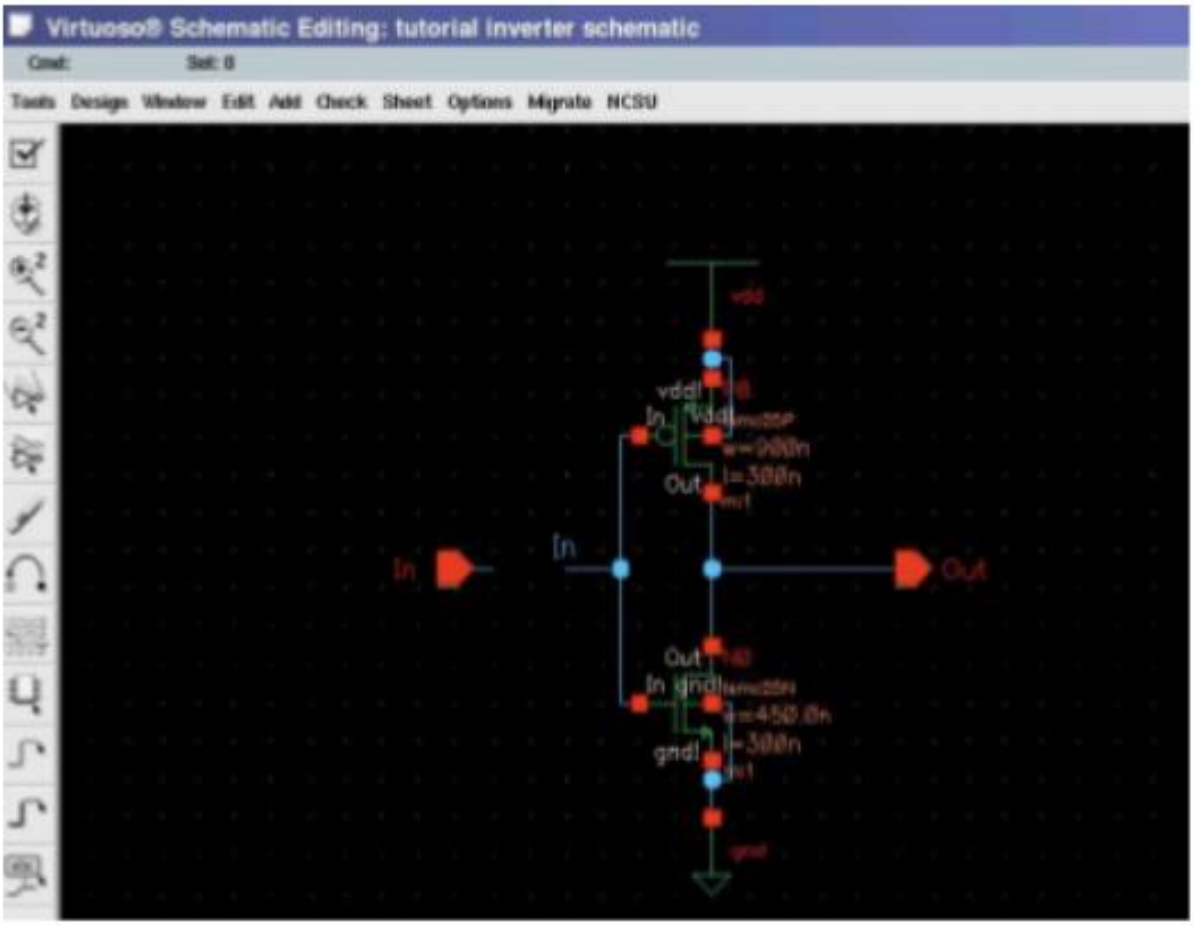


Figure 5.1:Inv schematic

Checking and Sparing Your Schematic

When you believe that your schematic is finished, you should run a beware of it. This check checks for extremely simple issues, (for example, detached sticks or dangling wires) and for some more unpretentious or cloud issues that may cause inconvenience later on in programs that endeavor to utilize your schematic. • To check your schematic, tap on the Check and Spare symbol. The aftereffects of the check are shown in the CIW. In the case of everything goes well, you should see a message in the CIW

Making and Altering an Image for Your Schematic

Now, you ought to have a schematic "view" of a CMOS inverter "cell" that passes the check without mistakes. You will now produce an image "see" for the inverter "cell".

• From your cellview of your inverter schematic, select Outline - › Make Cellview - › From Cellview starting from the drop menu. Another window named CellviewFromCellview shows up. The window demonstrates sections for the dynamic

plan, so Library Name ought to be set to instructional exercise, Cell name to inverter, and From View Name to schematic. Check to ensure that To View Name is set to image and all the above data is right, at that point click alright.

• The Image Manager window shows up, showing the inverter image produced by the schematic writer programming. This image is utilitarian and can be promptly utilized, however the shape is a straightforward rectangle and not the customary inverter image.Checking and Saving Your Schematic

Once you think that your schematic is complete, you will need to run a check on it. This check only checks for very rudimentary problems (such as unconnected pins or dangling wires) and for many more subtle or obscure problems that may cause trouble later on in programs that try to use your schematic. • To check your schematic, click on the Check and Save icon. The results of the check are displayed in the CIW. If everything goes well, you should see a message in the CIW

Making and Altering an Image for Your Schematic

Now, you ought to have a schematic "view" of a CMOS inverter "cell" that passes the check without blunders. You will now create an image "see" for the inverter "cell".

• From your cellview of your inverter schematic, select Plan - › Make Cellview - › From Cellview starting from the drop menu. Another window named CellviewFromCellview shows up. The window indicates sections for the dynamic outline, so Library Name ought to be set to instructional exercise, Cell name to inverter, and From View Name to schematic. Check to ensure that To View Name is set to image and all the above data is right, at that point click alright.

• The Image Editorial manager window shows up, showing the inverter image produced by the schematic arranger programming. This image is useful and can be

promptly utilized, however the shape is a basic rectangle and not the customary inverter

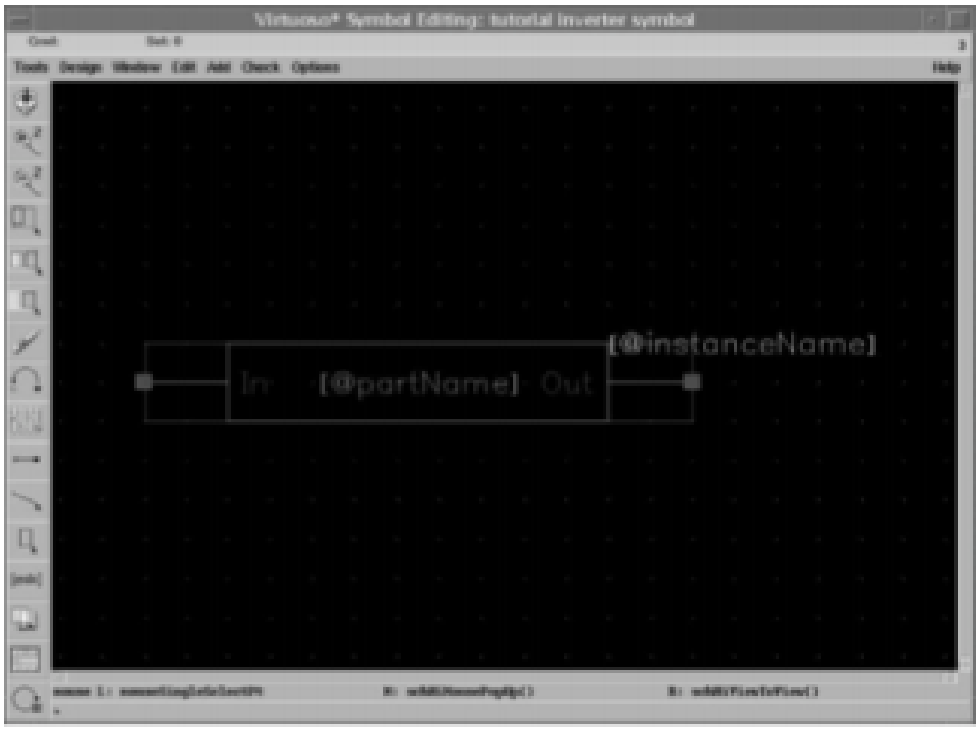


image.

Figure 5.2:Inv symbol

• Note that the symbols on the left are somewhat unique in relation to the ones in the Schematic Editorial manager window.

• To draw the new shape, select Include - › Shape - › Polygon. Point to the principal purpose of the polygon, trailed by the following point until the point that you end with your unique beginning stage and frame a triangle. Include a little hover at the pinnacle of the triangle at the yield end by choosing Include - › Shape - › Circle. Point and snap to characterize the focal point of the circle and move to measure the hover by moving the mouse.

• Painstakingly erase the internal box. Try not to erase the outside box that goes through the stick squares.

• Select the best and base sides of the outside box and move them out to the focuses on the triangle (snap and drag), with the goal that the whole triangle is inside the container. This case decides the limits of the image (i.e., figures out what region you tap on the schematic to choose the image)

• The last outcome should resemble this:

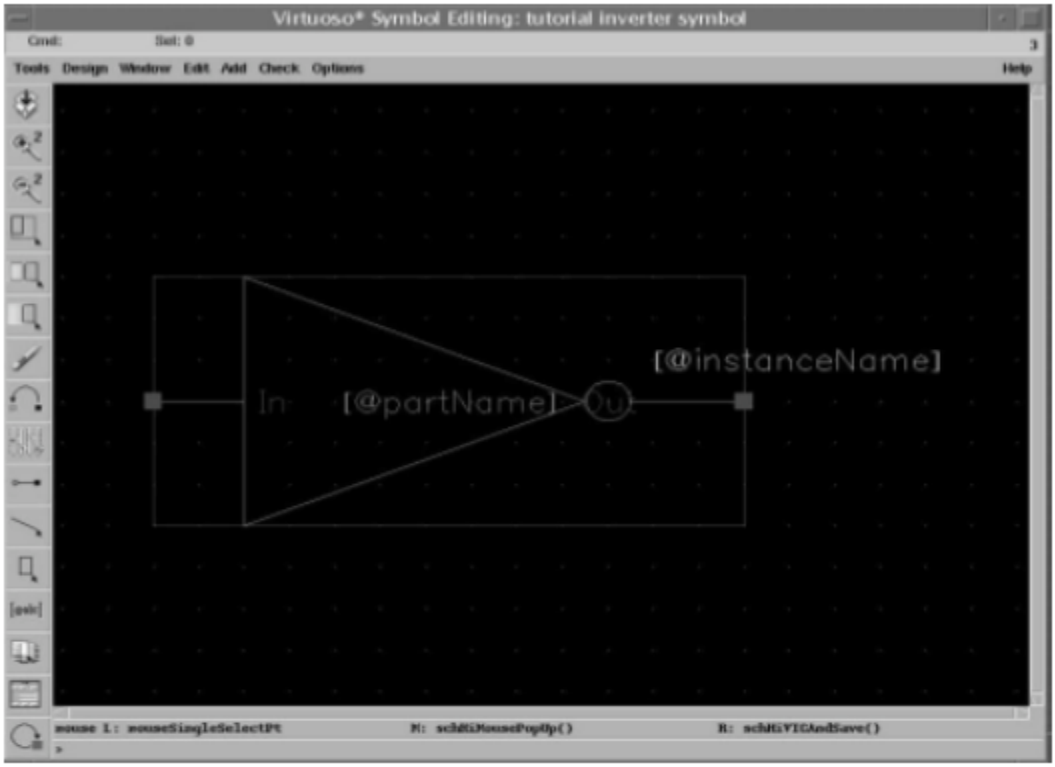


Figure 5.3:Invcellview

• Check and spare the image by utilizing the Plan - › Check and Spare order starting from the drop menu.

• On the off chance that you investigate the inverter cell in the instructional exercise library, you can see that it has now a schematic cellview and an image cellview.

4.2 VIRTUOSO L-EDIT

Cadence layout editor called Virtuoso, extracting layout, and running simulation on the created layout.

Make New Design View

To make a design see, go to Record - > New - > Cell View, select the Virtuoso apparatus in the instrument choice menu and sort in Cell Name as appeared in Figure 1. Snap alright, two windows will fly up; a design window and a LSW window. The format window is the principle window where you do your plan design. The LSW or the layer choice window gives you a rundown of every accessible layer in the present innovation. They will incorporate layers like poly, nactive, pactive, nselect, pselect, metal1, cc, by means of and so forth relying upon the innovation you are manufacturing

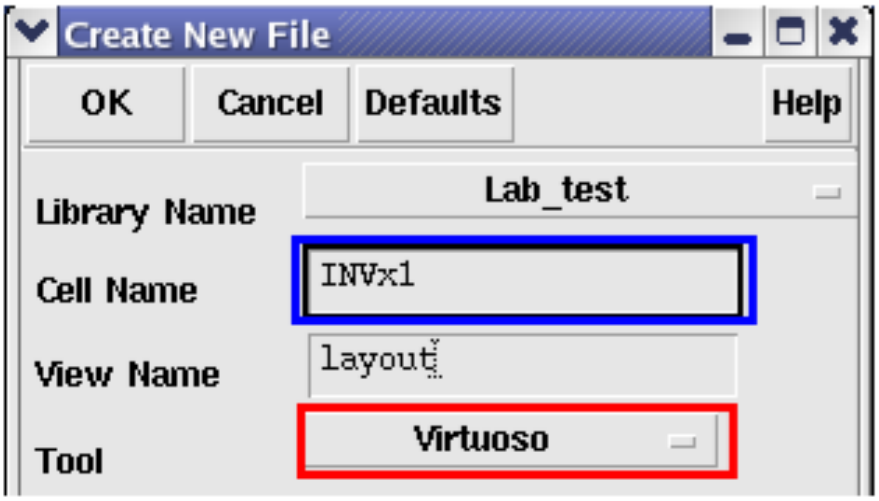


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Figure 5.4.New cell view

Setup Show Choices

To begin the design the main thing that you have to do is settle you matrix estimating. Go to Alternatives - > Show, the choices window appeared in Figure 2 will fly up. Set the matrix control parameters in the correct hand upper corner to the accompanying esteems. CMPE 315/CMPE640 Virtuoso Format Editorial manager UMBC Instructional exercise EkaratLaohavaleesonChintan Patel Minor Separating = λ Real Dispersing = 5λ X Snap Dividing = λ/2 Y Snap Dispersing = λ./2 Recall λ is a large portion of the element measure so on the off chance that you are utilizing a 0.6 µm. process then the λ esteem is 0.3. Likewise ensure that the Snap Modes Make and Alter settings in the correct base corner are set to anyAngle. Set the Show Levels to Begin = 0 and Stop = 20. Select Library on the base and snap Spare To. When you spare the choices to the library, you don't need to set up the show choices again when working in a similar library. Snap alright and after that go the Window - > redraw to refresh new setting on the screen. On the off chance that you are working in NCSU_TechLib_ami06 connected library, you can essentially take after the setup precisely

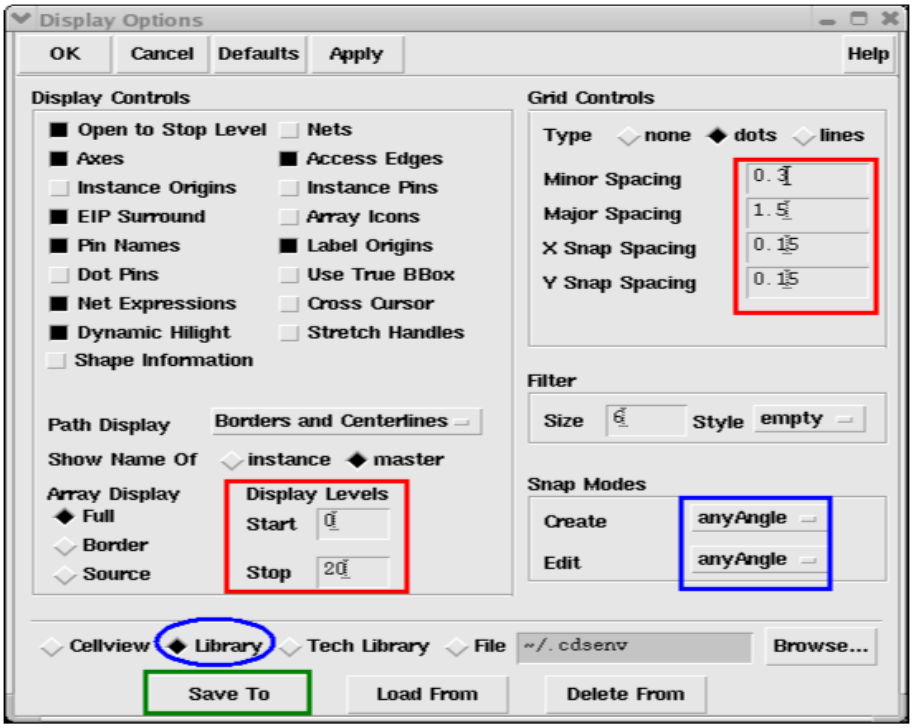


Figure 5.5.Display options

Becoming acquainted with Virtuoso Menu

The accompanying menu things are much of the time utilized amid making circuit design.

Plan Menu:

Spare: spare you formats.

Plot: Used to create a postscript petition for your design for printing.

Select submit and after that plot alternatives. Determine a record name and snap alright. At that point click alright on the primary submit plot frame and it will create a ps petition for you format.

Make Menu:

- Rectangle: makes a rectangle of the layer chose in the LSW.

- Way: Makes a way of the layer chose in the LSW. Double tap to end the way. - Occasion: used to import another current cell see into this cell see.

- Stick: Make sticks as clarified in later segment. Alter Menu: - Fix: fix the past orders.

- Re-try: re-try fixed charges. - Move: tap on any protest and move it around in the design. - Duplicate: Make a duplicate of any question in the format.

- Extend: Tap on the edge of a rectangle and size it. - Erase: Erase a question in the design.

- Properties: Change the properties of items in the design. Change the layer definitions and the progressions are quickly reflected in the design.

Confirm Menu:

- DRC: Check the format for configuration control infringement.

- Concentrate: Make a separated perspective of the format. This view is utilized for reproductions.

- Markers: Clarify: tap on the marker to discover the outline administer abused. - Erase all: Evacuate the markers after a DRC run.

Drawing Transistors

To make an inverter, as a matter of first importance you have to make p and n transistors. To begin with we will make the p transistor. The vast majority of the innovations you will configuration in will utilize a n-well process. In this way the dark foundation in the primary format window will go about as your p-substrate. Therefore you can put n transistors straightforwardly in the p substrate. However your p transistor should be put in n-well that you should draw particularly. Figure 3 demonstrates the

distinctive layers required to fabricate a p transistor.

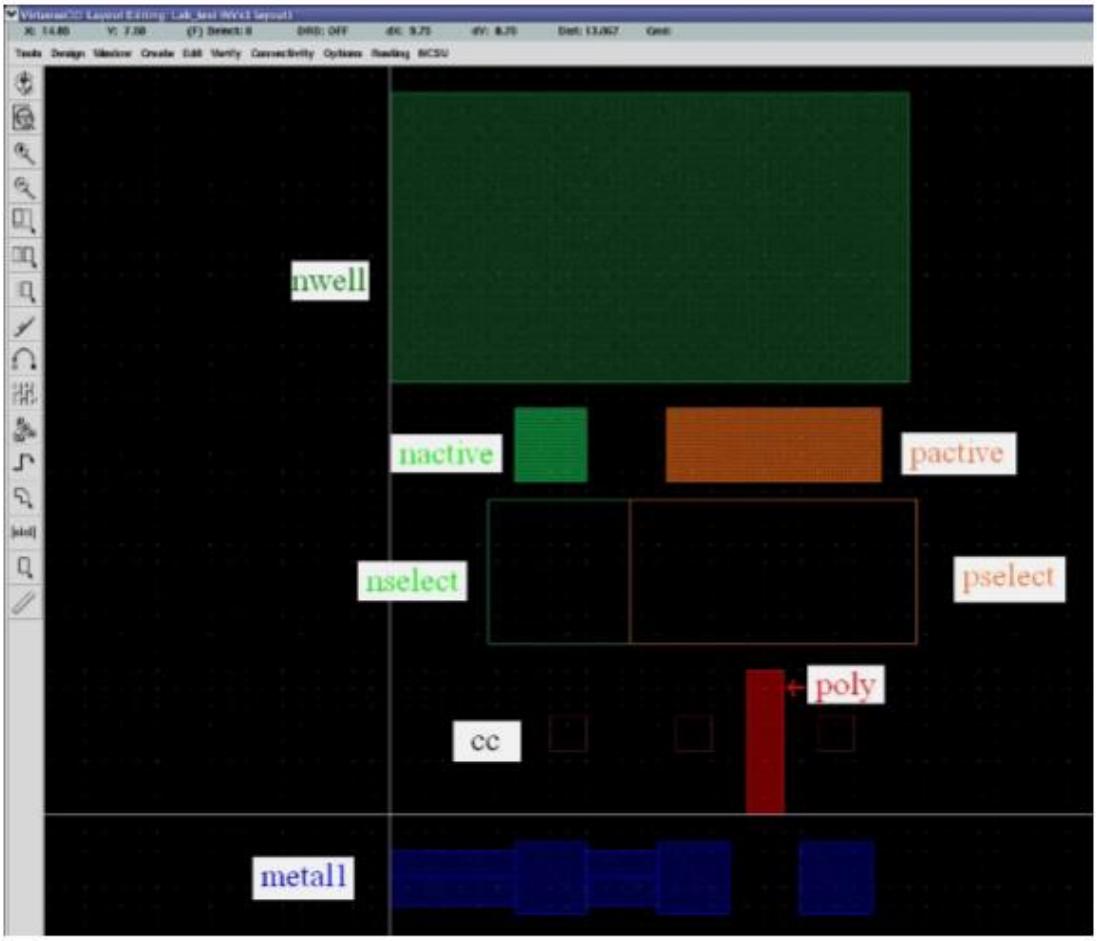


Figure 5.6.layers for buidingpmos

The p transistor is made by utilizing the layers as appeared in the figure above. You can make each shape appeared in Figure 3 by first select layer you need to make on LSW window and utilize make rectangle order (Make - > Rectangle) or make way summon (Make >Path). The extent of the layers relies upon the DRC rules characterized for the library and they can be gotten to at the site: www.mosis.org. Go to specialized help and after that to mosis configuration manages and select the innovation that you are utilizing.

The p transistor is set in the nwell and a n contact is set in the nwell to interface it to Vdd. The layers expected to make the p transistor are cc, metal1, pactive, poly and pselect. The pselect district should cover the whole dynamic region and the poly door. The nwell should encompass the whole ptransistor alongside the select district. Presently you require ancontact to associate the nwell to Vdd. The nwell is comprised of cc, nactive

and metal1 encompassed by a nactive rectangle. The contact is put inside the nwell and after that associated with the primary Vdd supply rail in the plan. The layers appeared in the figure above are consolidated as appeared in Figure 4 to frame the whole p transistor.

The request in which the layers are set isn't vital the main necessity is that every one of the layers ought to be available. The layers are shown in the format window as characterized by the apparatus and the cover of two distinct layers will be unmistakably recognizable.

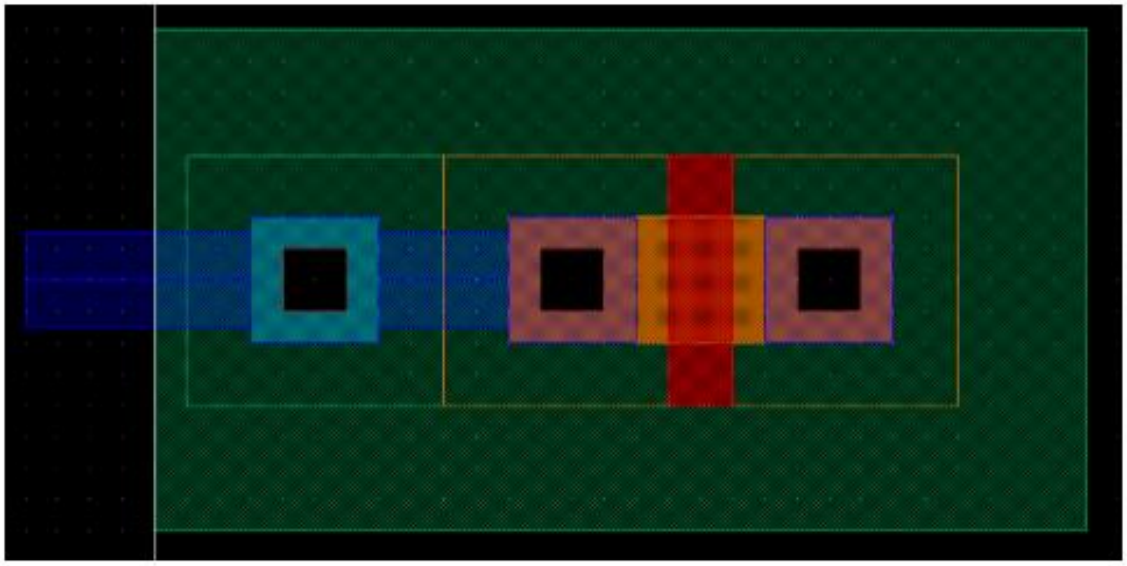


Figure 5.7.pmos layout

The n transistor is laid out in a comparable manner and the layers required for the same are appeared in Figure 10. However the n transistor will have a nactive layer rather than pactive layer in the ptransistor and will be encompassed by n select rather than the p select. As the innovation is anwell innovation the dark foundation is the p-substrate and thusly you require not put a pwell layer around the n transistor. In any case despite everything you have to put a contact to interface the p substrate to ground. The p contact is reciprocal to the n contact and is made of cc, pactive and metal1 encompassed by a pselect rectangle. The joined p and n transistor are appeared in Figure 11.

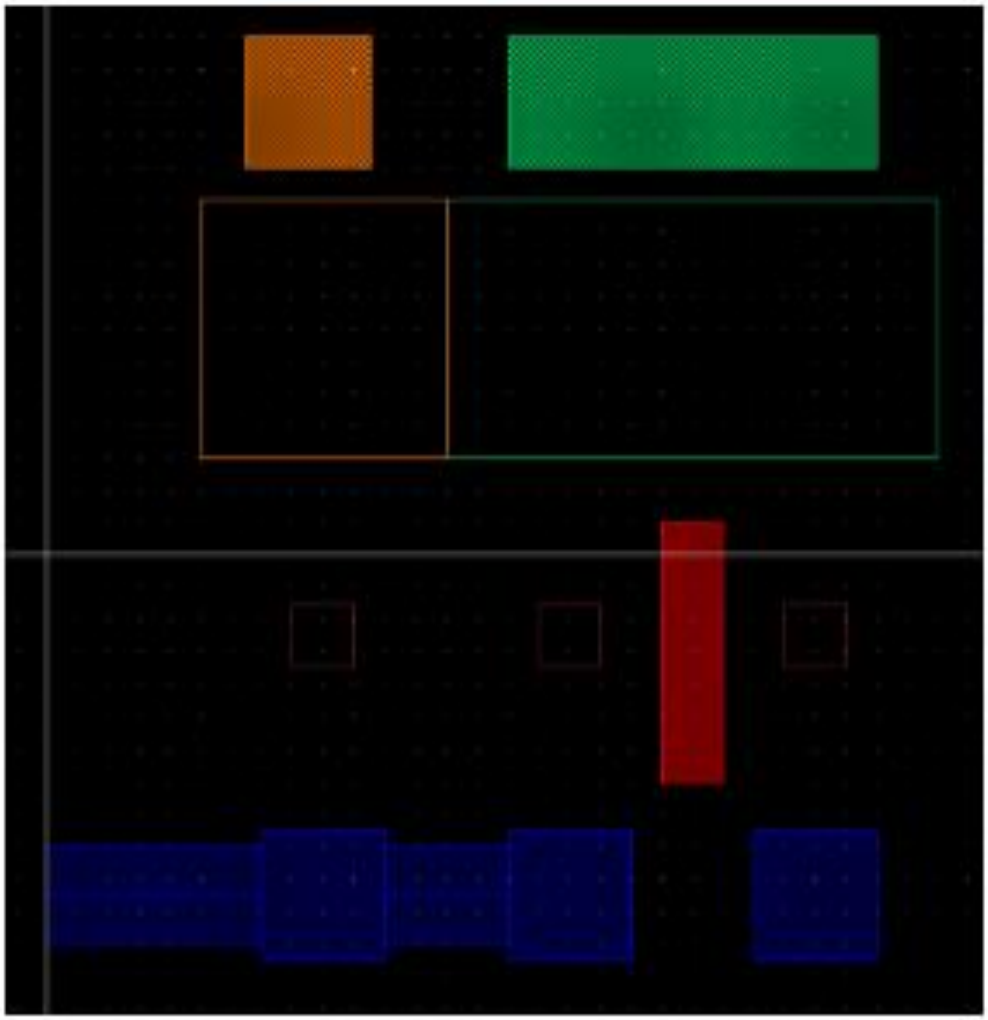


Figure 5.8.layers for building nmos

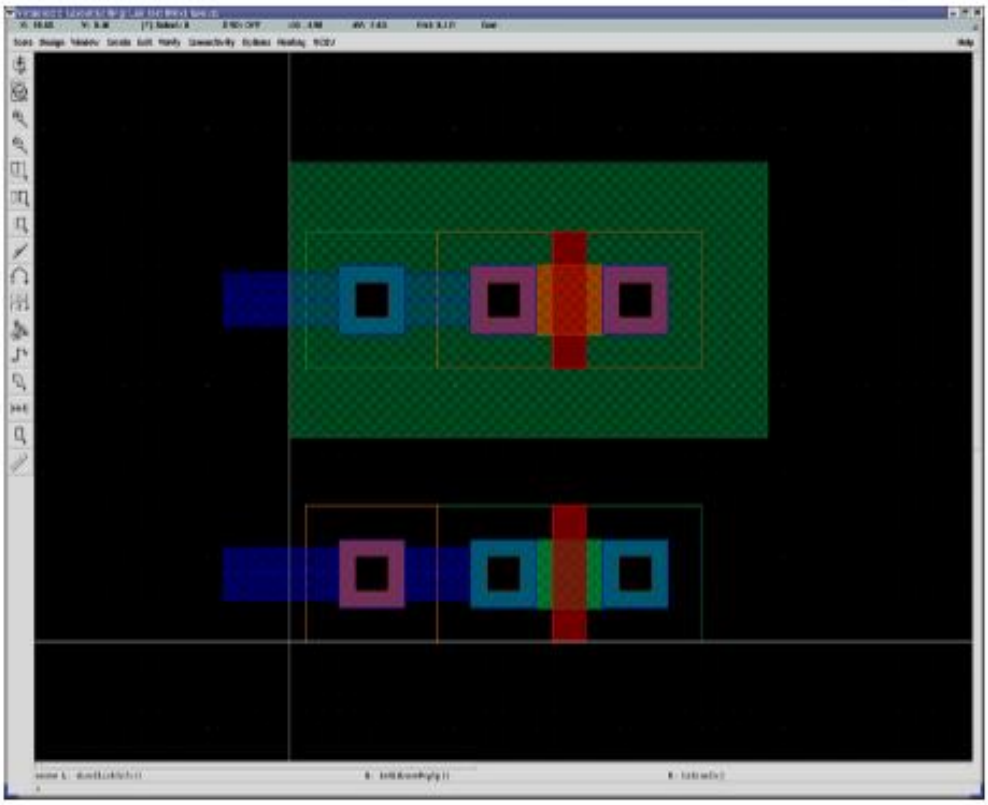


Figure 5.9.pmos and nmos layout

3.3 ASSURA

Assura is maily used for DRC and LVS

Design Rule Check

There is a decide checking device that is accessible with the rhythm conveyance which checks a large portion of the guidelines. To run configuration run check (DRC), go to Confirm - > DRC. The DRC discourse as appeared in Figure 12 ought to show up, click alright. Figure 13 demonstrates DRC report showed on CIW window, in the figure no mistakes are found on the plan.

You have to run the outline manage checker at each progression of you plan. It is extremely hard to repair the sizes of different parts after they are associated together in the format so ensure that everything that you put in the design is perfect with the outline rules.

A large portion of the mistakes found by the outline control checker are clarified in detail in the CIW window and are anything but difficult to settle. Here and there a

format might not have DRC mistakes but rather just notices. It is smarter to illuminate these notices previously going further. The most well-known cautioning is for pins. When you put two sticks on a similar way the DRC device will produce a notice marker yet won't clarify it in the CIW window.

To check which marker remains for which mistake tap on Confirm - Markers - Clarify and after that tap on any marker in the format window. A content box will fly up determining the outline decide that is being damaged. Fix the mistake in your format and run DRC until the point when your outline is totally blunder free.

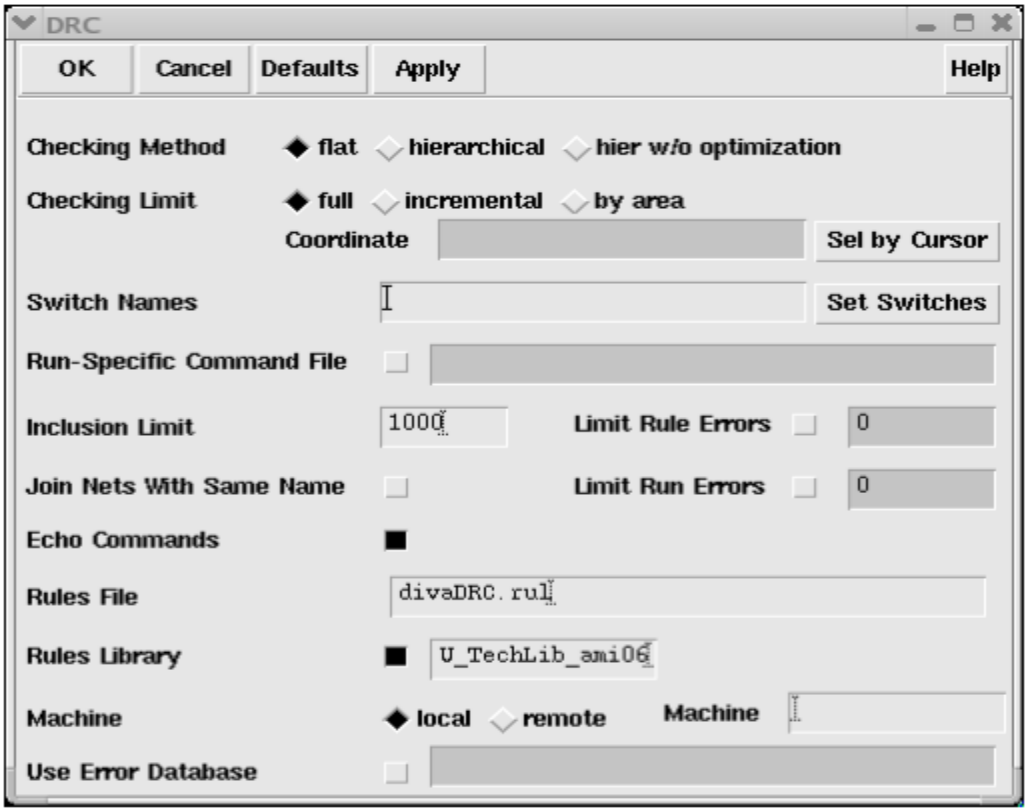


Figure5.10.Design rules check

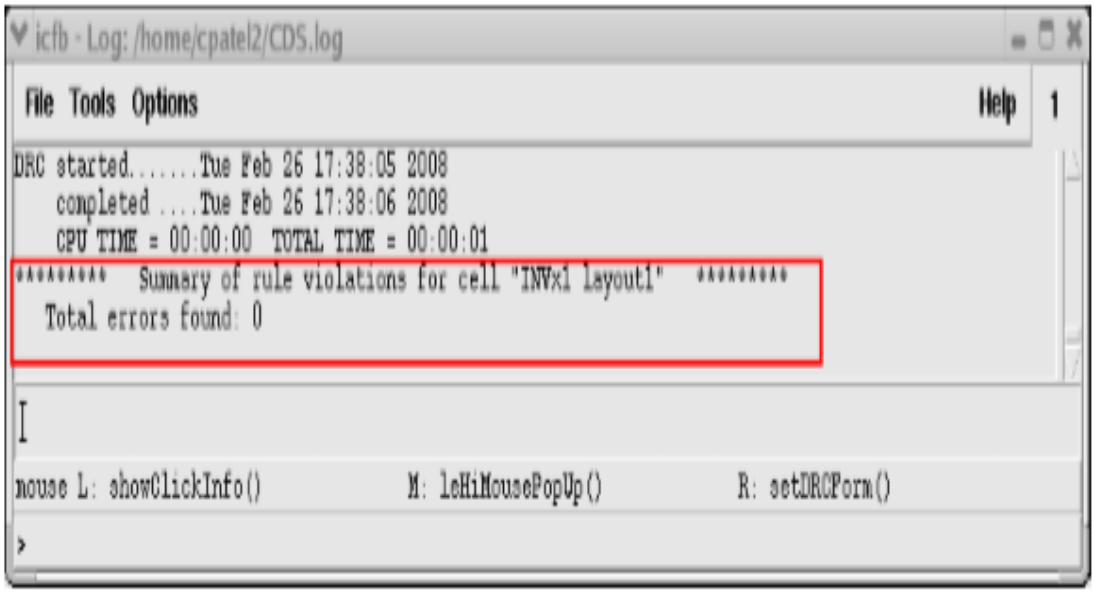


Figure 5.11.DRC report

LVS

Format extraction apparatus is utilized to create genuine circuit netlist from your design. The separated view can be utilized to run Design Versus Schematic (LVS) and to run reenactment. To run format extraction device, go to Confirm - > Concentrate. The extractor discourse as appeared on the left of Figure 15 ought to show up. Tap on Set Switches and afterward the switches choice window should fly up as appeared on the privilege of Figure 15. Select Extract_parasitic_caps and Keep_labels_in_extractd_view choices as appeared in the figure (hold Ctrl key and tap on choices to choose numerous alternatives). Snap alright to close set switches discourse and snap alright again on Extractor exchange to run the design extraction.

You should see extraction provide details regarding CIW window (on the off chance that you have substantial design, the extraction may take a couple of minutes before the report appears) as appeared in Figure 16. You ought not have any blunders/notices, if there're any, settle it. The most widely recognized blunders/notices is having numerous pins on similar nets which implies that you may have a shorting net (e.g., vdd is shorted to different nets) or have various pins put on a similar net (e.g., having pin named In and Contribution on a similar info net).

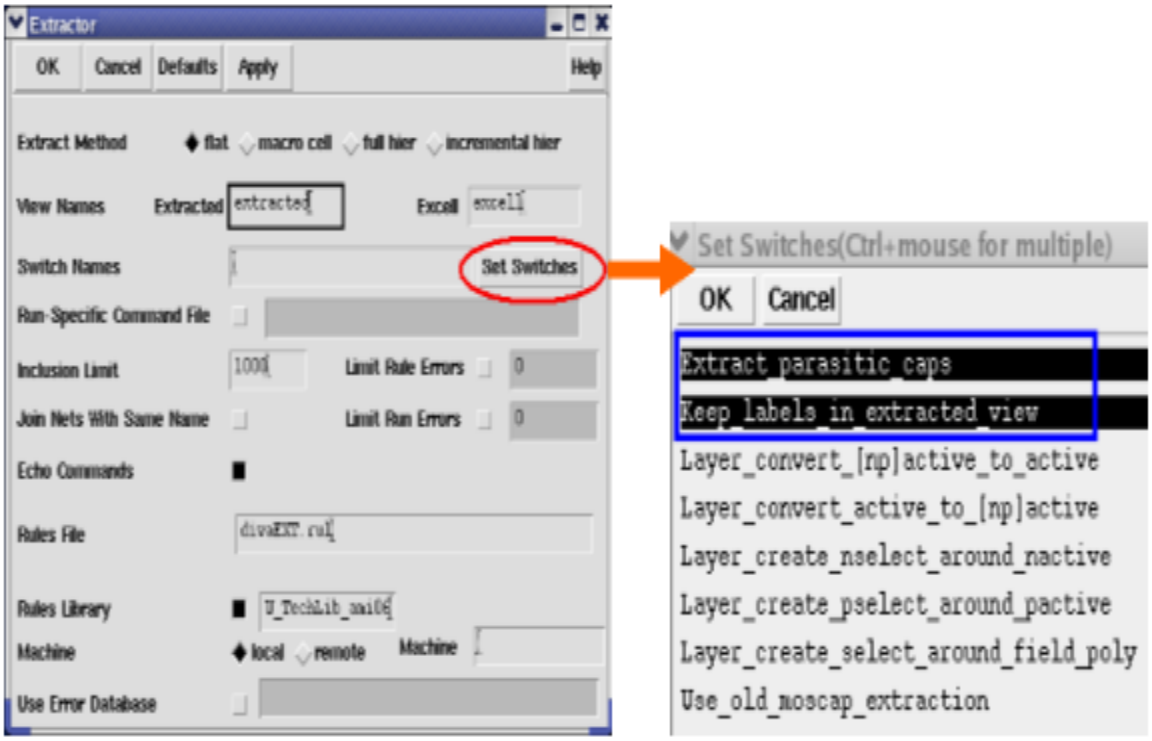


Figure 5.12.Layout extractor

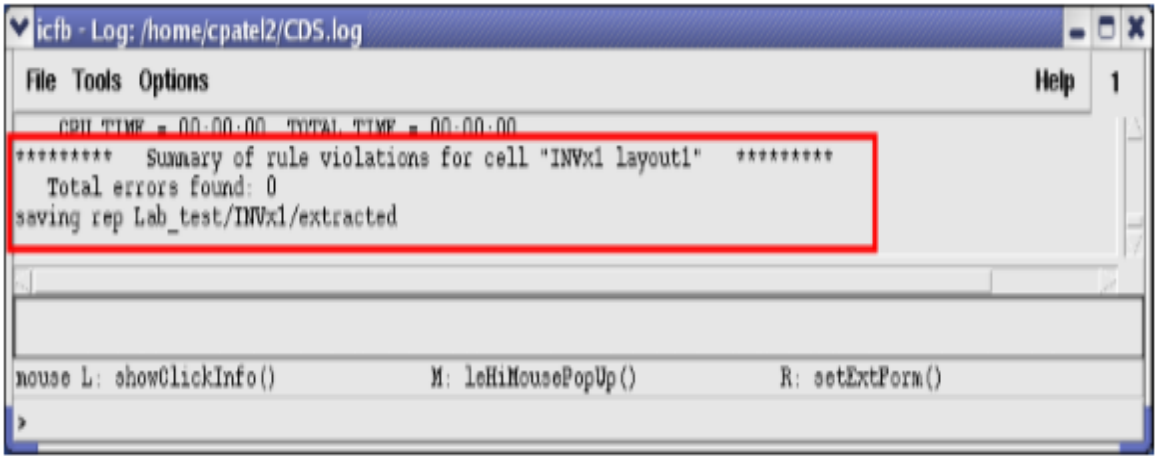


Figure 5.13.Extracted report

CHAPTER-5

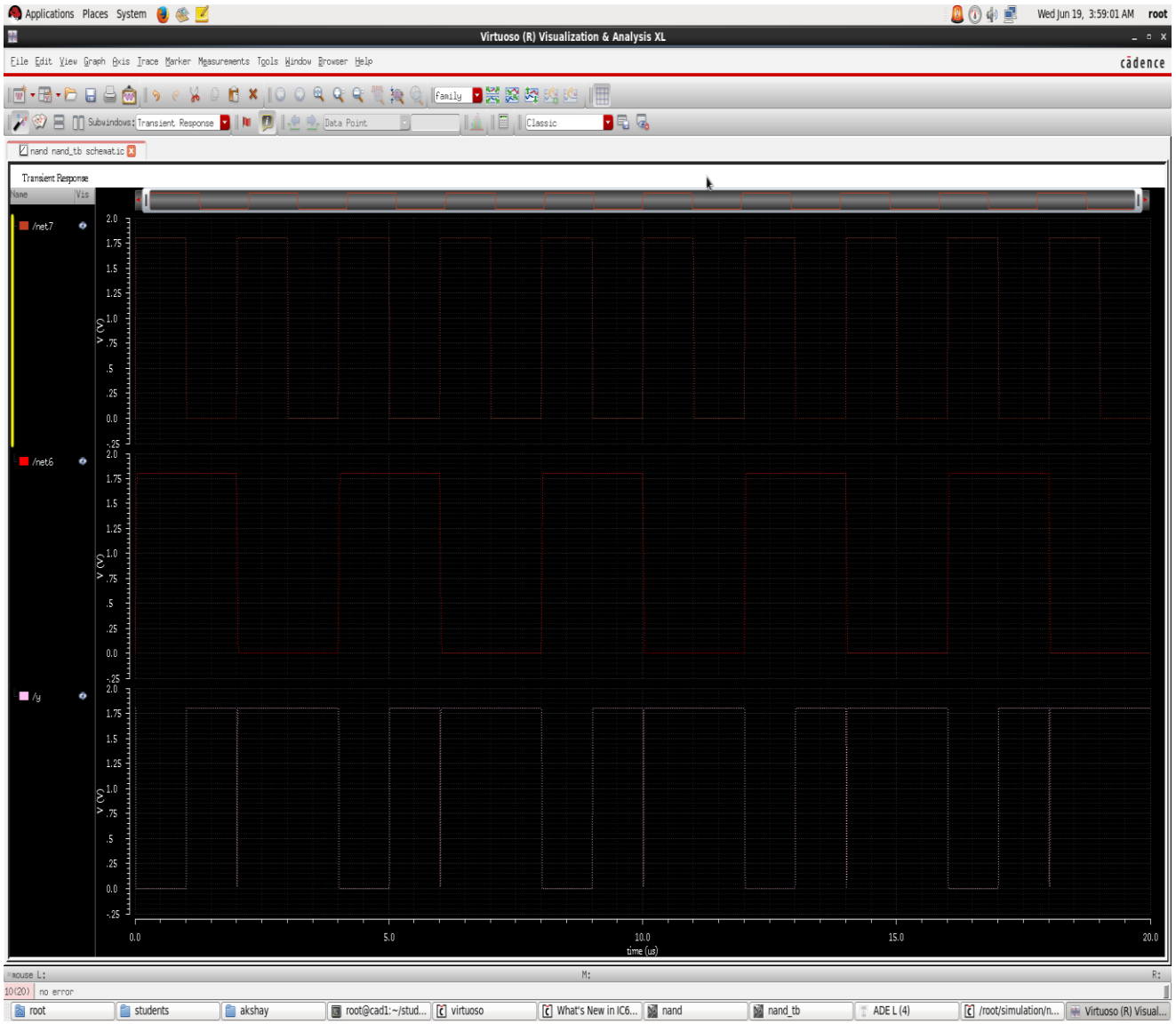
*Results

Power Dissipation & propagation Delay of CMOS at Different Tech.

Circuits	90nm	45nm	35nm	45um
inv_conv	4.019997	1.021826	2.460309	1.0058
Inv_lector	3.426373	1.204296	2.639254	1.0288
Inv_onofic	4.950182	4.546152	8.994829	1.0109
Nand_conv	6.053454	2.003633	4.893321	1.0359
Nand_lector	3.621849	2.213076	5.062619	1.0273
Nand_onofic	3.780632	5.469471	1.121113	1.0242

The result of 90nm ,45nm and 32nm technologies has got different power consumption as technology goes in reduced accordingly losses are increased so ONOFIC took less propagation delay method is got more advantages

One for ONOFIC approach and the other for LECTOR logic respectively. The main components in the circuit are XOR , AND and OR gates. In ONOFIC block, the drain of PMOS transistor is connected to the gate of NMOS transistor and the output is connected to the gate of PMOS transistor. The drain of the pull down network is connected to the source of NMOS transistor and PMOS source terminal is connected to VDD of the circuit. The NMOS transistor drain is connected to the output of the circuit and the substrate of NMOS transistor is connected to the ground while the substrate of PMOS transistor is connected to the VDD. LECTOR technique utilizes two leakage control transistors (LCT) which are inserted between PUN (Pull Up Network) and PDN (Pull Down Network) circuit within the logic gate for which the gate terminal of each leakage control transistor is controlled by source of other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Virtuoso (R) Visualization & Analysis XL
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Transient Response
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/net6
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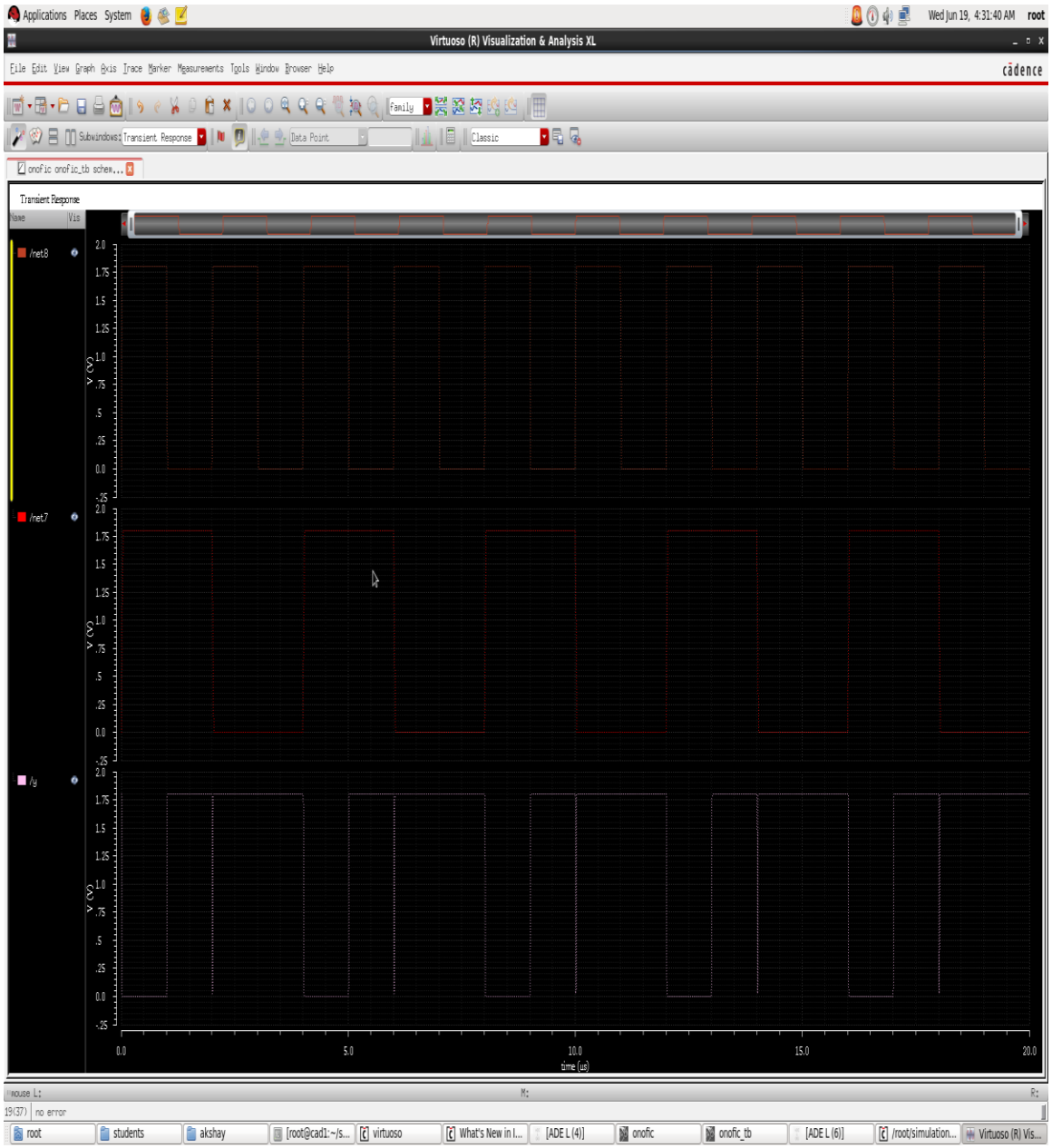
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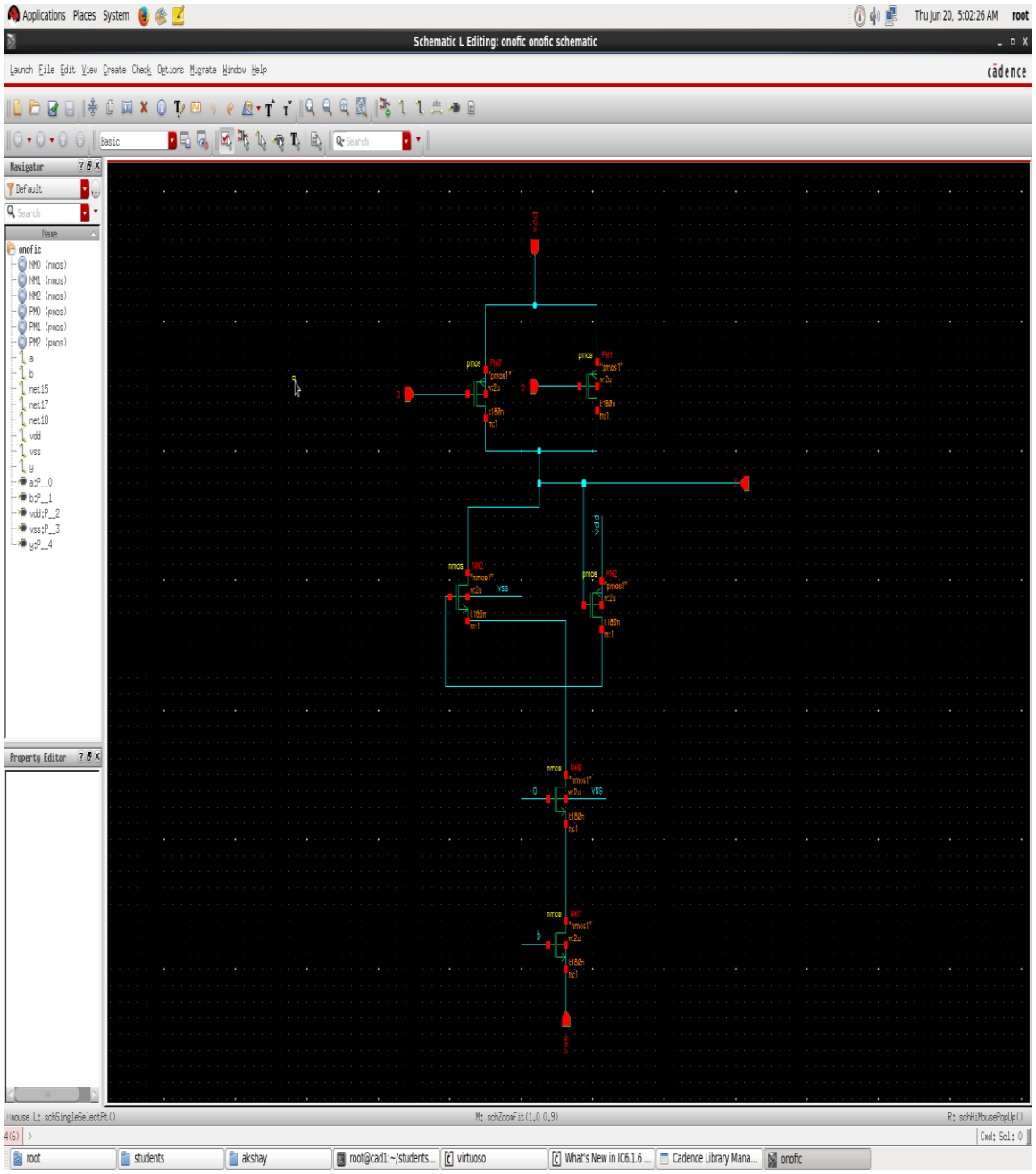
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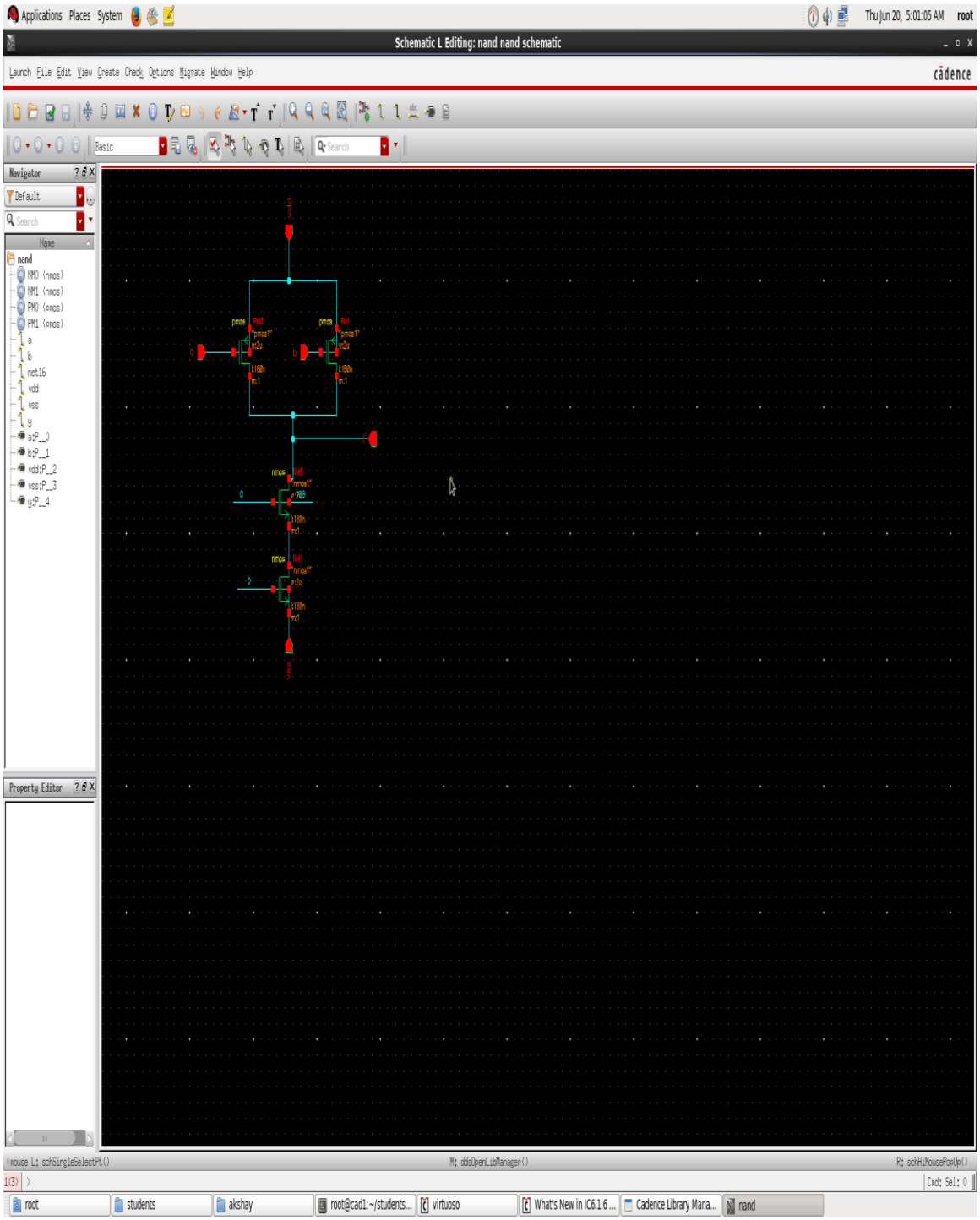
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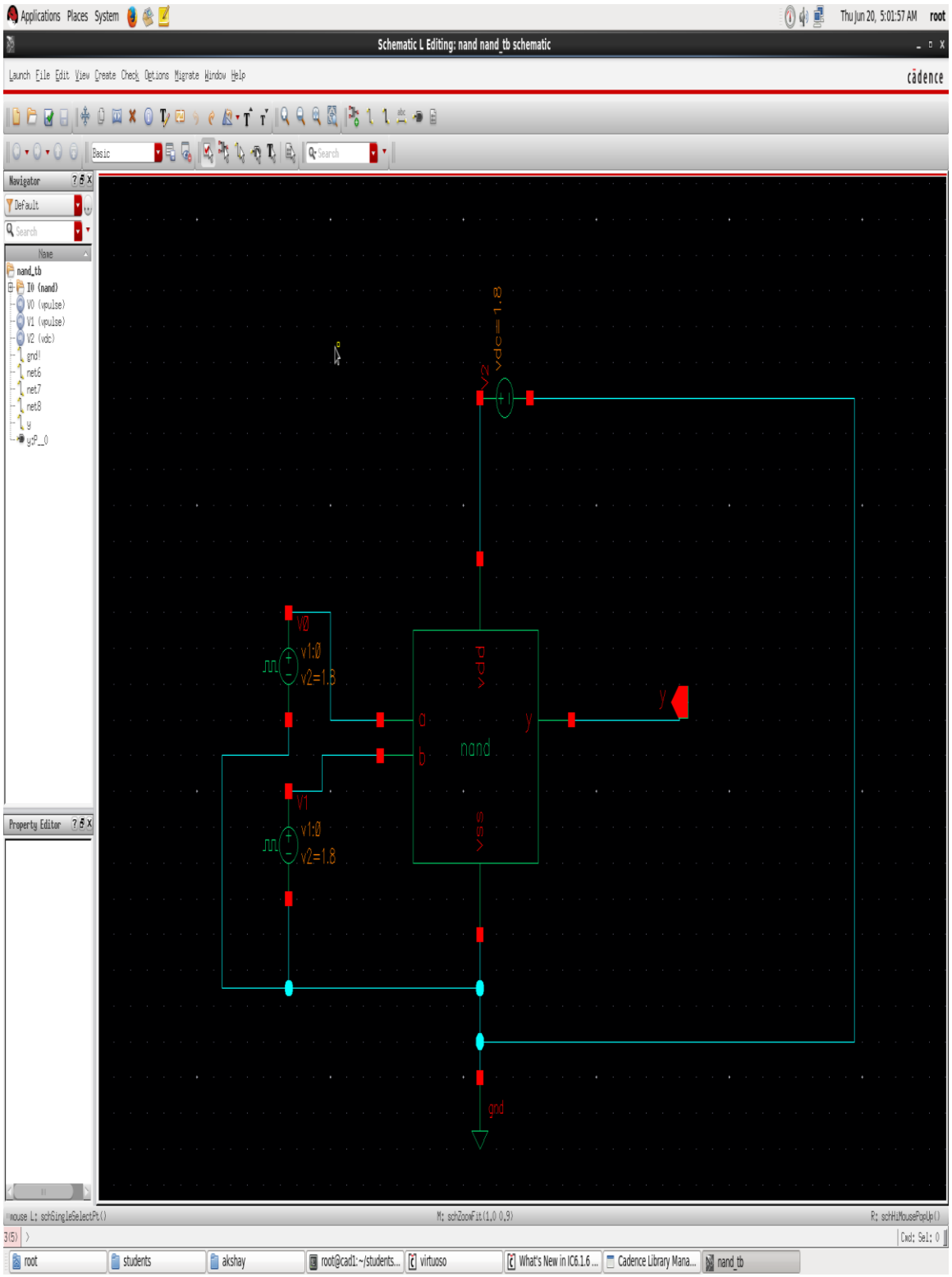
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V2
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V0
v1:0
v2=1.8
V1
v1:0
v2=1.8
vdd
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b
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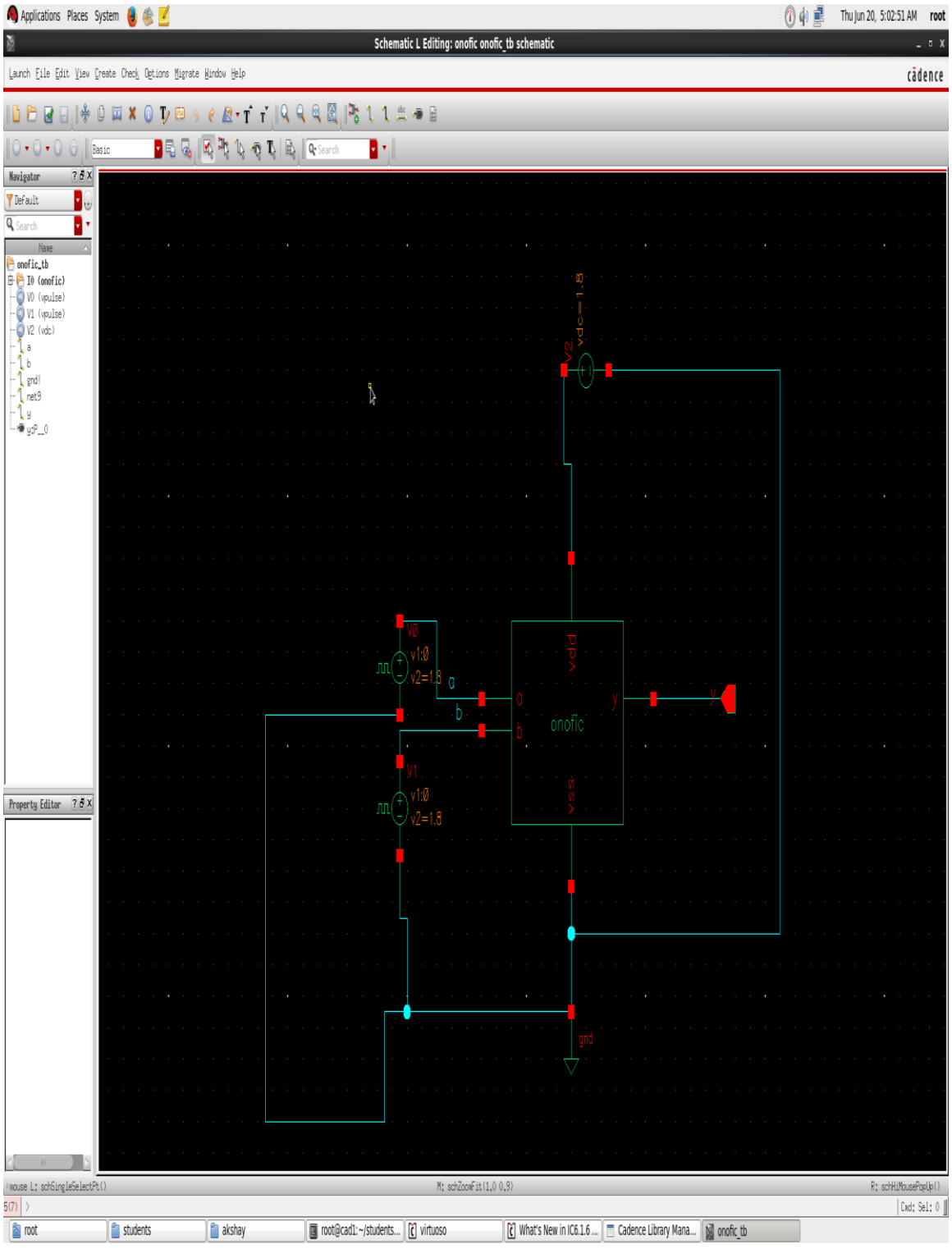
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V2 (vdc)
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b
gnd!
net9
y
V2
vdc=1.8
V0
v1:0
v2=1.8
a
b
V1
v1:0
v2=1.8
vdd
a
b
onofic
y
vss
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Conclusion:

The problem of dissipation power is reduced for different technology, This work addresses the challenge of obtaining of power losses and efficiently use IC's and electronics devices Is applied to solve its energy consumption and performance is improved and it can helpful in power saving in CMOS circuits which has been compared conventional, Lector and ONOFIC method hence the ONFIC method is suitable for design circuits and efficient using Cadence .

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