High Performance and Low Power ONOFIC Approach for VLSI CMOS Circuits Design

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***Abstract*—Improving high performance with reduced power consumption and chip area are the main constraint for designing VLSI CMOS circuits. In this paper, high performance and low power ONOFIC approach for VLSI CMOS circuits have been implemented. The proposed method reduces the power dissipation and improves the speed of a VLSI circuit design. Mostly the concentrated part in deep sub micron regime is the power dissipation. Many techniques have been proposed for reducing leakage current in deep sub micron but with some limitations they are not suitable for actual requirements. The proposed On/Off Logic (ONOFIC) serves the needs for deep sub micron with its reduced power dissipation and increased performance in VLSI circuits. Thus, the proposed ONOFIC approach results have been compared with LECTOR technique and observed that the proposed technique shows the improved performance and reduced power dissipation. The tool used for implementing the design is Tanner EDA.**

***Keywords*—ONOFIC, Deep sub micron, LECTOR, Leakage Current.**

I. INTRODUCTION

The design of a low power circuits mainly focus on a problem occurred due to the performance, power dissipation and chip area. The constraint in deep sub micron is to reduce the device dimensions in the design of logic circuit leads to decreased chip area [1]. To improve the reliability of a logic circuit in deep sub micron regime, the supply voltage is reduced. In electronic devices, to control the power consumption a supply voltage plays an important role. Supply voltage scaling without scaling of threshold voltage degrades the performance of the device. By reduction of threshold voltage and supply voltages proportionally retains the performance. The threshold voltage reduction leads to the five times higher leakage current [2].

Adopting new lower level technologies leads to the increase in power dissipation in integrated circuits. The power dissipation trends according to the reduced gate length are shown in Fig.1.[2].This plot shows that, as the technology scaled down the leakage power dissipation goes up [3-6].

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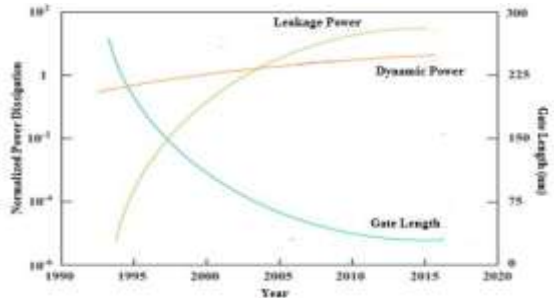

Fig. 1. Trends of Recent Power Dissipation

A perfect designer concentrates mostly for efficient techniques for leakage current reduction in deep sub micron regime. For designing high performance and low power CMOS circuits a new method is implemented in this paper which is On/Off logic (ONOFIC) approach. The remaining paper is organized as follows. Section II briefly describes the previous techniques used for leakage reduction. Section III describes the proposed ONOFIC approach for leakage reduction. Section IV describes the Results and discussion and Section V is about conclusion.

II. RELATED PREVIOUS WORK

The active and standby mode of device may arise the leakage power dissipation, thus in deep sub micron regime every logic circuits should built up with leakage reduction techniques. In [4], the model of virtual power rail is used in MTCMOS technique. Through high threshold transistor the virtual power or ground line is connected to actual power or ground line. MTCMOS technique is suitable for standby mode device leakage reductions because of increase in chip area. This technique needs two distinct threshold voltage transistors which lead to extra mask layers. In [7-9] S. Narendra et al. discovered that by connecting off state transistors in series can reduce the leakage power. By adding the off state transistors path resistance increases and hence reduces the leakage current of the logic circuit. The Added series transistors increases chip area and propagation delay. In [10] SCCMOS technique is implemented to decrease the leakage current in standby mode by turning off the transistors which connects the main circuit to power supply. The PMOS sleep transistor gate voltage is maintained higher when compared to the power supply VDD voltage to make for maintaining the transistor in off condition. For increasing the gate voltage strong charge pump circuit is

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needed. The charge pump circuit design may leads to increase in chip area, power consumption and propagation delay. In [11] authors J.C. Park and V.J. Mooney combined the forced stack and an MTCMOS technique. With this method leakage current can be controlled in active mode and also reduces the delay. The main drawbacks of this technique are replacing the one transistor with three transistors causes the extra area for sleep signals.

In [12] the authors N. Hachette and N. Ranganathan proposed a reliable LECTOR technique which uses two Leakage Control Transistors connected in a manner so that one of the LCT transistors will be in off state for any input signal combination. This technique gives an advantage of reducing the leakage current in a path from VDD to ground due to transistors act as a large value resistance by turning off for different input signal combination. In [13], the force stacking concept is introduced by introducing the additional two high threshold transistors in the logic circuit. In force stack concept the leakage current is reduced by increasing the resistance of the leakage path. The drawback of this technique is the low signal is not equal to ground and high is not equal to VDD. Other drawbacks are the propagation delay is increased with reduced output voltage swing and implementing two different threshold voltages on single IC. In [14] three sleep transistors are used in logic circuit for leakage reduction. Among three transistors two NMOS and PMOS transistors have same threshold voltage and third PMOS transistor have high threshold voltage. The connection between pull-up and pull-down networks is connected with high threshold voltage sleep transistor. By breaking the path between pull-up and pull-down networks reduces the leakage current. So this technique needs the controller for automatically controlling and generating sleep signals when required to make the circuit in standby mode and active mode. The need of controller is the drawback of this technique.Xiaying Zhao and Jiangfang[7] leakage power reduction for CMOS combination Circuits. The conventional nand designed is show figure 2.[15]

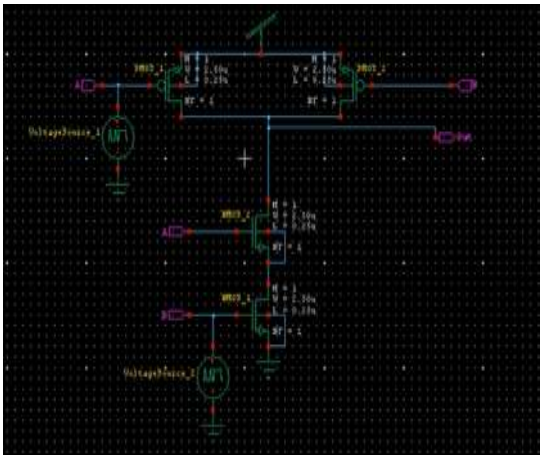

Fig. 2. Conventional NAND gate design

III. PROPOSED ONOFIC APPROACH

The proposed On/Off logic (ONOFIC) approach reduces the leakage current and leakage power with simple and single threshold voltage circuit level approach. The ONOFIC approach efficiently reduces the leakage current in both active and standby mode of logic circuit. It introduced the extra logic between pull-up and pull-down networks for leakage reduction. This additional introduced logic circuit is called as On/Off logic (ONOFIC) circuit. The ONOFIC logic circuit contains one PMOS and one NMOS transistor. The connection of ONOFIC transistors is as shown in Fig. 2. Due to maintaining on or off condition for any output logic level this circuit is called as ONOFIC. This logic directly affects the power dissipation and propagation delay of the logic circuit. ONOFIC circuit uses the logic of force stacking for controlling the leakage current by providing the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state. In ONOFIC block the operation of NMOS transistor is controlled by a PMOS transistor. Depending on the output logic ONOFIC NMOS or PMOS transistors must be in cut-off or in linear mode [16].

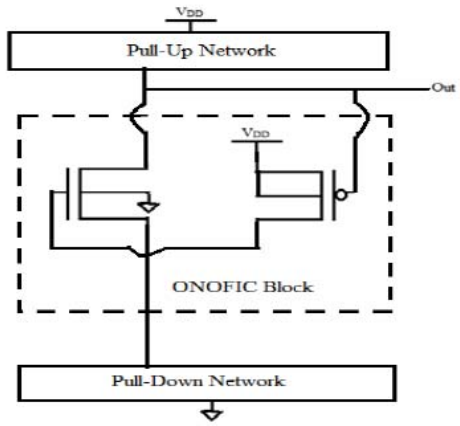

Fig. 3. Schematic of ONOFIC logic

In ONOFIC block, the drain of PMOS transistor is connected to the gate of NMOS transistor and the output is connected to the gate of PMOS transistor. The drain of the pull-down network is connected to the source of NMOS transistor and PMOS source terminal is connected to VDD of the circuit. The NMOS transistor drain is connected to the output of the circuit and the substrate of NMOS transistor is connected to the ground while the substrate of PMOS transistor is connected to the VDD. The ONOFIC CMOS inverter logic is explained in Table I. The main concept of this technique is the property of on/off. The both ONOFIC transistors are in linear region when ONOFIC logic is in on condition while both transistors are in cut-off mode if ONOFIC logic is in off state. This reduces the leakage current at both active and standby mode with accurate logic level at the output. The good conducting path is obtained by turning on the ONOFIC block and it acts as a good resistance to control the leakage current when it is in off state.

The ONOFIC circuit designed in in EDA Tanner Tool As show Fig. 4

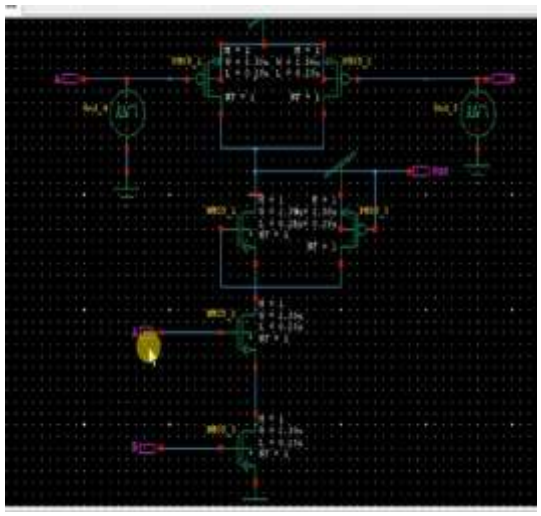

Fig. 4. ONOFIC Approach NAND gate Circuit diagram

TABLE I
THE TRANSISTOR OPERATION OF AN ONOFIC CMOS INVERTER.

Input level	PMOS	ONOFIC PMOS	ONOFIC NMOS	NMOS
Logic low	On	Off	Off	Off
Logic high	Off	On	On	On

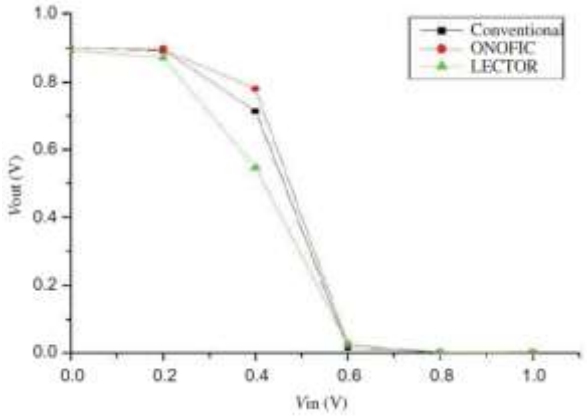

Fig. 5. CMOS inverter DC characteristic.

From Fig. 5 when compared to the other controller circuits the ONOFIC technique uses the same threshold voltage throughout the entire block which can improve the performance of the logic circuits. From the literature survey the LECTOR technique is also used a same threshold voltage throughout the circuit block. The Fig. 3 shows the DC characteristic of three techniques conventional, LECTOR and ONOFIC CMOS inverters. From the Fig. 3 we observed that the DC characteristics of conventional and ONOFIC inverter is similar to each other with large slope when compared to LECTOR CMOS inverter has low slope. Hence, when compared to LECTOR technique ONOFIC technique has less propagation delay and high voltage swing. The output waveforms shown in Fig. 4 are of conventional; LECTOR and ONOFIC CMOS inverter at 32 nm technology shows the reduced leakage power obtained by ONOFIC approach. The slope of the CMOS inverter circuit with any input combination is given as Equation (1),

$$\text{Slope} = \delta V_{out}/\delta V_{in} = \delta(I_{out}R_{out})/\delta V_{in}; \quad (1)$$

$$I_{out} = k/2\,(VT)^2\, e^{(V_{in}-V_{th})/VT}\,(1- e^{-V_{out}/VT}); \quad (2)$$

Here k is device process parameter, VT is voltage temperature. Where Vth is device threshold voltage and which depends on doping densities of the material with material's quality factor, the flat voltage and charge storing capacitances. From the Equations (1) and (2) observed that the large slope is occurred due to large Iout current which leads to large static power dissipation and hence LECTOR technique has low static power dissipation when compared to conventional and ONOFIC approach. Equation (3) gives the propagation delay,

$$t_p = (R_{out}\Delta V_{out})/I_{out}; \quad (3)$$

Where, Rout is the sum of loads of resistive and capacitive of the CMOS circuit. ONOFIC and conventional circuits have less propagation delay when compared to LECTOR technique due to large Iout as observed from Equation (3). Due to less propagation delay the output values obtained quicker when input combination applied. The concept of stacking provides the ONOFIC circuit for controlling leakage current with maximum resistance when it is in off state and minimum resistance when it is in on state. In ONOFIC block, the operation of NMOS transistor is controlled by the PMOS transistor. ONOFIC NMOS transistor mode is depends upon the output logic. The minimum propagation delay is obtained due to fast performance of turning-off and turning on of a PMOS transistor when compared to other techniques.

IV. RESULTS AND DISCUSSIONS

Power Dissipation & propagation Delay of CMOS at Deferent Tech. (All Technology microwatts & PDelay in µWats)

Circuits	90nm	45nm	32nm	45µm
inv_conv	4.019997	1.021826	2.460309	1.0058
inv_lector	3.426373	1.204296	2.639254	1.0288
inv_onofic	4.950182	4.546152	8.994829	1.0109
nand_conv	6.053454	2.003633	4.893321	1.0359
nand_lector	3.621849	2.213076	5.062619	1.0273
nand_onofic	3.780632	5.469471	1.121113	1.0242

The result of 90nm ,45nm and 32nm technologies has got different power consumption as technology goes in reduced accordingly losses are increased so ONOFIC took less propagation delay method is got more advantages[18-21].

V. CONCLUSION

The problem of dissipation power is reduced for different technology, This work addresses the challenge of obtaining of power losses and efficiently use IC's and electronics devices Is applied to solve its energy consumption and performance is improved and it can helpful in power saving in CMOS circuits which has been compared conventional, Lector and ONOFIC method hence the ONFIC method is suitable for design circuits and efficient using EDA tanner tool.

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