Setting up the DBBC3 for DDC_V mode

Version 124 – 17.06.2020

The Control Software is configured with four types of config-files, located in the folder C:\DBBC_CONF:
- The main config file *dbbc3_config_file_ddc_V_124.txt*
- The config-file *config_adb3l.txt* for the initial settings of the ADB3L sampler boards
- The config-file *config_ddc_V.txt* for the initial settings of the DDC units
- one config-file for each Core3H, f.e. *ddc_V_core3H_1.fila10g*

1. Set up the config-file for the Control Software

The config-file for the Control Software is called *dbbc3_config_file_ddc_V_124.txt* located in the folder C:\DBBC_CONF

Line	dbbc3_config_file_ddc_V_123.txt (example)
1	config_adb3l.txt
2	config_ddc_V_12bbc.txt
3	3 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_1.fila10g COM12
4	3 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_2.fila10g COM13
5	30 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_3.fila10g COM14
6	30 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_4.fila10g COM15
7	0 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_5.fila10g COM8
8	0 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_6.fila10g COM9
9	0 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_7.fila10g COM10
10	0 dbbc3_ddc_V_2hv2_8bbc_130518_2.bit ddc_V_core3H_8.fila10g COM11
11	3 4096 10 32000 COM3
12	3 4096 10 32000
13	3 4096 10 32000 COM4
14	3 4096 10 32000
15	0 32000
16	0 32000
17	0 32000
18	0 32000
19	GCAT 2048 10 COM5
20	192.168.0.60
21	224.0.0.255:25000

Line 1: name of the config-file for the ADB3L-sampler settings

Line 2: name of the config-file for the DDC frequency and bandwidth settings

Lines 3-10: configuration settings for the Core3H-Boards, one line per board
- first number indicates status of Board (0 – no board present, 3 – board present and signal connected to corresponding IF, 30 – board present but no signal connected to corresponding IF.
- name of bit-File (Core3H-Firmware, must be located in Folder „C:\DBBC_CONF\FilesDBBC“)
- Core3H config-file containing the configuration settings specific to each Core3H
- COM-Port for serial communication with Core3H-Board

Lines 11-18: configuration for GCoMo IFs:
- type of IF: 3 for GCoMo, 2 for CoMo, 0 if no (G)CoMo present
- synthesizer frequency, **half of LO-frequency,** in MHz
- attenuation of synthesizer frequency in dB
- AGC target reference
- COM-Port for serial communication with synthesizers, one per GCoMo

Line 19: configuration for clock generator:

- clock type (GCAT for Valon synthesizer, CAT3 for internal synthesizer)
- clock frequency in MHz
- reference frequency in MHz (only for GCAT)
- COM-Port for serial communication with synthesizer (only for GCAT)

Line 20: The IP-Address of the DBBC3 (for multicast-support)

Line 21: The IP-Address of the Multicast-Group and Multicast-Port (optional, default is 25000)

2. Setting up the config-file for the ADB3L-Samplers:

The config-file for the ADB3L-Samplers is called *config_adb3l.txt* and is located in the folder C:\DBBC_CONF. It contains the initial sequence for reseting the samplers and configuring the settings for offset, gain and delay.
For the commands see document „ADB3L commands.pdf“.

3. Setting up the config-file for the the BBC-Units:

Each Core3H contains 8, 12 or 16 BBCs depending on the Firmware version used, so there are up to 128 BBCs, numbered from 1 to 128. The distribution of the BBCs on the Core3H is shown in the following table:

Firmware version	**1(IFA)**	**2(IFB)**	**3(IFC)**	**4(IFD)**	**5(IFE)**	**6(IFF)**	**7(IFG)**	**8(IFH)**
8 BBCs	1-8	9-16	17-24	25-32	33-40	41-48	49-56	57-64
12 BBCs	1-8 65-68	9-16 73-76	17-24 81-84	25-32 89-92	33-40 97-100	41-48 105-108	49-56 113-116	57-64 121-124
16 BBCs	1-8 65-72	9-16 73-80	17-24 81-88	25-32 89-96	33-40 87-104	41-48 105-112	49-56 113-120	57-64 121-128

The initial frequency and bandwidth for each BBC that should be used can be set in the config-file *config_ddc_V.txt* or *config_ddc_V_12bbc.txt* The DDC_V version only supports 32 MHz bandwidth.

Line	**config_ddc_V.txt (example)**
1	1 1500.0 32
2	2 2000.5 32
3	3 2500.5 32
4	4 3000.0 32
	...

Each line consists of the BBC-Number, the frequency in range from 0.0 up to 4096.0 MHz and the bandwidth (32) MHz. Lines for unused BBCs can be omitted, they also don‘t need to be in order.

4. Setting up the config-files for the Core3H modules:

There is one config-file for each Core3H, typically named ddc_V_core3H_1.fila10g with the last number in the name indicating the board number.
It contains all necessary commands for initializing the Core3H.

Line	ddc_V_core3H_1.fila10g (example)
1	core3_init
2	core3_mode pfb
3	regwrite core3 0 0x25252525
4	regwrite core3 1 0xBFBFBFBF
5	regwrite core3 9 1
6	reboot
7	inputselect vsi1
8	vsi_samplerate 128000000 2
9	splitmode off
10	reset
11	vdif_frame 2 1 8192 ct=off
12	tengbcfg eth0 ip=192.168.1.30 gateway=192.168.1.1 nm=27
13	tengbarp eth0 3 00:60:dd:44:47:61
14	destination 0 192.168.1.3:46227
15	timesync
16	start vdif
17	sysstat

The lines 12-14 determine the ethernet configuration and need to be adapted to the stations requirements.
Line 12 sets the IP-Address, gateway and netmask for the source, i.e. the Core3H.
Line 13 sets the MAC Address of the target, as required by some recorders.
The second parameter (number 3 in this example) is the least significand byte of the target-IP-Address, that is set in line 14.
Keep in mind that in DDC mode only Ethernet-Port eth0 of the Core3H is used.
For a full list of the commands see document „Core3H commands DDC_V v124.pdf“

5. Starting the Control Software

- Start the control software via the link „DBBC3 Control DDC_V_v124.exe“ on the desktop.
- When asked `"Configure y/n? "` press „y“ if the correct firmware for the Core3H has not yet been loaded, otherwise press „n“, and on the second question `"Initialize ADB3L/Core3H y/n? "` press „y“ to initialize the DBBC3.
- As soon as initialization has finished the console will prompt
`„Waiting for connection on port 4000“`.
- Start the DBBC-client via the link „DBBC client v4.exe“ on the desktop.

6. Checking the system status

a) To check for problems with the board connections, set attenuation of GCoMo to high attenuation to get a low power level, and verify that the power values read from the Core3H don't diverge by more than a factor of 1000 (Example for IF A and Core3H 1):
dbbcifa=2,63
dsc_tp=1
b) Set GCoMo IF to agc and verify that that the attenuation value set by the agc is within range 20-40 (Example for IF A) to get to the TP target of around 32000. It may take some time for the GCoMo to reach the required attenuation:
dbbcifa=2,agc
dbbcifa (to show attenuation value and power level)

c) Check that the sampling clocks are in correct phase relation:
checkphase

If the test is not ok, it may be necessary to reinitialize the system by restarting the control software, selecting „n“ when prompted for `"Configure y/n? "` and „y“ when prompted `"Initialize ADB3L/Core3H y/n? ".` If this doesn't help, it might be required to restart the control software with reloading the firmware. Sometimes a hard reset of the electronics is required.

d) Check if time-synchronization was successful with command:

time

The timestamps should be identical and have the correct GPS time and date. For systems with more than four Boards the timestamps may differ by one second, this is due to the serial connection speed and still correct.

e) Check that the PPS synchronization was successful with the command:

pps_delay

This gives the delay of the generated PPS from the incoming PPS for each Core3H, the value should be below 100 ns.

If it is more, a restart of the control software should be performed.