Setting up the DBBC3 for OCT_D v120

author: Sven Dornbusch, dornbusch@mpifr-bonn.mpg.de 27.09.2021

The Control Software is configured with three types of config-files located in the folder C:\DBBC_CONF\OCT_D_120\:
- The main config file *dbbc3_config_file_oct_D_120.txt*
- one config-file for each Core3H, f.e. *oct_D_core3H_1.fila10g*
- The filter files with the coefficients (file ending *.flt)

(In earlier version these config files were located in the folder C:\DBBC_CONF, but improve the overview starting with OCT_D version 120 these files will be located in a separate subfolder.)

The config-file *config_adb3l.txt* for the initial settings of the ADB3L sampler boards is located in the folder C:\DBBC_CONF\ because it is shared between all observation modes.

1. Setting up the main config-file for the Control Software

The main config-file for the Control Software is called *dbbc3_config_file_oct_D_120.txt* and is stored in the folder C:\DBBC_CONF\OCT_D_120\

Line	dbbc3_config_file_oct_D_120.txt (example)
1	config_adb3l.txt
2	3 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_1.fila10g COM3
3	3 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_2.fila10g COM4
4	30 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_3.fila10g COM5
5	30 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_4.fila10g COM6
6	0 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_5.fila10g COM7
7	0 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_5.fila10g COM8
8	0 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_5.fila10g COM9
9	0 dbbc3_oct_D_2hv2_270921.bit oct_D_core3H_5.fila10g COM10
10	3 4500 10 32000 COM11
11	3 4500 10 32000
12	3 4500 10 32000 COM12
13	3 4500 10 32000
14	0 28000
15	0 28000
16	0 28000
17	0 28000
18	CAT3 2048
19	134.104.30.223
20	224.0.0.255:25000
21	10

Line 1: name of the config-file for the ADB3L-Samplers

Lines 2-9: configuration for the Core3H-Boards (one line for each board)

- first number indicates status of Board:
  0 – no board present
  3 – board present and signal connected to corresponding IF
  30 – board present but no signal connected to corresponding IF.
- name of bit-File (Core3H-Firmware, must be stored in Folder „C:\DBBC_CONF\ FilesDBBC“)
- name of corresponding config-file for the Core3H
- COM-Port for serial communication with Core3H-Boards

Lines 10-17: configuration for GCoMo IFs:

- type of IF:
  3 for GCoMo,
  2 for CoMo,
  0 if not present
- synthesizer frequency, **half of LO-frequency,** in MHz
- attenuation of synthesizer frequency in dB
- AGC target reference
- COM-Port for serial communication with synthesizers, one per GcoMo

Line 18: configuration for clock generator:

- clock type (GCAT for Valon synthesizer, CAT3 for internal synthesizer)
- clock frequency in MHz
- reference frequency in MHz (only for GCAT)
- COM-Port for serial communication with synthesizer (only for GCAT)

Line 19: IP address of the DBBC3, needed for multicast transmission

Line 20: Multicast group address and port used for multicast transmission

Line 21: number of times the initial phasecheck is performed

2. Setting up the config-files for the Core3H:

There is one config-file for each Core3H, typically named oct_D_core3H_1.fila10g with the last number in the name indicating the board number.

An example config file is shown below:

```
reboot
core3_init
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbcfg eth1 ip=192.168.1.17 gateway=192.168.1.1 nm=27
tengbcfg eth2 ip=192.168.1.18 gateway=192.168.1.1 nm=27
tengbcfg eth3 ip=192.168.1.19 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:44:47:60
tengbarp eth1 3 00:60:dd:44:47:61
tengbarp eth2 4 00:60:dd:44:0b:8a
tengbarp eth3 5 00:60:dd:44:0b:8b
destination 0 192.168.1.2:46220
destination 1 none
destination 2 192.168.1.4:46222
destination 3 none
timesync
start vdif
sysstat
```

It contains all necessary commands for initializing the Core3H, and is used to configure the required vdif-format and the ethernet setup.

In version 120 a lot of the initial commands in the config file have been removed.
So if the configuration from a config-file of a previous version is used as a base for the v120 config files, only the commands for the ethernet configuration should be copied over.
The vdif_frame command can be left out as shown above if the standard setup of 2 bits, 1 channel and 8192 bytes frame size is used.

For the commands see document „Core3H commands OCT_D v120.pdf“

3. Starting the Control Software

1. Start the control software via the link „DBBC3 Control OCT_D_v120“ on the desktop.
2. When asked `"Configure y/n? "` press „y“ if the correct firmware for the Core3H has not yet been loaded, otherwise press „n“, and on the second question `"Initialize ADB3L/Core3H y/n? "` press „y“ to initialize the DBBC3.
3. As soon as initialization has finished the console will prompt „`Waiting for connection on port 4000`“.
4. Start the DBBC-client via the link „DBBC client v4.exe“ on the desktop or connect via a remote client or FS (field system).

4. Loading the filter coefficients:

Loading the filter coefficient manually is only necessary if the default EHT setup is not used, which is loaded automatically by the Control Software during startup.

The default EHT setup uses a 2-4 GHz taps for filter 1, and a 0-2 GHz taps for filter 2.

Each Core3H board has two 64tap-FIR filters. The first filter is sending its data stream to eth0 and eth1 (copy), the second filter is sending its data stream to eth2 and eth3 (copy).

The filter coefficients can be loaded with the command:
tap=board_nr,filter_nr,filtername.flt
board_nr (1-8) Number of Core3H
filter_nr (1-2) Number of Filter
filtername.flt Name of the file with the filter taps (located in C:\DBBC_CONF\OCT_D_120\)

5. Checking System Status

1. Check that all IFs with an input connected have enough power and enough dynamic range.
   This can be done with the commands:
   dbbcifa, dbbcifb, dbbcifc, ... dbbcifh
   The power level should be around 32000 (plus/minus 1000)
   and the gain level between 20-40.
2. Check the sampler statistics for each used board with the command:
   samplerstats=board_nr
   All sampler statistics (powerlevel, offset and phase delay) are printed out and validated.
   If a value is marked as not ok the issue should be investigated. Small deviations in power or offset could be fixed by recalibration or ignored if small enough.
   If the delay values show [NOT OK], the command:
   checkphase=board_nr
   must be used to verify that the sampler is still synced, otherwise a restart of the control software might be necessary.
3. Check the filter statistics for each boards with the command:
   core3hstats=board_nr
   The bit statistics for each filter should have the pattern 18/32/32/18 with only 1-2% deviation.
4. Check that the delay between external and internal 1PPS is in a reasonable range (<100ns):
   pps_delay