JTAG introduction

2019-09-13

1 About

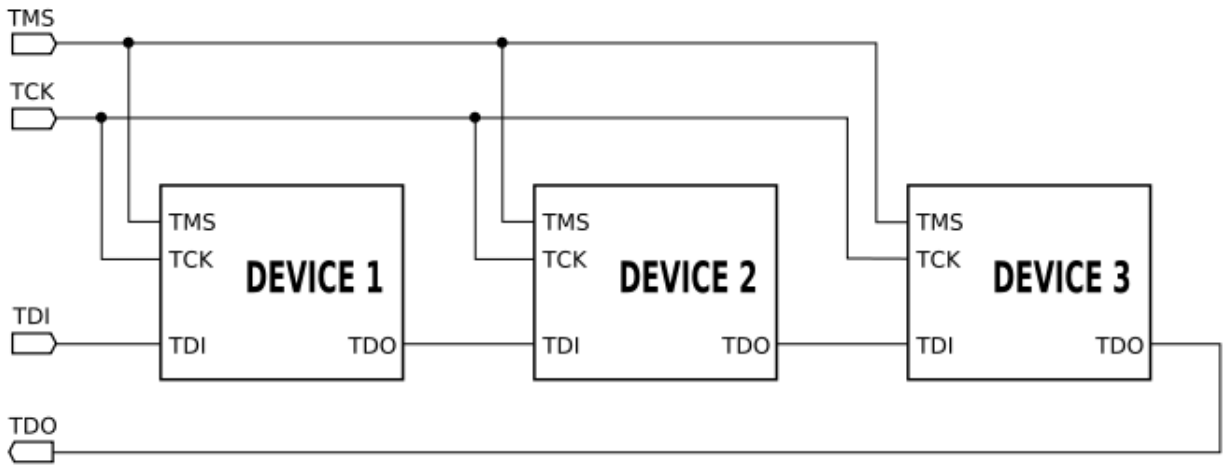
JTAG (Joint Test Action Group) is a standard for testing and verifying printed circuit boards.

It allows access to internal registers of a device and has multiple applications: debugging, programming, testing, etc.

2 Connections

A JTAG compliant device presents at least one TAP (Test Acces Port). The daisy-chained JTAG (IEEE 1149.1) uses the following signals:

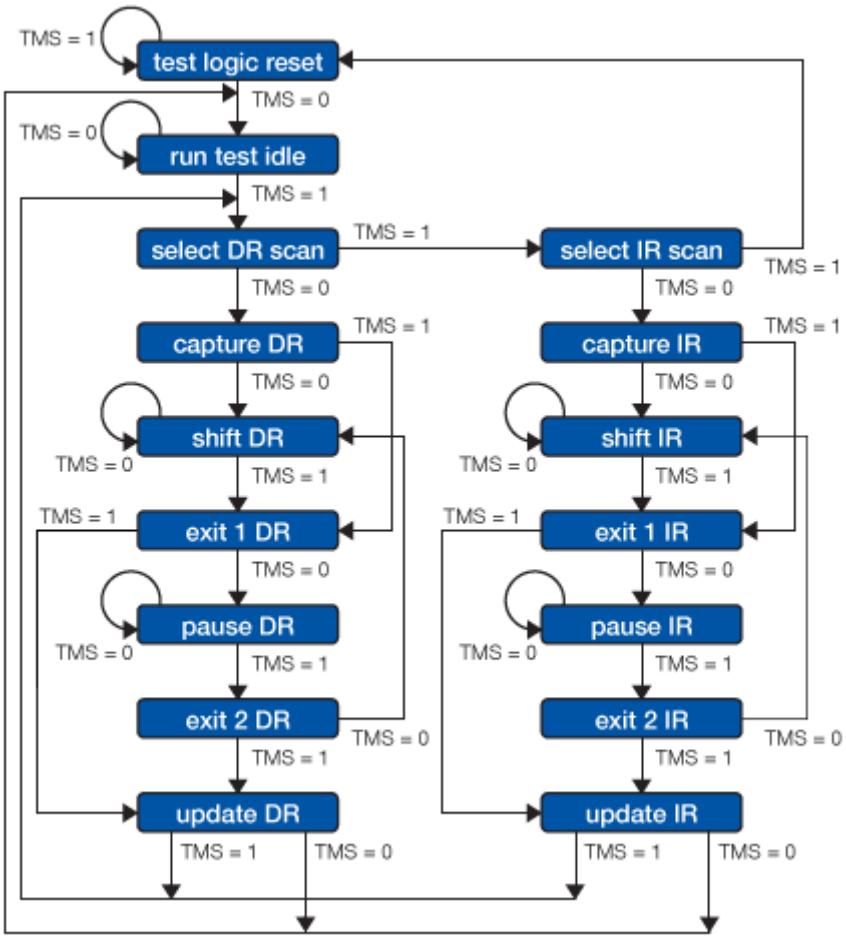
- **TDI**: Test Data In
- **TDO**: Test Data Out
- **TCK**: Test Clock
- **TMS**: Test Mode Select
- **TRST**: Test Reset (optionnal)



Multiple TAPs can be chained by connecting the TDI and TDO together.

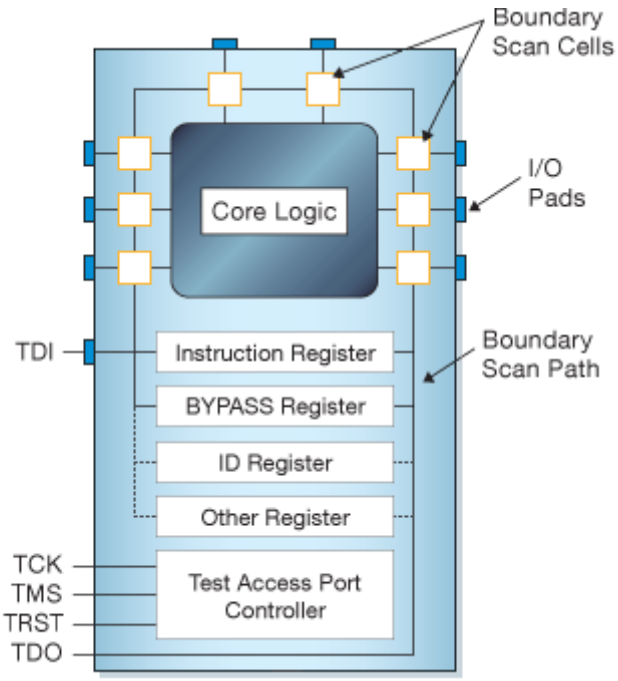
3 TAP controller

The behaviour of the JTAG system is controlled by an internal state machine. The transitions are decided by the TMS signal, sampled by the TCK clock.



4 Registers and instructions

Operating the state machine allows accessing the TAP internal registers.



4.1 Instruction register

The instruction register can be small (a few bits, the RISC-V debug specification demands at least 5 bits for example). It contains the opcode of the current instruction. Each instruction can be associated with a data register.

Except for BYPASS and EXTEST, the exact opcodes are defined by the TAP implementor.

The IR is directly manipulated by the state machine and other data registers are accessed through it.

4.2 IDCODE

This instruction is associated with a 32-bit register which contains a manufacturer code, a part number and a part version code.

4.3 BYPASS

An opcode of all ones must implement this instruction.

The associated register is only 1-bit wide and has no effect. It is used to bypass the TAP.

4.4 Other

Other instructions and associated registers can be defined by the TAP implementor, so other features can be implemented, like debugging or data access.

These instructions are specific to each device.

4.5 Boundary scan

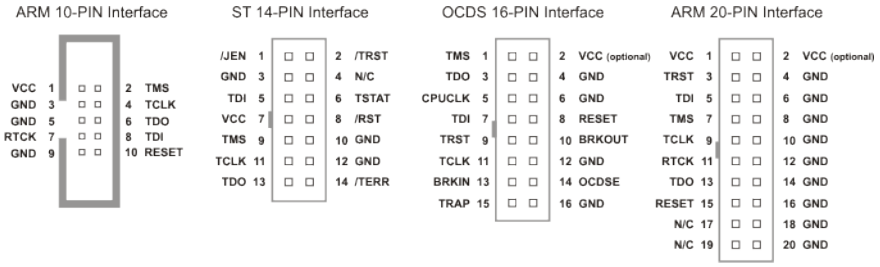
A TAP may or may not implement the Boundary Scan feature.

The boudary scan cells and some instructions provide access to the device's I/Os in a path around the device's boundary. It is possible to read and write the values of individual pins.

5 In practice

5.1 Connectors

There is no standard JTAG connector. Existing connectors depend on the manufacturer. They have various pinouts, forms, and sizes.



5.2 USB

It is possible to use USB to access a JTAG scan chain. The converter circuitry can be mounted on the cable or integrated in the PCB.

5.3 Bit banging

Due to the low complexity of the TAP controller state machine, it is possible to bit-bang the JTAG interface. OpenOCD has a *sysfsgpio* driver that does it using gpio lines via sysfs.

6 References

https://en.wikipedia.org/wiki/JTAG

https://standards.ieee.org/standard/1149_1-2013.html

https://www.xjtag.com/about-jtag/jtag-a-technical-overview/

https://blog.senr.io/blog/jtag-explained

http://openocd.org/doc/doxygen/html/sysfsgpio_8c.html#details