COL215 Hardware Assignment 1

~by Adithya Bijoy and Anish Banerjee

(2021CS10571 and 2021CS10134)
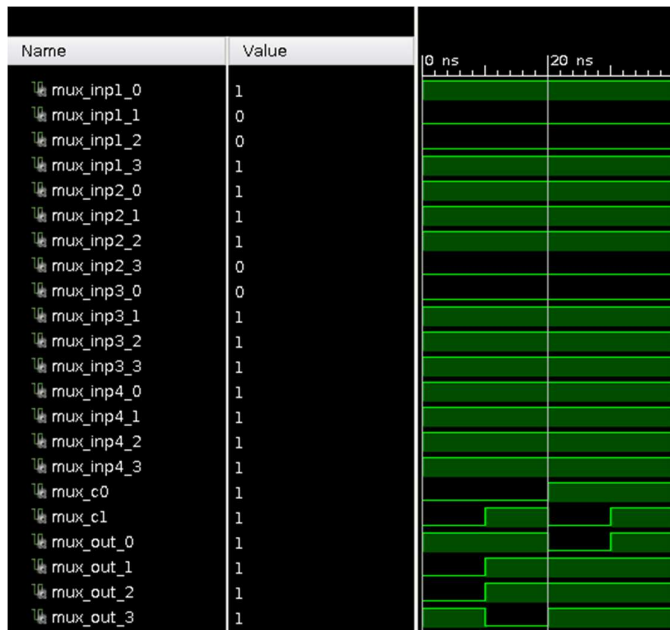
Design Decisions and Lab Work

We began by making the seven-segment decoder, MUX and timing circuit in separate modules. Then we imported them as components in a file to combine them and make the final design.

In the lab, we programmed our device and tried some inputs. The snapshots of the outputs obtained have been attached below.
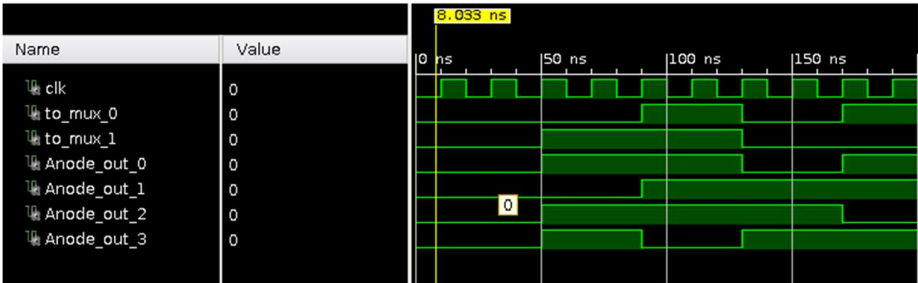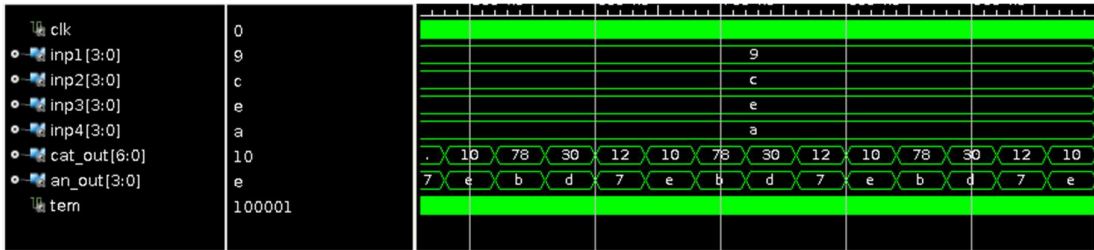
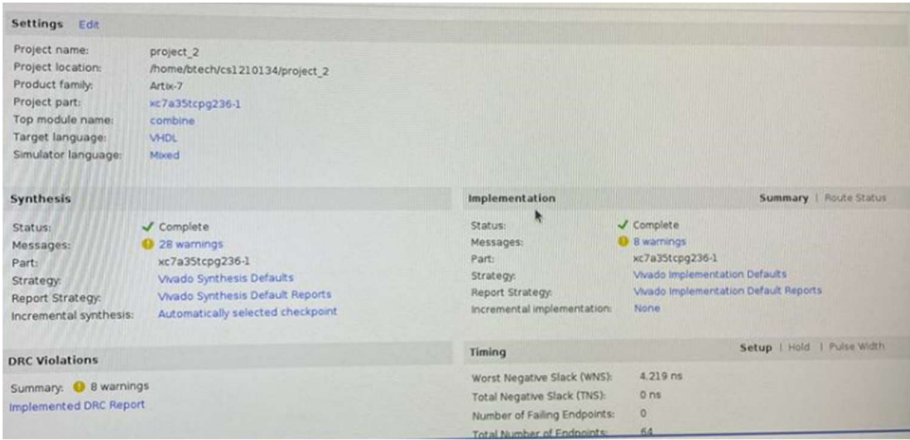## Simulator for Decoder
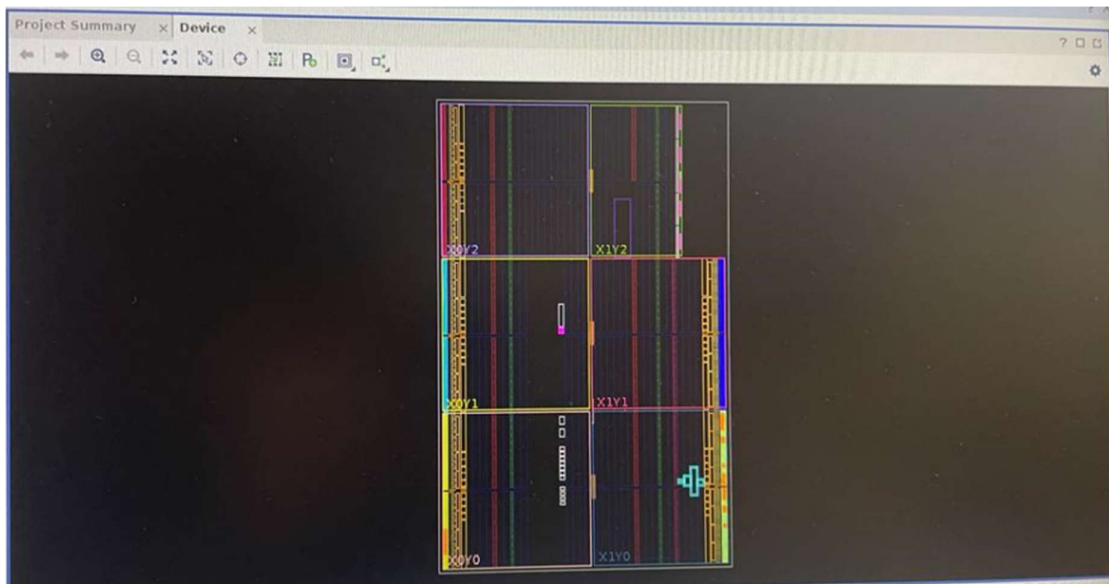

Simulator for MUX

Simulator for Timing Circuit

8.033 ns

Name	Value
clk	0
to_mux_0	0
to_mux_1	0
Anode_out_0	0
Anode_out_1	0
Anode_out_2	0
Anode_out_3	0

0 ns   50 ns   100 ns   150 ns

0

Simulator for combine

	Value
clk	0
inp1 [3:0]	9
inp2 [3:0]	c
inp3 [3:0]	e
inp4 [3:0]	a
cat_out [6:0]	10
an_out [3:0]	e
tem	100001

9
c
e
a

cat_out: . 10 78 30 12 10 78 30 12 10 78 30 12 10
an_out: 7 e b d 7 e b d 7 e b d 7 e

Synthesis Report

Settings Edit

Project name:	project_2
Project location:	/home/btech/cs1210134/project_2
Product family:	Artix-7
Project part:	xc7a35tcpg236-1
Top module name:	combine
Target language:	VHDL
Simulator language:	Mixed

Synthesis

Status:	✓ Complete
Messages:	ⓘ 28 warnings
Part:	xc7a35tcpg236-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	Automatically selected checkpoint

Implementation   Summary | Route Status

Status:	✓ Complete
Messages:	ⓘ 8 warnings
Part:	xc7a35tcpg236-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: ⓘ 8 warnings
Implemented DRC Report

Timing   Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	4.219 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	64

DRC Violations

Summary: ⓘ 8 warnings
Implemented DRC Report

Timing   Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	4.219 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
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Implemented Timing Report

Utilization   Post-Synthesis | Post-Implementation

Graph | Table

LUT 1%
FF   1%
IO   26%
BUFG 3%

0   25   50   75   100
Estimated Utilization (%)

Power   Summary | On-Chip

Total On-Chip Power:	0.083 W
Junction Temperature:	25.4 °C
Thermal Margin:	59.6 °C (11.9 W)
Effective θJA:	5.0 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Snapshots of Working of the Implementation