COL215 Hardware Assignment 3

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(2021CS10571 and 2021CS10134)

Our approach

We began by making the MAC. The MAC takes two bits, a counter, clock and cntrl as input. The accumulator is set to zero when the cntrl input is 1.

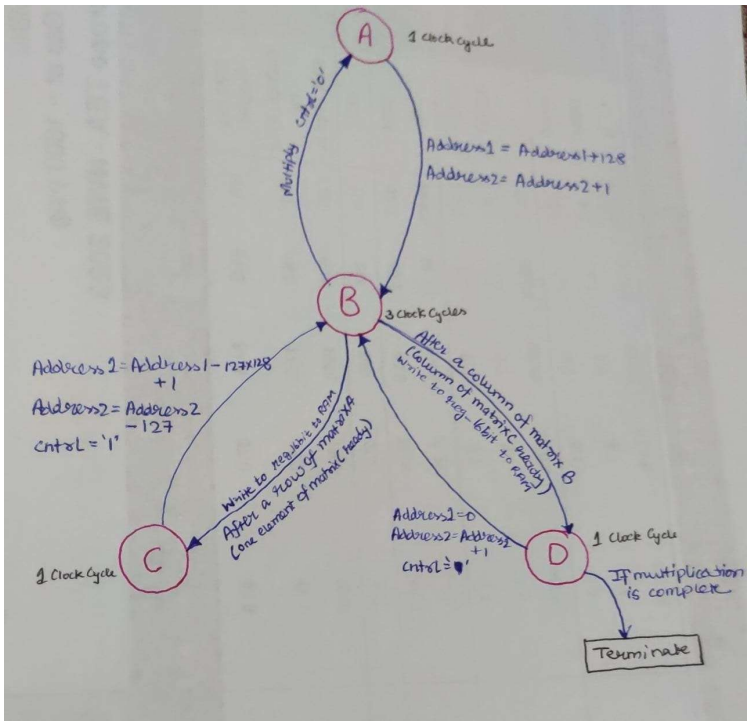
Then we proceeded to make 2 ROM blocks, a RAM block and 8bit and 16 bit registers.

We made an FSM to take the inputs from the ROM and give it to the multiplier. The finite state machine has a counter and 4 states-> A, B, C, D. We complete a single multiplication in 4 clock cycles. We start with state B. When the state transition happens from state B to state A (after 3 clock cycles), the current value is fed to the multiplier and the cntrl bit is set to 0 (if it was 1 before). When the state changes from A to B, the addresses from which the input is taken from the ROM are changed.

This cycle repeats 128 times after which, the state changes to C. One element in the product matrix is computed, which is written to the register, which in turn writes it to the RAM. When the state transition from state C to state B happens (after 1 clock cycle), the addresses from which the input from ROM is taken changes and the cntrl bit is set to 1.

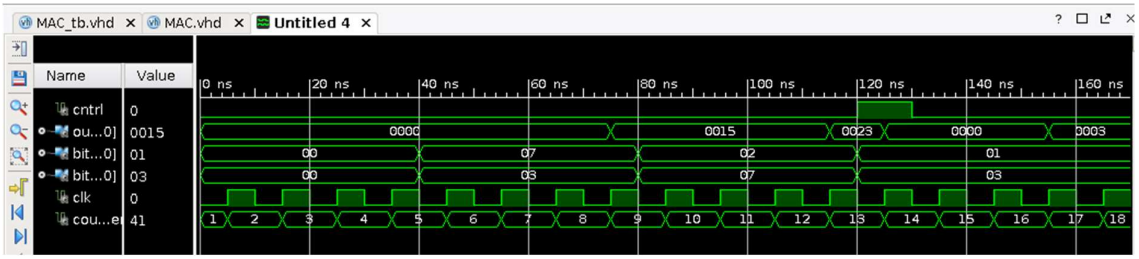
This entire process of going in a cycle of (A->B, B->A) 128 times and then going to C repeats 128 times. Then the state is changed to D (where the address is changed and the cntrl bit is again set to 1) and then again set to B. The entire process repeats 128 times to complete the multiplication.

Here is the image of out FSM

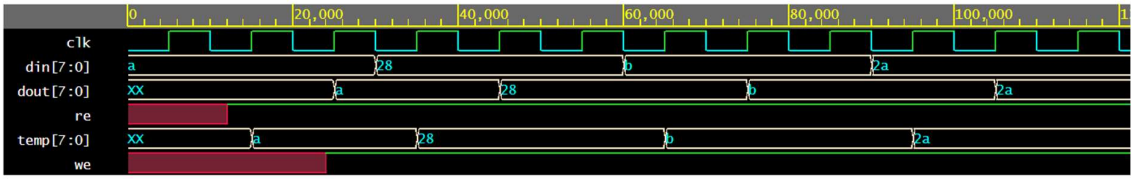


Simulations

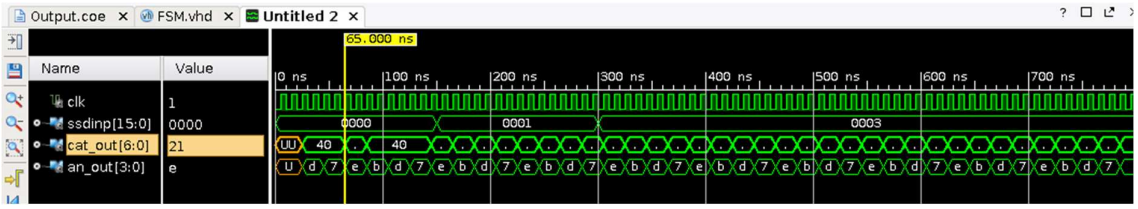
MAC Simulation



Register Simulation

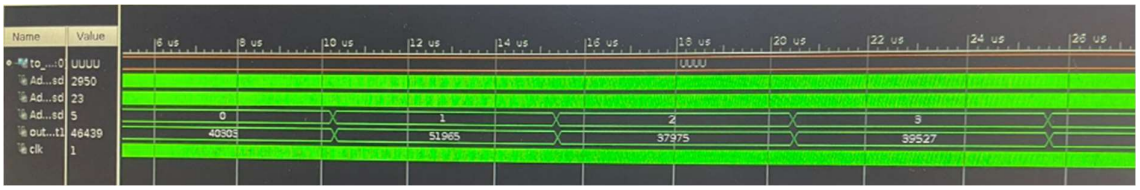


Reader (This was integrated into the FSM)



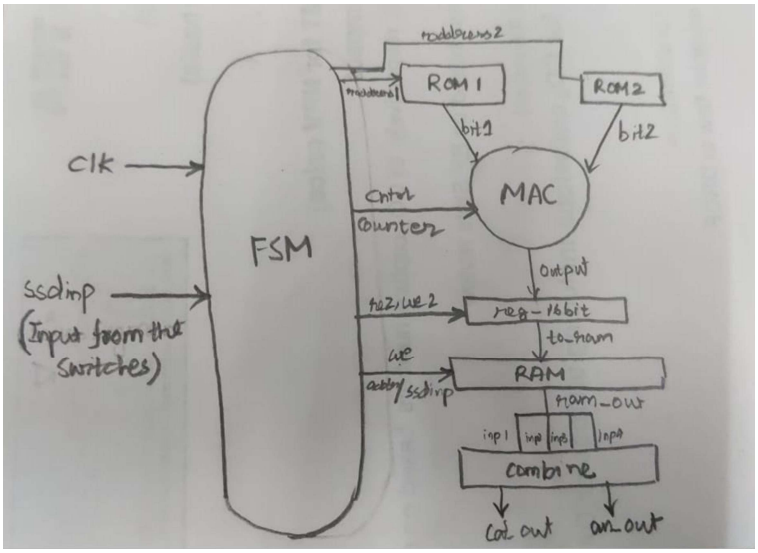
The role of this was to take the input from the switches and give the corresponding value stored in the RAM.

FSM Simulation



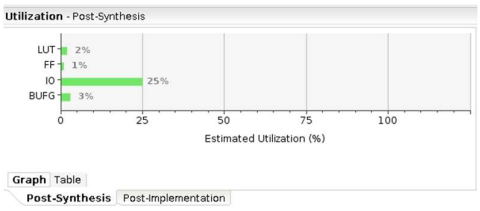
Final Simulation

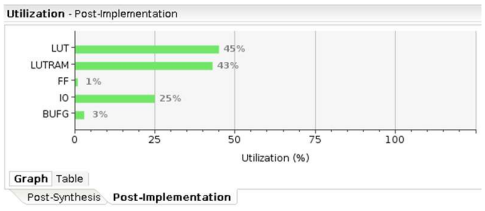
Block Diagram

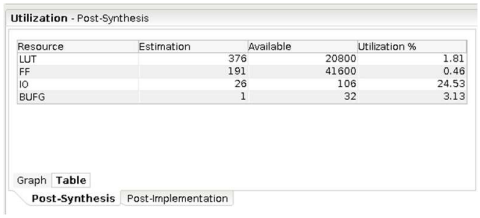


Here, combine is the same module that we used in our assignment 1 (7 Segment Display).

Synthesis Report



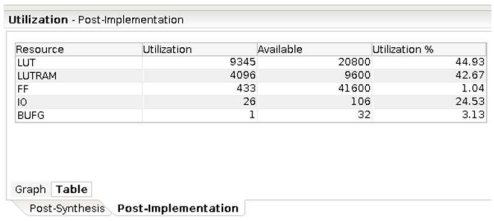




Utilization - Post-Synthesis

Resource	Estimation	Available	Utilization %
LUT	376	20800	1.81
FF	191	41600	0.46
IO	26	106	24.53
BUFG	1	32	3.13

Graph Table
Post-Synthesis Post-Implementation



Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	9345	20800	44.93
LUTRAM	4096	9600	42.67
FF	433	41600	1.04
IO	26	106	24.53
BUFG	1	32	3.13

Graph Table
Post-Synthesis Post-Implementation