

Digital Logic and System Design

4. Gate-level Minimisation

COL215, I Semester 2022-2023

Venue: LHC 111

'E' Slot: Tue, Wed, Fri 10:00-11:00

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Optimising a Gate-level Implementation

- Improving a gate-level design
- Objective?
 - Area
 - Delay
 - Power/Energy
 - Temperature
 - Testability/Reliability/Security/...
- Smaller is better
 - Always?

Literal Count

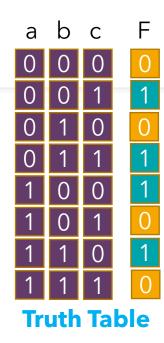
- Optimal circuit: minimum number of literals
- Focus on Area
 - #literals proportional to #transistors
- Simplification in using Literals:
 - Ignoring complement operations
 - Ignoring wires
 - Ignoring blank spaces
 - Ignoring transistor dimensions

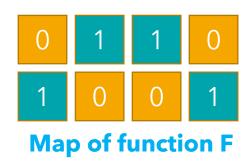
Circular Design Flow

- Literal Count useful in spite of limitations
 - Fast decisions
 - Don't need to generate full gate-level circuit, physical layout
- Gate-level decision
 - depends on geometry
 - ...which depends on gate-level decision 😁
- Fast estimates are critical!

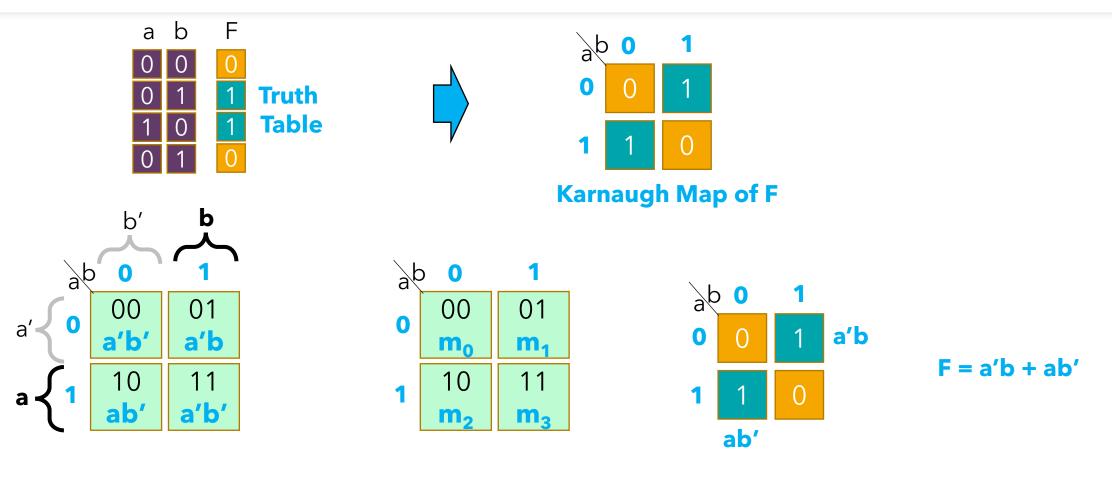
Logic minimisation

- Optimization by applying Boolean Algebra theorems
 - Problem: in what order?
- Map method (Karnaugh Map or K-Map)
 - Pictorial representation of Truth Table
 - 2ⁿ squares/cells for n-variable function
 - one square for each input combination (truth table row)
 - value = 1 if corresponding minterm included in function
 - otherwise, value = 0

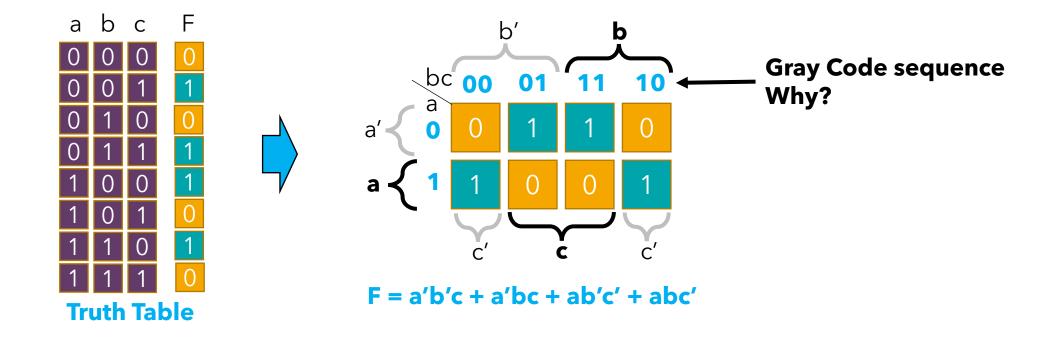




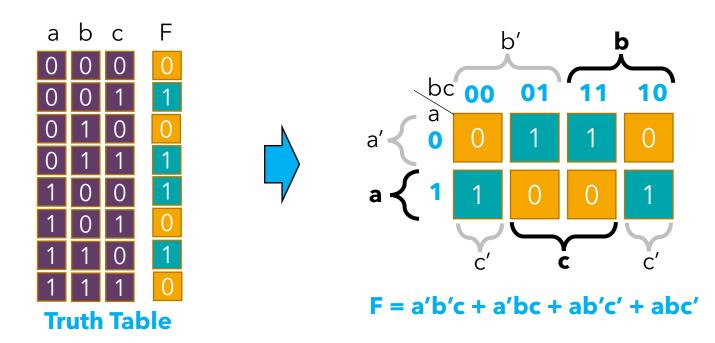
2-variable Karnaugh Map

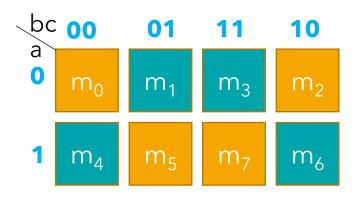


3-variable Karnaugh Map



3-variable Karnaugh Map





$$F = m_1 + m_3 + m_4 + m_6$$

= $\sum (1,3,4,6)$