Basics of ESD Protection (TVS) Diodes

Outline:

This document describes electrostatic discharges (ESD)/ESD tests (operation of MM/HBM/CDM/IEC61000-4-2)/operation of ESD protecting diodes (ESD pulsing/normal operation)/selection methods/caution in designing (laying out) boards/Maximum ratings/electrical properties as described in the datasheet.

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1. Introduction

Electronic devices are becoming increasingly versatile, faster, and smaller. To meet their requirements, semiconductor manufacturers steadily improve the performance and reduce the size of semiconductor devices for electronic applications by shrinking process geometries and increasing the dopant concentration. Because of the downscaling of the process and the ever-higher dopant concentration, semiconductor devices are becoming less immune to electrostatic discharge (ESD) damage. Unless countermeasures are taken, electronic devices are susceptible to degradation and damage due to ESD. In addition, electronic devices are subject to increasing exposure to ESD events as USB, LAN, and other cables are frequently plugged and unplugged for data communication with IoT and other devices and battery recharging.

To protect against ESD, it is therefore becoming essential to add ESD protection diodes to USB, HDMI, and other external ports as well as to the parts that might come into contact with or close to the human body or any manufacturing system during production.

2. What is an ESD?

Static electricity is the charge generated on the surface of dielectric materials. Static electricity is discharged when positively and negatively charged objects are brought into contact with or close to each other. This phenomenon is called an electrostatic discharge (ESD). When a charged human body touches an electronic device, the resulting ESD can be several thousand volts.

2.1. Why does static electricity occur?

When two different objects are rubbed together, brought into contact with each other, or separated from each other (e.g., when plastic wrap is unrolled), electrons may move from one object to the other. Some materials tend to lose electrons and become positively charged while others tend to receive electrons and become negatively charged. A list of materials arranged according to the tendency to gain or lose electrons easily is called the triboelectric series. The farther away two materials are from each other on the triboelectric series, the greater the charge transferred when they are brought into contact with each other. All materials consist of atoms, which normally have an equal number of positively charged protons and negatively charged electrons, making them electrically neutral. For example, friction causes electrons to move from one object to the other, creating an imbalance of positive and negative charges.

Figure 2.1 Triboelectric series

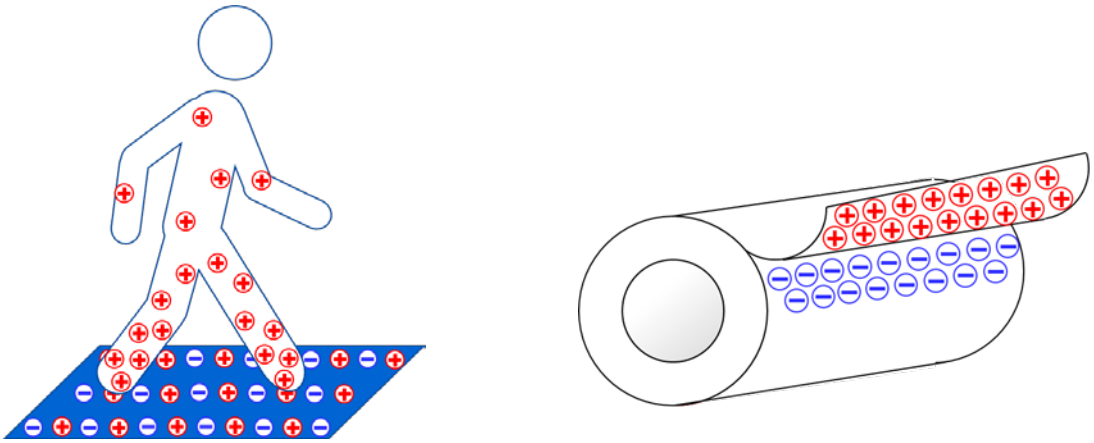


Figure 2.2 How static electricity occurs

2.2. Why are ESD protection devices necessary?

Semiconductor manufacturers have continually developed new processes with ever-smaller geometries to improve the performance and reduce the size of semiconductor devices for electronic applications. There is a law regarding transistor scaling, which states that scaling the size of transistors to 1/k reduces their area to $1/k^2$, power consumption to 1/k, and circuit delays to 1/k. According to this scaling law, geometry scaling helps reduce the size and power consumption and improve the performance of semiconductor devices.

However, when the width and the length are scaled to 1/k, the thickness is also generally scaled proportionally. This means that the thickness of the insulation film used for semiconductor device fabrication is also reduced to 1/k. Silicon oxide (SiO_2) is commonly used as an insulator for silicon semiconductor devices. SiO_2 exhibits a dielectric strength of 8 to 10 MV/cm, which is constant per centimeter. Therefore, when the thickness of an insulation film is reduced to 1/k, its dielectric strength is reduced to 1/k.

The shrinking of semiconductor processes described above is just one of the factors that make semiconductor devices more susceptible to static electricity. Reducing the size and improving the performance of semiconductors and other electronic components exacerbate the effect of ESD. Various factors also complicate ESD protection, including the size reduction of electronic devices themselves.

Furthermore, the way in which people use electronic devices has considerably changed. Since most electronic devices were stationary devices used only at home twenty years ago, their cables were rarely reconnected. At present, however, USB and LAN cables are plugged into and unplugged from smartphones, notebook PCs, and other mobile devices many times a week for battery recharging and data communication.

As described in the previous subsection, ESD can be introduced into an electronic device when it is brought into contact with or close to another object. In other words, nowadays, electronic devices are exposed to ESD more frequently.

Because of a decrease in ESD immunity and an increase in the number of ESD strikes, electronic devices have an increased risk of being degraded by ESD events. It is therefore becoming more important to use ESD protection devices than ever before.

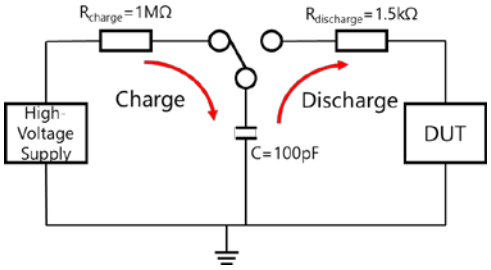
2.3. ESD and surge tests (electrostatic breakdown and surge immunity tests)

ESD and surge tests are broadly divided into device- and system-level tests.

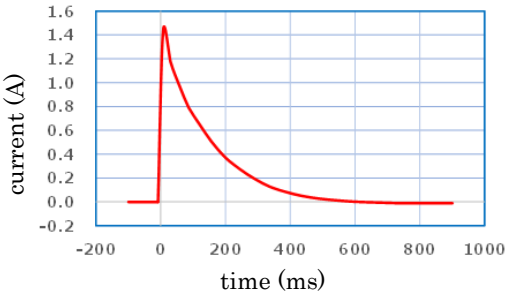
2.3.1. Device-level tests

Device-level tests model a factory or similar environment to ensure that unmounted semiconductor devices are not degraded or destroyed by ESD pulses in places where ESD is controlled. There are three major ESD models:

1. Human body model (HBM): Models a discharge that might occur when a charged human touches a device
2. Machine model (MM): Models a discharge that might be released from charged machines such as manufacturing systems
3. Charged-device model (CDM): Models a discharge that might occur when a charged electrically isolated device touches an earthed circuit board during assembly

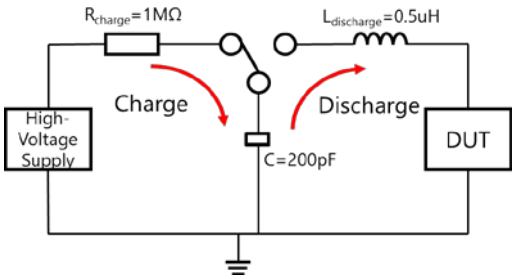


Test circuit example

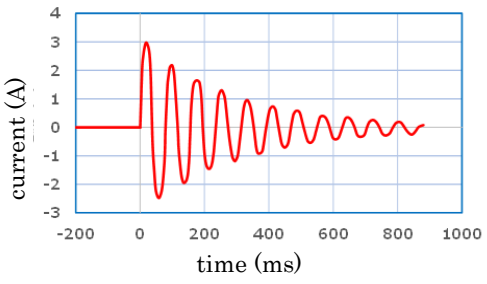


Test waveform example

Figure 2.3 Human body model (HBM)

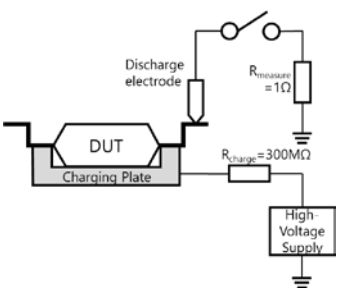


Test circuit example

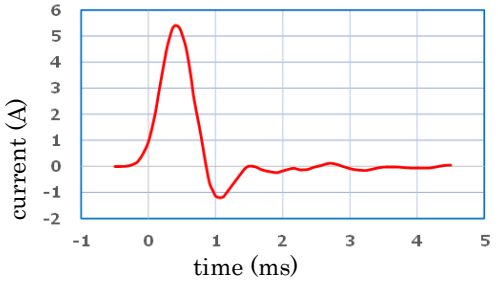


Test waveform example

Figure 2.4 Machine model (MM)



Test circuit example



Test waveform example

Figure 2.5 Charged-device model (CDM)

2.3.2. System-level tests

This test is designed to ensure that electronic systems will not be degraded or destroyed by ESD in the everyday environment.

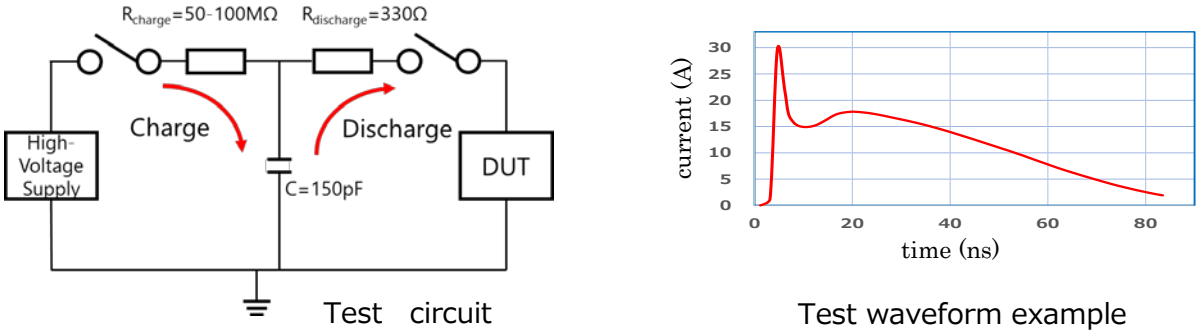
1. IEC 61000-4-2 (ESD immunity test: Human body model)

As is the case with the HBM, this test simulates a discharge that might be released from a charged human body. Two methods are used for ESD testing:

- Direct discharge: Tests a discharge that might occur when a human directly touches an exposed metal surface of a system or a device.
- Air discharge: Tests a discharge that might occur between a device under test (DUT) and a discharge gun through an air layer when the surface of a system or a device is coated with resin or other coating materials.

These ESD tests are stipulated in IEC 61000-4-2 from the International Electrotechnical Commission (IEC).

Toshiba's ESD protection (TVS) diodes are tested using both the direct and air discharge methods.



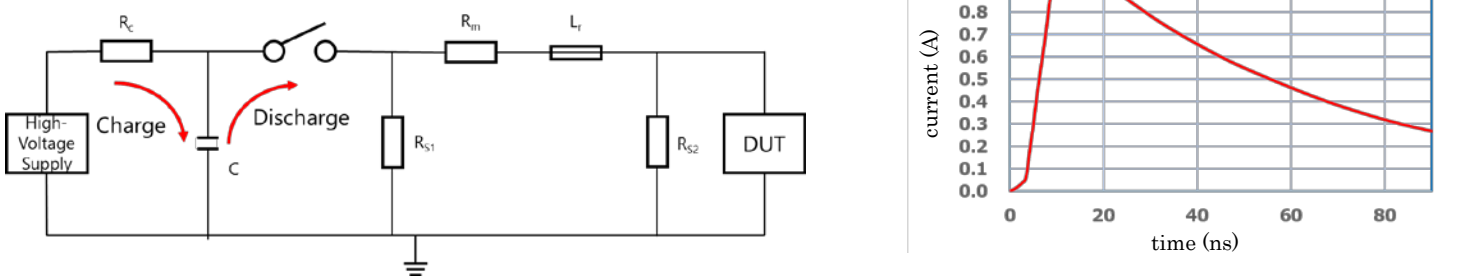
Test circuit　　Test waveform example

Figure 2.6 IEC 61000-4-2 test

2. IEC 61000-4-5 test (Surge immunity test: Lightning surge test)

Also known as a lightning surge test, a surge immunity test models voltage and current surges induced by a nearby lightning strike. This test also includes transient switching phenomena such as a sharp load variation and a load short circuit that might occur when the power switch is turned on. IEC 61000-4-5 test is the most stringent system-level surge immunity test in terms of the level and cycle time of the surge current applied.

The surge immunity test is stipulated in IEC 61000-4-5.



Test circuit example　　Test waveform example

Figure 2.7 IEC 61000-4-5 test

3. ESD protection diodes

3.1. Classification of diodes

Diodes are broadly classified into two types: p-n diodes based on the p-n junction formed by p-type and n-type semiconductors and metal-semiconductor diodes (commonly known as Schottky barrier diodes or SBDs) formed by the junction of a metal with either an n-type or p-type semiconductor.

ESD protection (TVS) diodes are designed based on constant-voltage diodes, a type of p-n diodes, specifically to protect devices from ESD.

The following subsections describe basic p-n diodes and the characteristics unique to ESD protection diodes.

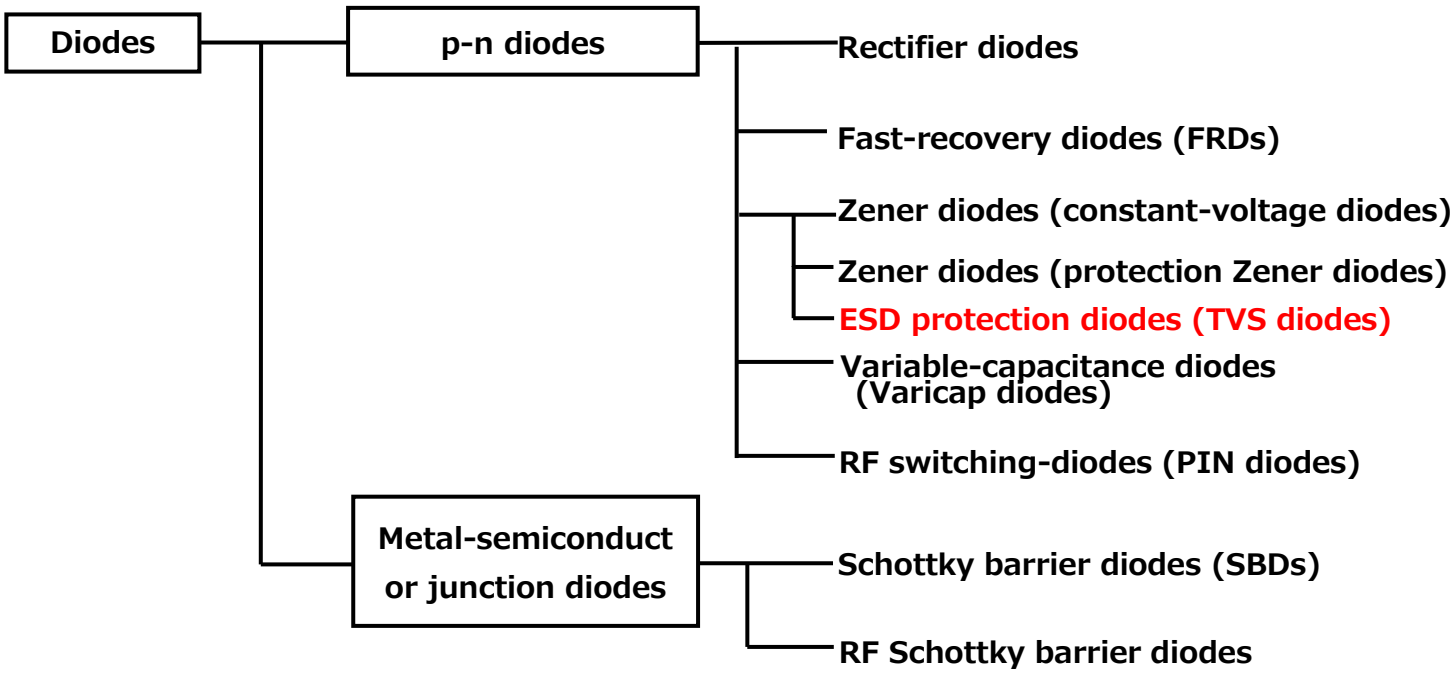


Figure 3.1 Example of diode classification

3.2. p-n diodes

A p-n diode is a diode formed by the junction of p-type and n-type semiconductors.

- p-type semiconductor: A p-type semiconductor is created by doping an intrinsic silicon semiconductor with boron (B) or other impurity elements and has a hole concentration larger than its electron concentration.
- n-type semiconductor: A n-type semiconductor is created by doping an intrinsic silicon semiconductor with phosphor (P) or other impurity elements and has an electron concentration larger than its hole concentration.

A p-n diode conducts when it is forward-biased (i.e., the P-terminal is positively biased relative to the N-terminal). The p-n diode does not conduct when it is reverse-biased (i.e., when the N-terminal is positively biased relative to the P-terminal). When the reverse bias is increased and reaches the reverse breakdown voltage (V_{BR}), the reverse current begins to increase suddenly.

ESD protection diodes are mainly used in the reverse breakdown and non-conductive states.

In the non-conductive state, a depletion region described in the next subsection (also known as a depletion layer) affects the characteristics of an ESD protection diode.

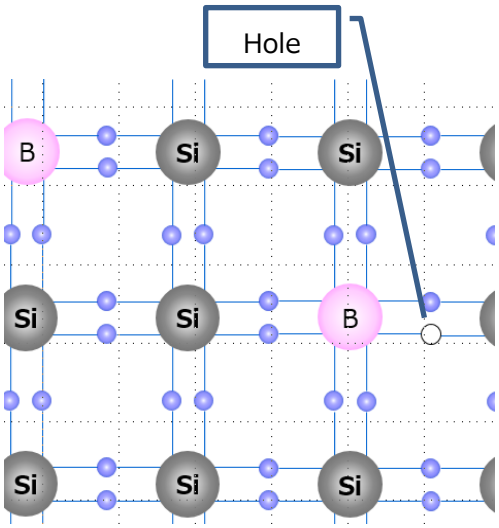


Figure 3.2 p-type semiconductor

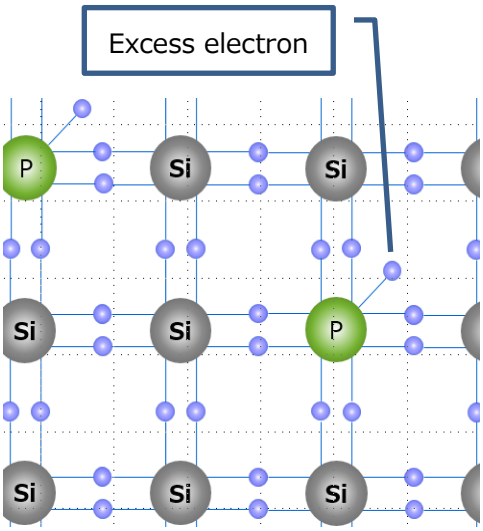


Figure 3.3 n-type semiconductor

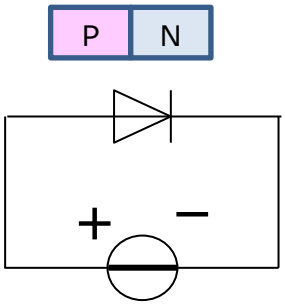


Figure 3.4 Forward biasing

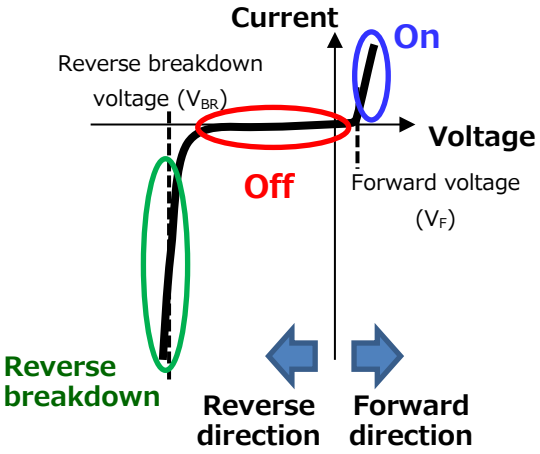


Figure 3.5 Conductive (on) and non-conductive (off) states of an ESD

3.3. ESD protection diodes

This section describes the operation of ESD protection diodes.

While no ESD pulse is being introduced into a system (i.e., while a system is in normal operation), ESD protection diodes should ideally be disconnected from a device under protection (DUP) so as not to affect its operation. The cathode and anode of each ESD protection diode are connected to a signal line and GND respectively as shown below. When ESD protection diodes are connected in this manner, they do not act as transient voltage suppressors while a system is in normal operation.

When an ESD pulse is introduced into the system, it is necessary to ensure that ESD protection diodes conduct to prevent the ESD pulse from reaching the DUP. From the connector, the ESD protection diodes and the DUP can be seen as being connected in parallel. It is therefore important to ensure that ESD protection diodes have low impedance so that most of the ESD energy is shunted through the ESD protection diodes.

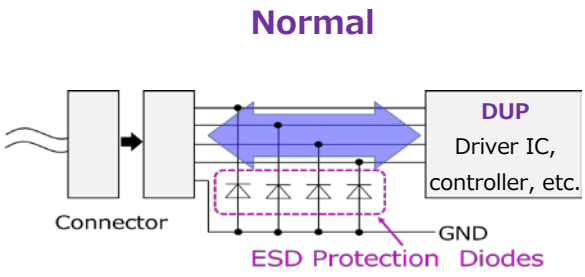


Figure 3.6 Normal system operation

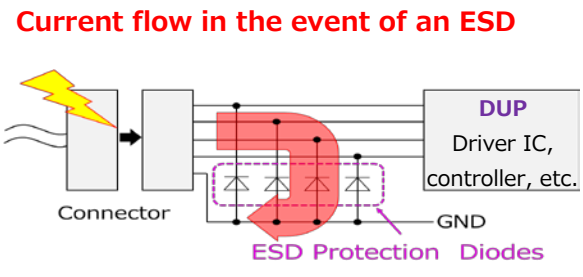


Figure 3.7 System operation in the event of an ESD strike

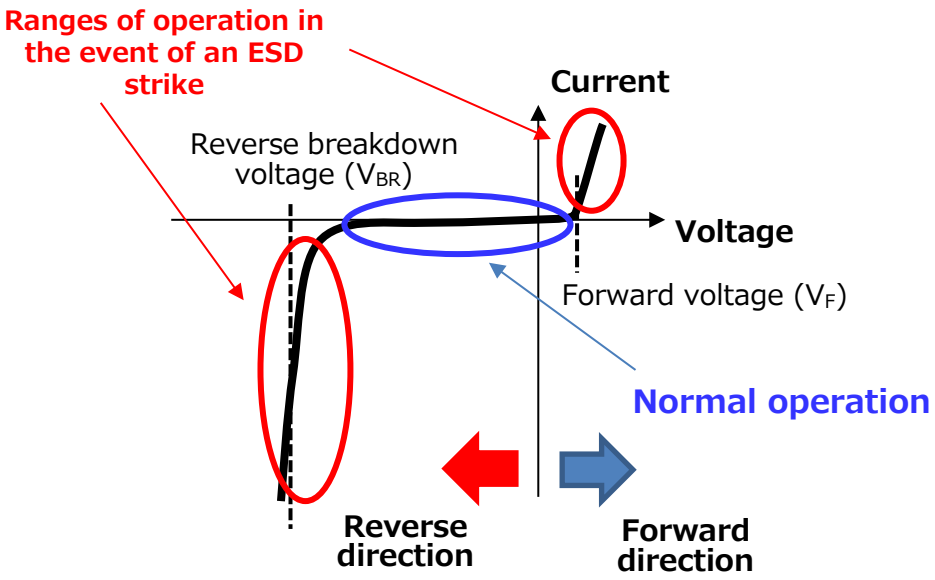


Figure 3.8 Voltage ranges in which ESD protection diodes act as transient voltage suppressors

3.3.1. During normal system operation (while no ESD pulse is being introduced)

ESD protection diodes are connected in the reverse direction so that they do not conduct when the voltage across an ESD protection diode is between forward voltage (V_F) and reverse breakdown voltage (V_{BR}). In this case, a depletion region is formed in the p-n junction, causing the diode to act as a capacitor.

The following three considerations apply to the selection of ESD protection diodes in terms of this voltage range:

1. Appropriate reverse breakdown voltage (V_{BR}) relative to the maximum voltage amplitude of the signal lines to be protected
2. Appropriate total capacitance (C_T) relative to the frequency of the signal lines to be protected
3. Signal polarity (signals crossing the GND level such as analog signals)

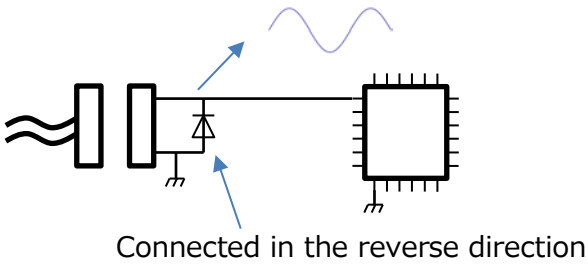
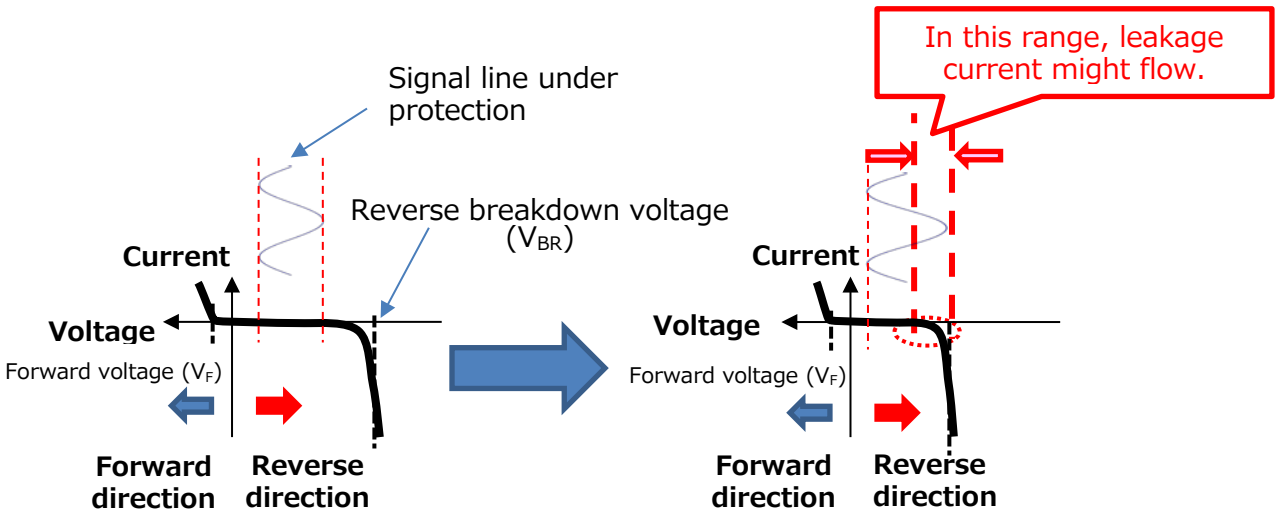


Figure 3.9 Connection of the ESD protection diode

1. Appropriate reverse breakdown voltage (V_{BR}) relative to the maximum voltage amplitude of the signal lines to be protected

As the voltage across an ESD protection diode approaches its reverse breakdown voltage (V_{BR}), leakage current increases as shown in Figure 3.10. When a signal approaches V_{BR}, its waveform

might be distorted by this leakage current. To avoid this, the V_{BR} of the ESD protection diode should have some margin relative to the voltage range of the signal line under protection.



When V_{BR} has a sufficient margin relative to the signal line under protection

When V_{BR} has no margin relative to the signal line under protection

Figure 3.10 ESD protection diodes with and without appropriate V_{BR}

The reverse breakdown voltage (V_{BR}) of the ESD protection diode is shown as follows in the datasheet. In the case of this ESD protection diode, the reverse voltage at which a reverse current of 5 mA flows at 25°C is specified as reverse breakdown voltage (V_{BR}). This ESD protection diode provides a typical V_{BR} of 6.8 V, which is equivalent to adding a 1.4-kΩ resistor between a signal line and GND when the diode's reverse voltage is 6.8 V. As shown in the figure, reverse current (I_R) increases exponentially with reverse voltage (V_R). As reverse voltage approaches V_{BR}, reverse current affects the linearity of the diode and might cause an increase in signal distortion.

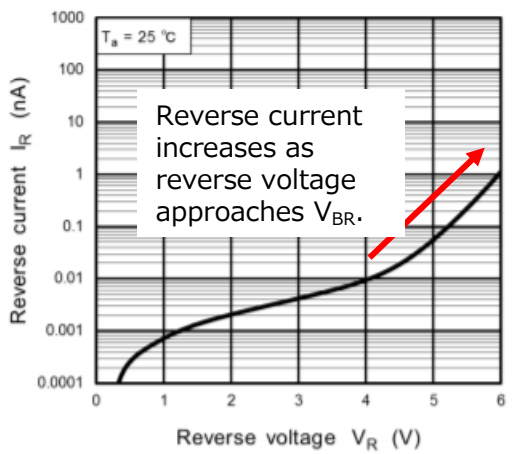
For some ESD protection diodes, the working peak reverse voltage (V_{RWM}) is specified. In the case of this ESD protection diode, V_{RWM} is specified as a voltage at which the maximum reverse current (I_R) is 0.5 μA (i.e., the diode's resistance is 1 MΩ or greater). It is important to select ESD protection diodes with V_{RWM} higher than the amplitude of the signal lines to be protected.

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}		—	—	—	5	V
Zener voltage (Reverse breakdown voltage)	V_Z (V_{BR})		I_Z = 5 mA (I_{BR} = 5 mA)	6.4	6.8	7.2	V
Dynamic impedance	Z_Z		I_Z = 5 mA (I_{BR} = 5 mA)	—	—	30	Ω
Reverse current	I_R		V_{RWM} = 5 V	—	—	0.5	μA

V_{RWM}

V_{BR}

Definition of V_{RWM}



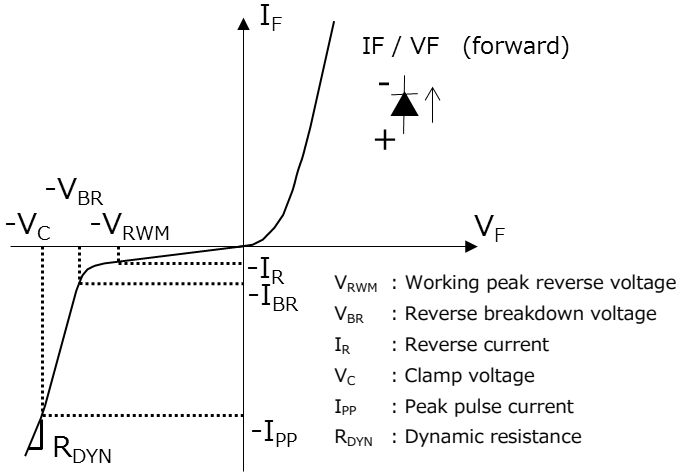


Figure 3.11 V_{BR} and V_{RWM} specifications of an actual ESD protection diode

2. Appropriate total capacitance (C_T) relative to the frequency of the signal lines to be protected

Figure 3.12 shows an equivalent circuit for the ESD protection diode. The diode does not conduct during normal operation. At this time, a depletion region is present at the interface of the p-n junction. The depletion region electrically acts as a capacitor.

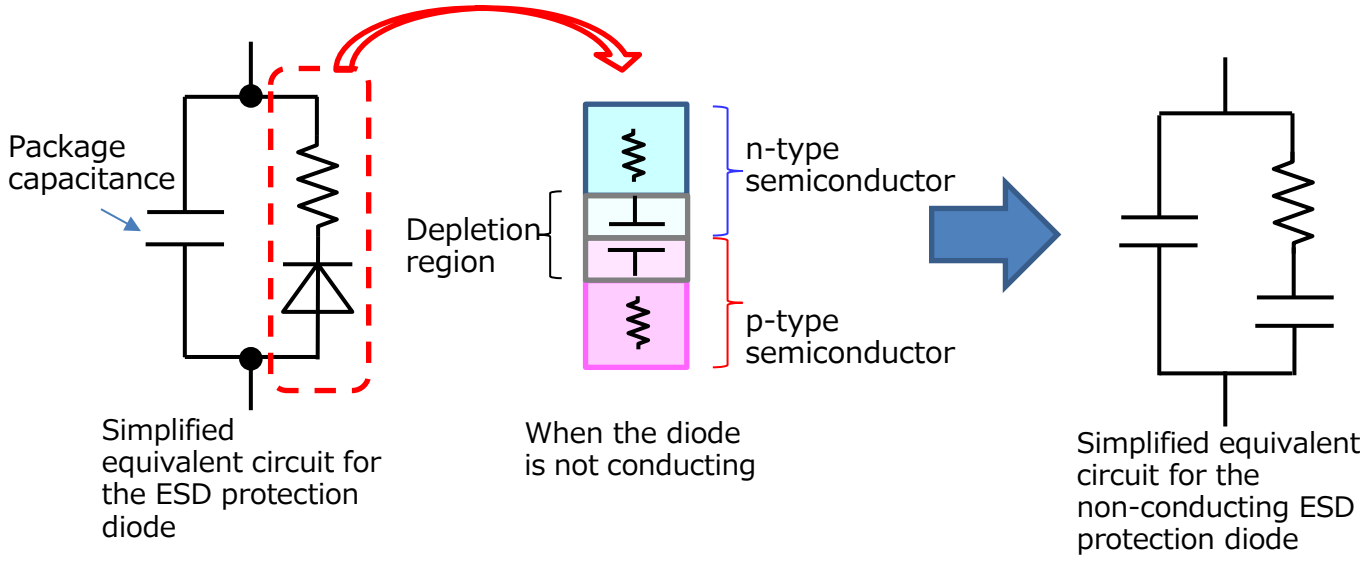


Figure 3.12 Simplified equivalent circuit for the non-conducting ESD protection diode

Therefore, the signal quality is degraded unless appropriate ESD protection diodes are selected, considering the frequency of the signal lines to be protected.

The following figure shows the insertion loss characteristics of the ESD protection diode with a total capacitance (C_T) of 5 pF, 0.3 pF, and 0.1 pF.

Diodes with a larger capacitance cause higher insertion loss (as indicated by a larger negative change in the characteristics curve) and are unable to track the changes in signal speed. For example, in the case of Thunderbolt (with a bandwidth of 10 Gbps, which is equivalent to a frequency of 5 GHz), ESD protection diodes with a small capacitance (0.1 to 0.3 pF) cause a small insertion loss and hardly affect the signal whereas an ESD protection diode with a capacitance of 5 pF causes a large insertion loss, considerably decaying a signal.

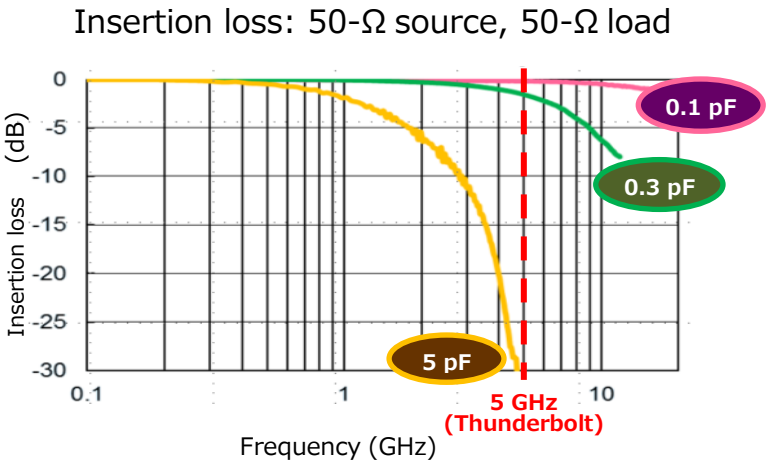


Figure 3.13 Total capacitance vs. insertion loss

Use the following figure as a guide when selecting ESD protection diodes.

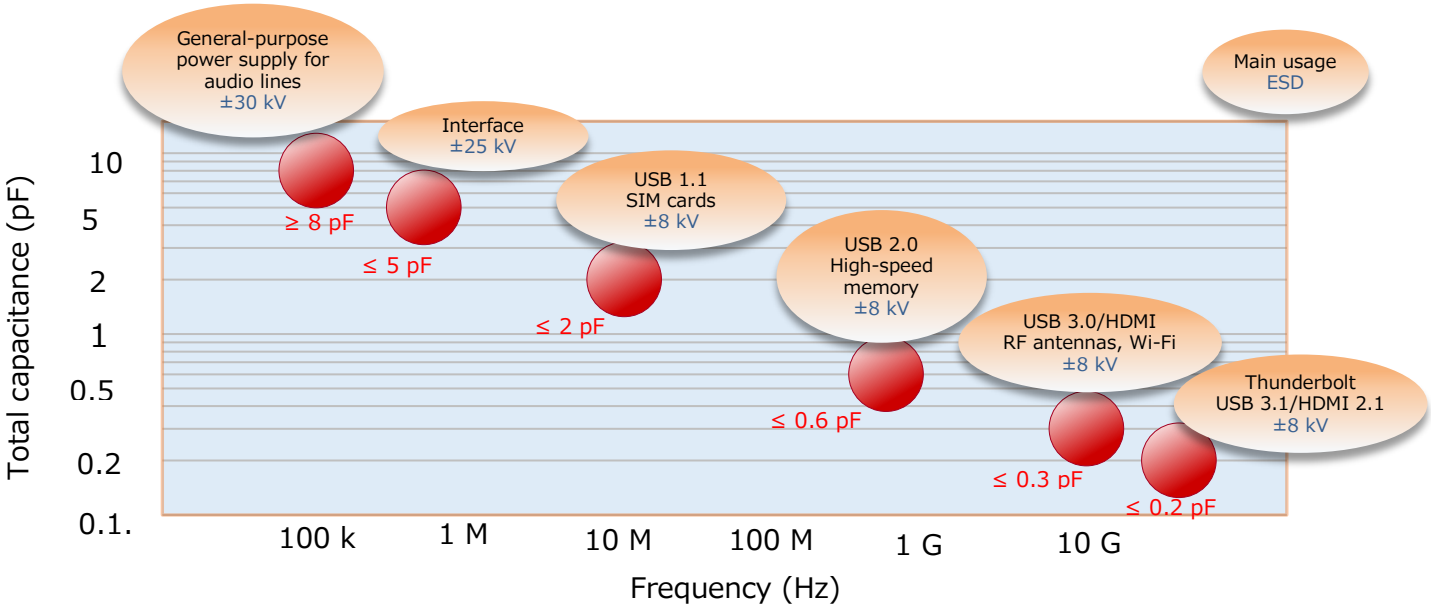


Figure 3.14 Selection of ESD protection diodes according to the signal frequency

3. Signal polarity (signals crossing the GND level such as analog signals)

It is necessary to select either unidirectional or bidirectional ESD protection diodes, considering the polarity of signal lines to be protected.

Different types of diodes should be selected for signals that swing only in the positive direction (e.g., between 0 V (logic Low) and 5 V (logic High)) such as unmodulated digital signals and unbiased analog signals whose voltage can be positive and negative.

Bidirectional ESD protection diodes should be used for signals that range above and below GND as shown below.

(Both unidirectional and bidirectional diodes can be used for signals whose voltage can only be positive or negative.)

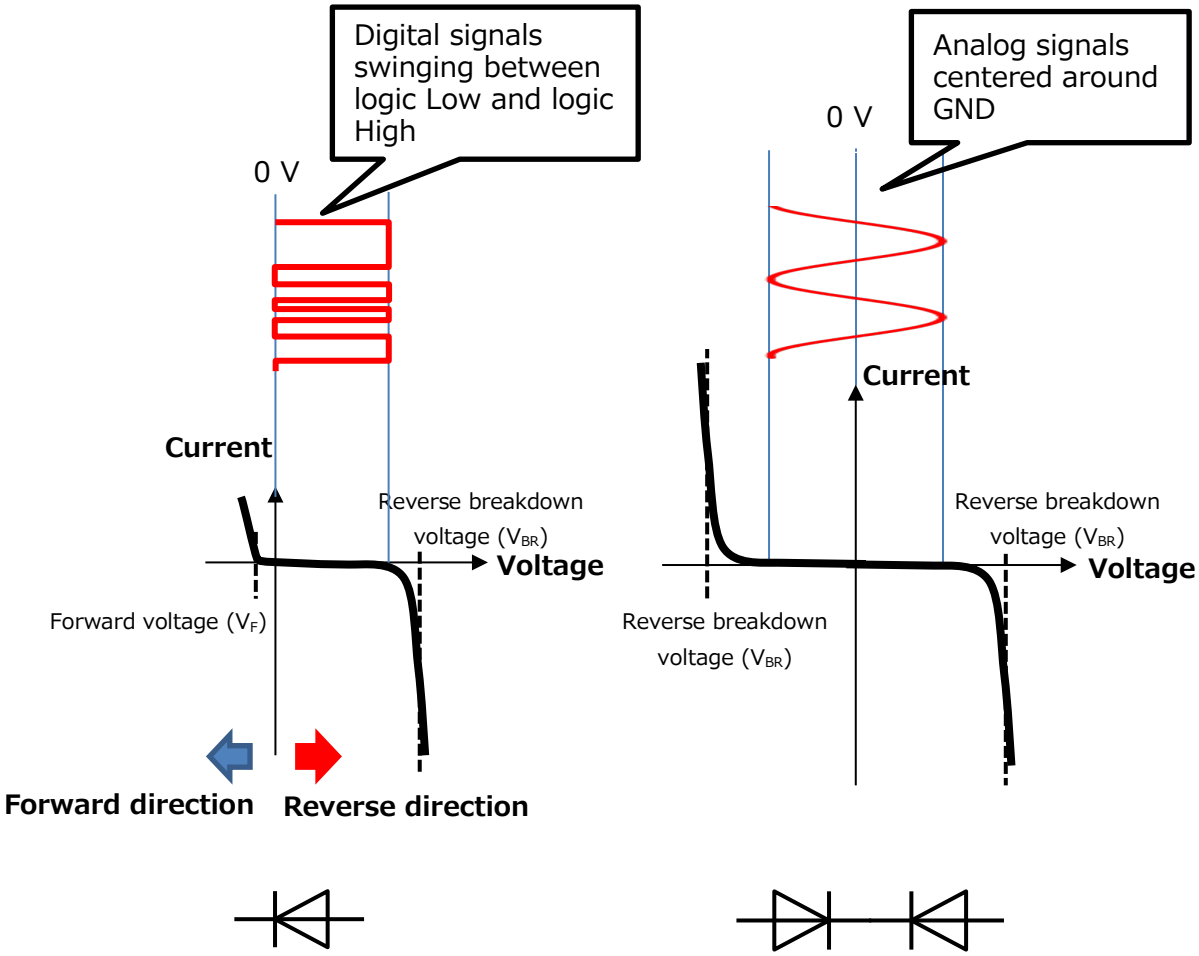


Figure 3.15 Unidirectional vs. bidirectional polarity

3.3.2. In the event of an ESD strike

When an ESD is introduced into a system, ESD protection diodes either conduct or enter reverse breakdown. A unidirectional ESD protection diode enters reverse breakdown in the event of a positive ESD strike and goes into conduction in the event of a negative ESD strike, as shown in Figure 3.16. This allows the ESD energy (current) to flow to GND, protecting the DUP.

There are three points to note to prevent the DUP from being destroyed by an ESD pulse:

I. ESD polarity: Both unidirectional and bidirectional ESD protection diodes can be used to absorb positive and negative ESD pulses as shown in Figure 3.16. It is therefore unnecessary to be concerned about signal polarity.
II. Low dynamic resistance (R_{DYN}): From the ESD entry point, ESD protection diodes and the DUP can be seen as being connected in parallel. The lower the R_{DYN} of ESD protection diodes, the lower the energy applied to the DUP and the less susceptible it is to destruction.
III. Low clamp voltage (V_C) and first peak voltage: If the protection element has a high first peak voltage or a high clamping voltage in the case that an ESD event occurs, it might not be able to absorb its energy, causing the DUP to be damaged.

I. Operations of an ESD protection diode to absorb ESD pulses with different polarities

Both unidirectional and bidirectional ESD protection diodes can absorb positive and negative ESD pulses, as highlighted by the arrows ⇩ in the following figure.

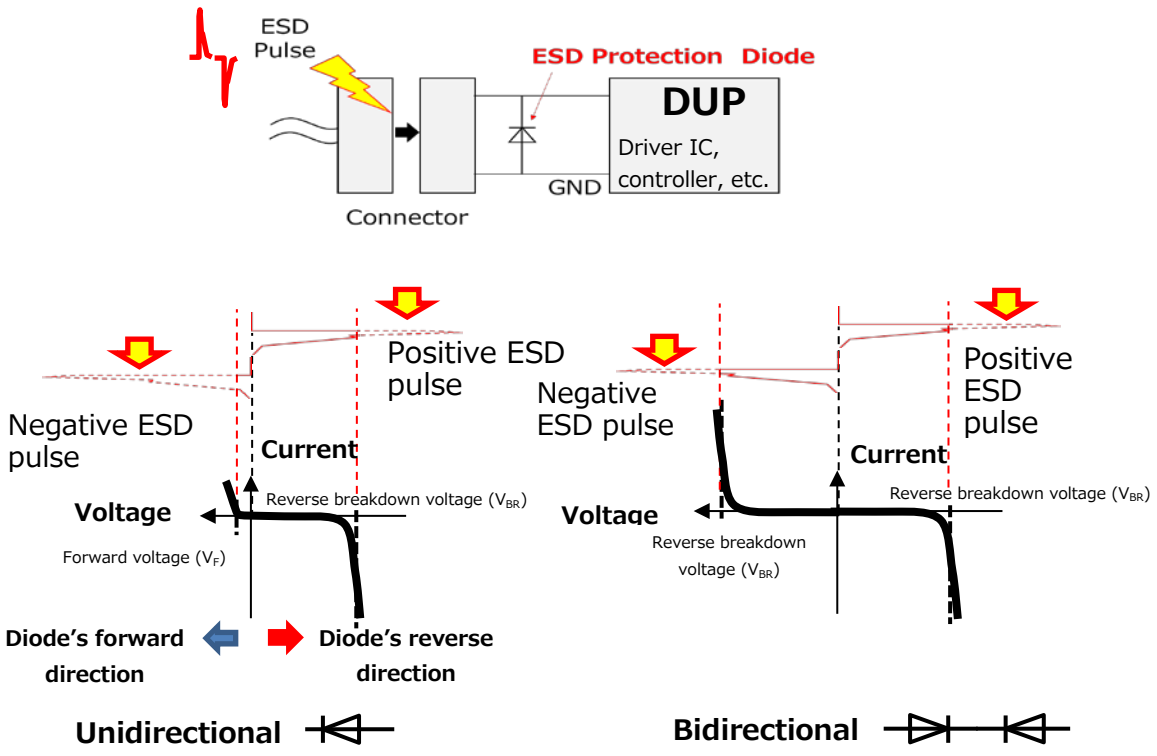


Figure 3.16 Absorption of positive and negative ESD pulses

II. Low dynamic resistance (R_{DYN})

In the event of an ESD strike, the ESD current flows to both ESD protection diodes and the DUP. It is important to reduce the current flowing to the DUP (i.e., increase the current shunted through the ESD protection diodes).

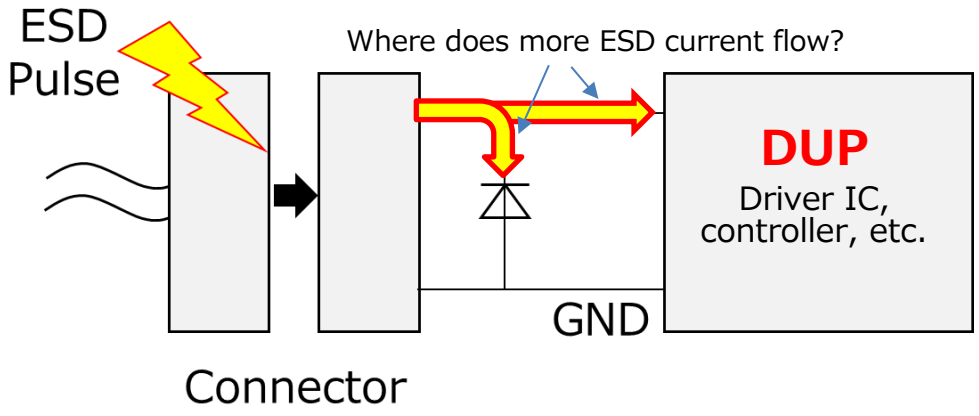


Figure 3.17 Where does more ESD current flow?

Nowadays, the datasheets for ESD protection diodes show their dynamic resistance (R_{DYN}). R_{DYN} is the slope of the V_F–I_F curve in reverse conduction mode. In the event of an ESD strike, ESD protection diodes with lower dynamic resistance conduct more current at a given voltage.

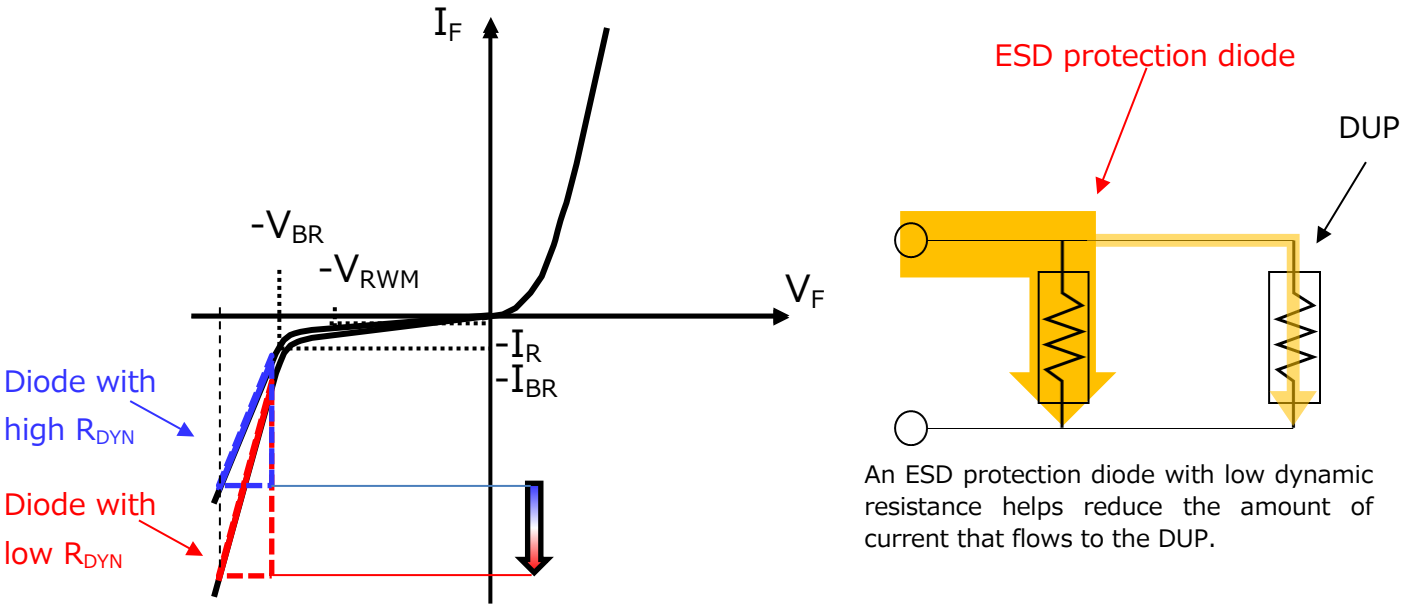


Figure 3.18 Dynamic resistance of an ESD protection diode

From the connector side, the impedances of the ESD protection diode and the DUP can be seen as being connected in parallel. If the ESD protection diode has low impedance (i.e., dynamic resistance), most of the ESD current is shunted through the ESD protection diode, reducing the current that flows to the DUP and therefore the possibility of its destruction.

III. Low clamp voltage (V_C) and first peak voltage

Figure 3.19 compares the ESD clamp voltage achievable with different ESD protection diodes.

Measurements at the input of the DUP indicate that the DF2B5M5SL and DF2B5M4SL provide lower clamp voltage than the DF2B26M4SL at 30 ns and 60 ns. The smaller the area under the curve of the clamp voltage waveform, the less damage the DUP suffers. Therefore, ESD protection diodes with low clamp voltage (V_C) provide better protection against ESD pulses.

In addition, ESD protection diodes do not respond immediately after an ESD entry. Therefore, if the first peak of the ESD pulse is higher than the clamp voltage of the ESD protection diode, it might be applied to the DUP, leading to its malfunction or destruction.

ESD protection diodes are designed to provide faster response than other types of protection devices.

Toshiba's DF2B5M5SL provides 50% lower first peak voltage than the DF2B5M4SL because of the optimized internal structure and manufacturing process.

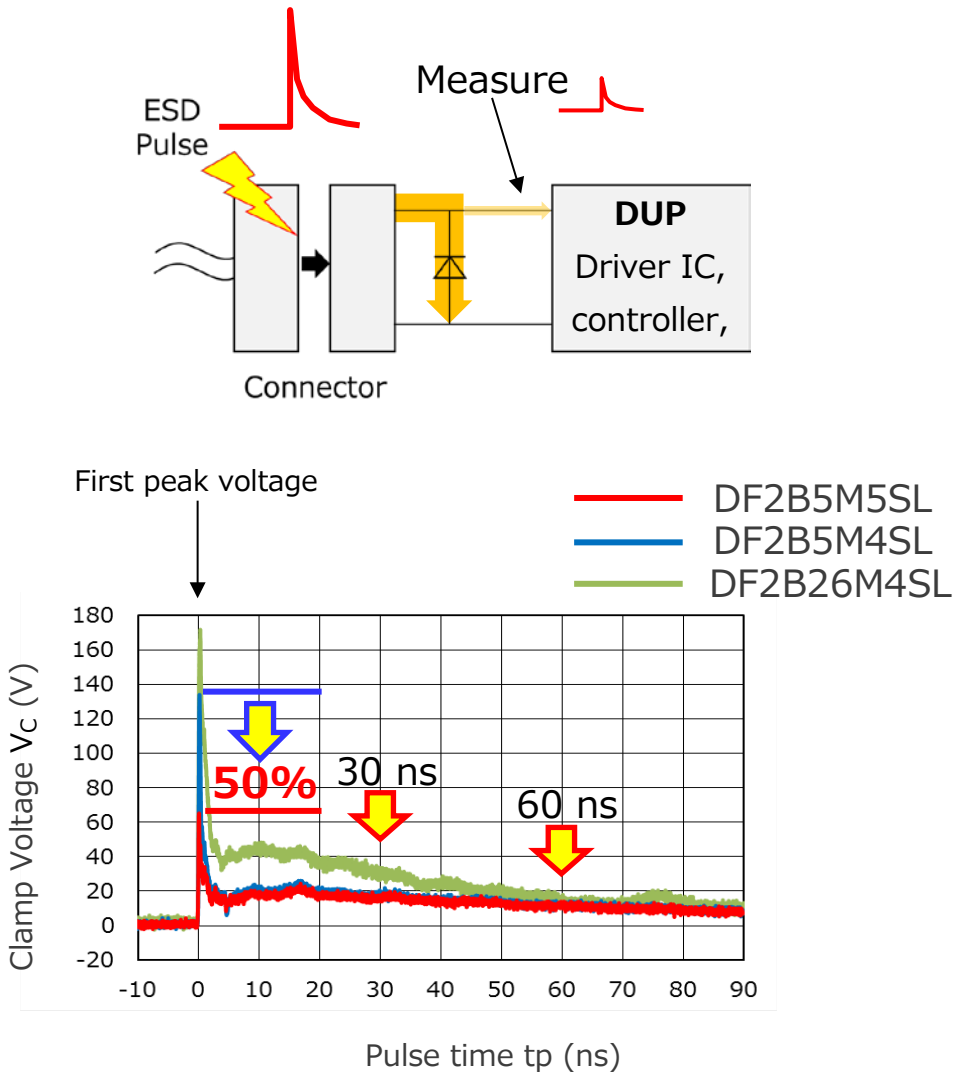


Figure 3.19 Differences in ESD absorption depending on the differences in clamp voltage (V_C) and first peak voltage

4. Selecting ESD protection diodes

Selection of ESD protection diodes should be considered from three angles. Since some of the aspects that should be taken into consideration have already been discussed, they are described below only briefly.

1. Maintaining the signal quality of the signal lines to be protected

1) Voltage of signal lines (see page 13)
Select ESD protection diodes with appropriate reverse breakdown voltage (V_{BR}) or working peak reverse voltage (V_{RWM}) according to the maximum voltage of the signal lines to be protected.

2) Signal speed (see page 15)
Select ESD protection diodes with appropriate total capacitance (C_T) according to the maximum frequency of the signal lines to be protected.

3) Signal polarity (see page 17)
Use bidirectional ESD protection diodes for signals that cross the GND level such as analog signals.

2. Better ESD protection performance

4) ESD polarity (see page 18)
Both unidirectional and bidirectional ESD protection diodes can absorb both positive and negative ESD pulses.

5) Clamp voltage (see page 20)
Select ESD protection diodes with the minimum clamp voltage (V_C) according to the V_{RWM} required.

3. ESD tolerance of ESD protection diodes

6) IEC 61000-4-2
Select ESD protection diodes with a guaranteed ESD performance higher than a system's ESD immunity requirement.
Note, however, that the ESD performance (immunity) of the ESD protection diode is generally proportional to its total capacitance.

7) IEC 61000-4-5
Select an ESD protection diode that has a higher guaranteed value than the required peak pulse power and current.

5. Board layout considerations

Without adequate board design, even ESD protection diodes with high ESD protection performance would not provide sufficient protection. In particular, board design greatly affects the instantaneous high-frequency pulse that occurs immediately after an ESD strike.

ESD pulses follow a low impedance path. It is necessary to pay attention to the length of the traces leading to the ESD protection diode and the DUP after the trace originating from the connector diverges into two paths, taking the board trace inductance into consideration. If the board trace leading to the ESD protection diode has large inductance, ESD energy is injected into the DUP. Figure 5.1 compares a circuit in which an ESD protection diode is added close to the DUP and a circuit in which it is placed near a connector. As can be seen from this figure, when an ESD protection diode is placed close to the connector, the first peak voltage is nearly 10 V lower than in the case that it is placed close to the DUP.

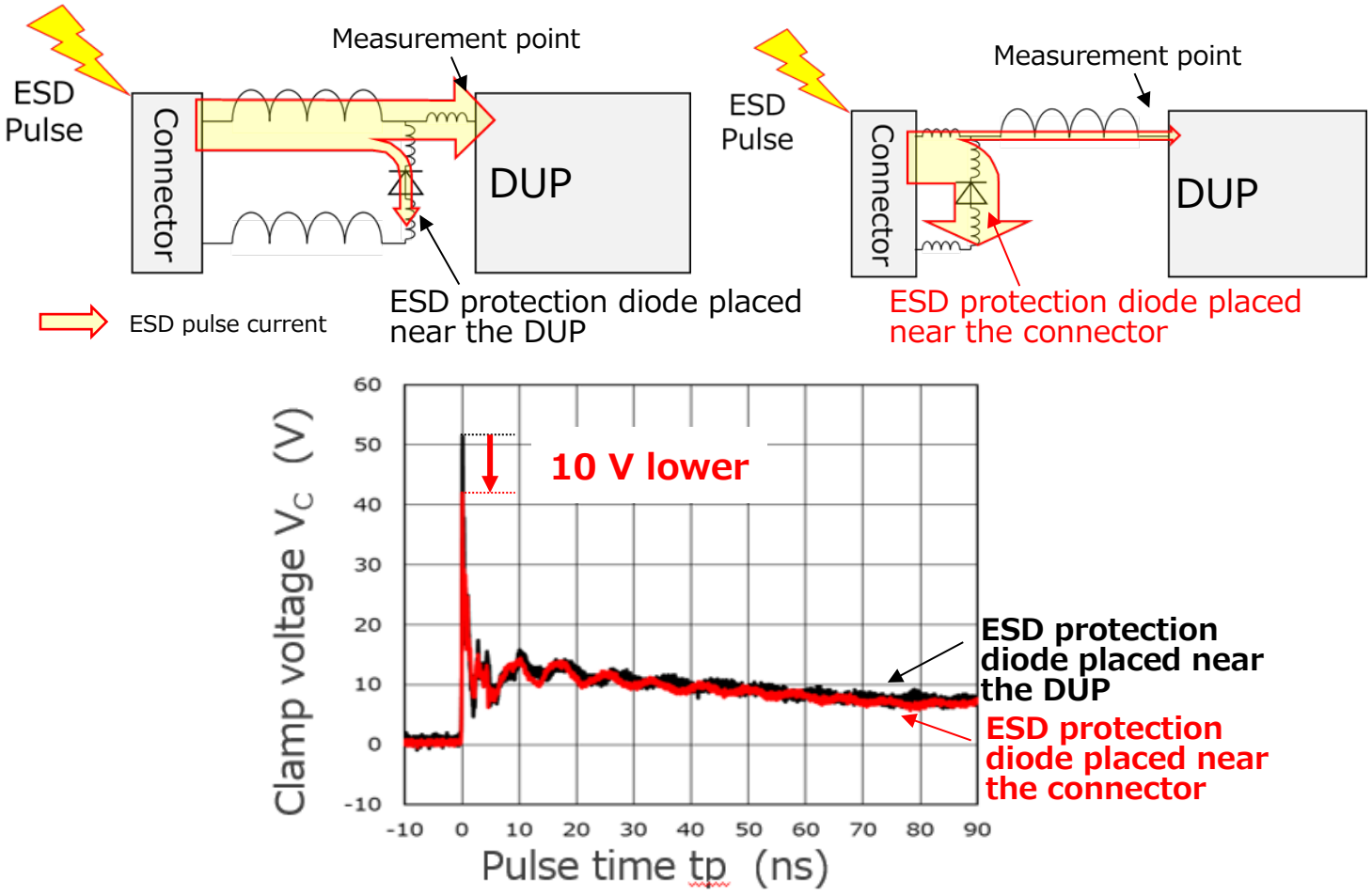
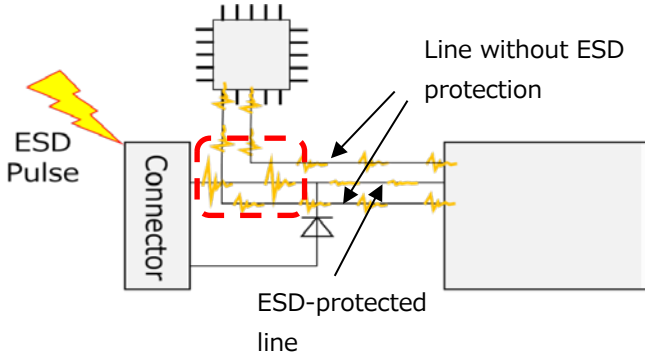


Figure 5.1 Effect of the diode placement on the first peak voltage

The following considerations apply to board design:

1. Place ESD protection diodes close to the ESD entry point.
2. Minimize trace inductance in series with ESD protection diodes including GND after signal lines originating from the connector diverge into two paths leading to ESD protection diodes and the DUP.
3. Do not run a wire in parallel with any wire through which ESD pulses might travel. Particular attention should be paid to the lines that are only internally connected.



Electromagnetic induction or capacitive coupling might cause an ESD pulse to travel from a connector connected to the external world to internal lines.
The segments of board traces from the connector to ESD protection diodes are vulnerable to ESD.

Figure 5.2 Traces running in parallel with a line connected to the external world

6. Electrical characteristics specified in the datasheet

6.1. Definition of absolute maximum ratings

For ESD protection diodes, the maximum allowable current, voltage, power dissipation, and other characteristics are specified as maximum ratings. In circuit design, understanding maximum ratings is crucial in order to obtain the best performance from ESD protection diodes and maintain device reliability throughout their target operating life.

In order to guarantee the lifespan and reliability of ESD protection diodes, maximum ratings must not be exceeded. For ESD protection diodes, maximum ratings are defined in accordance with the absolute maximum rating system.

The absolute maximum ratings are the highest values that must not be exceeded even instantaneously under any conditions.

If a stress exceeding the specified rating is applied, a device might be permanently degraded. None of the absolute maximum ratings may be exceeded. Therefore, care should be exercised as to supply voltage bounces, variations in the characteristics of electronic devices, possible exposure to stress higher than maximum ratings during circuit adjustment, changes in ambient temperature, input signal fluctuations, and so on. The major ratings that should be considered include the ESD tolerance, peak pulse power, junction temperature, and storage temperature of ESD protection diodes. These parameters are interrelated and cannot be considered separately. They also depend on external circuit conditions. Although the absolute maximum ratings are generally specified at an ambient temperature (T_a) of 25°C, some parameters are specified at different temperatures.

6.1.1. Electrostatic discharge voltage (IEC 61000-4-2) (Contact), V_{ESD}

The ESD tolerance of a contact discharge, i.e., a discharge through a direct contact with equipment under protection

The ESD tolerance is measured according to the method and ESD waveform specified in the IEC 61000-4-2 standard from the International Electrotechnical Commission (IEC). The specified V_{ESD} value is the peak value of the test waveform.

6.1.2. Electrostatic discharge voltage (IEC 61000-4-2) (Air), V_{ESD}

The ESD tolerance to an air discharge, i.e., a discharge that occurs between equipment under test (EUT) and a discharge gun through an air layer. The test method and the ESD waveform are specified in IEC 61000-4-2.

6.1.3. Peak pulse power (t_p = 8/20 μs), P_{PK}

The maximum surge power that can be shunted before an ESD protection diode itself is damaged

The peak pulse power is measured using an 8/20 μs pulse waveform shown in Figure 6.1. (8/20 μs means that it takes 8 μs for the waveform to rise to 100% and 20 μs to fall from 100% to 50%.)

6.1.4. Peak pulse current (t_p = 8/20 μs), I_{PP}

The peak pulse current that can be shunted before an ESD protection diode itself is damaged

The peak pulse current is measured using a test waveform shown in Figure 6.1.

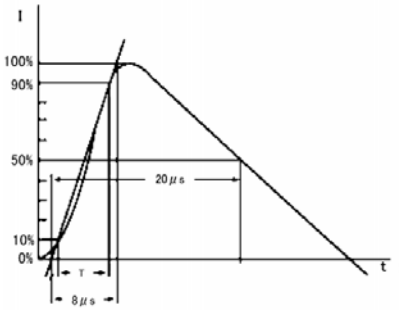


Figure 6.1 8/20 μs waveform specified in IEC 61000-4-5

6.1.5. Junction temperature, T_j

The maximum junction temperature at which an ESD protection diode can operate without degradation or self-damage

6.1.6. Storage temperature, T_{stg}

The ambient temperature range in which an ESD protection diode can be stored and transported without voltage application

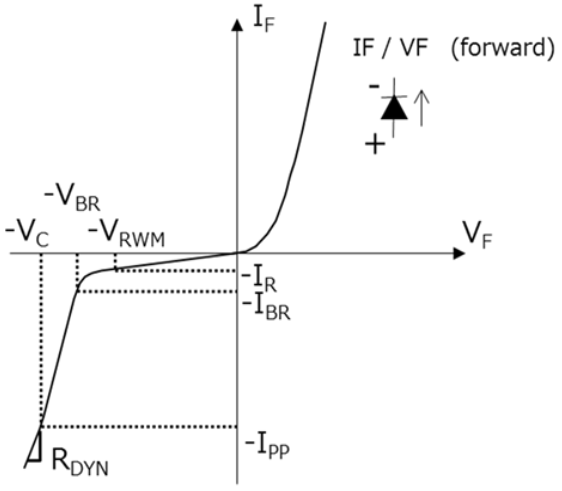
6.2. Electrical characteristics

6.2.1. Working peak reverse voltage, V_{RWM}

At the working peak reverse voltage, an ESD protection diode exhibits a very high impedance. (Even if this voltage is applied, only the specified leakage current flows.) The designer can use this parameter as a guide to ensure that it is above the maximum operating voltage of the signal line to be protected.

6.2.2. Total capacitance, C_T

The equivalent capacitance across a diode's terminals when a small signal is applied at the specified reverse voltage and frequency. The total capacitance is the sum of the junction capacitance of a diode and the parasitic capacitance of its package. Junction capacitance decreases as reverse voltage increases.



VRWM	: Working peak reverse voltage
VBR	: Reverse breakdown voltage
IR	: Reverse current
VC	: Clamp voltage
IPP	: Peak pulse current
RDYN	: Dynamic resistance

Figure 6.2 Definitions of electrical characteristics

6.2.3. Dynamic resistance, R_{DYN}

The dynamic resistance is the current slope (resistance value) at two specified high-current points on the V_F–I_F curve when the reverse voltage that causes a breakdown is applied to the ESD protection diode. The dynamic resistance and the clamp voltage described below represent the ESD performance of an ESD protection diode.

6.2.4. Reverse breakdown voltage, V_{BR}

The voltage at which an ESD protection diode begins to conduct the specified amount of current under specified conditions (defined typically at 1 mA, although this differs from device to device). V_{BR} is originally a parameter defined for Zener diodes. V_{BR} is defined as the voltage at which an ESD protection diode turns on.

6.2.5. Reverse current, I_R

The leakage current that flows in the reverse direction when an ESD protection diode is reverse-biased at the specified voltage. In the case of ESD protection diodes, I_R is defined at the working peak reverse voltage (V_{RWM}).

6.2.6. Clamp voltage, V_C

The maximum voltage to which an ESD protection diode is clamped when exposed to the specified peak pulse current. V_C is generally measured at multiple peak pulse current points. As described in Section 6.1.4, an 8/20 μs waveform is used for the peak pulse current. The dynamic resistance and the clamp voltage represent the ESD performance of an ESD protection diode.

To view the lineup of ESD protection (TVS) diodes → Click Here

7. Related Links

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