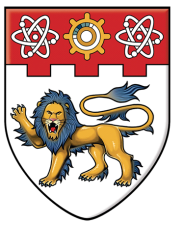

NANYANG
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POWER OPTIMISATION FOR ADAPTIVE EMBEDDED WIDEBAND RADIOS

A Thesis submitted to
the School of Computer Engineering
of Nanyang Technological University

by

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in fulfillment of the requirement for
the Degree of Doctor of Philosophy of
for Computer Engineering

February 9, 2015

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2.1 Power Consumption

The increasing computational requirements, and growing requirements for deployment in portable devices have prompted serious attention to reducing the power consumption of wireless communication systems, especially in the physical layer. High power dissipation by a system introduces high operating temperatures and follow-on effects that increase the cost of packaging as well as requiring larger batteries in the case of portable devices, or other power supply solutions. Power dissipation has thus come to be considered as one of the most important design metrics, along with area and performance. Reducing power consumption has been investigated at all levels of the digital design flow: from the system design stage to the layout stage. At every stage, the designer can act to optimise the power consumption of the design. However, small changes at the lower levels may require more work and time to update the higher level optimisations, thus increasing the complexity of the optimization process. Moreover, at the system design level stage, the designer has more options to reduce power dissipation by a greater degree. At the lower level, the architecture of the system is designed in terms of data flow between registers, leaving few options to optimize the system. Thus, most power saving opportunities may exist at the highest level of design abstraction [1]. FPGAs, with their highly parallel architecture, are suitable for the increasing computational requirement of signal processing in wireless communication systems such as modulation, channel coding, and so on. In order to optimise the power dissipation of systems on FPGA, the power consumption of FPGAs needs to be clearly understood, and accurate, as well as flexible, power estimation tools are needed in order to provide power profiles of the system to help the designer makes the best

decisions. In addition, low power design techniques must be investigated to optimise power consumption when a system design is implemented.

2.1.1 Power Dissipation on FPGA

Fast time-to-market, flexible programmability, and improving performance continue to render FPGAs an attractive platform for digital circuit implementation. FPGAs have been gaining ground as an alternative implementation technology in a wide range of application domains, due primarily to the increased cost and diminished economies of scale when building custom ASICs. However, power remains a key metric in which FPGAs lag behind custom ICs, although this gap is narrowing. Total FPGA power is calculated as follows:

$$P_{total} = P_{devicestatic} + P_{designstatic} + P_{dynamic}, \tag{2.1}$$

where P_{total} represent the total power consumption of the FPGA, $P_{devicestatic}$ refers to the leakage power when the device is powered, $P_{designstatic}$ is the additional power dissipation when the design is configured on the device and has no switching activity. The leakage current is the only source of this static power dissipation. $P_{dynamic}$ represents the additional average power consumption from user logic utilization and switching activity caused by signal transitions in the design. Increasing operating speed leads to a rise in switching activity and thus results in increased dynamic power consumption. The most significant source of dynamic power dissipation is the charging and discharging of parasitic capacitance in signal transitions.

Efficient power-aware designs for FPGA-based systems require estimation tools that gauge power consumption at an early stage in the design flow. These tools allow design tradeoffs to be considered at a high level of abstraction, thus reducing design effort and cost. Significant research on FPGA power consumption has appeared in the literature [2–6]. These cited papers have shown that power consumption of FPGA devices is predominantly confined to the programmable interconnection. In the Xilinx Virtex-II family, for instance, it was reported that between 50-70% of total power is dissipated on the interconnection network [2]. The majority of power dissipation in FPGAs is dynamic power dissipation [2] as characterized by:

$$P_{dynamic} = \frac{1}{2} \sum_{i \in allnets} C_i \cdot f_i \cdot V^2, \tag{2.2}$$

where $P_{dynamic}$ represents average power consumption, C_i is the capacitance of a net, f_i is the average transition rate (switching activity) of corresponding net, and V is the voltage supply. Thus, estimating dynamic power (2.2) requires two parameters for each net: switching activity and capacitance. The net's capacitance is the parasitic effects on interconnection wires. It depends on the interconnection used resources. The switching activity represents the signal transitions on the net, depending on how circuit delays are accounted for. Zero delay activity can be calculated assuming logic and routing delays are zero. Logic delay activity can be calculated considering only logic delays. Routed delay activity can be calculated using complete logic and routing delays. When delays are accounted for, the presence of glitches, which are spurious logic transitions due to unequal path delays to the nets driving gate, leads to an increase in switching activity. The additional activity due to glitching actually causes a significant increase in dynamic power [3]. The path delays in FPGAs are also significantly dominated by interconnects, which have a different delay, compared to primitive logic delays. Therefore, the result of glitching on total power consumption may be more severe in FPGAs versus ASICs.

2.1.2 Power Estimation

Several studies investigating power estimation techniques at different levels from the circuit level up to the system level have appeared in the literature. At the circuit level, a circuit simulator such as SPICE [7] provides one of the most accurate power estimation methods but the computational overhead involved in this is not really suitable for highly integrated and dense FPGA based systems and complex designs.

A large amount of research has focused on logic-level power estimation [3–5]. Logic-level techniques can be classified into three categorises: simulation-based techniques, probability propagation techniques, and statistical techniques.

Simulation-based techniques rely on simulating the logic response with specific input signals to compute the power consumption. The PowerPlay power analyzer integrated in Altera

Quartus II [8] and the XPower Analyzer integrated in Xilinx ISE Design [9] are both able to support computing of the switching activities of signals and dynamic power consumption from a simulation file; Secondly, probability-based propagation techniques calculate the value and transition probabilities of all logic signals in the circuit according to the given value and transition probabilities of the primary inputs from which the power consumption is estimated based on the computed probabilities. Statistical techniques such as Monte-Carlo simulation will monitor values of power consumption according to stimulating generated input patterns until it converges to within user-defined error and confidence levels. Todorovich et al. [5] presented the development of a new FPGA-oriented power estimation tool based on this statistical approach.

With increasing system complexity, several studies have recently paid attention to power estimation and optimization at higher level and earlier stages of the design such as the register-transfer and behavioural levels. The large run-times required by lower level power analysis tools, and the need to synthesize and validate a gate- or transistor-level netlist make previous techniques highly inefficient for exploring high-level design tradeoffs, and infeasible for use in automatic high-level and system-level synthesis and optimization tools.

Several studies have shown that the efficiency of power optimization is significantly better at the higher levels [6, 10–12]. High-level power estimation is needed to conveniently validate power budgets for the different parts of the design and identify the most power hungry part in the design and also evaluate quickly the effect of various optimized techniques to obtain the power budget of systems. Furthermore, the long run time and and the complexity of synthesizing and validating a gate-level netlist make lower level estimation approaches highly inefficient for exploring high-level design abstraction tradeoffs.

High Level Power Estimation

Power estimation performed at higher levels of design abstraction is more efficient due to the reduction in complexity of netlists in the design, and due to the availability of behavioural information which is more difficult to obtain at the lower levels. However it also introduces an accuracy penalty due to reducing the complexity of analysis. The absolute accuracy of high level power estimation is typically lower than the accuracy of estimation at the lower levels of the design hierarchy.

Recently, more research has focused on the RTL/architecture level power estimation to obtain the power profile for optimizing at high level designs as well as for software programs. Raghunathan et al. [12] classified high level power estimation into three broad approaches, namely analytical models, control logic analysis techniques, and characterisation-based macro-modeling. At an architectural design level, different parts such as arithmetic macro blocks, control logic, memory, clock network, and I/O are analysed using different estimation approaches.

Analytical power modelling techniques are based on correlating power consumption to measures of design complexity. These techniques may be used to estimate in the early stages of a design when complexity is known after synthesizing or mapping the design. For example, the design power estimation tool, XPower Estimator [13], computes the dynamic power consumption of a logic block based on its used resource count, load capacitance per logic element, the clock frequency, and the average switching activity factor. The designer has to provide estimates for some of these parameters such as clock frequency and the average switching activity factor. The result depends significantly on the designer's judgment. Generally, such techniques are not highly accurate, however, they may be suitable for specific modules of a design such as memories for which the complexity parameters are easy to estimate and also can be used to estimate power in the early stages.

Control logic analysis techniques consider the control logic parts of a design. The activity-based control model [10] is an example of this approach. The switching activities of a control unit show significant spatial and temporal correlations to the remaining parts of a design. So computing the power consumed in the control logic and taking into account its impact on the design can estimate the power consumption of the design. Furthermore, since the control logic is typically smaller in size than the datapath, it can have low overheads and be fast to synthesis, followed by estimating its power consumption at a lower level. In addition, the glitching activity of the control signals have a significant impact on the power consumption in the rest of the design.

Characterization-based macro-modeling is an approach mostly used in high level power estimation that uses a macro-model abstraction to obtain and characterize the power consumption of macro-blocks using the measure of lower level methods. A gate-level or logic-level power estimation tool is used to observe the power consumption of the macro-block for various input samples, called training sequences. Based on this observation, a macro-model is built, in which

the macro-block's power dissipation is considered as a function of various selected parameters such as the statistics of the inputs and outputs. This approach is best suited for bottom-up design methodologies where models of macro-blocks instantiated from a component library can be used to estimated the power consumption of design.

Xilinx Power Tool

The contemporary Xilinx FPGA design suite supports two tools: XPower Estimator (XPE) and XPower Analyzer (XPA) to estimate and analyse the power dissipation of systems that are implemented on Xilinx FPGA devices. These tools provide the power profile of a system in the early stages when the RTL description is being implemented that helps the designer highly optimise power when implementing the system. XPE is a Microsoft Excel spreadsheet that is used to estimate power distribution typically used in the pre-design and pre-implementation phases of design flow [13] . XPE supports selecting the relevant power supply and thermal management components based on the system's architecture evaluation and device selection. XPE reads the resource usage of the implemented system, toggle rates, I/O loading, and many other factors from a designer's input and combines these with the appropriate device models to estimate power distribution. The appropriate device models are obtained from measurements, simulation, and/or extrapolation. There are two primary components that contribute to the accuracy of XPE. One is the designer's input estimates such as toggle rates, I/O loading. The other is device data models integrated into the spreadsheet that are selected based on the device selection. Realistic input must be provided to obtain an accurate estimation.

XPE is used in the early stages when the RTL description is being implemented. However, XPE depends significantly on the designer's input estimates that result in poor accuracy of estimation. After the system is synthesised and implemented, XPA tool can be used for more accurate estimation and power analysis.

XPA analyses the design on real design data from the system such as the NCD file output from Place & Route (PAR) after the system is implemented. The latest version of XPA employs a vectorless estimation algorithm in which switching activity of nodes are assigned to appropriate values even if they are not defined in the input file. However, simulation activity files such as SAIF or the VCD file from simulation in timing mode are required for accurate power analysis.

XPA is used at the stage when a system design has successfully completed PAR and generated an NCD output file and been simulated to verify its functionality. The power profile of the system such as resource usage, capacitance of nodes and nets can be extracted from the NCD file while switching activities are computed with high accuracy based on timing simulation from SAIF or VCD files. Much more realistic power information is obtained at this stage, thus, XPA can achieve more accurate results in terms power estimation. XPA generates a text-based power report that shows the power distribution on the system that can used for optimisation.

2.1.3 Low power design strategies

It is well known that the dominant source of optimising power dissipation on FPGA is optimising dynamic power dissipation. Dynamic power dissipation is proportional to switching activity and the equivalent capacitance of the circuit. There are many techniques and strategies to reduce the power dissipation in FPGA presented in the literature [14–18]. However, only the strategies which appear to be suitable for wireless systems are investigated. These strategies will be discussed in detail for specific implementations in the following chapters, but the general approach is discussed here.

Firstly, in signal processing dominated systems, storing and transferring data between functional modules consumes a large proportion of total energy [17]. The power consumption thus heavily depends on the way a system is partitioned and modularised and hence the use of data buffers to synchronously transfer data between functional modules. In order to optimise power dissipation at a system level, such systems are often realised to support stream processing in which buffering data between functional modules requires much less memory. The energy for storing and transferring data is thus reduced significantly.

Secondly, the latch registers with enable signals must be used at the inputs of functional modules. They can reduce the switching activity inside functional modules when the modules must wait for synchronisation in a streaming process. Apart from the above strategies, in low power design, the power estimation tools must be used to evaluate the power dissipation of the system at each stage of the flow. This provides information for power dissipation optimisation.

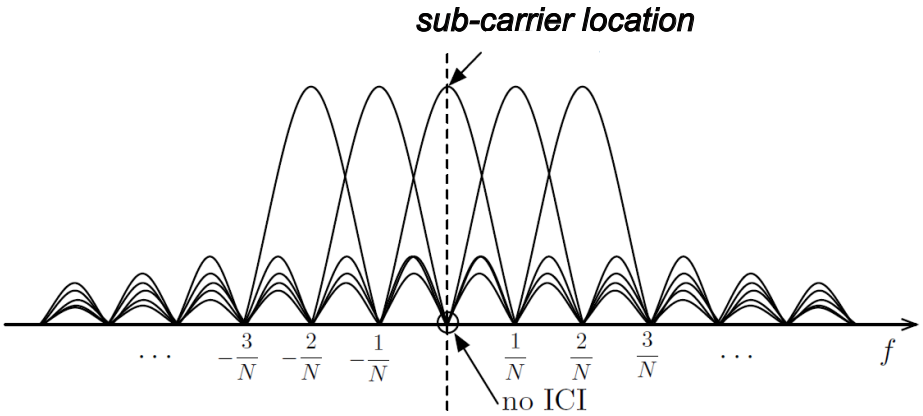

Figure 2.1: The spectrum of subcarriers in OFDM [19]

2.2 Orthogonal Frequency Division Multiplexing

OFDM is a multicarrier modulation scheme used in both wireline and wireless communication in which a high-rate data stream is split into multiple parallel low rate streams that are modulated by multiple sub-carriers. The adjacent modulated sub-carriers are theoretically orthogonal with zero mutual interfere to each other. OFDM signals are modulated using sub-carriers across the frequency range similar to frequency division multiplexing (FDM). But the main difference is that FDM conventionally multiplexes the signals into separatele small bands in which the signal in each band is modulated using a specific sinusoidal carrier, while OFDM signals are modulated using orthogonal sub-subcarriers. Each sub-carrier is mathematically represented by a sinc pulse, which is overlapped with other subcarriers in the frequency domain as shown in Fig. 2.1. Note that the sub-carrier of the $sinc$ pulses will null at the centre points where the other subcarriers are located. Ideally, there is thus zero ICI in an OFDM signal.

An OFDM symbol signal can be expressed at baseband by a sum of modulated complex exponentials as:

$$s(t) = \sum_{k=0}^{N-1} X_k e^{i2\pi\Delta f t}, \tag{2.3}$$

where X_k represents a data modulated symbol such as a BPSK, QPSK, or QAM symbol, and is a complex number modulated by the kth subcarrier of N subcarriers and Δf is the subcarrier spacing. Sampling this OFDM symbol signal with sampling period of T_S is expressed as:

$$s(nT_S) = \sum_{k=0}^{N-1} X_k e^{i2\pi\Delta f n T_S}, \tag{2.4}$$

A sample of the OFDM signal is equivalent to an inverse N-point discrete Fourier transform (IDFT), taking X_k as a discrete point in the frequency domain. Inversely, the sampled OFDM symbol signal can be demodulated using the discrete Fourier transform (DFT). The OFDM modulation and demodulation are hence performed by computing the IDFT and DFT, respectively, expressed as:

$$s[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{i2\pi \frac{k}{N} n}, \tag{2.5}$$

$$X[k] = \sum_{n=0}^{N-1} s[n] e^{-i2\pi \frac{k}{N} n}, \tag{2.6}$$

In order to achieve efficient computation, The inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) are implemented in an OFDM system to modulate and demodulate the signal instead of the IDFT and DFT, respectively. These optimised algorithms generally rely on the number of points, and hence carriers, being a power of 2.

2.2.1 Cyclic Prefix

When transmitting OFDM symbols over a delay-dispersive multi-path channel, the received signal is the linear convolution of the transmitted symbol with the channel impulse response (CIR)

$$y[n] = h * s[n], \tag{2.7}$$

where h, assuming it has a length of L, denotes the equivalent impulse response of the channel. and $*$ is the convolution operation. The received symbols $y[n]$ are the result of convolution between CIR h and transmitted symbols $s[n]$ which has a length of N. So, $y[n]$ has a length of $N+L-1$. In addition, the received signal is obtained by concatenating the received

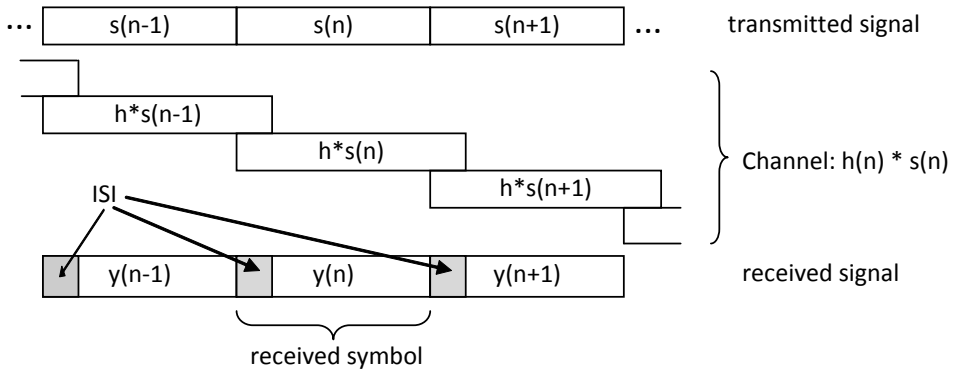

Figure 2.2: OFDM transmission without cyclic prefix results ISI among adjacent symbol

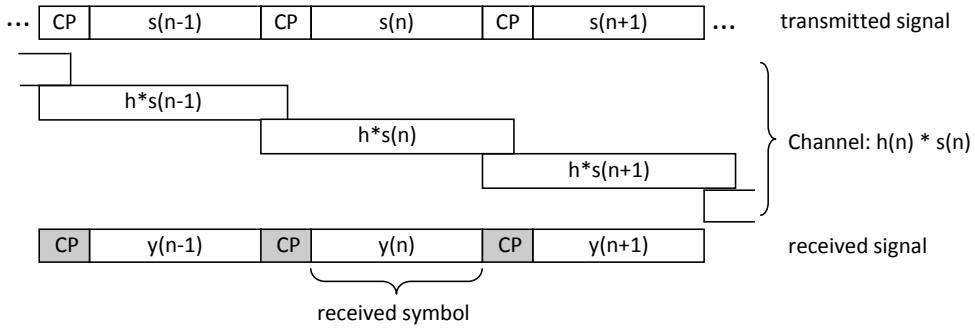

Figure 2.3: OFDM transmission with cyclic prefix avoids ISI among adjacent symbol

OFDM symbols. Because the received symbols, having a length of $N + L - 1$, are overlapped with the adjacent received symbols, adding the overlap of adjacent received symbols leads to the introduction of the Inter Symbol Interference (ISI) in the received signal shown in Fig. 2.2.

In order to avoid ISI, a guard interval (or cyclic prefix), having a length of L_{CP}, has to be added before each OFDM symbol as demonstrated in Fig. 2.3. If the length of CIR, L, is smaller than that of the guard interval, L_{CP}, adding the overlap of adjacent received symbols will not interfere with the succeeding received OFDM symbol. The ISI is hence missing in the received symbol. The guard interval, adopted in standards, can be commonly performed by a copy of the last L_{CP} samples of the symbol as shown in Fig. 2.4, that is called a cyclic prefix (CP)

In addition, the use of CP also guarantees the orthogonality of subcarriers avoiding the ICI. Performing DFT operation and a single-tap equalizer per subcarrier allows recovery of the transmitted symbols [19].

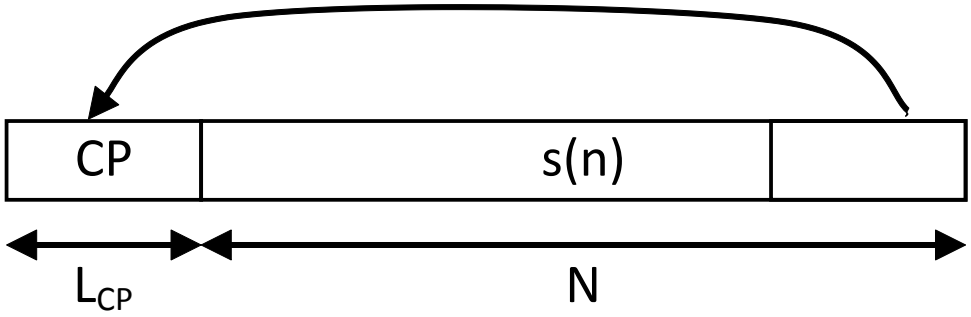

Figure 2.4: Inserting Cyclic Prefix in the OFDM symbol

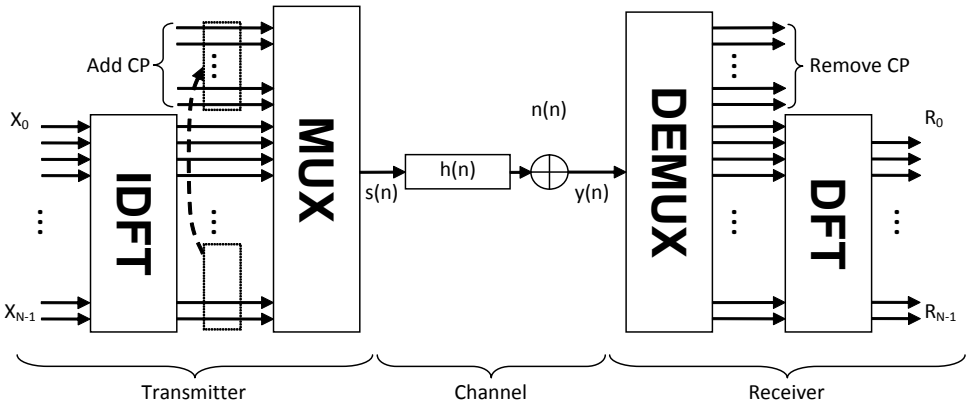

Figure 2.5: the OFDM system model

2.2.2 OFDM-based system

In the above section, the OFDM modulation technique was presented, and inserting CP was introduced to improve the performance of OFDM in multi path channel. A OFDM-based system model can be equivalently considered as shown in Fig. 2.5.

In the transmitter, the data modulated symbols $X[n]$ are grouped in a blocks of N sub-carrier symbols known as an OFDM symbol, expressed by a vector $X[n] = (X[1], X[2], ..., X[n])^T$. Next, the OFDM symbol signal in the time domain is modulated by performing IDFT on each OFDM symbol, and a cyclic prefix of length L_{CP} is inserted at the begin of OFDM signal. So, the complex signal of m, the OFDM-symbol in baseband discrete time, can be expressed as

$$s_m[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{i2\pi k \frac{n-L_{CP}}{N}}, \tag{2.8}$$

where n is the discrete time index, m denotes the index of the OFDM symbol. The complete transmitted signal in the discrete time domain, $s[n]$, is given by the concatenation of all OFDM

symbols, $s_m[n]$,

$$s[n] = \sum_{m=0}^{\infty} s_m[n - m(N + L_{CP})], \tag{2.9}$$

When transmitting OFDM signals over a multi-path channel, the received signal is obtained through the linear convolution of the transmitted symbol with CIR $h[i]$ and adding additive white Gaussian noise (AWGN) n. Assuming that the synchronisation between the transmitter and receiver are perfectly achieved, the channel fading is slow enough to consider as a time invariant channel during one OFDM symbol interval, and the length of cyclic prefix is longer than that of CIR ($h[i] = 0$ for $i < 0 i > L_{CP} - 1$),

$$y[n] = \sum_{i=0}^{L_{CP}-1} h[i]s[n - i] + n[n], \tag{2.10}$$

In the receiver, the incoming samples $y[n]$ are synchronously grouped into block of OFDM symbols and then the cyclic prefix in each OFDM symbol is removed. The received symbols can be expressed in a vector $y_m = (y_1, y_2, ...)$, with $y_m[n] = y[m(Nc+Ncp)+Ncp+n]$. The received data symbols associated with m^{th} OFDM symbol $R_m[n]$ are retrieved by performing a N-point DFT:

$$R_m[n] = \sum_{n=0}^{N-1} y_m[n]e^{-i2\pi \frac{nk}{N}}, \tag{2.11}$$

Fig. 2.6 presents the common block diagram of an OFDM-based RF system. OFDM is perform in the baseband, IFFT and FFT blocks are used to compute IDFT and DFT for OFDM modulation and demodulation, respectively. In the transceiver, the channel coded data from higher abstracted layers is modulated to data symbols (BPSK, QPSK, QAM, ...). The data symbols are then grouped together with the pilots to form N FFT points in parallel. After performing IFFT, the CP is inserted, and then the OFDM samples are serialised and split in to in-phase (I) and quadrature (Q) channels corresponding to the real and imaginary parts of the OFDM sample. The digital to analogue converted signals of I and Q channels are modulated by an intermediate frequency, f_{IF}, then the signal is up-converted to high frequency by an

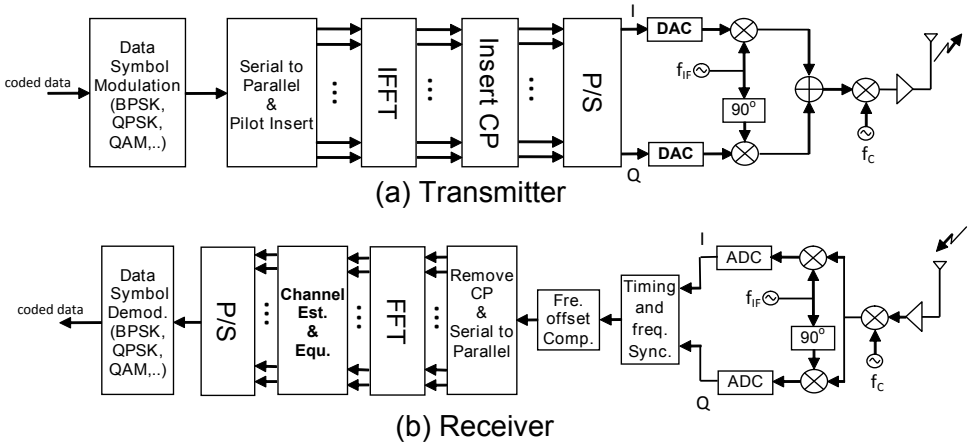

Figure 2.6: The block diagram of OFDM-based RF systems

RF carrier, f_C. Before transmitting, the signal should be amplified by an low noise amplifier (LNA).

In the receiver, after down-converting and IQ demodulation, the signal is sampled. The samples are formed from I and Q channels corresponding to the real and imaginary parts of the OFDM sample. The timing and frequency synchronisation blocks detect the frame, recover timing of the frame and estimate the frequency offset. The received samples are then compensated by estimated frequency offset in the discrete time domain. After demodulating an OFDM symbol using FFT, estimating the channel and then channel equalisation as well as phase error compensation are performed to improve performance. The block of parallel samples in an OFDM symbol is serialised to data symbol sequences that are then demodulated, and coded data is sent to higher abstracted layers to decode.

2.2.3 Evaluating OFDM

The main advantages of OFDM are its spectrally efficient usage and robustness against multi path propagation. This makes OFDM suitable for high performance wireless applications. OFDM uses multiple sub-carriers which are overlapped with other subcarriers in the frequency domain, resulting in greater spectral efficiency than FDM. Performing OFDM is equivalent to splitting a data stream into several parallel low-rate streams before transmission. This makes the OFDM signal more robust against fading when transmitted through the channel. Thanks to the cyclic prefix, the ISI and ICI caused by the multi-path channel can be eliminated. The CP

creates a guard period for an OFDM symbol, which should be longer than the CIR to ensure no ISI. Repeating samples of the OFDM symbol in a guard period, the CP helps to maintain the orthogonality of subcarriers avoiding the ICI. Thus, performing the DFT and a single-tap equalizer per subcarrier allows recovery of the transmitted symbols.

On the other hand, OFDM has some disadvantages. Firstly, an OFDM signal is the sum of multiple modulated sub-carriers, and thus suffers a high peak-to-average power ratio (PAPR). This results in demand on high power and wide range linearity in amplifiers increasing the cost of OFDM-based systems. Secondly, the usage of guard period reduces bandwidth efficiency of OFDM. Last but not least, OFDM performance is sensitive to receiver synchronisation. Frequency offset causes inter-subcarrier interference and errors in timing synchronisation can lead to inter-symbol interference. Much effort is needed to improve the accuracy of both frequency and time synchronizers for OFDM.

2.3 Multiple Standard Cognitive Radios

The spectral resource demands of wireless telecommunication systems continues to increase. Cognitive Radios (CRs), that have ability to adapte to channel conditions, ensuring effective spectrum usage, are an important technology for achieving this. They are designed to transmit in currently unused spectrum without causing harmful interference to primary users (PUs) or incumbent users (IUs). Apart from the critical issues of spectrum sensing and band allocation, the lower priority of secondary users (SUs) raises a challenge in terms of transmission capability and quality of service in cognitive radios. When the spectrum allowed for a CR system is fully occupied by PUs and IUs, the transmission of CRs can be blocked. Multiple Standard Cognitive Radios (MSCRs) are able to operate in multiple frequency bands with different specified standards. MSCRs are hence a more flexible generalisation of CRs as they can operate across different bands and standards.

Multi-carrier modulation techniques offer an ideal opportunity for such systems due to their regularity and parameterisation. OFDM and Filter Bank Multi Carrier (FBMC) are two types of multi-carrier modulations. OFDM modulation has been the dominant technique adopted for many standards and has been investigated in terms of spectral sensing and carrier allocation for CRs. Furthermore, OFDM system implementation is simple, low cost, and can be effectively parameterised in comparison to FBMC systems. OFDM is a suitable candidate for a

MSCR system. The advantages of coupling OFDM modulation with an FPGA platform are investigated for the feasibility of implementing the proposed MSCR system. The flexibility requirement of a MSCR is to support existing standards like 802.11, 802.16, and 802.22, as well as supporting future OFDM-based standards.

A feasible OFDM-based MSCR requires the ability to switch baseband processing from one standard to another. This means that the system needs to rapidly adapt its functionality to perform variable numbers of FFT/IFFT operations, insert CP of configurable length, and handle differend pilot vectors as well as different preambles. The hardware implementation of an OFDM-based MSCR can be based on the original architecture of an OFDM system illustrated in Fig. 2.6. However, each sub-module of the system needs to be designed to perform with all parameters of the supported standards. This results in significantly increasing system complexity as well as reconfiguration time.

Beside the challenge of long configuration time for MSCR, there are two key challenges of the baseband related to the synchronizer and spectral shaper. OFDM systems typically tolerate a small carrier frequency offset (CFO) leading to strict constraints on the design of the RF front-end. In an MSCR system, the RF front-end should access a wide range of frequencies depending on the standard in operation. Such a precise and yet wide ranging frequency requirement makes the RF front-end design difficult if not impossible or require very expensive components. CRs also demand small spectral leakage for both in-band and out-of-band transmitted signals to avoid causing harmful interference to primary users, while OFDM signals have intrinsically large side lobes leading to a potentially large degree of spectral leakage. Flexibility in the baseband can allow a frequency guard extending technique to achieve spectral leakage requirements.

The interface to the higher layer processing is another important factor. Many hardware radio platforms are extremely difficult to design for or to modify. Hence, only hardware experts can use them. While detailed optimisation of low level blocks is important, providing a general interface for implementing higher layer processing is also important. This ensures that radio experts may use the system to investigate cognitive radio techniques without the need for specific advanced low-level FPGA expertise.

2.4 OFDM Synchronisation

OFDM performance is sensitive to receiver synchronisation. Frequency offset causes inter-subcarrier interference, and errors in timing synchronisation can lead to intersymbol interference. Therefore, synchronisation is critical for good performance in OFDM systems. There are two main errors implicit in synchronisation: sample clock timing offsets and carrier frequency offsets. In order to obtain good synchronisation performance, timing offsets and frequency offsets must be studied in terms of their cause and effect on the degradation of OFDM received data symbols. Additionally, there are issues of common phase error (CPE), generated from clock jitter and phase noise, that causes a random rotation of the entire signal constellation. This must also be taken into account and compensated for in order to achieve good performance.

2.4.1 Timing Offsets

When sampling a signal at the receiver, the different times of sampling between samples in the receiver and transmitter are referred as timing error. In a single carrier system, the symbol clock in the transmitter can be recovered at the receiver using a phase-lock loop (PLL) [19]. This can correct a timing error in the receiver relatively easily.

In OFDM, however, timing errors can be considered in two categories: fractional and integer. Fractional timing error, that is errors that are smaller than one sample period, are caused by different phases between the sampling clock of the analogue to digital converter (ADC) in the receiver and the phase of the transmitted signal, while integer timing error is that which is greater than one sample period, causing index shifting, or offset, in the sample sequence.

The timing error in the time domain is equivalent to a phase rotation in the frequency domain expressed in Equ. (2.12),

$$s(t-\tau) \Leftrightarrow e^{-i2\pi f\tau} R(f), \tag{2.12}$$

where τ denotes timing error resulting in a phase shift of $e^{-i2\pi f\tau}$. $s(t)$ is the received signal in the time domain, and $R(f)$ is the spectrum of $s(t)$ in the frequency domain. The phase shift is proportional to both time errors and the frequency of carriers. In the case of multi-carriers with

increasing frequency, the phase shift is increased according to the carriers leading to the phase rotation of subcarriers. Carrier rotations caused by fractional timing error Δt like that caused by fading can be estimated by a channel estimator and compensated for after performing the DFT,

$$\widehat{R[n]} = R[n]e^{\frac{i2\pi n\Delta t}{N}}, \tag{2.13}$$

where $R[n]$, $\widehat{R[n]}$ denotes received data symbols before and after compensation, respectively. Δt is estimated phase rotation, and N is the number of sub-carriers.

Moreover, the received samples in the receiver are synchronously grouped into blocks of OFDM symbols. Integer timing errors lead to a symbol timing offset (STO) referring to the difference between correct sample index and the actual sample index of received samples that causes a misaligned window for DFT demodulation in the receiver. If the timing offset is late, the samples of the following symbol are used for the current symbol, resulting in ISI and hence degrading the performance of the OFDM system. The effect of ISI caused by later timing offsets on the OFDM received symbol is illustrated in Fig. 2.7(a) and Fig. 2.7(c). If the timing offset is early, some samples in the CP of the current symbol are used to calculate the DFT, leading to sub-carrier rotation expressed in Equ.2.12 in the frequency domain. The effect of sub-carrier rotation caused by earlier timing offsets on the OFDM received symbol is illustrated in Fig. 2.7(b) and Fig. 2.7(d).

$$s[n - t_{off}] \Leftrightarrow R[n]e^{\frac{i2\pi nt_{off}}{N}}, \tag{2.14}$$

where $s[n]$, $R[n]$ denotes received data symbols in the timing domain and the frequency domain, respectively. t_{off} is a timing offset, and N is the number of sub-carriers.

Fig. 2.7 illustrates the effect of timing offset on a single 256 subcarrier OFDM symbol utilizing QPSK subcarriers (based on the IEEE 802.16). As can be seen, the earlier timing, for instance timing offsets of 1 and 5, shown respectively in Figs. 2.7(b) and 2.7(d), cause a carriers rotation similar to that of fractional timing errors, and fading that can be estimated by a channel estimator. However, the later timing, for instance timing offsets of 1 and 5, as shown in Figs. 2.7(a) and 2.7(c), lead to ISI that prevents the OFDM constellation from being recovered. Therefore, timing synchronisation is required to correct the timing offset, and avoid ISI.

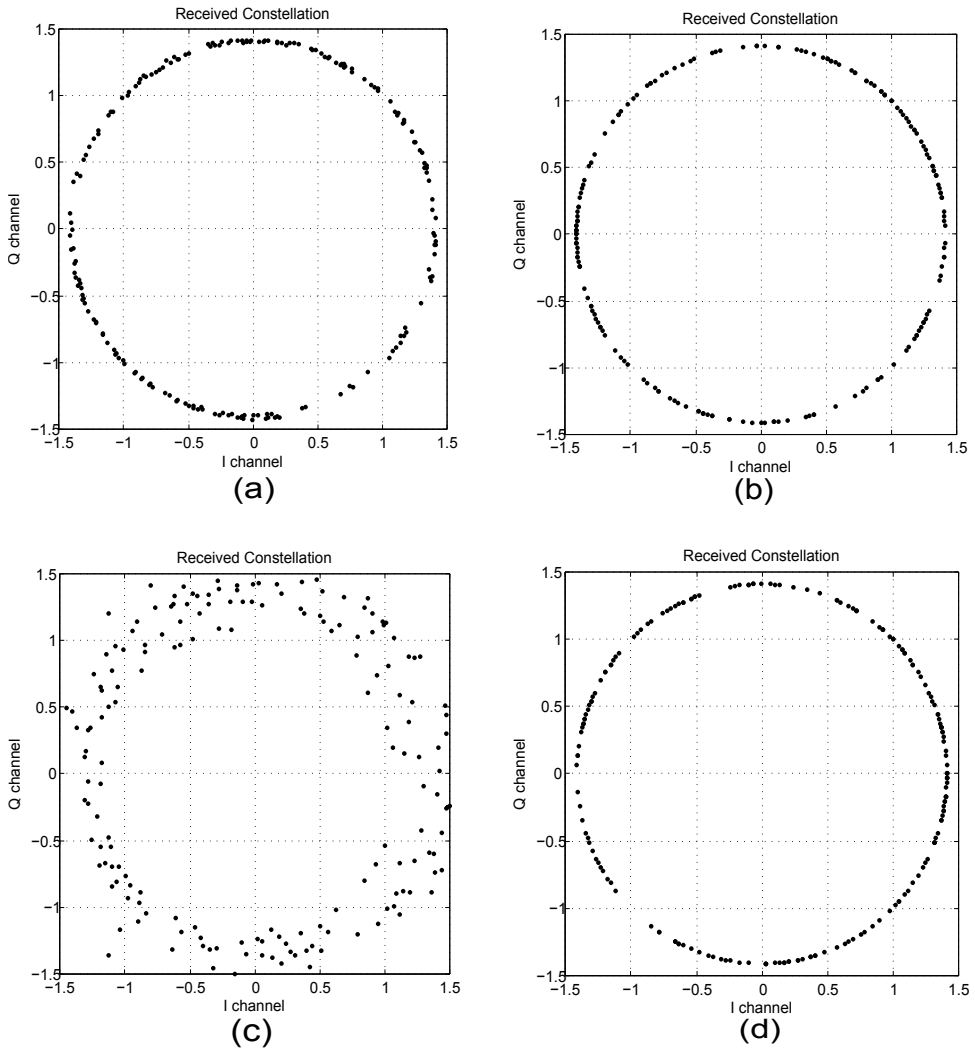

Figure 2.7: OFDM received symbol with timing offets of -1, 1, -5 and 5 in a, b, c, d, respectively.

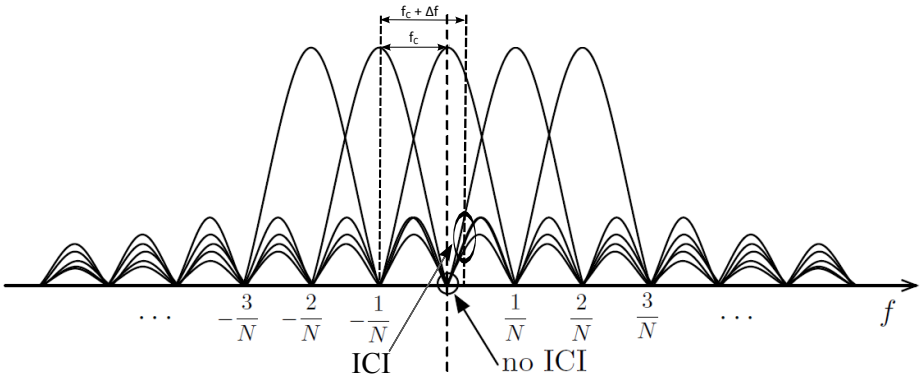

Figure 2.8: Inter carrier interference (ICI) caused by frequency ofsset Δf.

2.4.2 Frequency Offset

CFO refers to a difference in frequency between the receiver clock with respect to the 'correct' frequency of carriers in a transmitted OFDM symbol. CFO is introduced by an imperfect clock in the RF front-end part, as well as by frequency variation caused by the Doppler effect when a signal is transmitted through a frequency selective channel. This leads to the misalignment of sampling in sub-carriers in the frequency domain that causes a loss of orthogonaltity because at the point of frequency offeset in the sub-carrier, the other sub-carriers are not null as expected (shown in Fig. 2.8).

With no frequency offset, the frequency bin of the DFT will be sampled at the value at the peak of each subcarrier, $sinc(x)$ pulse, and other adjacent pulses are null at this point. However, if frequency offset is introduced, the frequency bin of the DFT will sum the energy from other sub-carriers. This means that the adjacent subcarrier introduces an interference component resulting in ICI.

As can be seen, the adjacent subcarrier introduces an interference component that is about half the amplitude of the subcarrier of interest. All other subcarriers introduce an interference component of much lower amplitude. This is known as a loss of orthogonality, and must be compensated for in order to properly demodulate the OFDM symbol. The effect of CFO can be easily considered in the time domain by taking an inverse Fourier transform expressed as follows:

$$R(f - \Delta f) \Leftrightarrow e^{i2\pi\Delta f t} s(t), \tag{2.15}$$

In the discrete time domain, the signal sample sequence can be expressed:

$$s[n]' = s[n]e^{\frac{i2\pi\Delta f n}{N}}, \tag{2.16}$$

where $s[n]'$ and $s[n]$ are the frequency offset samples and the original samples, respectively. Δf denotes the frequency offset, and N is the number of subcarriers.

The effect of frequency offset is shown in Fig. 2.9. Each plot illutrates the constellation of QPSK symbols demodulated from one 256 sub-carrier OFDM symbol based on the IEEE 802.16 standard.

As can be seen, OFDM performance is sensitive to even small frequency offsets. The effect of CFO causes dispersion, similarly to AWGN, and also phase rotation in the QPSK constellation demodulated from OFDM symbol. If multiple data symbols are transmitted in a packet, the phase rotation of each OFDM symbol increases, and even small CFO will lead to a large drift of constellation points, shown in Fig. 2.10 degrading the performance of demodulation. CFO must be estimated and compensated for, in order to properly demodulate the OFDM symbol.

2.4.3 Phase Noise

The intrinsic imperfection of the local clock at the RF front-end of a receiver or clock jitter of an ADC may introduce a parasitic phase noise which can affect the performance of baseband data symbols, such as QPSK, QAM, ..., during demodulation. Phase noise can be considered in two different parts: common phase error and inter-carrier interference [20]. The effect of phase noise can be expressed in the discrete time domain as:

$$s[n]' = s[n]e^{i\phi[n]}, \tag{2.17}$$

where $s[n]$ and $s[n]$ are the frequency offset samples and the original samples, respectively. $\phi[n]$ denotes the phase noise.

If the phase noise is varying more slowly than the OFDM symbol interval, it can be considered a constant phase term added to each sample resulting in CPE [20]. However, if the phase noise is varying much faster than the OFDM interval, different phase noise is added to each sample causing the loss of orthogonality, and thus, intercarrier interference. Fig. 2.11 illustrates the effect of phase noise on baseband data symbol demodulation in an OFDM received symbol and 5 consecutive OFDM received symbols.

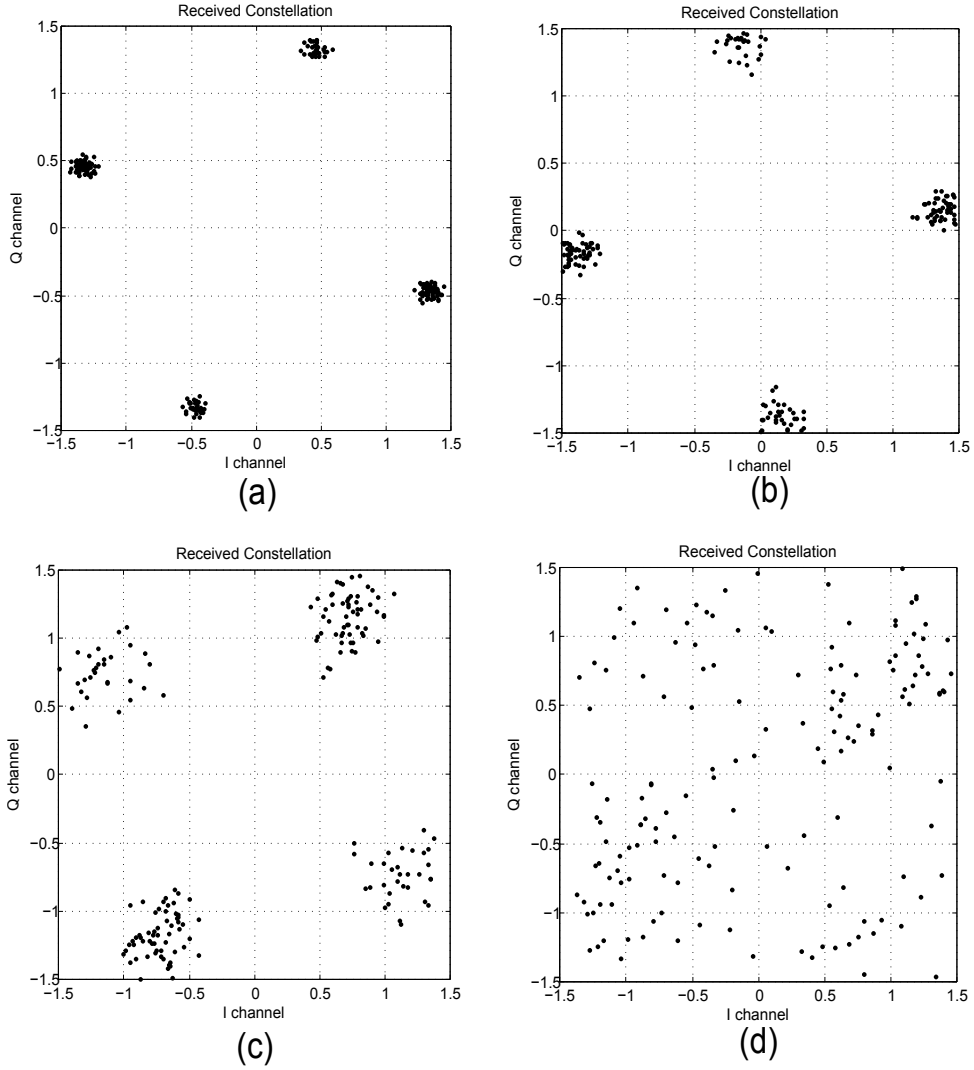

Figure 2.9: The constellations of OFDM received symbol with frequency offets of 0.025, 0.5, 0.1 and 0.25 sub-carries spacing in a, b, c, d, respectively.

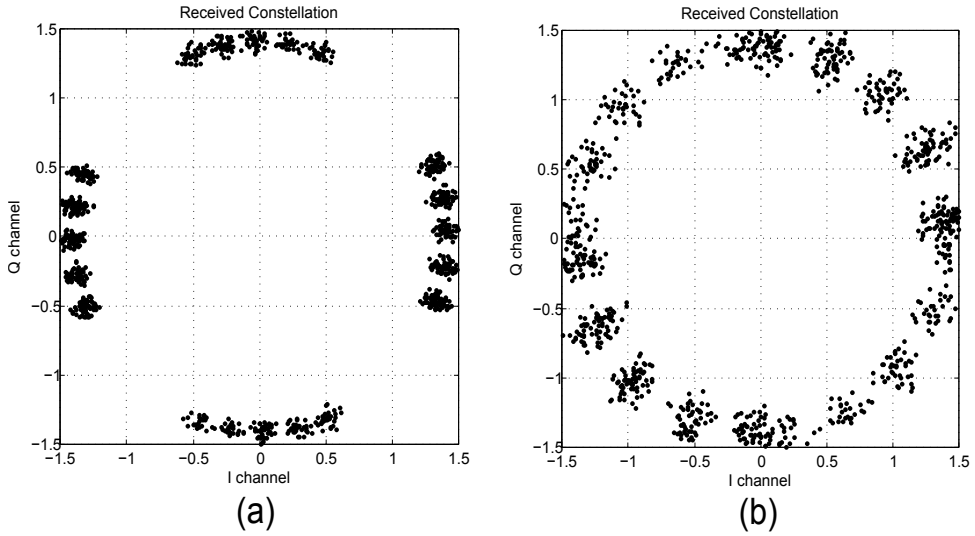

Figure 2.10: The constellations of 5 consecutive OFDM received symbols with frequency offets of 0.025 and 0.05 in a, b respectively.

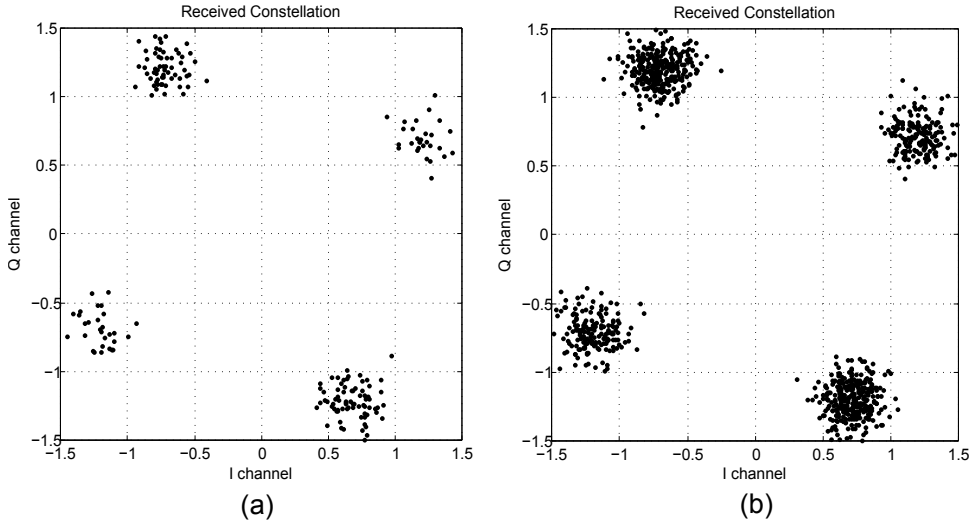

Figure 2.11: The constellations of an OFDM received symbol and 5 consecutive OFDM received symbols with phase noise variance of 0.25 rad^2 in (a), (b) respectively.

As can be seen in Fig. 2.11, the degradation of OFDM demodulation includes two different phenomena affected by phase noise. First, the constellations of the data symbol are rotated similarly to the effect of fractional timing error or residual frequency offset. Second, the constellations of data symbols are dispersed like the effect of AWGN, that causes a loss of orthogonality between the sub-carriers. However, the difference from the effect of frequency offset will be a constant constellation rotation for all OFDM symbol instead of a different constellation rotation for each symbol in the case of frequency offset.

2.5 Shaping OFDM Spectral Leakage

OFDM modulation techniques have been adopted for many wireless standards as well as enabling technology for cognitive radios. However, one of their main disadvantages is spectral leakage due to the summation of sinusoidal subcarriers and having been windowed by a rectangular function. In addition, some recent OFDM-based standards demand very strict requirements on spectral leakage to avoid inter-channel interference. This raises a significant challenge in how to shape the spectrum of the OFDM signal.

In 2009, the FCC issued regulatory rules for reusing the television white space (TVWS) spectrum. IEEE 802.11af was developed under the 802.11 Working Group as a standard that enables a Wi-Fi service in the TVWS spectral regions [21]. The scope of the standard is to define amendments to the high throughput 802.11's PHY and MAC layers to meet the requirements for channel access and coexistence in the TVWS regions. One of the main challenges is the stringent SEM requirements that are mandated by the FCC for these services.. The high throughput 802.11 scaled SEM has a large gap between current performance and the required spectral emissions shape for TVWS [22]. For instance, the 802.11 scaled SEM requires an attenuation of 20 dB at the edge of the channel whereas the equivalent this requirement for portable TV band devices (TVBD) is 55 dB.

In 2010, the IEEE defined a standard for PHY and MAC layers [23], named IEEE 802.11p, for Dedicated Short-Range Communications (DSRC), the wireless channel for new vehicular safety applications through vehicle-to-vehicle (V2V) and Road to Vehicle (RTV) communications. The PHY in 802.11p is largely inherited from the well-established IEEE 802.11a OFDM PHY, with several changes aimed at improving performance in vehicular environments. The

advantage of building on 802.11a is a potential significant reduction in the cost and development effort necessary to develop the new 802.11p hardware and software. It also plays an important role in allowing backwards compatibility from 802.11p to 802.11a [24, 25]. Essentially, three changes are made in IEEE 802.11p [26]: First, 802.11p defines a 10 MHz channel width instead of the 20 MHz used by 802.11a. This extends the guard interval to address the effects of Doppler spread and inter-symbol interference in a VC channel. Secondly, 802.11p defines several improvements in receiver adjacent channel rejection performance to reduce the effect of cross channel interference that is especially important in dense vehicle communication channels. Finally, 802.11p defines four SEMs corresponding to class A to D operations that are specified and issued in FCC CFR47 Sections 90.377 and 95.1509. These are more stringent than for current 802.11 radios, in order to improve performance in urban vehicle scenarios. In addition, 802.11p will operate in the 5.9 GHz DSRC spectrum divided into seven 10 MHz bands. This channelization allows the MAC upper layer to perform multi-channel operations [27]. The mechanism allows safety and other applications to occupy separate channels to reduce interference. The four strict 802.11p SEMs are defined to reduce the effect of ICI between the channels. Wu et al. [28] showed that transmitters on adjacent service channels still cause inter-channel interference (ICI) in the safety channel, even if they satisfy the class C requirement. Shaping 802.11p spectral leakage is thus potentially important in helping to eliminate ICI.

Conventionally, there are two methods that can be employed to compress the spectral leakage for OFDM-based system, namely pulse shaping and image spectrum compression. Pulse shaping, recommended in 802.11a, is effective at reducing side lobes. Considering an OFDM symbol to have IFFT length and CP length N and N_{CP}, respectively, the length of the symbol including its CP is $N_T = N + N_{CP}$, a sample $x[m]$ of the OFDM symbol $(0 \leq m \leq N_T - 1)$ can be expressed in the time domain as,

$$x[m] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{i2\pi \frac{k}{N}(m - N_{CP})}, \tag{2.18}$$

where $X[k]$ denotes the frequency domain representation of the data sub-carriers. Since OFDM symbol samples are generally transmitted sequentially, this is equivalent to multiplying symbols with a rectangular window function, p. Then the transmitted OFDM samples can be

expressed as;

$$x[n] = \frac{1}{N} \sum_{l=-\infty}^{\infty} \sum_{k=0}^{N-1} X[k] p[n - lN_T] e^{i2\pi \frac{k}{N}(n - N_{CP} - lN_T)} \tag{2.19}$$

In a conventional OFDM system, the window function, $p(m)$, is rectangular and simply described as;

$$p[m] = \begin{cases} 1, & m = 0, 1, ..., N_T \\ 0, & otherwise \end{cases} \tag{2.20}$$

In pulse shaping OFDM, the window function, $p[m]$, uses a smooth rather than rectangular pulse resulting in inducing distortion in the subcarriers. One way to avoid this is to add extending parts, i.e. CP and a cyclic suffix (CS) before and after each conventional OFDM symbol respectively, and to multiply the extended symbol with a smoothing function. While the CP in conventional OFDM is used as a guard interval, here it is also used for pulse shaping. Pulse shaping extends the N_T length of the OFDM signal by a roll-off factor, β. The overhead of extending CS results in spectral loss; overlapping of the CP and CS of consecutive symbols shown in Fig. 2.12 is needed to form a transmitted symbol to reduce this loss, but causes ISI in the overlapped region. Pulse shaping using the overlapping method is effectively equivalent to shortening the OFDM guard interval. A larger β obtains greater compression in spectral leakage but reduces the effective guard interval. When βN_T is increased to equal the CP length, the effective guard interval is reduced to zero (no guard interval) to prevent channel-induced ISI.

Image spectrum compression is implemented as an FIR filter to cancel image spectra. The Interpolation can be used at baseband to increase sampling frequency, thereby extending baseband bandwidth. Image spectra are repeats of the original baseband spectrum, present because of interpolation or digital analogue converter (DAC) effects. On one hand, the narrow band gap between main and adjacent image spectra requires a long impulse response FIR filter. On the other hand, according to the performance of FIR expressed in (2.21), the impulse response of the FIR filter h with length L_{FIR} has a similar effect to the impulse response of the overall channel in terms of inducing ISI.

$$y[n] = \sum_{i=0}^{L_{FIR}-1} h[i] x[n - i] \tag{2.21}$$

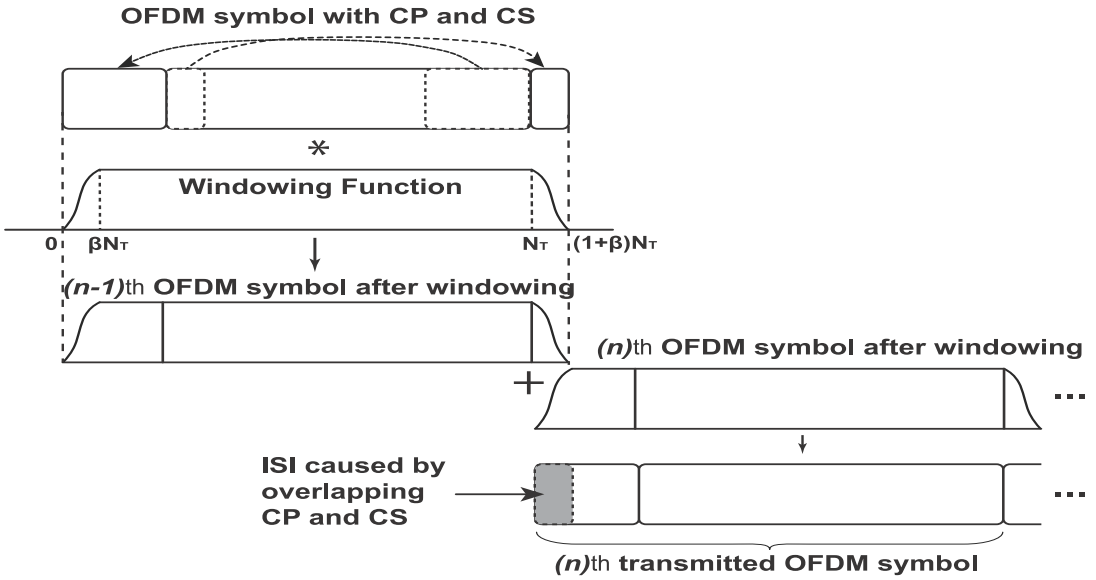

Figure 2.12: Pulse Shaping operation performed on OFDM symbols.

The FIR filter reduces the effective guard interval of OFDM symbols [19]. Its design also needs to deal with the tradeoff between the length of filter to avoid ISI and the transition band and attenuation of the filter to meet the requirement of SEMs.

2.6 Summary

Reducing power dissipation has become a crucial issue in wireless communication systems, especially for portable devices. In this chapter, the power consumption of FPGA systems is discussed. The power estimation and analysis tools of Xilinx are also studied and employed in this research to evaluate the power dissipation of the researched system for power consumption optimisation. Some low-power design strategies are suggested. This chapter also provides the background of OFDM in terms of its mathematical representation and functionality, and then the advantages and limitations of OFDM are also discussed. The concept of a MSRC based on OFDM techniques is presented. The challenges of implementing the MSCR system are introduced regarding the architecture and its performance. The synchronisation effects on the OFDM performance are also considered. Last but not least, the challenge in terms of OFDM spectral leakage are discussed in case of the strict requirements imposed by recent wireless standards.

Chapter 3

Multiplierless Correlator Design for low-power systems

Chapter 4

A Method for OFDM Timing Synchronisation

Chapter 5

A CFO Estimation Method for OFDM Synchronisation

Chapter 6

A Spectrum Efficient Shaping Method

Chapter 7

A Novel Architecture for Multiple Standard Cognitive Radios

Chapter 8

Conclusion and Future Work

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