Power Optimisation for Adaptive Embedded Wideband Radios

A Thesis submitted to
the School of Computer Engineering
of Nanyang Technological University

by

Pham Hung Thinh

in fulfillment of the requirement for
the Degree of Doctor of Philosophy of
for Computer Engineering

March 24, 2015

Publications

Journals

J1. **T. H. Pham**, S. A. Fahmy, and I. V. McLoughlin, "Low-power correlation for IEEE 802.16 synchronisation on FPGA," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 8, pp. 15491553, Aug. 2013.*

J2. **T. H. Pham**, I. V. McLoughlin, and S. A. Fahmy, "Robust and Efficient OFDM Synchronisation for FPGA-Based Radios," *Circuits, Systems, and Signal Processing, vol. 33, no. 8, pp. 24752493, Aug. 2014, Springer.*

Conferences

C1. **T. H. Pham**, I. V. McLoughlin, and S. A. Fahmy, "Shaping Spectral Leakage for IEEE 802.11p Vehicular Communications," in *Proceedings of the IEEE Vehicular Technology Conference (VTC Spring), Seoul, Korea, May 2014.*

C2. **T. H. Pham**, S. A. Fahmy, and I. V. McLoughlin, "Efficient Multi-Standard Cognitive Radios on FPGAs," PhD Forum Poster in *Proceedings of the International Conference on Field Programmable Logic and Applications (FPL), Munich, Germany, September 2014.*

Papers under Review

J3. **T. H. Pham**, S. A. Fahmy, and I. V. McLoughlin, "Enhanced OFDM Synchronization Through Novel Integer Frequency Offset Estimation Architecture,"

J4. **T. H. Pham**, S. A. Fahmy, and I. V. McLoughlin, "Spectrally Efficient Emission Mask Shaping for OFDM Cognitive Radios,"

J5. **T. H. Pham**, S. A. Fahmy, and I. V. McLoughlin, "Efficient Multi-Standard Cognitive Radios on FPGAs,"

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Wireless transmission plays a key role in our everyday lives, and has enabled the exponential growth in connectivity that we have witnessed over the last few decades. An exponential increase in the number of users and nodes, and the throughput demanded between them, means significant developments are crucial in the fundamental methods by which this wireless communication is enabled. The previous approach of defining fixed wireless standards for use in fixed portions of radio spectrum is giving way to a more dynamic approach to exploiting this scarce resource. Practical studies have shown that many licensed bands are relatively unused across time and frequency [1]. To improve the efficiency of radio spectrum use, the concept of unlicensed users temporarily reusing unused spectrum in licensed bands is currently being researched. This concept is known as dynamic spectrum access (DSA) [2]. Wireless communication systems for realising DSA must be reconfigurable, to support different radio standards in different environments, and adaptive, to react to changing channel conditions without interfering with licensed users and other unlicensed opportunistic users.

A cognitive radio (CR) is a node that is able to adapt its parameters to optimise performance based on interaction with the environment, as well as to perform DSA. A cognitive radio can modify parameters such as transmit power, coding rate, frame size, bandwidth, and centre frequency, in real time, to obtain suitable performance in a changing, environment. The radio baseband should also be reconfigurable to enable support for multiples standards such as WiFi, WiMAX, GSM, WCDMA, and other defined access schemes. More advanced adaptive standards are intrinsically flexible and this flexibility should be managed to optimise performance in the channel.

This thesis explores techniques for enabling the mapping and implementation of dynamic cognitive radios on FPGA platforms. By dynamic, we are referring to the ability to modify baseband processing to suit difference transmission standards and scenarios. The cognitive portion of a radio is where decisions are made to modify properties of the communication. In the context of our work, we are interested in providing a generalised interface for cognitive radio designers to be able to leverage the dynamic capabilities of the hardware platform at a higher level.

FPGAs are silicon devices that allow us to build customised hardware datapaths for a variety of applications. By exploiting parellelism inherent in many algorithms, it is possible to develop implementations that are significantly faster than equivalent software running on general purpose processors. FPGAs have long been established as a platform of choice in signal processing due to their suitability for parallel bit-level architectures that align well with many signal processing algorithms [3]. Another key capability of FPGAs that makes them attractive for cognitive radios is their reconfigurability. The hardware implemented on an FPGA can be modified at runtime, thereby enabling the dynamic capability required for implementing cognitive radios. While a number of radio research groups have used FPGAs in their platforms, we believe our FPGA expertise can help develop a platform that is both easier to use, and that exploits the more advanced capabilities of FPGAs.

Orthogonal Frequency Division Multiplexing (OFDM) is commonly adopted for CR implementation, and is a prime candidate for DSA, where the radio is required to be spectrally aware and able to dynamically access idle parts of the spectrum. It is an efficient multicarrier modulation (MCM) technique that provides robustness to frequency selective channels and a DSA ability based upon spectrum pooling, where unlicensed users may temporarily access spectral resources during the idle periods of licensed users [4]. Furthermore, when utilising a given spectral channel, OFDM subcarriers that cause interference with licensed users can be selectively disabled. This technique is known as non-contiguous orthogonal frequency multiplexing (NC-OFDM) [5]. OFDM is currently the dominant technique for multiple applications in high bit-rate wireless communication systems such as Wireless Local Area Networks (WLAN) standardized in IEEE 802.11 and Metropolitan Area Networks (MAN) in IEEE 802.16. In terms of implementation, OFDM has relatively simple hardware requirements, and the ability to effectively parameterise key parameters to switch between OFDM-based standards.

Multiple Standard Cognitive Radios (MSCRs) are those with the agility to operate in multiple frequency bands with different specified standards and are hence a more flexible generalisation of CRs.Given the ability to perform spectral sensing, and handle flexible carrier allogation, OFDM is widely considered a suitable candidate for future MSCR systems.

1.1 Motivation

In practice, implementing an MSCR requires a technology platform to provides sufficient flexibility, high computational throughput, and ideally power efficiency. While most practical CRs are built using powerful general purpose processors to achieve flexibility through software, these often fail to achieve the required computational throughput and suffer from high power consumption. Multiple processor-on-chip (MPoC) architectures can meet the throughput needs, however these platforms require algorithms to be formulated in a way suitable for parallel programming. They also tend to rely upon additional memory elements to buffer data being transferred between parallel processes, driving up implementation cost and power consumption. By contrast, custom hardware designs such as application specific integrated circuits (ASICs) offer highly efficient computation, high data throughput and potentially low power dissipation; however, they suffer from a lack of flexibility, in that many operating parameters will need to be fixed at design time. In an application area characterised by multiple fast moving standards, ASICs are likely to be inefficient in terms of both time and cost for MSCR. However, modern FPGAs which support partial reconfiguration (PR), are an attractive candidate for cognitive radios. They not only achieve the high performance of a custom data-path implementation, but also offer design flexibility and the potential for low power dissipation.

The feasibility of MSCR implementation depends on the ability to flexibly switch system parameters from those specified for one standard to those specified for another.

Given the advantages and flexibility of OFDM modulation and the benefits of the FPGA platform, a combination of these technologies is likely to be a good candidate for MSCR implementation. The ability to perform PR in FPGA and allow effective parameterisation of OFDM modulation enable an MSCR to be built not only for current OFDM-based standards such as 802.11, 802.16, and 802.22, but also be potentially able to accept soft upgrades for future OFDM-based standards.

1.2 Objectives

Despite having several advantages for MSCR, OFDM has two particular disadvantages related to synchronisation and spectral leakage. These become critical challenges when OFDM is used for MSCR. Firstly, the state of the art OFDM synchronisation methods can only tolerate a small carrier frequency offset (CFO), leading to very strict constraints for RF front-end design. In MSCR systems, an RF front-end is required to have the ability to rapidly switch frequency carriers across a wide frequency range. Such agility is difficult to achieve while ensuring that CFO is tightly constrained. New synchronisation methods are therefore required for use in OFDM-based MSCR systems that are robust to large CFO: one such novel method is introduced in this thesis.

Secondly, CRs normally demand small spectral leakage for both in-band and out-of-band of transmitted signals, whereas OFDM is well known to induce significant amounts of spectral leakage. Pulse shaping techniques that are able to limit OFDM spectral leakage have been widely researched, but pulse shaping cannot help to effectively filter out-of-band spectrum when only small frequency guards are present, because of the influence of an image spectrum caused by interpolation or DAC operation. Fortunately, MSCR systems provide flexible parameterisation, allowing the proposal in this thesis of a frequency guard extending technique which can meet the spectral leakage requirements.

The overriding objective for this research is a low power and agile architecture for MSCR, based on coupling PR modules and parameterised modules, incorporating the spectral leakage and synchronization methods mentioned above.

1.3 Research Contributions

This thesis addresses the design of flexible MSCRs on FPGAs. This includes contributions at a platform level, algorithm level and signal processing techniques, creating a general OFDM-based FPGA architecture with a high level of adaptation and parameterization. In detail, the research contributions include:

(i) A multipilerless cross-correlation technique for OFDM timing synchronisation, demonstrating low power and low resource utilisation on modern FPGA devices. We show that

DSP blocks, while functionally suited to such tasks, increase power consumption and do not offer improved synchronisation accuracy. We show that wordlength can be optimised to maintain synchronisation performance while minimising area, and also making the design suitable for FPGA devices with a small number of DSP blocks like the low power Xilinx Spartan 6.

(ii) A novel OFDM synchronisation method combining robust performance with computational efficiency. We introduce an improved timing metric for synchronisation, resulting in significant efficiency improvements over other methods in the literature. This provides robust fractional CFO estimation and STO estimation over a range of channels. In particular, it is robust to larger CFO ranges than many state-of-the-art synchronization implementations can handle. We demonstrate efficient resource usage and reduced power consumption compared to existing methods, and this is explored as a fine-grained trade-off between performance and power consumption.

(iii) A novel IFO estimation technique that reduces both the power and computational cost in robust OFDM implementations. Performing the IFO cross-correlation using four-fold resource sharing reduces the estimation cost. Meanwhile, adopting a multiplierless technique and carefully optimising word lengths yields significant power reduction, while maintaining sufficient accuracy to meet synchronisation requirements. Performance is significantly better than conventional techniques, while being much more efficient. Robust OFDM synchronisation with IFO estimation at baseband is important to allow the RF front-end specification to be relaxed, thus reducing system cost. In fact, for some multi-standard radios, and applications suffering significant Doppler shift, RF constraints may be infeasible without techniques such as IFO estimation.

(iv) A novel filtering scheme for adaptively shaping the spectral leakage of OFDM signals according to the transmitted power and Spectrum Emission Mask (SEM) requirements. Recent OFDM-based standards such as 802.11p for vehicular communication and 802.11af for reusing Television White Spaces (TVWS) impose strict limits on spectral leakage, setting a difficult challenge for front-end radio frequency (RF) circuits. The method proposed in this reearch is the first implementation technique that can achieve the specification for the most stringent SEM of 802.11p. For 802.11af, it not only meets the requirement for strict SEM filtering but also enables increased spectral efficiency by allowing 10 more subcarriers than conventional techniques per basic channel band, without violating the SEM specifications.

(v) A system-level approach for designing multi-standard radios on FPGAs. We show that by mixing partial reconfiguration (PR) with static parameterised modules, it is possible to minimise reconfiguration time compared to a full PR implementation. We also show that it is possible to buffer internal data while reconfiguring the radio, leading to no loss during reconfiguration.

Each of these contributions solves one of the pressing challenges of implementing OFDM-based MSCR on FPGA and, taken together, moves the research community closer to future MSCR products.

1.4 Organisation

This thesis is organized as follows: Chapter 2 presents a comprehensive background on cognitive radio platforms and OFDM techniques. It also discusses relevant background knowledge relating to FPGAs and power considerations. Chapter 3 presents the multiplierless correlation technique for OFDM synchronisation. In Chapter 4, our combined CFO and STO synchronisation design is outlined and evaluated. Chapter 6 considers spectral leakage for OFDM-based cognitive radios, and proposes a mitigation technique which is assessed for use with both 802.11p and 802.11af. Chapter 7 discusses the system-level design approach for cognitive radio implementation on FPGAs, which combines the techniques discussed in earlier chapters into a cohesive MSCR approach. Finally, Chapter 8 concludes the thesis and presents several extensions for future work in this domain.

1.5 Publications

Some of the work presented in the thesis has been written up in a number of published and submitted papers listed below:

(i) T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Low-power correlation for IEEE 802.16 synchronisation on FPGA," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 8, pp. 1549 - 1553, Aug. 2013.

(ii) T. H. Pham, I. V. McLoughlin, and S. A. Fahmy, "Robust and Efficient OFDM Synchronisation for FPGA-Based Radios," in *Circuits, Systems, and Signal Processing*, vol. 33, no. 8, pp. 2475 - 2493, Aug. 2014, Springer.

(iii) T. H. Pham, I. V. McLoughlin, and S. A. Fahmy, "Shaping Spectral Leakage for IEEE 802.11p Vehicular Communications," in *Proceedings of IEEE Vehicular Technology Conference (VTC Spring)*, Seoul, Korea, May 2014.

(iv) T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Efficient Multi-Standard Cognitive Radios on FPGAs," PhD Forum Poster in *Proceedings of the International Conference on Field Programmable Logic and Applications (FPL)*, Munich, Germany, September 2014.

(v) T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Efficient Integer Frequency Offset Estimation Architecture for Enhanced OFDM Synchronisation," under review for *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.

(vi) T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Spectrally Efficient Emission Mask Shaping for OFDM Cognitive Radios," under review for *IEEE Transactions on Communications (TCOM)*.

(vii) T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Efficient OFDM-based baseband processing for Multi-Standard Cognitive Radios on FPGAs," in preparation for submission to *ACM Transactions on Embedded Computing Systems*.

Chapter 2

Background Literature

Chapter 3

Multiplierless Correlator Design for low-power systems

Chapter 4

A Method for OFDM Timing Synchronisation

Chapter 5

A CFO Estimation Method for OFDM Synchronisation

Chapter 6

A Spectrum Efficient Shaping Method

Chapter 7

A Novel Architecture for Multiple Standard Cognitive Radios

Chapter 8

Conclusion and Future Work

References

[1] Federal Communications Commission, "Spectrum policy task force report," Tech. Rep. No. 02135, 2002.

[2] R. Rajbanshi, A. M. Wyglinski, and G. J. Minden, "OFDM-based cognitive radios for dynamic spectrum access networks," in *Cognitive Wireless Communication Networks*, pp. 165–188, Springer US, 2007.

[3] M. Cummings and S. Haruyama, "FPGA in the software radio," *IEEE Communications Magazine*, vol. 37, pp. 108–112, Feb. 1999.

[4] T. A. Weiss and F. K. Jondral, "Spectrum pooling: An innovative strategy for the enhancement of spectrum efficiency," *IEEE Radio Communications*, March 2004.

[5] R. Rajbanshi, A. M. Wyglinski, and G. J. Minden, "An efficient implementation of NC-OFDM transceivers for cognitive radios," in *Proceedings of the 1st International Conference on Cognitive Radio Oriented Wireless Networks and Communications*, June 2006.