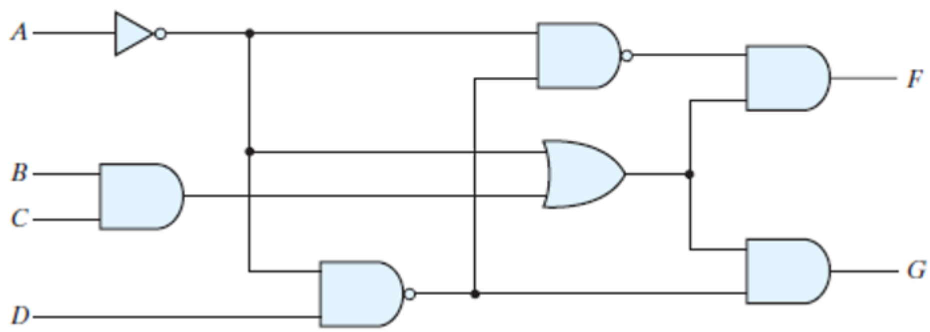
Assignment 4

[1] Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the circuit of the Fig.



AB\CD	00	01	11	10
00		1	1	
01		1	1	
11			1	1
10				

F=A’D+ABC

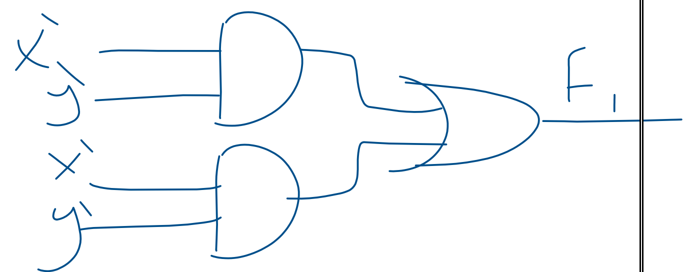
AB\CD	00	01	11	10
00	1			1
01	1			1
11			1	1
10				

G=A’D’+ABC

[2] **Design a combinational circuit with three inputs and one output.**

(a) The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.

x y z	F1
000	1
001	1
010	1
011	0
100	0
101	0
110	0
111	0

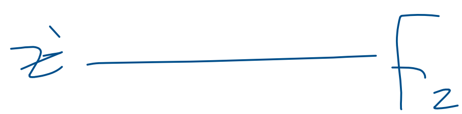


xy \ z	0	1
00	1	1
01	1	
11		
10		

=x'z'+x'y'

(b) The output is 1 when the binary value of the inputs is an even number.

x y z	F2
000	1
001	0
010	1
011	0
100	1
101	0
110	1
111	0

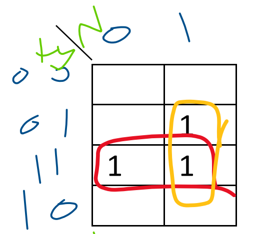


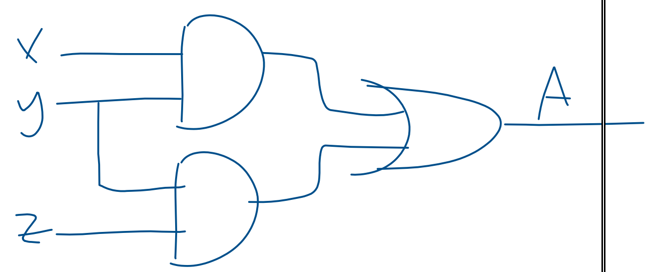
xy \ z	0	1
00	1	
01	1	
11	1	
10	1	

=z'

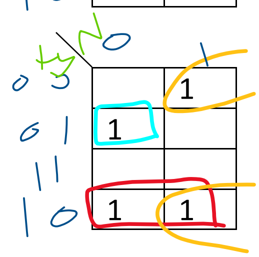
[3] Design a combinational circuit with three inputs, x , y , and z , and three outputs, A, B, and C . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input

x y z	A B C
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	0 1 0
1 0 1	0 1 1
1 1 0	1 0 0
1 1 1	1 1 1

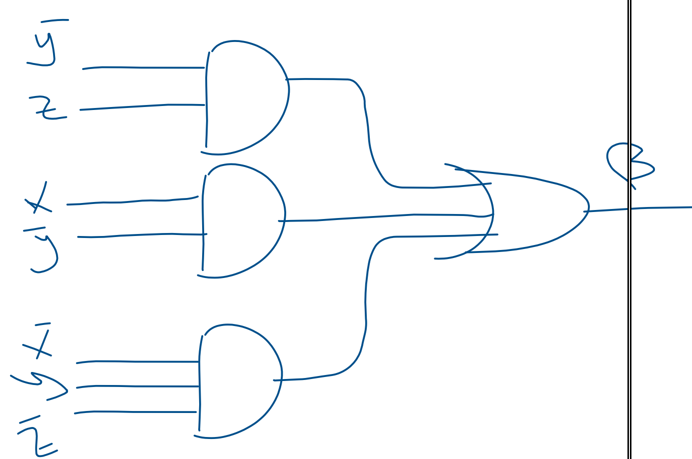


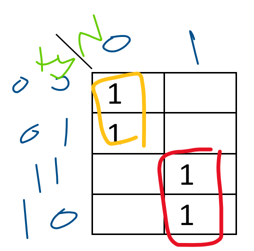


A=xy+yz



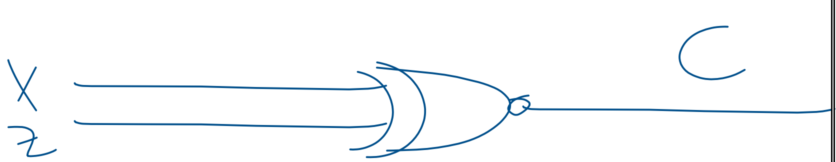
B=xy’+y’z+x’yz’





C=xz+x’z’

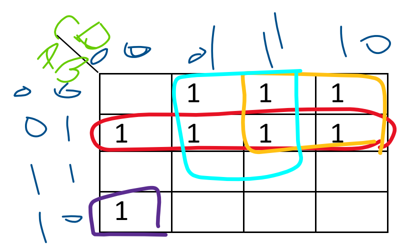
C = (X⊕Z)’ XNOR



[4] Design a four-bit combinational circuit 2’s complementer. (The output generates the 2’s complement of the input binary number.)

A B C D	w x y z	
0 0 0 0	0 0 0 0	M0
0 0 0 1	1 1 1 1	M1
0 0 1 0	1 1 1 0	M2
0 0 1 1	1 1 0 1	M3
0 1 0 0	1 1 0 0	M4
0 1 0 1	1 0 1 1	M5
0 1 1 0	1 0 1 0	M6
0 1 1 1	1 0 0 1	M7
1 0 0 0	1 0 0 0	M8
1 0 0 1	0 1 1 1	M9
1 0 1 0	0 1 1 0	M10
1 0 1 1	0 1 0 1	M11
1 1 0 0	0 1 0 0	M12
1 1 0 1	0 0 1 1	M13
1 1 1 0	0 0 1 0	M14
1 1 1 1	0 0 0 1	M15

w

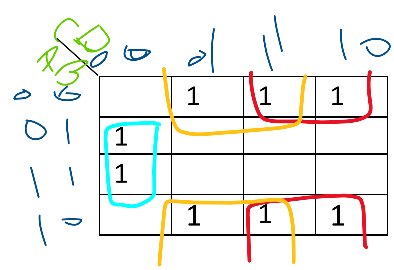


w=A’B+A’D+A’C+AB’C’D’

w= A’ (B+C+D) + A (B+C+D)’

w= A ⊕ (B+C+D)

x



x=B’D+B’C+BC’D’

x= B’ (C+D) + B (C+D)’

x= B ⊕ (C+D)

y

AB \ CD	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

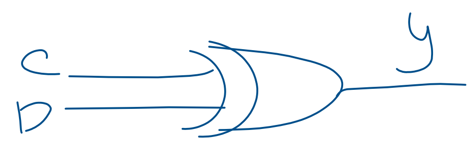
y= C’D + CD’

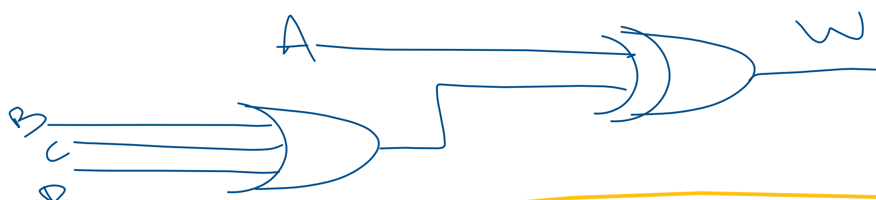
y= C ⊕ D

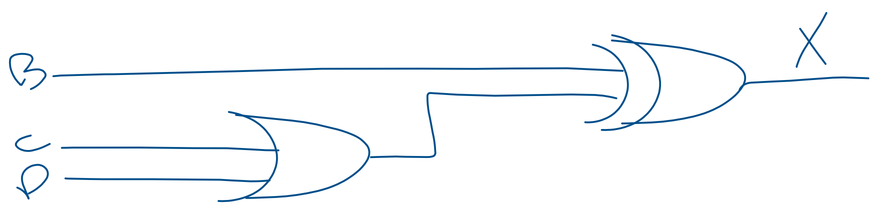
z

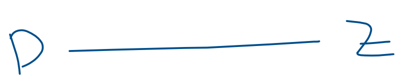
AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

Z= D



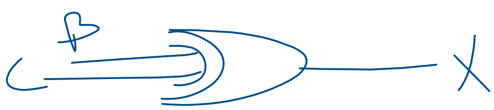






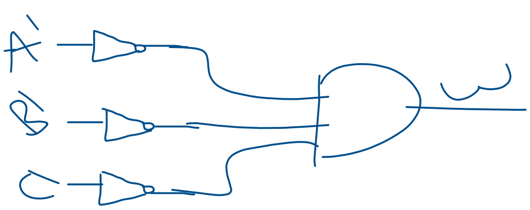
[5] **Design a combinational circuit that generates the 9's complement of a BCD digit.**

BCD	9's
ABCD	WXYZ
0000	1001
0001	1000
0010	0111
0011	0110
0100	0101
0101	0100
0110	0011
0111	0010
1000	0001
1001	0000
1010	XXXX
1011	XXXX
1100	XXXX
1101	XXXX
1110	XXXX
1111	XXXX



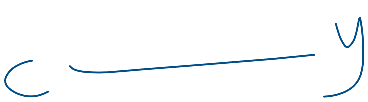
AB \ CD	00	01	11	10
00			1	1
01	1	1		
11	X	X	X	X
10			X	X

X=B'C+BC' = B⊕C



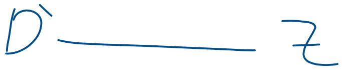
AB \ CD	00	01	11	10
00	1	1		
01				
11	X	X	X	X
10			X	X

W=A'B'C'



AB \ CD	00	01	11	10
00			1	1
01			**1**	1
11	X	**X**	X	X
10			X	X

Y=C



AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	**X**	X	X
10	**1**			X

Z=D'

[6] Design the following circuits:

(a) Design a half-subtractor circuit with inputs x and y and outputs Diff and Bout. The circuit subtracts the bits x – y and places the difference in D and the borrow in Bout.

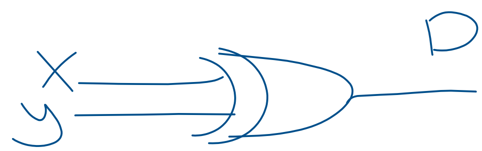
a)

x	y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

B = x'y

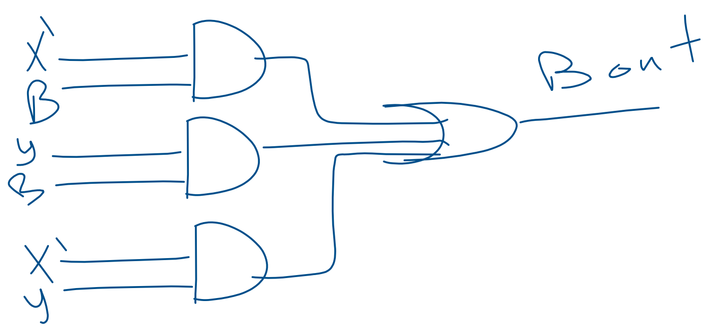
D= x'y + xy'

D= x ⊕ y



(b) Design a full-subtractor circuit with three inputs x, y, Bin and two outputs Diff and Bout. The circuit subtracts x – y – Bin , where is the input borrow, Bout is the output borrow, and Diff is the difference.

x	y	Bin	Buot	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



xy \ Bin	0	1
00		1
01	1	1
11		1
10		

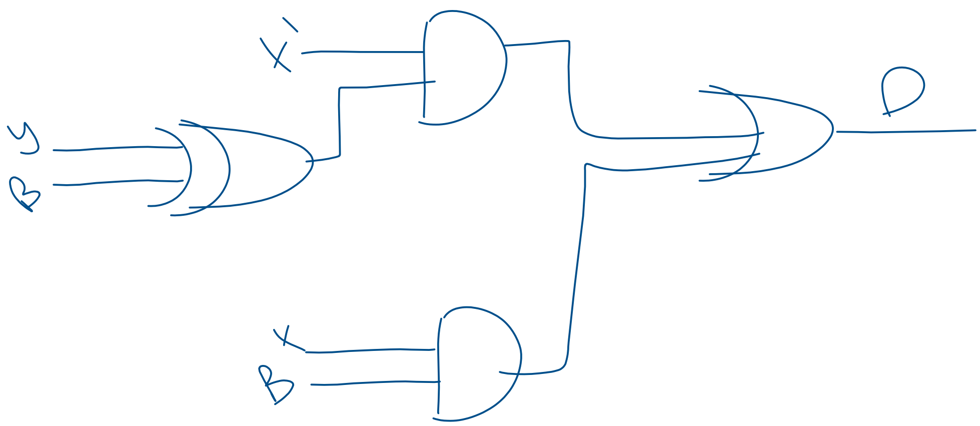
Bout=x'y+yB+x'B

xy \ Bin	0	1
00		1
01	1	
11		1
10	1	

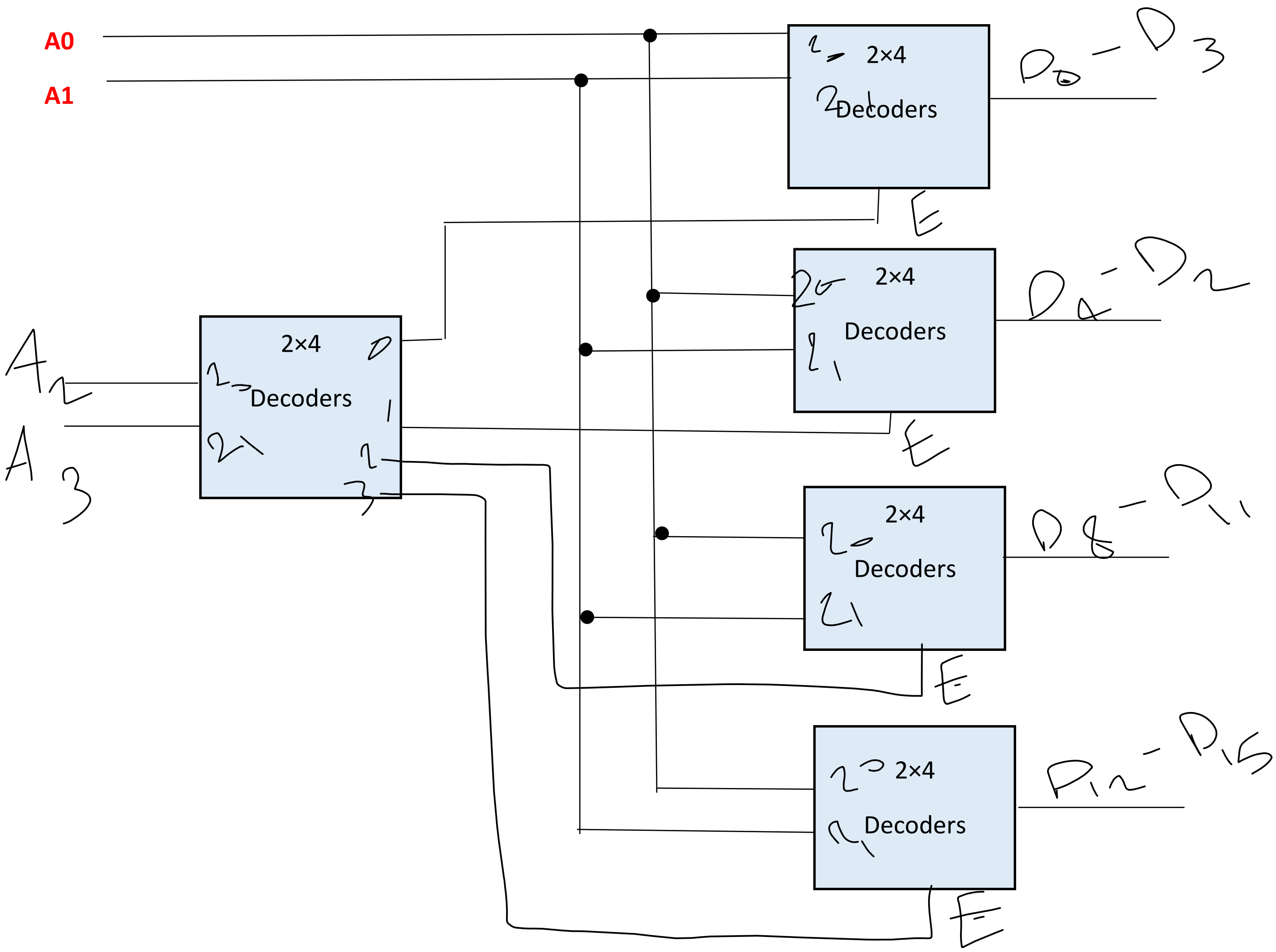
$D = x'yB' + xy'B' + xyB + x'y'B$

$= x'(yB' + y'B) + xy'B' + xyB$

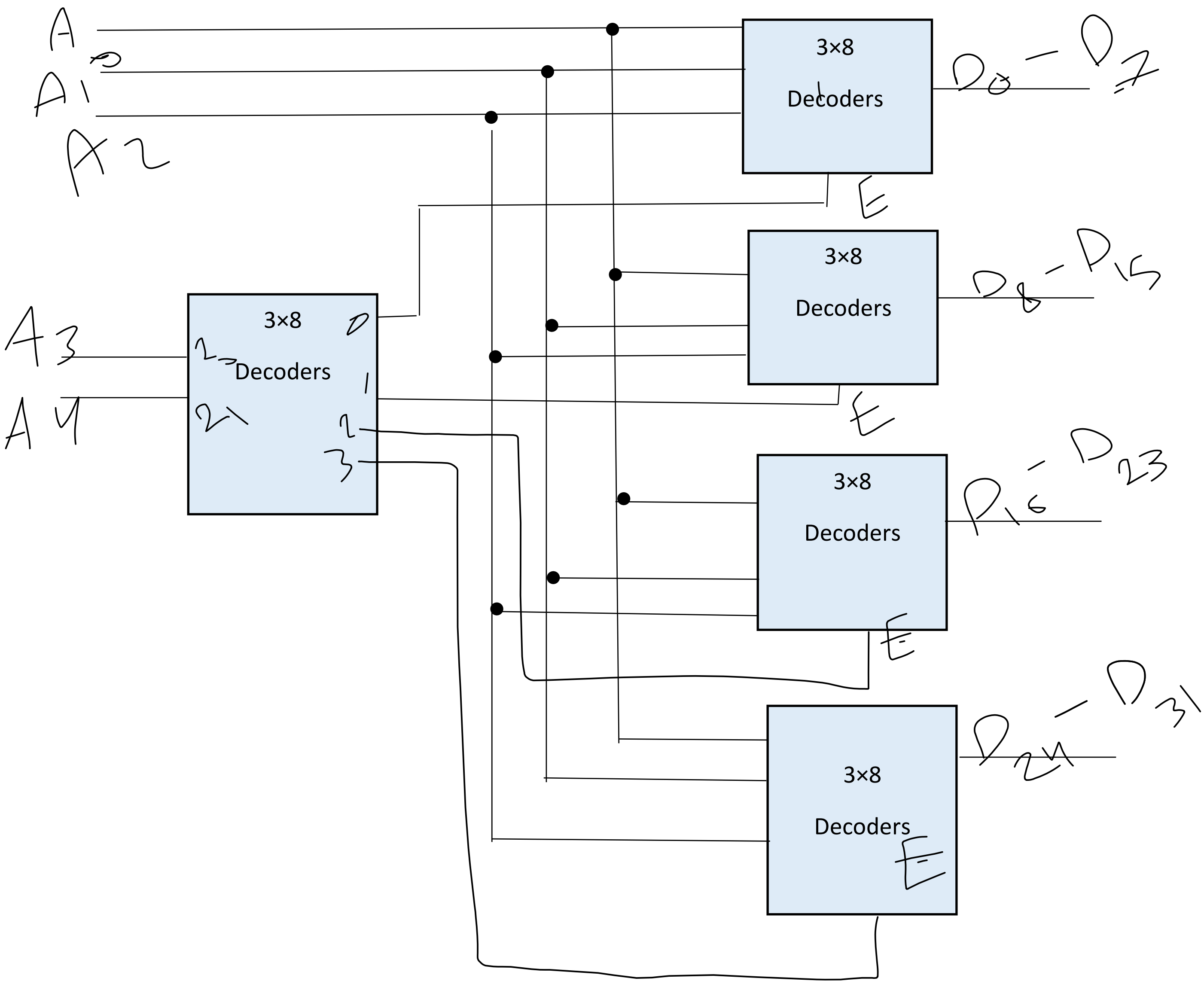
$= x'(y \oplus B) + xB$



[7] Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.



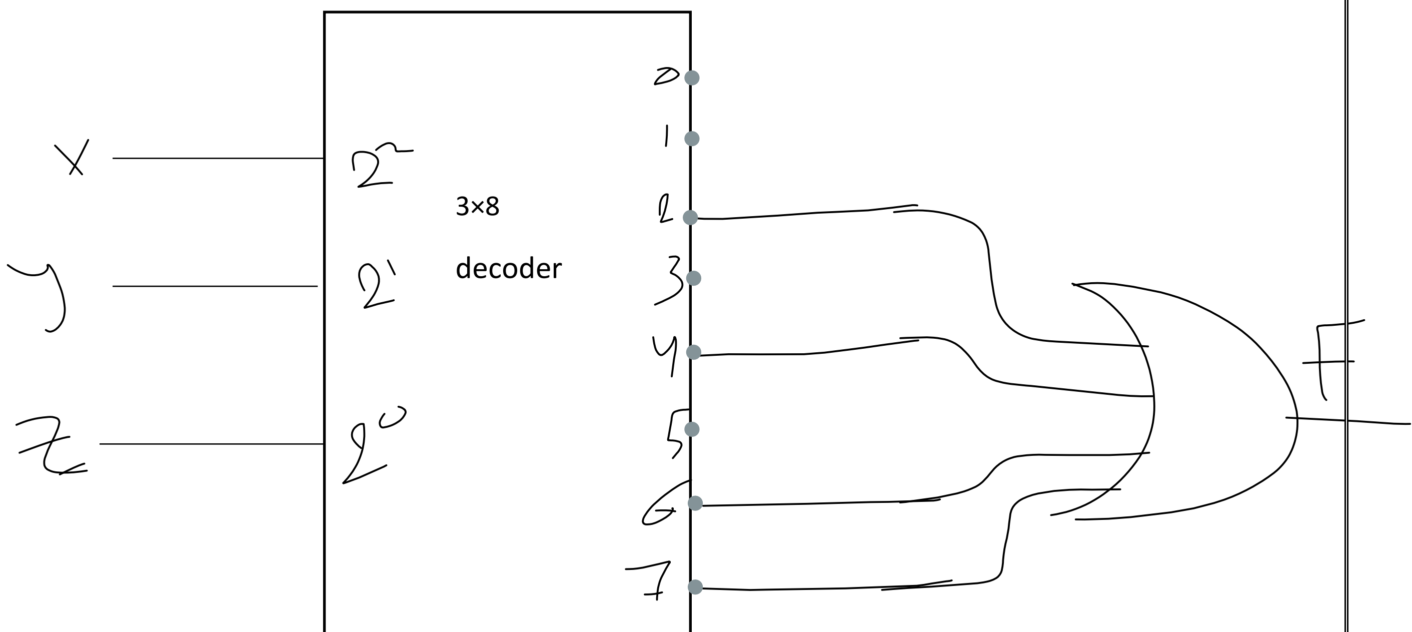
[8] Construct a 5-to-32-line decoder with enable by using 3-to-8 and 2-to-4-line decoders with enables



[9] A combinational circuit is specified by the following Boolean function:

$F(x,y,z) = \sum(2,4,6,7)$

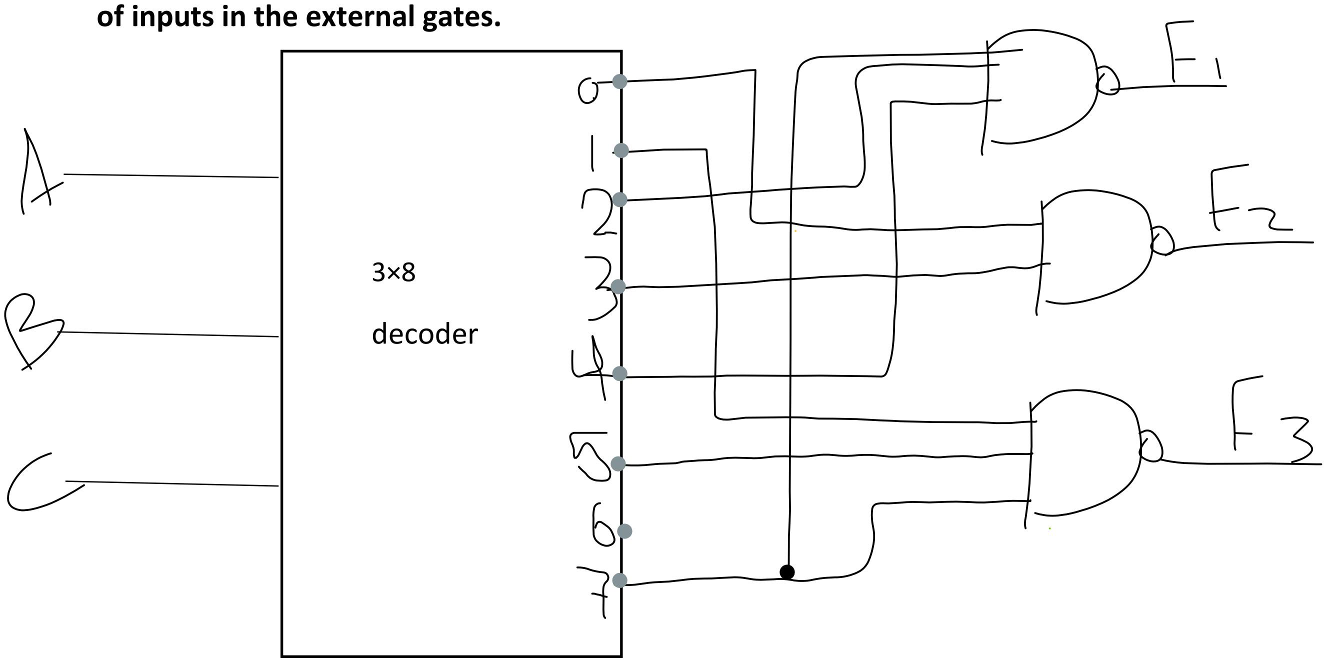
Implement the circuit with a decoder and external gates.



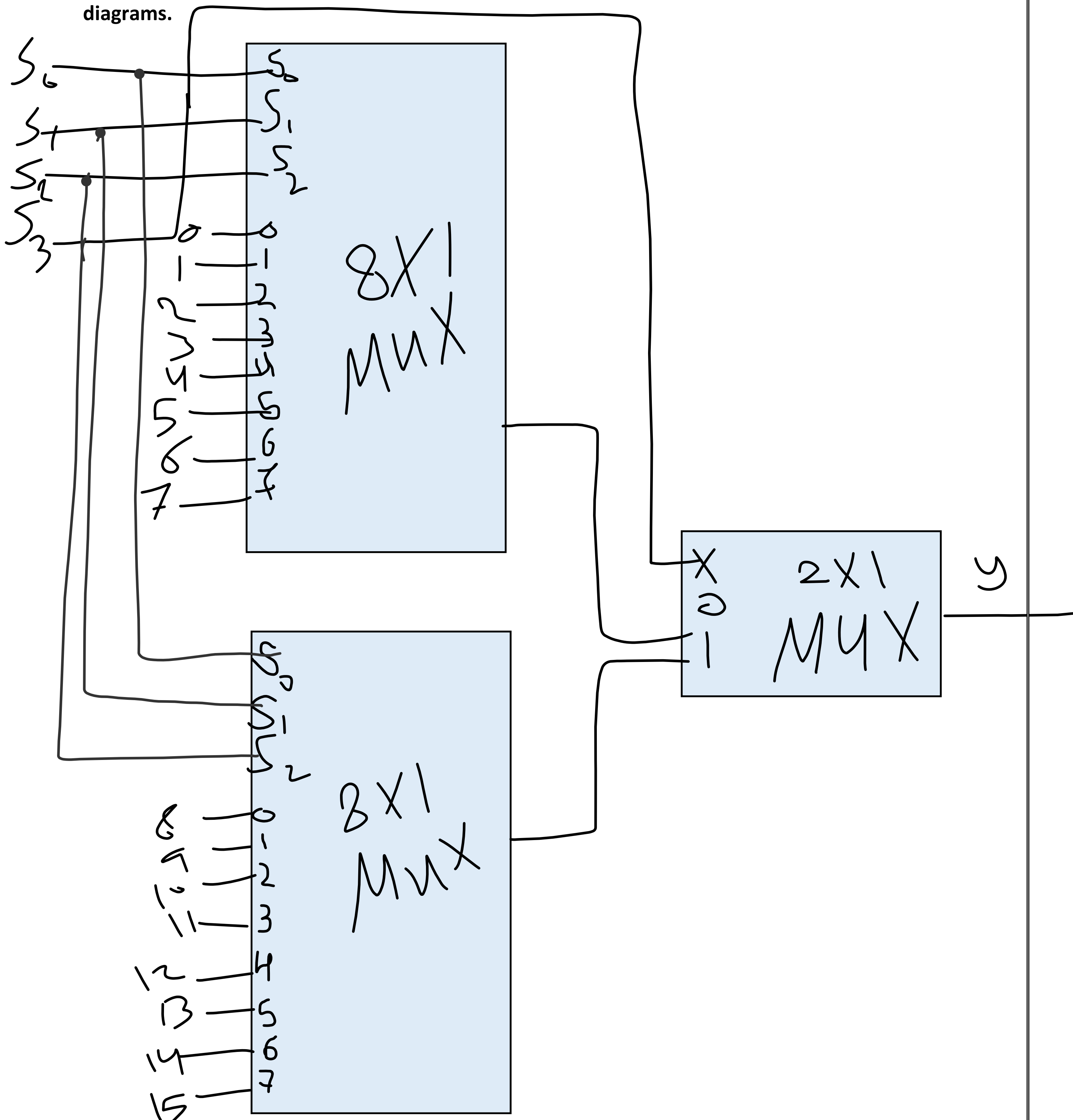
[10] A combinational circuit is specified by the following three Boolean function:

$F1(A,B,C) = \sum(2,4,7)$ $F2(A,B,C) = \sum(0,3)$ $F3(A,B,C) = \sum(0,2,3,4,7)$

Implement the circuit with a decoder constructed with NAND gates and NAND or NOR gates connected to the decoder outp uts. Use block diagram for the decoder. Minimize the number of inputs in the external gates.



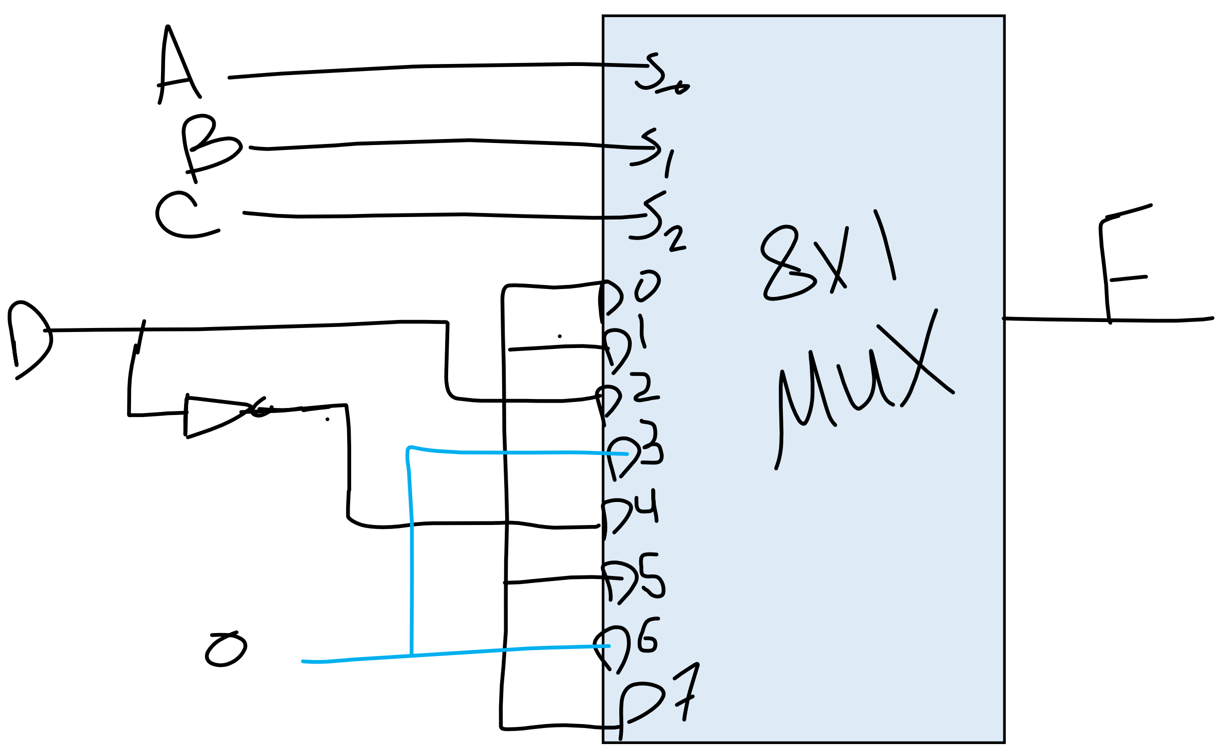
[11] Construct a 16 x 1 multiplexer with two 8 x 1 and one 2 x 1 multiplexers. Use block diagrams.



[12] Implement the following Boolean function with a multiplexer:

(a) $F(A,B,C,D) = \sum(0, 2, 5, 8, 10, 14)$

ABCD	F
0000	1
0001	0
0010	1
0011	0
0100	0
0101	1
0110	0
0111	0
1000	1
1001	0
1010	1
1011	0
1100	0
1101	0
1110	1
1111	0



(b) $F A,B,C,D = \prod(2, 6, 11)$

ABCD	F
0000	1
0001	1
0010	0
0011	1
0100	1
0101	1
0110	0
0111	1
1000	1
1001	1
1010	1
1011	0
1100	1
1101	1
1110	1
1111	1