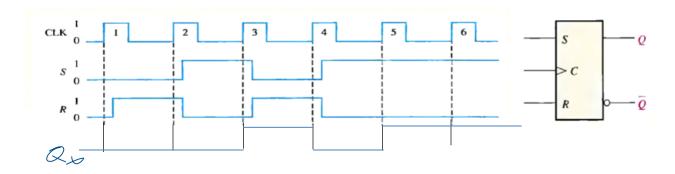


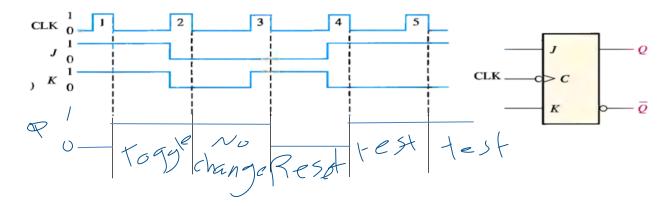
المملكة العربية السعودية وزارة التعليم جامعة الطائف كلية الحاسبات وتقنية المعلومات تصميم منطقي رقمي 1439 - 1438

Assignment 5

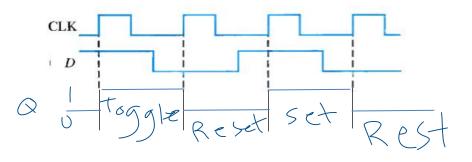
[1] Draw the Q output waveform of the flip-flop in the following figure for the S, R, and CLK inputs. Assume that the positive edge-triggered flip-flop is initially RESET.

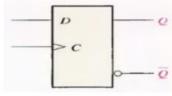


[2] The waveforms in the following figure are applied to the J, K, and clock inputs as indicated. Draw the Q output waveform, assuming that the flip-flop is initially RESET.

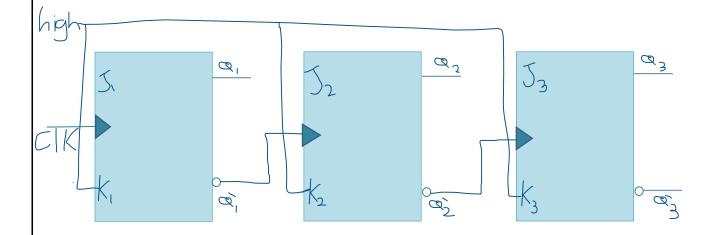


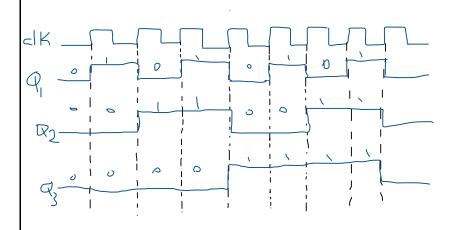
[3] Draw the Q output waveform if the inputs shown in the following figure are applied to a gated D latch, which is initially RESET.





[4] Design a 3-bit ripple up counter using positive edge trigger J-K flip-flops.





[5] Design a BCD ripple up counter using positive edge trigger J-K flip-flops. a^3 Q, Q2 53 Ju 9 -K~ 6,00 \mathbb{R}_{1}