A Low-Power Multiplier With the Spurious Power Suppression Technique

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RS encoder has been proposed. The problems related to the presence of undetected faults in parity check-based schemes has been faced by imposing some constrains in the logical net-list implementation for the constant multiplier. Evaluations of area and delay overhead for the self-checking RS encoder has been provided. For the self-checking RS decoder two main properties of the fault free decoder have been identified and used to detect faults inside the decoder. The proposed method can be used for a wide range of algorithm implementing the decoder function. Some concurrent error detection schemes have been explained in the paper and some evaluations of area overhead has been provided. Our method is nonintrusive, i.e., the decoder architecture is not modified. This fact enables the use of the reusability concept, for the design of very complex digital systems.

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A Low-Power Multiplier With the Spurious Power Suppression Technique

Kuan-Hung Chen and Yuan-Sun Chu

***Abstract*—This paper provides the experience of applying an advanced version of our former spurious power suppression technique (SPST) on multipliers for high-speed and low-power purposes. To filter out the useless switching power, there are two approaches, i.e., using registers and using AND gates, to assert the data signals of multipliers after the data transition. The SPST has been applied on both the modified Booth decoder and the compression tree of multipliers to enlarge the power reduction. The simulation results show that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a 40% speed improvement. Adopting a 0.18-μm CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction.**

***Index Terms*—H.264, low-power, multiplier, spurious power suppression technique (SPST).**

I. INTRODUCTION

Lowering down the power consumption and enhancing the processing performance of the circuit designs are undoubtedly the two important design challenges of wireless multimedia and digital signal processor (DSP) applications, in which multiplications are frequently used for key computations, such as fast Fourier transform (FFT), discrete cosine transform (DCT), quantization, and filtering. To save significant power consumption of a VLSI design, it is a good direction to reduce its dynamic power that is the major part of total power dissipation.

The designs [1]–[7] are existing works that reduce the dynamic power consumption by minimizing the switched capacitance. The design [1] proposes a concept called *partially guarded computation* (PGC), which divides the arithmetic units, e.g., adders, and multipliers, into two parts, and turns off the unused part to minimize the power consumption. The reported results show that the PGC can reduce power consumption by 10% to 44% in an array multiplier with 30% to 36% area overheads in speech related applications. Design [2] proposes a 32-bit 2's complement adder equipping a master-stage flip-flop and a slave-stage flip-flop for both operands of the adder, a *dynamic-range determination* (DRD) unit, and a sign-extension unit. This design tends to reduce the power dissipation of conventional adders for multimedia applications. Additionally, design [3] presents a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth codes. The direct report of [3] shows that the multiplier can save over 30% power dissipation than conventional ones. Design [4] incorporates a technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be "frozen" by asserting a control signal. This technique can be applied to replace layout-level descriptions and guarantees predictable results. However, it can only achieve savings of 6.3% in total power dissipation since it operates in

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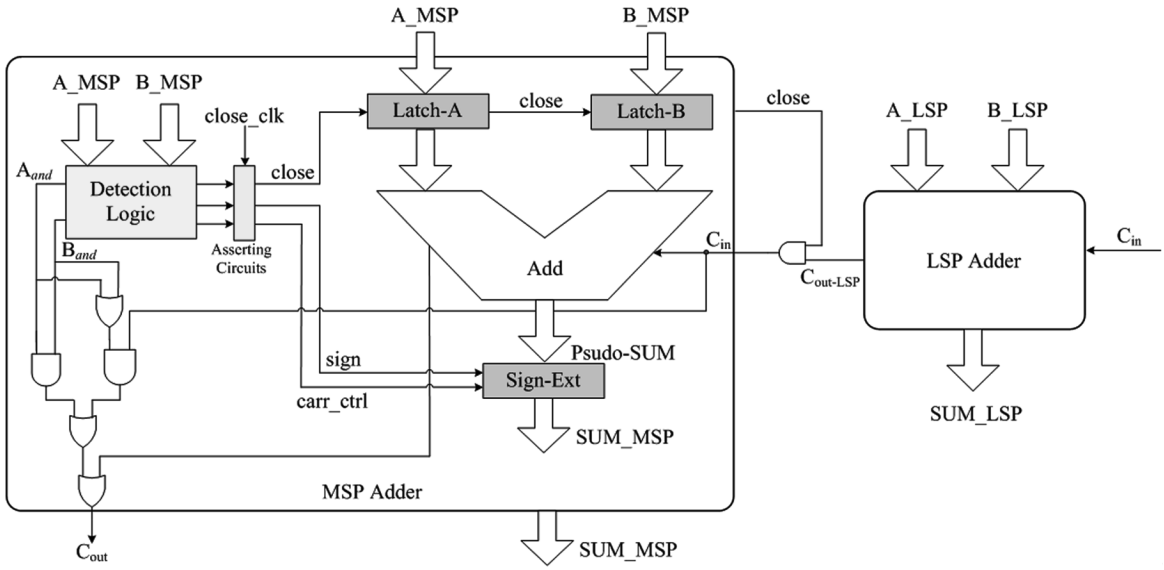

Fig. 1. Low-power adder/subtractor design example adopting the SPST.

the layout-level environment which is tightly restricted. The design [5] proposes a double-switch circuit-block switch scheme capable of reducing power dissipation during down time by shortening the settling time after reactivation. The drawbacks of the scheme are the necessity for two independent virtual power rails and the necessity for two additional transistors for switching each cell. Design [6] and design [7], respectively, study signal gating schemes for adders and multipliers. Design [6] presents the arithmetic details about the signal gating schemes and illustrates 10% to 45% power reduction for adders.

Furthermore, this study examined some modern multiplier or MAC designs [8]–[15]. The design [8] includes three techniques, i.e., the signal flow optimization (SFO), left-to-right leapfrog (LRLF) structure, and upper/lower split structure, to optimize the array multipliers. The SFO and LRLF techniques are used for signal balancing of the partial product reducing (PPR) stage in a multiplier. Moreover, the upper/lower split structure is used to shorten the path of the PPR stage to prevent the snowballing glitch effect. Thus, design [8] can save about 20% power dissipation when compared with conventional right-to-left multipliers. Design [9] turns off some columns in the multiplier array whenever their outputs are known, thus saving 10% power consumption at the cost of 20% area overhead for random input under a 0.35-μm CMOS technology. Design [10] uses a DRD unit to detect the dynamic range of the inputs, and adopts three separate Wallace trees for the 4×4, 8×8, and 16×16 multiplications which certainly induce area and capacitance penalties. Under a 0.13-μm CMOS technology, design [10] can obtain a 20% power reduction over the conventional multiplier at a cost of 44% in area overheads. Design [11] proposes a 32-bit SIMD MAC unit which is a coprocessor to the Intel XScale microprocessor. Under a 0.18-μm CMOS technology, [11] presents that the processor dissipates 450 mW at 600 MHz with 1.3-V supply voltage. Design [12] is a vector MAC unit that can perform one 64×64, two 32×32, four 16×16, or eight 8×8 signed/unsigned multiply-accumulations. Design [13] involves a fixed-width 32-bit left-to-right multiplier which obtains an 8% speed improvement, a 14% power reduction, and a 13% area saving. Meanwhile, design [14] explores a design methodology for high-speed modified Booth multipliers. Finally, design [15] adopts an advanced 90-nm dual-V_t CMOS technology to implement a 16×16 bit multiplier that consumes 9 mW at 1 GHz with 1.3 V.

Our former SPST is demonstrated to reduce 20% to 30% power dissipation of H.264 transform coding and some multimedia computations [16], [17]. The SPST uses a detection logic circuit to detect the effective data range of arithmetic units, e.g., adders or multipliers. When a portion of data does not affect the final computing results, the data controlling circuits of the SPST latch this portion to avoid useless data transitions occurring inside the arithmetic units. Besides, there is a data asserting control realized by using registers to further filter out the useless spurious signals of the arithmetic units every time when the latched portion is being turned on. Although this asserting control brings evident power reduction, it may induce additional delay which is the problem this study wants to solve. When implemented in a 0.18-μm CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction than the conventional multiplier. Compared with the former SPST, the new approach improves 40% speed of the SPST-equipped multipliers.

The remainder of this paper is arranged as follows. Section II briefly reviews the former SPS technique, and then introduces the new implementing approach. Section III discusses the application of the SPST on multipliers. Section IV shortly describes the implementation and verification of this design, and then evaluates its performance. Finally, a conclusion is given in Section V.

II. Proposed Spurious Power Suppression Technique (SPST)

The former SPST has been discussed in [16] and [17]. The main contribution of this paper is exploring two implementing approaches for the SPST and comparing their efficiency, which provide diverse reference materials for applying the SPST. For completeness of this paper and easy understanding for the readers, we simply review the former SPST first. In Fig. 1, the SPST is illustrated through a low-power adder/subtractor design example. The adder/subtractor is divided into two parts, i.e., the most significant part (MSP) and the least significant part (LSP). The MSP of the original adder/subtractor is modified to include detection logic circuits, data controlling circuits, denoted as latch-A and latch-B in Fig. 1, sign extension circuits, and some glue logics for calculating the carry in and carry out signals. The most important part of this study is the design of the control signal asserting circuits, denoted as asserting circuits in Fig. 1, following the detection logic circuits.

The first implementing approach of the control signal assertion circuits is using registers, which is illustrated in the shadow area in

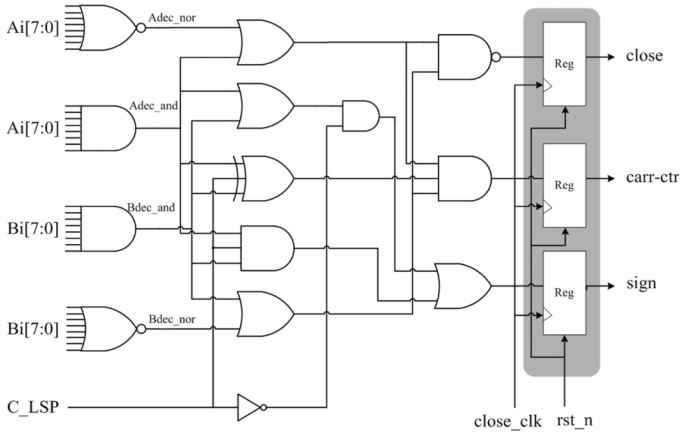

Fig. 2. Detection logic circuits using registers to assert the control signals.

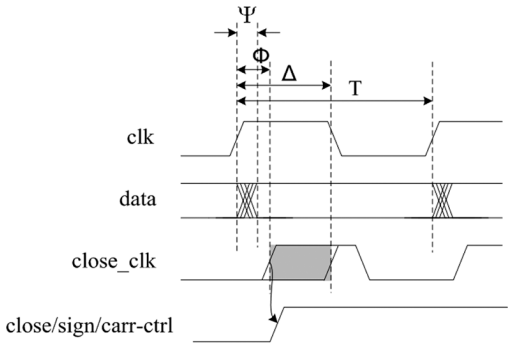

Fig. 3. Timing diagram of the control signals of detection logic circuits after assertions.

Fig. 2. The three output signals of the detection logic are given a certain amount of delay before they assert, demonstrated in the timing diagram shown in Fig. 3. The delay Φ, used to assert the three output signals, must be set in the range of $\Psi < \Phi < \Delta$ to filter out the glitch signals as well as to keep the computation results correct, where Ψ and Δ, respectively, denote the data transient period and the earliest required time of all the inputs. The range of Φ is also shown as the shadow area in Fig. 3. Readers, who have interests in other details of this part, please refer to [16] and [17].

Using registers to control the signal assertions can obviously reduce the spurious power dissipation of adders/subtractors [16], [17]. However, the restriction that Φ must be greater than Ψ to guarantee the registers from latching the wrong values of control signals usually decreases the overall speed of the applied designs. This issue should be noticed in high-end applications which demands both high-speed and low-power requirements.

To solve the previously mentioned problem, we adopt the other implementing approach of the control signal assertion circuits illustrated in the shadow area in Fig. 4, using an AND gate in place of the registers to control the signal assertion. The timing control of the delay Φ in this implementation is slightly different from the one in the first implementation. That is, the range of Φ can be set as $0 < \Phi < \Delta$ to filter out the glitch signals and to keep the computation results correct, as well. This feature allows upper-level systems to assert the *close* signal with an arbitrarily short delay closing to the positive edge of the clock signal, which provides a more flexible controlling space for the delay Φ. When speed is seriously concerned, this implementing approach enables an extremely high flexibility on adjusting the data asserting time of the SPST-equipped multipliers. Therefore, the proposed advanced

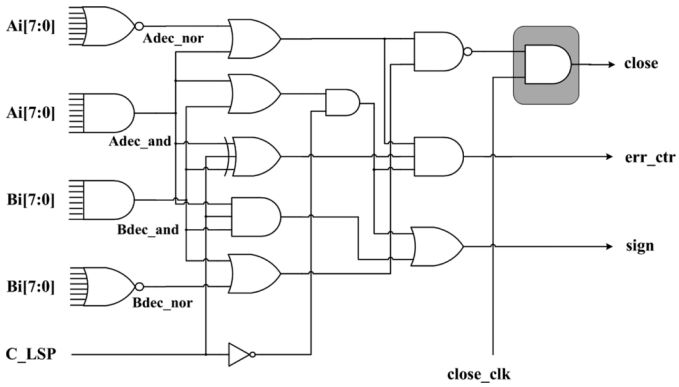

Fig. 4. Detection logic circuits using an AND gate to assert the control signal.

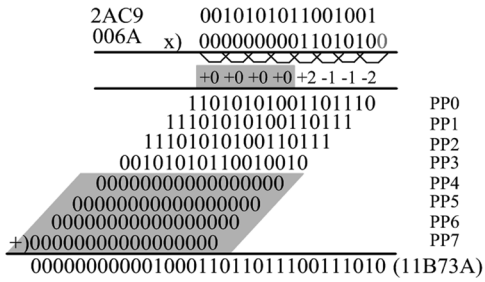

Fig. 5. Illustration of multiplication using modified Booth encoding, where PP0 to PP7 denote the partial products.

SPST can benefit multipliers on both high-speed and low-power features.

III. Low-Power Multiplier Design

The proposed low-power multiplier is designed by equipping the SPST on a tree multiplier. There are two distinguishing design considerations in designing the proposed multiplier, as listed in the following.

A. Applying the SPST on the Modified Booth Encoder

Fig. 5 shows a computing example of Booth multiplying two numbers "2AC9" and "006A," where the shadow denotes that the numbers in this part of Booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals. According to the analysis of the multiplication shown in Fig. 5, we propose the SPST-equipped modified-Booth encoder, which is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. As shown in Fig. 6, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero, to reduce the transition power dissipation. Such cases occur frequently in e.g., FFT/IFFT, DCT/IDCT, and Q/IQ which are adopted in encoding or decoding multimedia data.

B. Applying the SPST on the Compression Tree

The proposed SPST-equipped multiplier is illustrated in Fig. 7. The PP generator generates five candidates of the partial products, i.e., $\{-2\mathrm{A}, -\mathrm{A}, 0, \mathrm{A}, 2\mathrm{A}\}$, which are then selected according to the Booth encoding results of the operand B. Moreover, when the operand besides the Booth encoded one has a small absolute value, there are

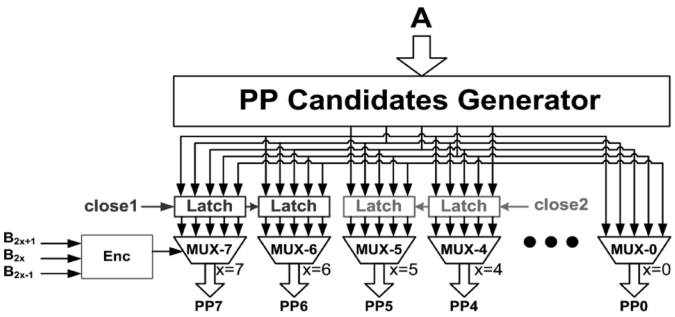

Fig. 6. SPST-equipped modified-Booth encoder.

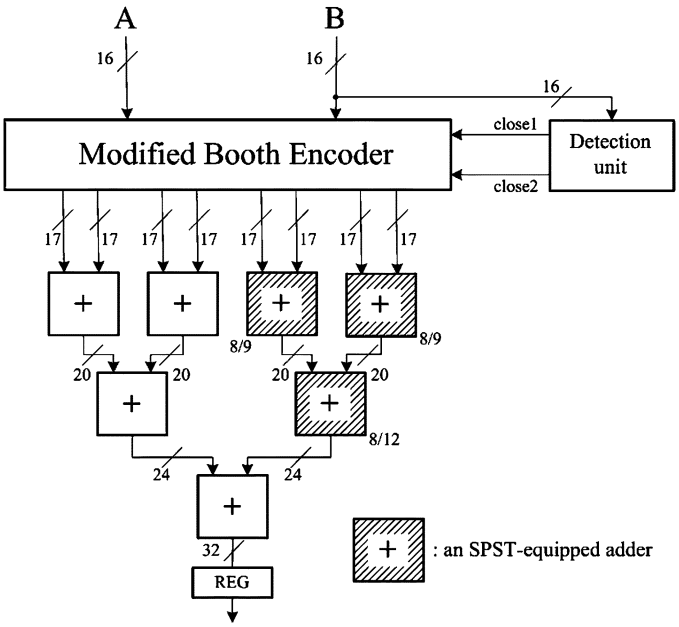

Fig. 7. Proposed low-power SPST-equipped multiplier, where the fraction values denote the bit-widths of the MSP and LSP of the SPST-equipped adders.

opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPST-equipped adders, which are marked with oblique lines in Fig. 7. The bit-widths of the MSP and LSP of each SPST-equipped adder are also indicated in fraction values nearing the corresponding adder in Fig. 7.

IV. Performance Evaluation and Comparison

The SPST-equipped multiplier design has been realized by following the standard cell-based design flow with an in-house 0.18-μm CMOS cell library which is constructed following the TSMC 1P6M 0.18-μ m CMOS technology. This design is verified via C/MATLAB behavioral simulation, *nLint* HDL coding rule check, *VERILOG* RTL simulation, *SYNOPSYS* logic synthesis, *VERILOG* gate-level simulation, and *NanoSim* transistor-level simulation.

We evaluate the efficiency of applying the SPST on modified Booth encoder as described in Section III-A. By the proposed SPST, 65.67% power dissipation and 28.02% area cost are saved. When computing the multiplication of the texture coding of H.264, the simulation results of the original tree multiplier and the two SPST-equipped multipliers with different implementing approaches are listed in Table I. From Table I, we can know that both the SPST-equipped multipliers

TABLE I
Simulation Results of Three Multipliers, Where the Power Dissipation is Measured Using *NANOSIM* When Computing Texture Coding of "Stefan" Sequence in H.264

Design	Power/MHz (P, mw)	Norm. P	Area (Tr.)	Max. Freq.
Original tree MUL	0.0201	1	10544	200 MHz
SPST using REG	0.0118	0.59	10910	142 MHz
SPST using *AND* gate	0.0121	0.60	11028	200 MHz

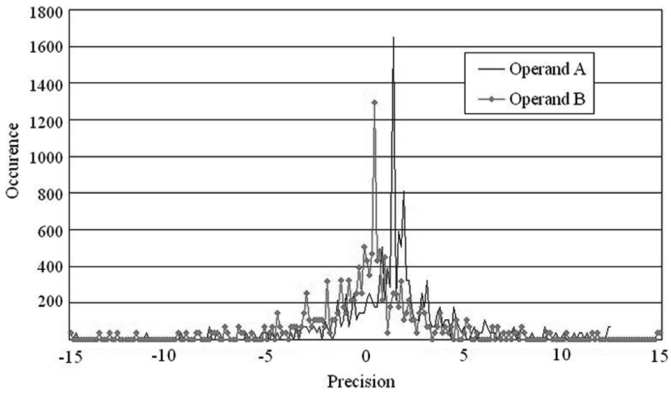

Fig. 8. Precision analysis of the "Stefan" sequence.

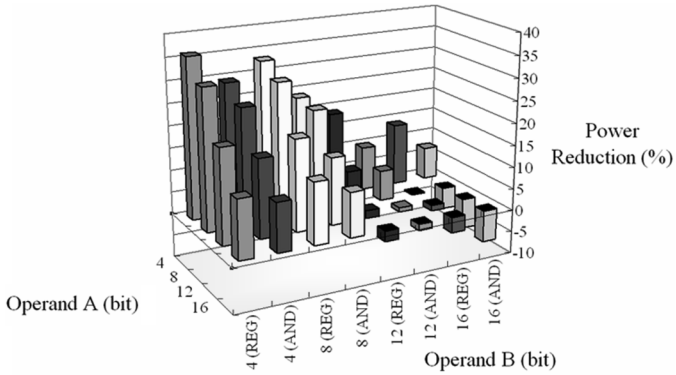

Fig. 9. Comparison of power dissipation of the tree multiplier and the SPST-equipped multipliers adopting the two implementing approaches, i.e., using registers and using AND gates, with Gaussian distributed inputs.

using registers and that using AND gates save about 40% power dissipation of the original tree multiplier. However, the maximum operating frequency of the SPST-equipped multipliers using AND gates is 40% higher $(200/142 - 1)$ than that using registers. Besides, Table I also shows that the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz when computing the multiplication of texture coding in H.264. The precision analysis of the test pattern "Stefan" sequence is shown in Fig. 8.

Furthermore, we measure the power dissipation of the previous three multipliers in terms of Gaussian distributed data patterns with different bit ranges, i.e., 4, 8, 12, and 16 bit. The results are illustrated in Fig. 9, where the X and Y-axis of the plots denote the bit-widths of the two operands of multipliers, respectively, and the Z-axis denotes the power reduction compared with the original tree multiplier. In Fig. 9, both SPST-equipped designs have the largest power saving when both the two input data are 4-bit wide. The power saving decreases as the data bit-widths increase. At last, the power saving becomes negative under

TABLE II
PERFORMANCE COMPARISON WITH THE EXISTING MULTIPLIERS

Design	Feature	Tech.	Power (mW)	Delay (ns)	Area
Huang [8]	(1) 32b × 32b	0.18 μm	(1) 19.65 for Djpeg (2) 40.65@ 100MHz for random data	7.25	74598 (tr.)
Liao [11]	(1) Coprocessor (2) SIMD (3) 32b MAC	0.18 μm	900@1.6V, 800MHz	1.25	N.A.
Wang [13]	(1) 32b × 32b (2) Fixed-width	0.35 μm/3.3V	79.86	14.01	19743 (gate)
Chen [3]	(1) 16b × 16b	0.25 μm	17.30 for *normal distribution* inputs	8.3	0.337 (mm^2)
Lee [10]	Scalable length of 4b, 8b, 16b	0.13 μm/1.2V	1.04@100MHz for random data	N.A.	6388 (gate)
Hsu [15]	(1) 16b × 16b (2) Sleep mode (3) Duel V_T	90 nm	(1) 9@1.3V, 1GHz (1) 7.9×10^{-2} @50MHz, 0.57V	1	0.03 (mm^2)
Proposed	(1) 16b × 16b (2) SPST	0.18 μm	(1) 1.21@100MHz, 1.8V for H.264 texture coding (2) 2.82@100MHz, 1.8V for avg. *normal distribution* inputs	5	11028 (tr.)

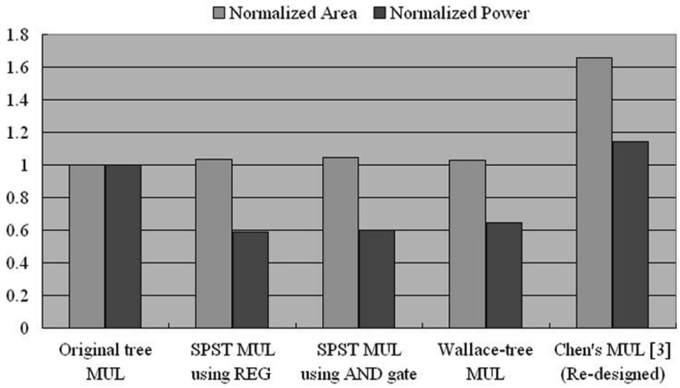

Fig. 10. Comparison in terms of normalized area and power consumption of the proposed multiplier.

some conditions with large input data bit-widths. From Fig. 9, we can also know that the power saving of the SPST-equipped multiplier using registers is slightly larger than that of the SPST-equipped multiplier using AND gates. Nevertheless, using registers results in longer critical path delay as shown in Table I.

The performance comparison of the proposed multiplier with some existing designs, which report more complete information, is listed in Table II. Designs [8], [11], and [13] are 32-bit multipliers which are considered as reference indexes only. Fig. 10 also illustrates that the proposed SPST-equipped multipliers dissipate fewer power consumption than Wallace-tree multipliers.

V. CONCLUSION

In this paper, we propose a multiplier adopting the new SPST implementing approach, i.e., using AND gates in the detection logic unit. The simulation results show that the power reduction of the new approach, i.e., a 40% saving, is very close to that of the former approach. Besides, the new approach leads to a 40% speed improvement when compared with the former one. When implemented in a 0.18-μm CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding. In addition, this paper explores the performance of the proposed design under the conditions of different bit-width input data. The results also show that the new SPST approach not only owns equivalent low-power performance but also leads to a higher maximum speed when compared with the former SPST approach. Moreover, the proposed SPST-equipped multiplier also has better power efficiency when compared with the existing modern multipliers.

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