Journal of Engineering Sciences
Vol 10, Issue 07, July/2019
ISSN NO:0377-9254

VLSI Design of Low Power Array Multiplier Using Modified Full Adder based on Verilog

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Abstract:

The development of high-speed, low-power, and regular-layout multipliers is a hot topic in research. The multiplier's speed can be boosted by lowering the threshold. Some items were created There have been numerous attempts to limit the quantity of incomplete items produced in a procedure of multiplication Array multiplier is one of them. To add the carry products, an array multipl ier half adder was employed.In a shorter pe riod of time Creating high-performance integrated circuits with The VLSI circuit's low power consumption is a crucial consideration. designers. The multiplier is used in the ma jority of arithmetic operations.which is the digital's most power-hungry component? circuits. Essentially, the multiplication process is realised in hardware as a shift and add operation. The performance of the multiplier has improved as a result of the optimization of the adder. A redesigned full adder with multiplexer is proposed in this paper to achieve reduced multiplier power consumption. The traditional array multiplier structure is utilised to evaluate the efficiency of the proposed architecture. The designs are created in Verilog HDL, and the functionality are confirmed using Xilinx simulation. In comparison to existing techniques, the suggested multiplier's ASIC synthesis results demonstrate a 35.45 percent reduction in power consumption, 40.75 percent reduction in area, and 15.65 percent reduction in delay.

I. INTRODUCTION:

For any chip designer, power consumption, latency, and area have always been significant design issues. Multipliers are used in the design of several DSP structures. The circuit's delay is inextricably linked to the multiplier's delay. As a result, work is being done to reduce the multiplier's delay so that the whole circuit's delay can be lowered. provided an early description of t he array multiplier. The array multiplier ha s evolved into a high-speed, space-saving multiplier. For the creation of partial products, the arr ay multiplier ANDs multiplier and multipli cand bits. In the second step, full adders a nd half adders were utilised in two rows to reduce the created partial products. The third stage involves the addition of two rows utilising rapid carry adders. A great deal of research has been done in recent years to minimise the multiplier's complexity. In, an innovative strategy for reducing the complexity of an array multiplier in terms of half adders is utilised. In, an innovative strategy for reducing the complexity of an array multiplier in terms of half adders is utilised. In, the approach p roposed in is improved further by adding o ne additional half adder to the rightmost co

lumns, resulting in a significant reduction i n area. Furthermore, in Booth, an encoding strategy combined with a compressor was employed to reduce the area as well as the latency.In addition, in [5,] the conventional half adder and full adder in the second sta ge are replaced by a 3:2 XOR-XNOR based adder. Compressors with ratios of 4:2 and 5:2 boo st the speed of the system operation. Estimation is suggested as an ef ficient strategy using each stage of the reduction tree's po wer Gate-level power estimator with a probabilistic gate. In [7], the reordering of partial products is employed in such a way so as to reduce the switching activity which leads to reduction in power. Partitioning the partial product tree into four groups and applying Dadda to one group and array multiplier to another and so on also achieves power reduction [8]. In [9], a modified full adder using 4:1 multiplexers is used in the reduction phase to reduce the power. In [11], full adder is designed using six 2:1 multiplexers. The architecture is designed in a unique way, such that it is reducing the short circuit current as well as the transition activity, thus the power is also getting reduced. But the area is increasing significantly. This work primarily deals with the replacement of full adders with changed full adder within the reduction phase of the array phase. within the proposed method, a modified full adder using multiplexer is applied to achieve power reduction compared to the present techniques with alittle area and delay improvement.

RELATED WORKS

A. ARRAY MULTIPLIER

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. In array multiplier, consider two binary numbers A and B, of m and n bits. There are an summands that are produced in parallel by a set of an AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n2 AND gates. Also, in array multiplier worst case delay would be (2n+1) td.

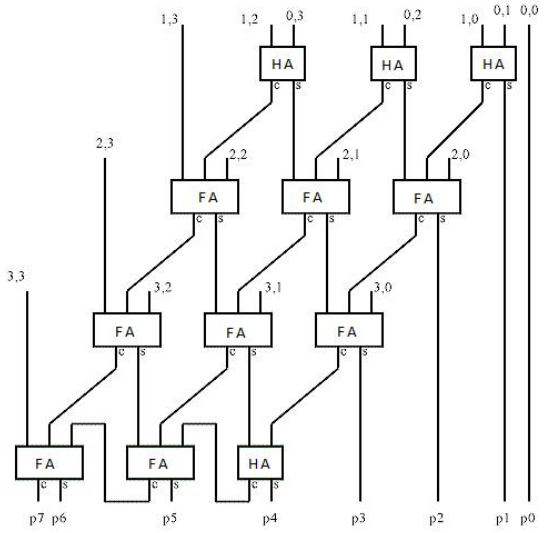


Figure.1.Array Multiplier

B. Full Adder

The hardware requirement in terms of full adder (FA) and the length of final adder (FAL) for different size of array multipliers is obtained in the manner given in below.

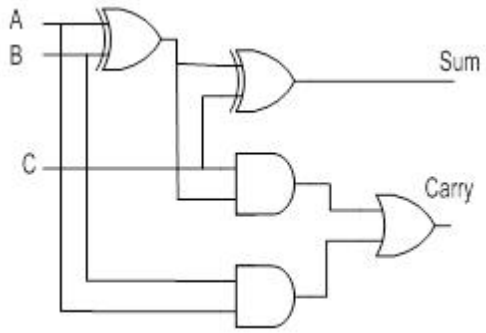


Figure. 2. Full Adder

C. Conventional Full adder

The conventional array multiplier uses full adder in its reduction phase. The bottleneck of full adder is high power consumption due to XOR gates. As shown in fig. 2 conventional full adder consists of two XOR gates in critical Delay = 2 XOR

path of sum and one XOR gate, one AND gate and one OR gate in the critical path of the carry.

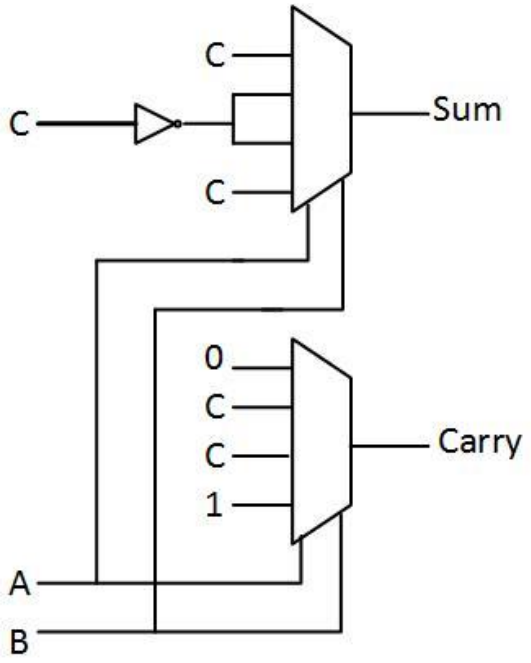


Figure. 3. 4:1 MUX based Full Adder

D. MUX based Full adder

In order to scale back the power and area, the conventional Full adder in reduction part of array multiplier factor is replaced by a changed full adder [9]. In MUX based mostly full adder the full adder is enforced using 4:1 multiplexers as shown in fig. 3. By implementing MUX based mostly full adder in reduction part of Array multiplier factor power reduction has been achieved. It is evident that, one 4:1 MUX is created using 3 2:1 MUX. The critical path delay is written as shown below The array multiplier factor is created additional efficient by further reducing the crucial path delay. a similar is achieved by using proposed full adder.

III.PROPOSED FULL ADDER

The proposed modified full adder circuit as shown in fig. 5, consists of 2 2:1 MUX and an XOR circuit. In the proposed structure, one XOR block in the conventional full adder is replaced by a multiplexer block so the crucial path delay is minimized. As are often seen from (14), the critical path delay is This can be implemented by using second MUX with XOR output as selection line. Since XOR employs most of the power consumption in the adder circuit, by reducing number of XOR gates, power consumption of the full adder can be reduced. The proposed full adder is applied into array multiplier reduction stage to validate the effectiveness. In array structure the partial products is split into certain levels. In every level, whenever there are 3 bits,

full adder should be used. Out of the 3 inputs, one input and its complement is provided as inputs to the primary multiplexer.

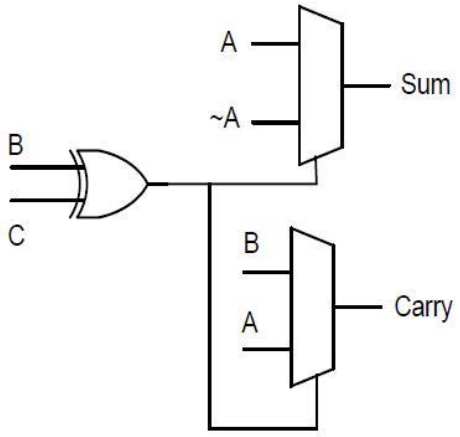


Figure. 4. Proposed Full Adder

the other 2 inputs are given to X-OR circuit, the output of which is able to act as a pick line to each the multiplexers. The inputs of the second multiplexer are, the bits apart from the carry bit. This distinctive way of designing leads to the reduction of the switching activity, that in turn reduces the ability. additionally to the present, the critical path delay is also reduced compared to the existing styles mentioned in literature, that ends up in reduction in delay and therefore increasing the speed. Operation of the proposed full adder can be explained as follows:

a) once each B and C are zero or one, sum =A;

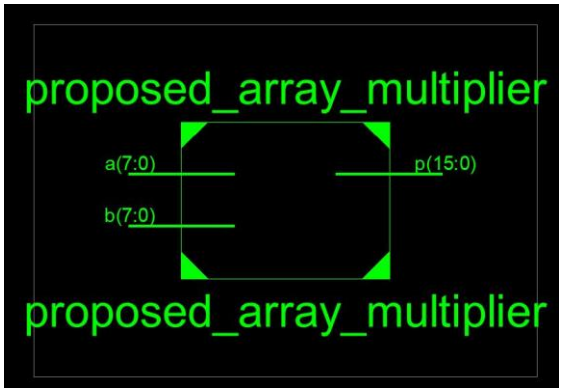
b) once either of B or C is one and another is zero, sum=A;

c) once each B and C are zero or one, carry=B;

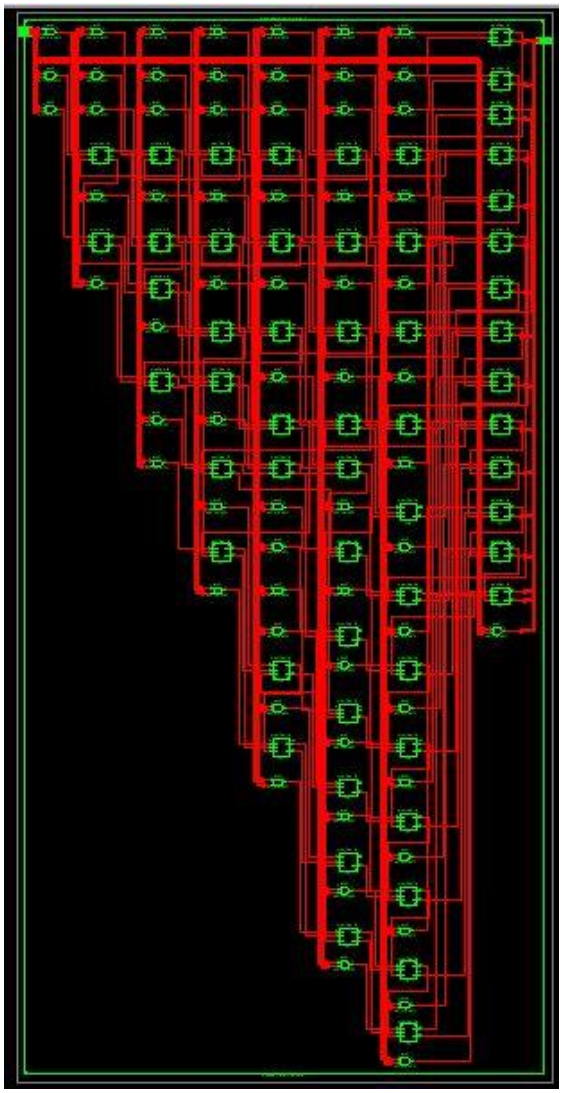
When either of B or C is one and another is zero,

carry=A;l

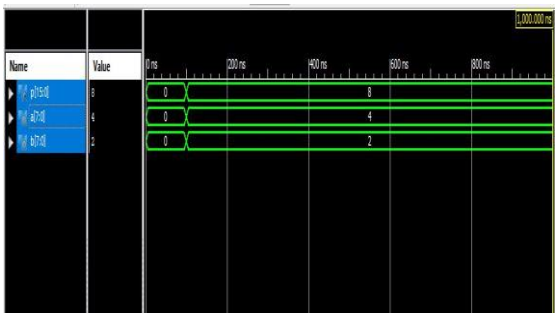
IV. OUTPUT RESULTS



Top level block



RTL schematic



Simulation output

V CONCLUSION:

In this paper, a modified full adder using multiplexers and XOR gate is proposed. By incorporating the modified full adder in the reduction stage of Wallace tree multiplier, an average power, area and delay reduction of 35.45% , 40.75% and 15.65% respectively, compared to existing methods respectively is achieved. The synthesis result confirms that the proposed Wallace tree multiplier is suitable for low power and small area applications.

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