IJournals: International Journal of Software & Hardware Research in Engineering
ISSN-2347-4890
Volume 3 Issue 12 December, 2015

Implementation and Analysis of Vedic Multiplier Using Different Adder

Ankita Jain; Atush Jain

M. Tech Scholar; Assistant Professor (Department of Electronics and Communication Engineering, AITR Indore)

E-mail: ankita.aj11@gmail.com; atushjain@acroplis.in

ABSTRACT

Multiplication is one of the basic arithmetic operations and it requires more hardware resources and processing time than addition and subtraction. Vedic multiplication is one of the most popular multiplication techniques. In this paper, comparative study of Vedic multiplier using two different adders is done. We have designed a 16-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. The partial product addition in Vedic multiplier is realized using carry select addition technique. A 16-bit multiplier is realized using 8-bit multiplier and carry select adders. While implementing the design, we use vertically and Crosswise method of Vedic Mathematics. The design is implemented using Verilog HDL, the combinational path delay of 16X16 bit Vedic multiplier using ripple carry adder is compared with 16X16 bit Vedic multiplier using carry select adder.

Keywords: Vedic Mathematics, Vedic Multiplication, Urdhva Tiryagbhyam method, Ripple Carry Adder, Carry select Adder.

1. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Vedic multiplier is one of the most popular multiplier. [1]

The multiplier is a basic building block in Standard Digital Signal Processors (DSP) [2]. Most of the DSP tasks require real-time processing with several multiplications. Multiplication is most important arithmetic operation having wide applications from normal multiplication in DSP. Multiplication process is used in many applications like instrumentation and measurement, communications, audio and video processing, animations, special effect, Graphics, Image enhancement, Navigation, GPS, and control applications like robotics, machine vision. For higher order multiplications, a large number of adders are to be used to perform the partial product addition. The need of high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The mathematical operations using Vedic Method are very fast and requires less hardware, also can be used to improve the computational speed of processors. This paper describes the design and implementation of 16x16 bit Vedic multiplier based on Urdhva Tiryagbhyam sutra (Vertically and Crosswise technique) using Ripple carry adder and using Carry Select Adder.

2. VEDIC MATHEMETICS

Vedic mathematics is part of four Vedas. It is part of Sthapatya Veda, which is an upa-veda of Atharva Veda. It is given by Jagadguru Shankaracharya bharati Krishna Teerthaji Maharaja. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (Sub formulae) after extensive research in Atharva Veda. [1]

These Sutras with their meanings are listed below alphabetically.

1. (Anurupye) Shunyamanyat: If one is in ratio, the other is zero.
2. ChalanaKalanabyham: Differences and similarities.
3. Ekadhikina Purvena: By one more than the previous One.
4. Ekanyunena Purvena: By one less than the previous One.
5. Gunakasamuchyah: Factors of the sum is equal to the sum of factors.
6. Gunitasamuchyah: The product of sum is equal to sum of the product.
7. Nikhilam Navatashcaramam Dashatah: All from 9 and last from 10
8. Paraavartya Yojayet: Transpose and adjust.
9. Puranapuranabyham: By the completion or non-completion.
10. Sankalana - vyavakalanabhyam: By addition and by subtraction.
11. Shesanyankena Charamena: The remainders by the last digit.
12. Shunyam Saamyasamuccaye: When the sum is same then sum is zero.
13. Sopaantyadvayamantyam: The ultimate and twice the penultimate.
14. Urdhva - tiryakbhyam: Vertically and crosswise.
15. Vyashtisamanstih: Part and Whole.
16. Yaavadunam: Whatever the extent of its deficiency.

3. URDHVA TIRYAGBHYAM METHOD

The use of Vedic mathematics [3] is that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

3.1 Vertically & Crosswise Technique

This Vedic multiplier is based on the Urdhva Tiryagbhyam sutra (algorithm) [3]. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise products". The algorithm can be generalized form x n bit number. [4].

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 * 846 by Urdhva Tiryagbhyam method as shown in Figure 1. The digits on the both sides of the line (say 2 and 6) are multiplied (6 * 2 = 12) and added with the carry from the previous step (initially, carry = 0). This generates one of the bits of the result (i.e. 2) and a carry (i.e. 1). This carry (1) is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, Least Significant Bit (LSB) acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero. [4].

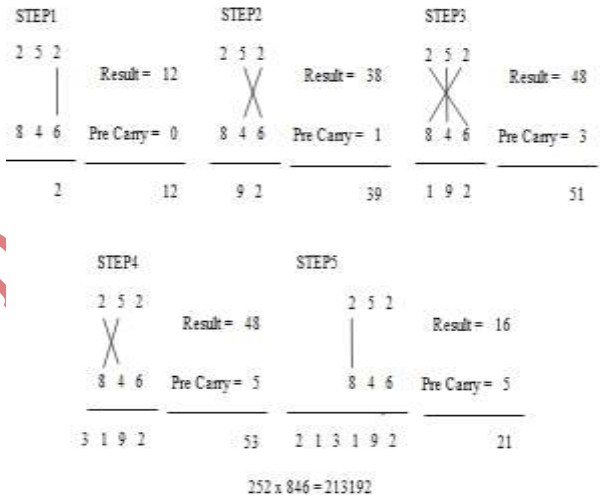

Fig.1. Multiplication of two Decimal Numbers

4. IMPLEMENTATION OF PROJECT

In this paper 16x16 Vedic multiplier is implemented by four 8x8 Vedic multiplier. 8x8 Vedic multiplier is consist of four 4x4 Vedic multiplier. 4x4 Vedic multiplier is consist of four 2x2 Vedic multiplier. Also three adders are required. Adder 1 is of 16 bit carry select adder which gives addition of two 8x8 Vedic multiplier. Adder 2 is another 16 bit carry select adder which produces addition of outputs from the adder 1 and one 8x8 Vedic multiplier. Adder 3 is one more 16 bit carry select adder which gives addition of output of adder 2 and one 8x8 Vedic multiplier. After these three adders final output is obtained.

Architecture of 16x16 Vedic Multiplier is shown figure below. It is consist of four 8x8 multipliers. Also three

adders are required. In this paper we have used two different adder. Firstly we have designed using ripple carry adder, than we have designed using carry select adder. Then delay comparison is done for both the architecture.

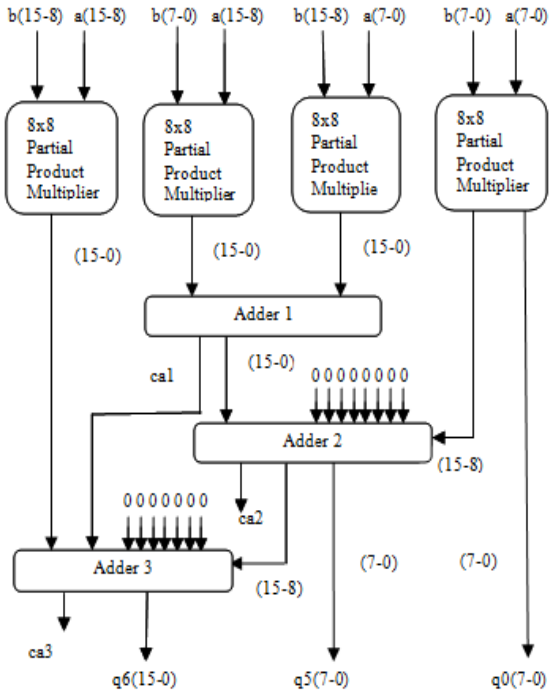

Fig.2. Block Diagram of 16 * 16 bit Vedic Multiplier

5. IMPLEMENTATION OF PROJECT

A 16x16 bit Vedic multiplier is designed using Verilog HDL. Logic synthesis and simulation was done in Xilinx ISE 14.2i. The Synthesis is done on Spartan 3E using device (xc3s500e-5pq208).

5.1 Synthesis Report

The device utilization summary of 16x16 bit Vedic multiplier using xc3s500e-5pq208 is shown below.

Vedic Multiplier Using Ripple Carry Adder

TABLE I

DEVICE UTILIZATION SUMMARY USING RIPPLE CARRY ADDER

	Used	Total	Used Percentage
Number of Slices	429	4656	9 %
Number of 4 input LUTs	755	9312	8 %
Number of bonded IOBs	64	158	40 %

Vedic Multiplier Using Carry Select Adder

TABLE II DEVICE UTILIZATION SUMMARY USING CARRY SELECT ADDER

	Used	Total	Used Percentage
Number of Slices	409	4656	8 %
Number of 4 input LUTs	716	9312	7 %
Number of bonded IOBs	64	158	40 %

TABLE III DELAY SUMMARY

Multiplier Type	16 bit Vedic Multiplier using RCA	16 bit Vedic Multiplier using CSA
Logic Delay	22.635 ns	21.077 ns
Route Delay	15.405 ns	14.176 ns
Total Delay	38.040 ns	35.253 ns

5.2 RTL View

A 16*16 bit Vedic multiplier is implemented in Verilog HDL and synthesized using Xilinx ISE 14.2i.

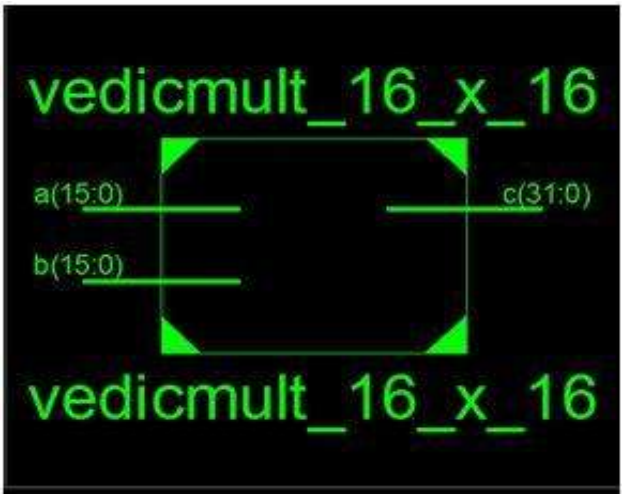

Fig.3. RTL View for Vedic Multiplier using Ripple Carry Adder

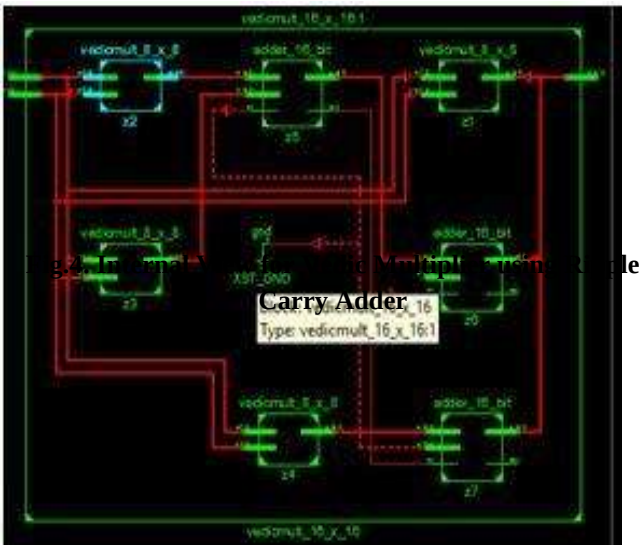

Fig.4. RTL View for Vedic Multiplier using Carry Select Adder

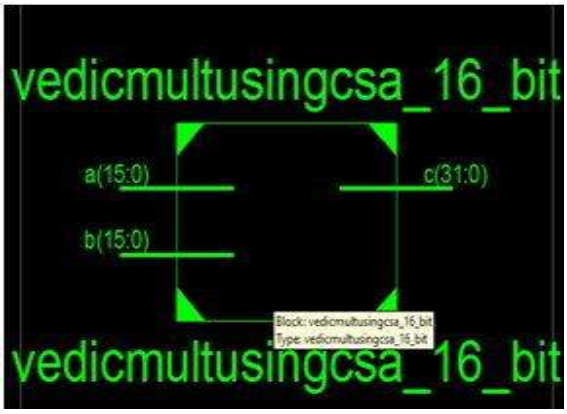

Fig.5. RTL View for Vedic Multiplier using Carry Select Adder

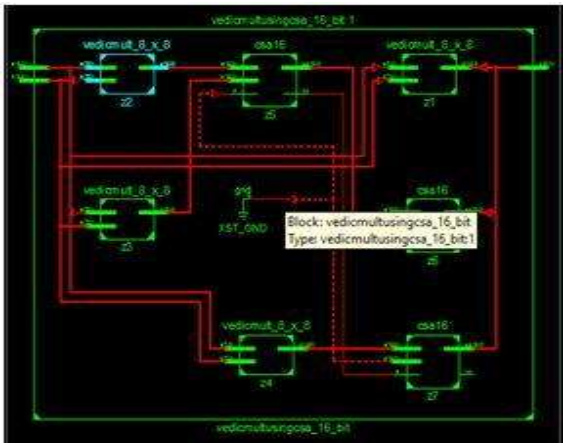

Fig.6. Internal View for Vedic Multiplier using Carry Select Adder

5.3 Simulation Waveform

A 16*16 bit Vedic Multiplier is implemented using Verilog HDL and simulated on Xilinx ISE 14.2i.

Fig.7. Simulation Waveform for Vedic Multiplier using Ripple Carry Adder

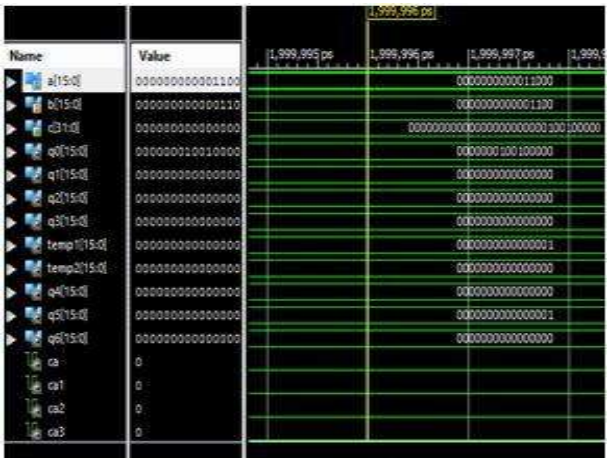

Fig.8. Simulation Waveform for Vedic Multiplier using Carry Select Adder

6. CONCLUSION

The Verilog HDL code is written for Vedic Multiplier using Urdhva Tiryagbhyam Sutra and it has been implemented and tested on Xilinx ISE 14.1i. The code has been synthesized and simulated successfully. The Vedic Multiplier is implemented using two different adders (Ripple Carry Adder and Carry Select Adder). We studied these adders and compared them by different criteria like Area, Delay etc. so that we can judge to know which adder was best. After comparing, we came to a point that Carry Select Adders are best suited when Speed is the only criteria while Ripple Carry Adders are best suited for Low Power Applications. Also, we implement the Vedic multiplier using these two adders and found that the carry select adder consume less area on chip and having less delay as compared to multiplier implemented using ripple carry adder.

7. REFERENCES

[1] Purnima M, Shivaraj Kumar Patil, Shivukumar, Shridhar K P ,Sanjay H, "Implementation of Multiplier using Vedic Algorithm", International Journal of Innovative Technology and Exploring Engineering (IJI-TEE) ISSN: 2278-3075,Volume-2, Issue-6, May 2013.

[2] Prakash Narchi, Siddalingesh S Kerur, Jayashree C Nidagundi, Harish M Kittur and Girish V, " A Implementation of Vedic Multiplier for Digital Signal Processing", IJCA Proceedings on International Conference on

VLSI, Communications and Instrumentation (ICVCI) (16):15,2.

[3] Swami Bharati Krishna Tirthaji Maharaja," Vedic Mathematics", Motilal Banarsidass Publishers,1965.

[4] Pushpalata Verme,"Design of 4x4 bit Vedic Multiplier using EDA Tool", International Journal of Computer Applications (0975 888) Volume 48 No. 20 June 2012.

[5] Premananda B.S., Samarth S. Pai, Shashank B., Shashank S. Bhat, "De-sign and Implementation of 8-Bit Vedic Multiplier", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering(An ISO 3297: 2007 Certified Organization) Vol. 2, Issue 12, December 2013.

[6] B. Ratna Raju, D. V. Satish , "A High Speed 16*16 Multiplier Based On Urdhva Tiryagbhyam Sutra", International Journal of Science Engineering and Advance Technology, IJSEAT, Vol 1, Issue 5, October 2013.

[7] Aniruddha Kanhe, Shishir Kumar Dasand Ankit Kumar Singh, "Design and Implementation of Low Power Multiplier using Vedic Multiplication Technique", International Journal of Computer Science and Communication, Vol. 3, No. 1, June 2012, pp. 131-132.

[8] Anju and V.K. Agrawal, "FPGA Implementation of Low Power and High Speed Vedic Multiplier using Vedic Mathematics ",IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 2, Issue 5 Jun. 2013, ISSN:2319, 4200,pp.51-57

