Comparative Study of Spurious Power Suppression Technique Based Carry Look Ahead Adder And Carry Select Adder

Swarnalika Nagi[1], Ms. Jagandeep Kaur[2], Ms. Nisha Charaya[2]
[1] Student M.Tech VLSI Design, Amity University Haryana
swarnalika10@gmail.com
[2]Asst. professor, Amity school of Engineering & Technology, Amity University Haryana
jkaur@ggn.amity.edu
charayanisha1010@gmail.com

***Abstract*:** In the current era, speed and power being the essential characteristics of any digital circuit, emphasis is on designing low power, high speed adders. The significance of adder, a digital sub-system is well known by designers and engineers. Research is still going on adders by the design engineers by including new novel design techniques to speed up the circuit along with power reduction. It's difficult to design a digital adder with sufficient power reduction with the reduced propagation delay. Most demanding adder is the carry select adder which is very useful in digital processing systems to achieve faster arithmetic results. There is a possibility of reducing the power consumption, area and propagation delay in the existing Carry select adders. In this paper, spurious power suppression technique (SPST) based carry select adder (CSLA) and carry look ahead adder (CLA) have been designed using Verilog and compared.

Keywords: *Carry Select Adder, SPST, Detection Unit, Carry Look ahead adder.*

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I. INTRODUCTION

Digital computers perform a variety of information tasks. Among the various functions performed are the arithmetic and logic operations with addition being the most basic arithmetic operation of two binary digits. Adders operate correctly on both unsigned and signed numbers. In many computation based processors, adders are used not only in the arithmetic logic unit (ALU), but also in other parts of the processor, where they are used to calculate addresses, table indices, and many more.

ALU is a feature of logic design which develops appropriate algorithms to attain an efficient utilization of the existing hardware. The backbone behind the functioning of hardware is the algorithm which builds a hierarchy of Boolean and arithmetic operations to be performed. In ALU, utilization of speed and power are mostly used measures of the effectiveness of an algorithm i.e. there is a need to design high speed, low power adders. Adders consumes most of the time in ALU, if it utilizes the traditional ripple-carry adder.

Design of adders with high speed and low power consumption along with less area is still a interesting area of research. Depending upon the constraints such as area, speed, and power, adders are of many types such as ripple carry adder (RCA), CSLA, and CLA.

The general strategy for designing fast adders is to modify the existing adders so as to reduce the execution time by reducing the time necessitates generating carries. Adders which use this strategy are known as carry look- ahead adder. Another essential requirement for any circuit is to minimize power dissipation which can be achieved by incorporating the SPST technique to reduce the unwanted switching activities.

II. SPURIOUS POWER SUPPRESSION TECHNIQUE

SPST is a low power VLSI technique to lessen the unwanted switching activities to reduce power dissipation in the circuit [8]. It utilizes a detection logic block to recognize the effectual or ineffectual data range of arithmetic units, e.g. adder. When a part of data does not influence the final results, the data monitoring units of the SPST latch this part to evade unnecessary data switching activities happening inside the adder. Data monitoring unit provides evident power reduction. It consists of a Pre-computation logic unit which splits the data range of arithmetic units in two categories, depending on whether it affects the results or not. When a part of MSB data doesn't influence the final result, it is stored by the latch circuit of the SPST adder to evade unwanted switching activities occurring inside the multipliers or adders which contributes in power reduction to a large extent.

To understand the SPST, some examples of a 16-bit addition with different conditions are shown in Figure. 1. Transient state has been described in 1st case, which shows that the specious transition of carries take place in the MSP even if the output of the MSP is unaffected. The second and third cases illustrate the addition of one negative and one positive binary numbers with and without carry from least significant positions (LSP). Furthermore, the 4^{th} and 5^{th}cases respectively show the conditions of two negative operands addition without and with Cin from LSP. In these cases, the MSP results are predictable, so the calculations in the MSP are of no use and can be neglected. Eliminating these redundant calculations will not only enhance the power consumption inside the SPST adder/subtractor but also reduce the glitching noises which will affect the next arithmetic circuits [1][5].

CASE 1:

(30) **0000000000011110**
+ (92) **0000000001011100**
(122) **0000000001111010**

(-30) **1111111111100010**
+ (122) **0000000001111010**
(92) **0000000001011100**

CASE 2:

(-71) **1111111110111001**
+ (40) **0000000000101000**
(-31) **1111111111100001**

CASE 3:

(54) **0000000000110110**
+ (-23) **1111111111101001**
(31) **0000000000011111**

CASE 4:

(200) **0000000011001000**
+ (-50) **1111111111001110**
(150) **0000000010010110**

(-63) **1111111111000001**
+ (-14) **1111111111110010**
(31) **1111111110110011**

Fig 1: SPST based Addition

III. CARRY LOOK-AHEAD ADDER

As it is a parallel adder, carry-Look ahead adder reduces the propagation delay. The More hardware complexity makes it a costlier adder. The carry logic over fixed groups of bits of the adder is compacted to two-level logic as a result of transformation in the ripple carry adder design. This method makes use of logic gates so as to look at the lower set of bits of the augend and addend to check whether a higher order carry bit is to be generated or not.

It consists of block of full adders and carry ahead logic unit which generates two signals; carry generation (Gi) and carry propagation (Pi) with mathematical representation as

$$Pi = Ai \wedge Bi$$

$$Gi = Ai \,\&\, Bi$$

Signal generation depends on whether the carry will be propagated or generated from previous stage. As propagation (Pi) and generation (Gi) depends on the bits in that particular position, they are generated separately and the adder doesn't have to wait for Cin. This way it reduces delay and speeds up the adder functionality.

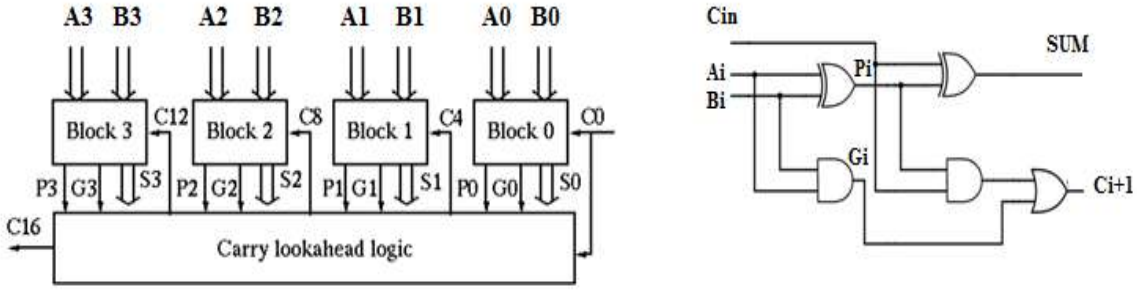

Fig 2: Carry Look Ahead Adder [5]

IV. SPST BASED CARRY LOOK AHEAD ADDER

The SPST based Low power CLA is shown in Fig. 3.This adder is using two blocks, one for MSB's known as Most Significant Part (MSP) and the another for LSB's known as the Least Significant Part (LSP).The LSP adder is implemented like a conventional adder [8].MSP differs from the existing design of adder and is improved with the help of pre-computation logic circuits, latches to store unwanted carry and a signed extension circuit. The pre-computation component uses detection unit to find out the unwanted switching activity from the MSB's of the input and required Cout from LSP part of the proposed adder[2]

provides three outputs as ‘close’ which is used to on/off the MSP circuits, ‘carry_ ctrl’ which represents the (n/2)+1th bit from the LSB of an ‘n’ bit adder and third one is ‘sign’ which represents the remaining (n/2-1) MSP bits of an ‘n’ bit adder[4] are the three outputs provided by Pre-computation or detection logic [8].

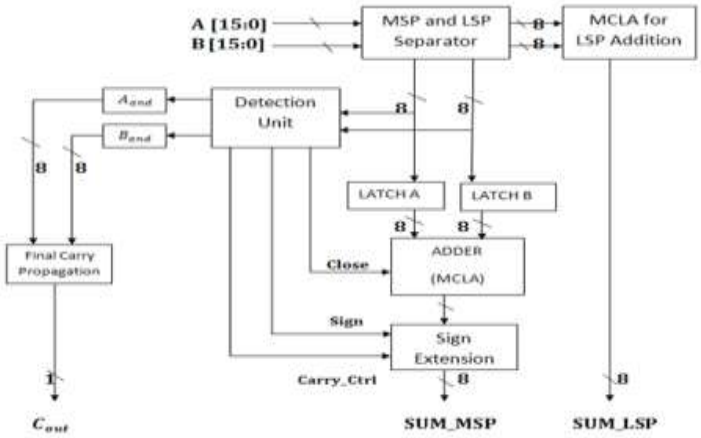

Fig 3: SPST based Carry Look Ahead Adder [7]

V. CARRY SELECT ADDER

The CSLA is modified traditional RCA to resolve the difficulty of propagation delay by producing multiple carry signals and then selecting a carry signal to get final sum. The key objective of carry-select adder is to utilize two ripple-carry adders block, one of which is fed with a Cin as 0 whereas the other is fed with a Cin as 1. As a result, calculation can be done in parallel by both blocks. When the exact Cin signal for the block enters, actual sum is selected by using multiplexers. Also, the final Cout is selected and propagated further. However , the adder for the LSB’s will always have a Cin as 0 so no parallel addition is required in this case.

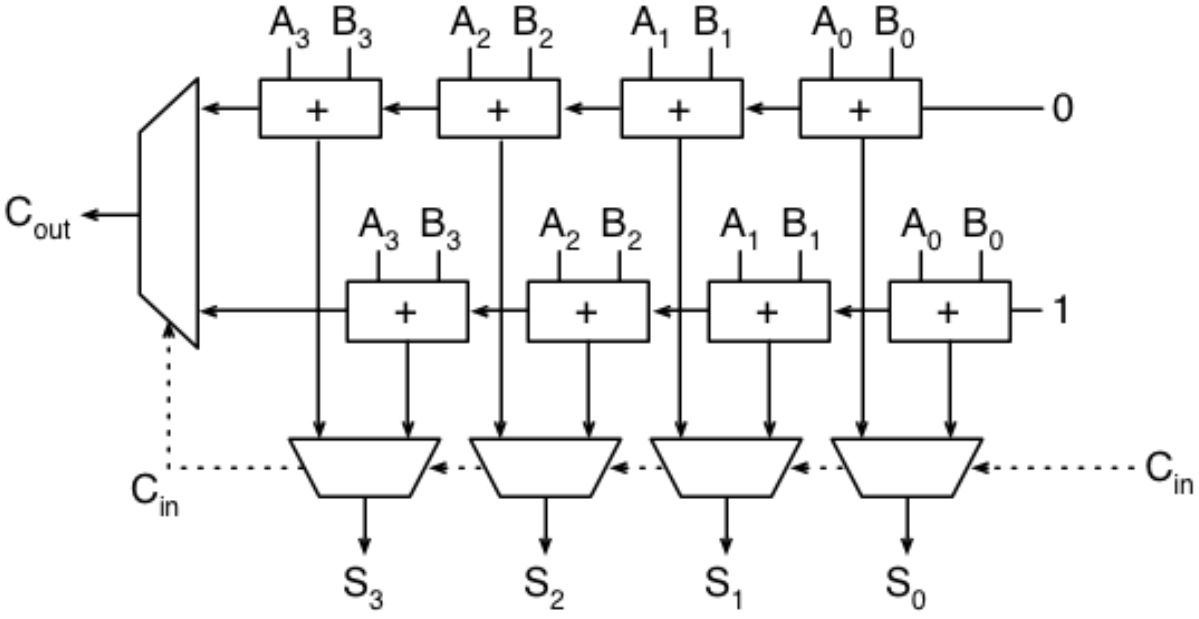

Fig 4: Carry Select Adder [6]

VI. PROPOSED WORK

SPST based Carry Select Adder

In modified carry select adder, technique named as Spurious Power suppression technique has been used. In this SPST carry select adder, a detection unit is used to avoid unwanted MSB carry. By using this technique, signed binary numbers can also be added by CSLA [4]. In modified CSLA, adder has been divided in two parts MSB CSLA and LSB CSLA as shown in fig 5.

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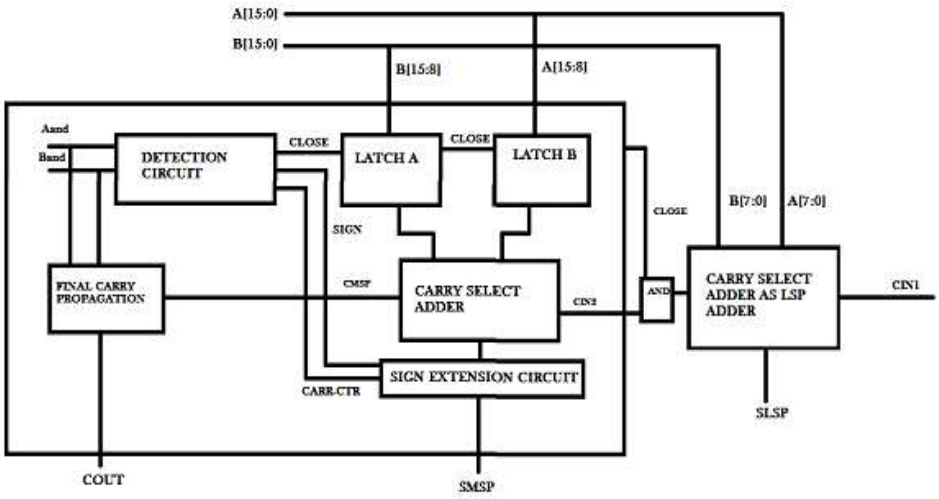
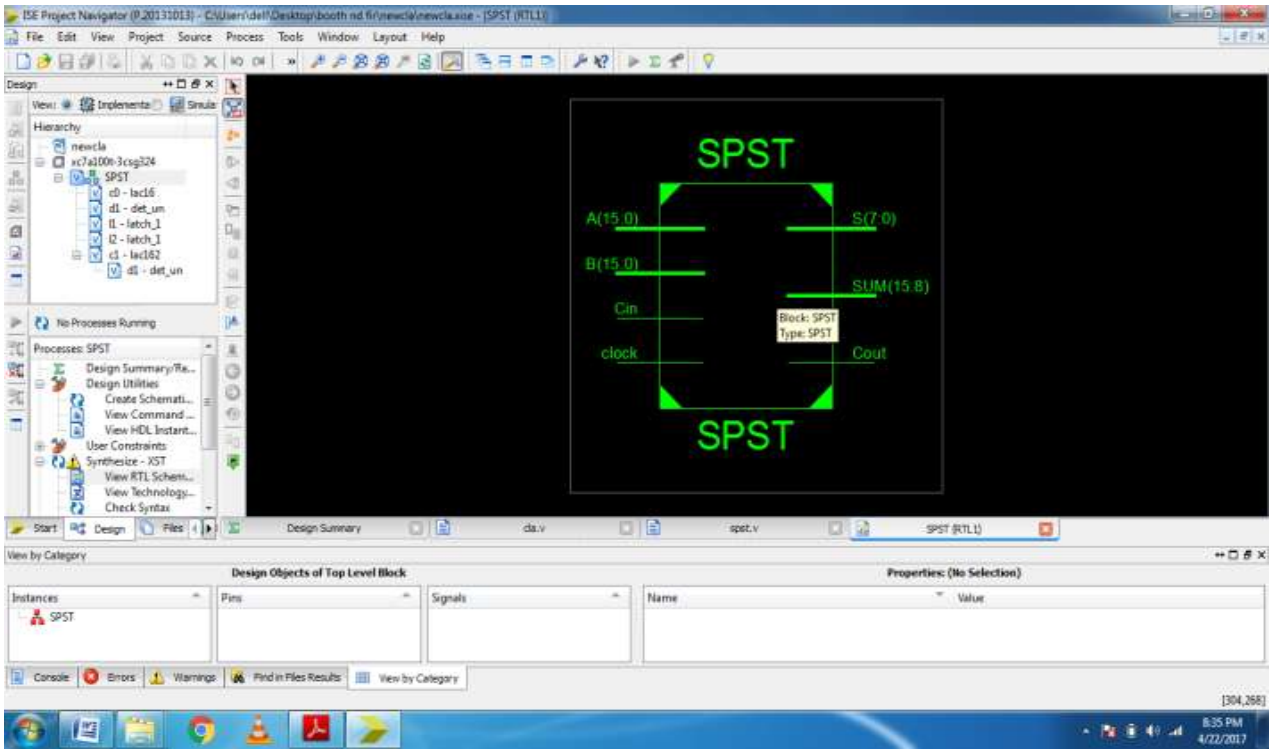


Fig 5: Carry Select Adder using SPST

VII. IMPLEMENTATION DESIGN

SPST based CLA and proposed SPST based CSLA have been implemented on Xilinx 14.7 using Verilog. The schematics of these two adders are summarized as follows:

SPST Based Carry Look-Ahead Adder



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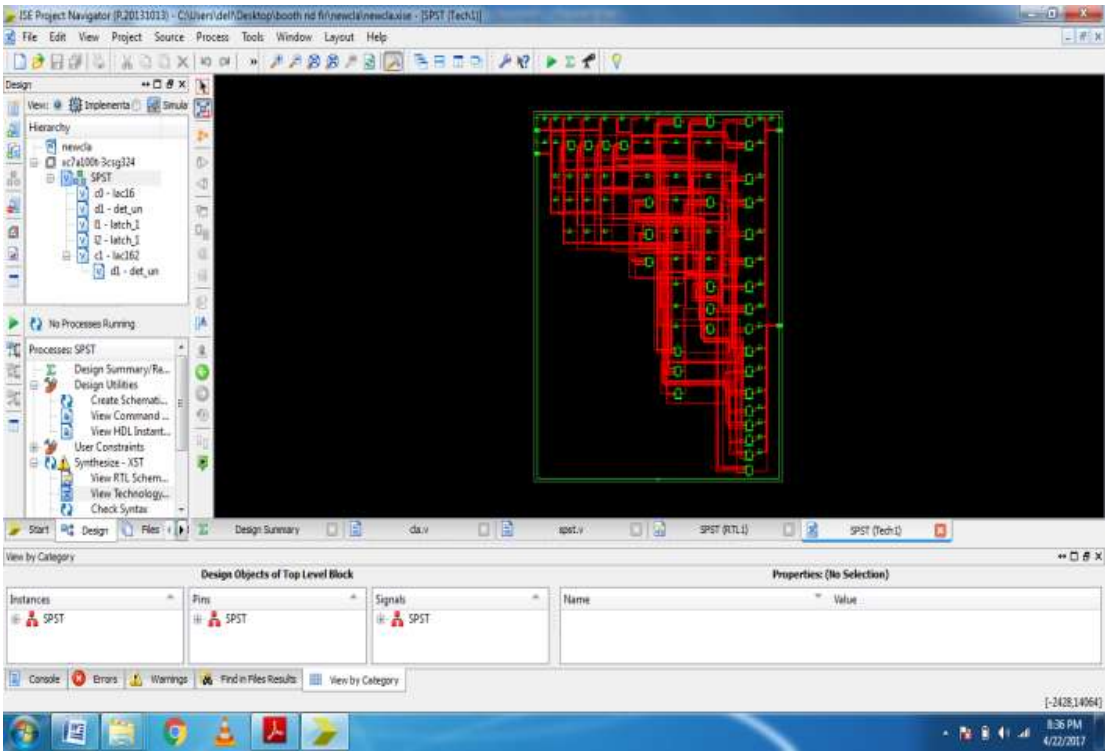

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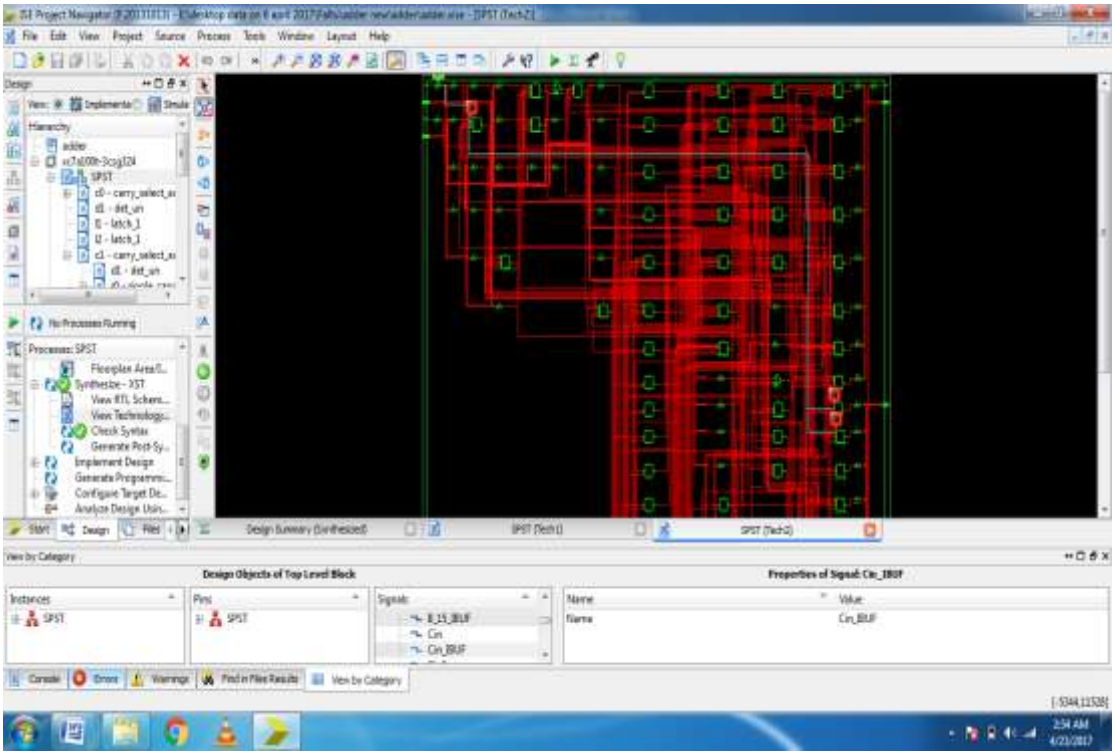
Fig 6: (a) RTL schematic, (b) Technology Schematic

SPST based Carry Select Adder



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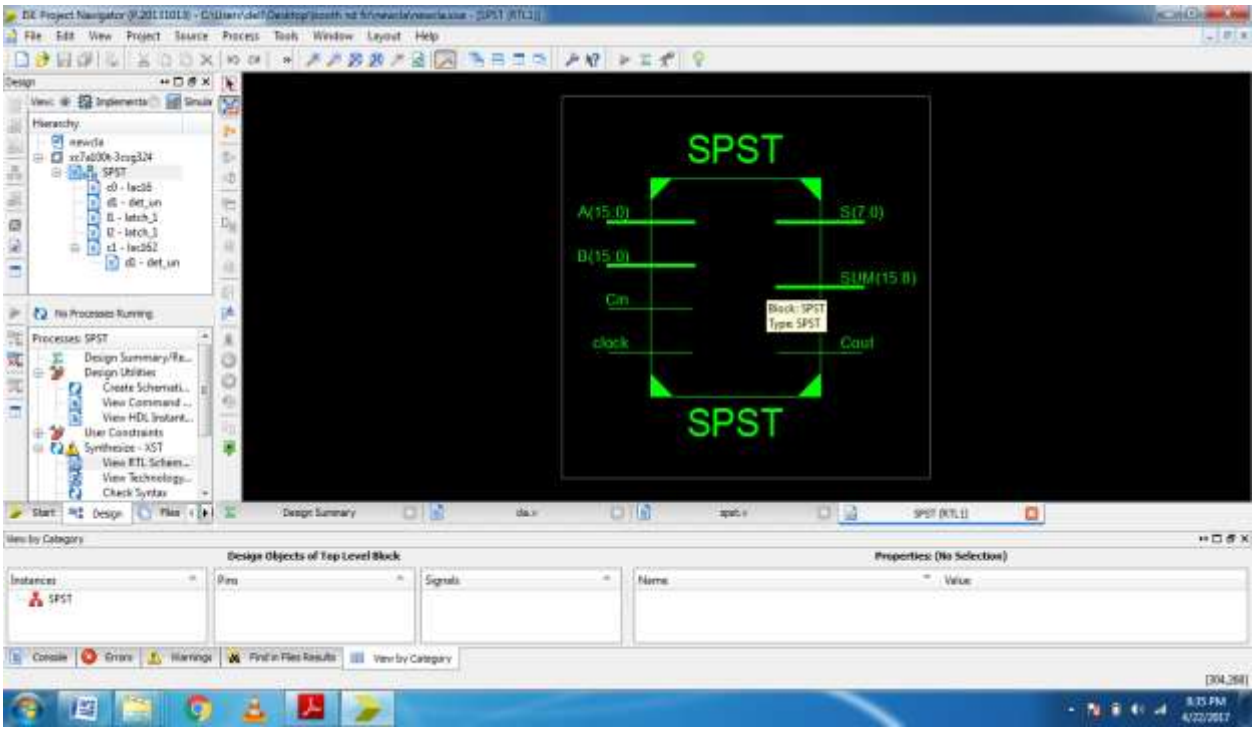

(b)

Fig 7: (a) Technology Schematic (b) RTL schematic

VIII. SIMULATION RESULTS

Output waveforms of SPST based CLA and proposed SPST based CSLA for unsigned & signed numbers are shown in Fig 8 and Fig 9. Table 1 shows comparison between the parameters of these two adders.

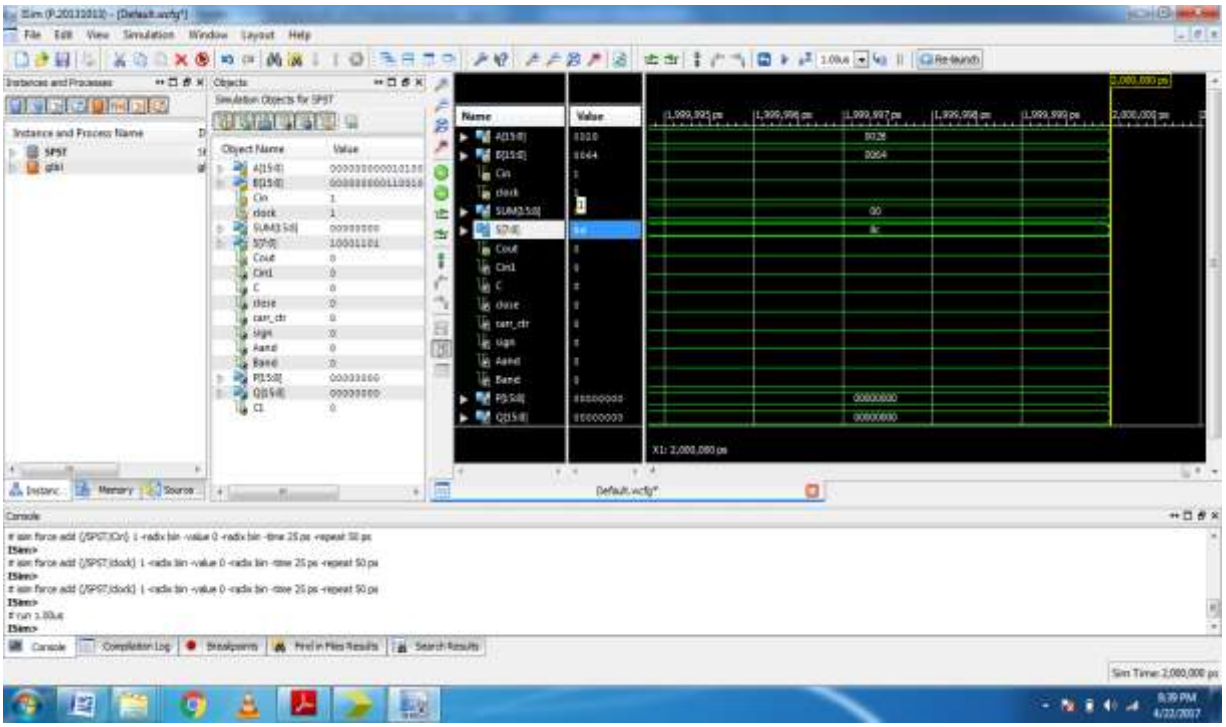

Fig 8: Output Waveform of SPST based CLA

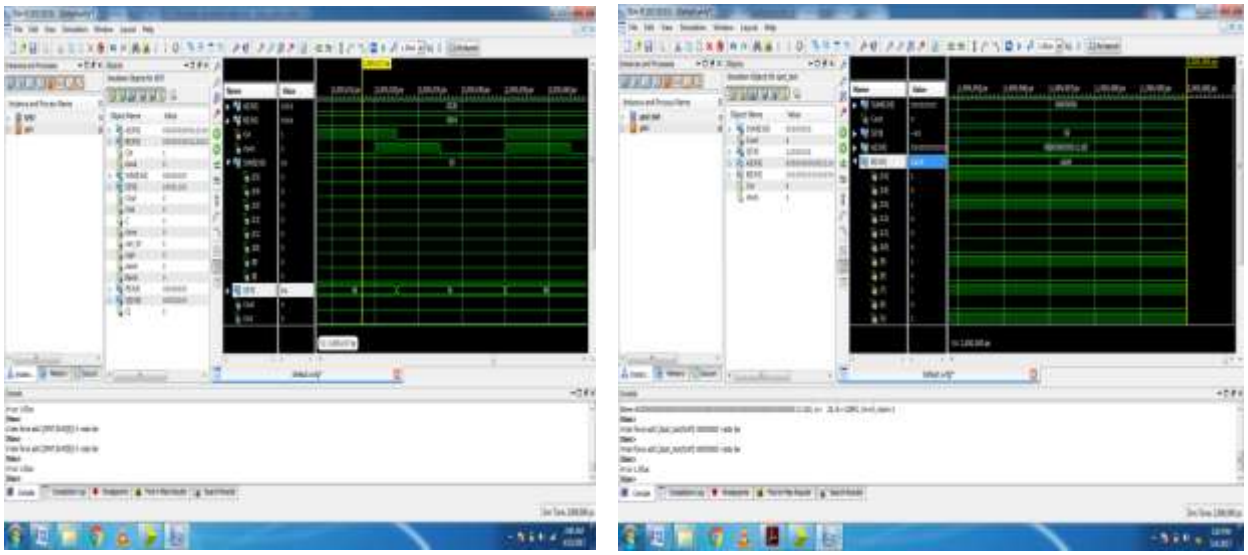

Fig 9: Output Waveforms of SPST based CSLA for unsigned and signed numbers

Table: 1 Comparison between SPST based CSLA and other adders

S.No.	ADDERS	No. of LUT used	DELAY(ns)	POWER(mW)
1.	Carry Look Ahead Adder	24	5.695	123
2.	SPST Carry Look Ahead Adder	16	4.709	105.97
3.	Carry Select Adder	12	4.950	116.39
4.	SPST Carry Select Adder	8	3.095	82

IX. CONCLUSION

A high speed and low power SPST based CSLA has been designed. Table 1 show that SPST based CSLA leads to an effective enhancement in the performance in terms of speed and power consumptions when compared with SPST based CLA. This design is synthesized using Xilinx 14.7 using Verilog HDL coding.

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