International Journal of VLSI System Design and Communication Systems

ISSN 2322-0929
Vol.04, Issue.13,
December-2016,
Pages:1633-1638

www.ijvdcs.org

A Spurious-Power Suppression Technique for Multimedia/DSP Applications

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Abstract: This project provides the experience of applying an advanced version of Spurious Power Suppression Technique (SPST) on multipliers for high speed and low power purposes. When a portion of data does not affect the final computing results, the data controlling circuits of SPST latch this portion to avoid useless data transition occurring inside the arithmetic units, so that the useless spurious signals of arithmetic units are filter out. Modified Booth Algorithm is used in this project for multiplication which reduces the number of partial product to n/2. To filter out the useless switching power, there are two approaches, i.e using registers and using AND gates, to assert the data signals of multipliers after data transition. The simulation result shows that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a speed improvement and power reduction.

Keywords: Digital-Signal Processing Chips, Image Coding, Low-Power Design, Video Coding.

I. INTRODUCTION

Multiplication is an important part of real-time digital signal processing (DSP) applications ranging from digital filtering to image processing. Lowering down the power consumption and enhancing the processing performance of the circuit designs are undoubtedly the two important design challenges of wireless multimedia and DSP applications, in which multiplications are frequently used for key computations, such as FFT, DCT, quantization, and filtering. All multiplication methods share the same basic procedure - addition of a number of partial products. A number of different methods can be used to add the partial products. The simple methods are easy to implement, but the more complex methods are needed to obtain the fastest possible speed. The simplest method of adding a series of partial products is shown in Fig.1. It is based upon an adder-accumulator, along with a partial product generator and a hard wired shifter. This is relatively slow, because adding N partial products requires N clock cycles. The easiest clocking scheme is to make use of the system clock, if the multiplier is embedded in a larger system. The system clock is normally much slower than the maximum speed at which the simple iterative multiplier can be clocked, so if the delay is to be minimized an expensive and tricky clock multiplier is needed, or the hardware must be self-clocking. In this paper Modified Booth Algorithm is used with detection logic, which will suppress the needless power in the circuit and also speed has been increased. Booth Algorithm also reduces the hardware size of the circuit by reducing the partial product by half.

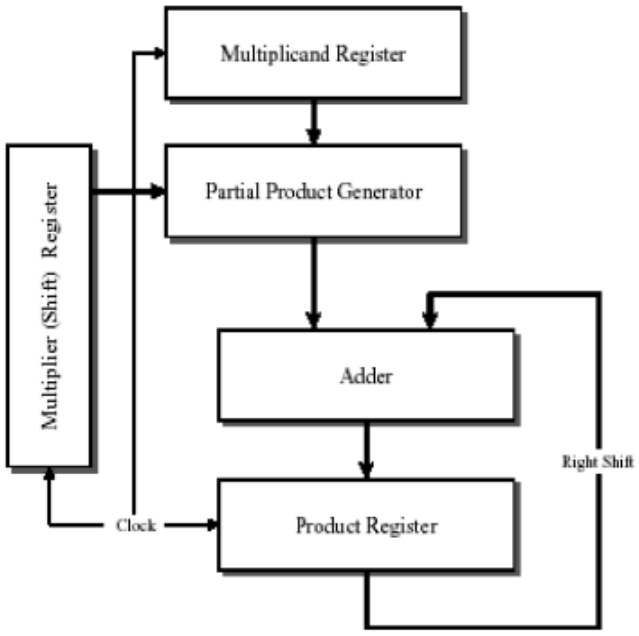

Fig.1.

II. SPST AS PRECOMPUTATION LOGIC

Pre Computation logic is one of the efficient Low power VLSI techniques to reduce the useless power dissipation in the circuits. The influence of the spurious signal transitions illustrated as five cases of a 16-bit addition is explored as shown in Fig. 2. The case1 illustrates a transient state in which the Spurious transitions of carry signals occur in the MSP though the fina1 result of the MSP are unchanged. The 2nd and 3rd cases describe the situations of one negative

operand adding another positive operand without and with carry from LSP, respectively. Moreover, the 4th 5th cases respectively demonstrate the conditions of two negative operands addition without and with carry-in from LSP. In those cases, the results of the MSP are predictable, therefore the computations in the MSP are useless and can be neglected. Eliminating those spurious computations will not only save the power consumed inside the SPST adder/subtractor but also decrease the glitching noises which will affect the next arithmetic circuits.

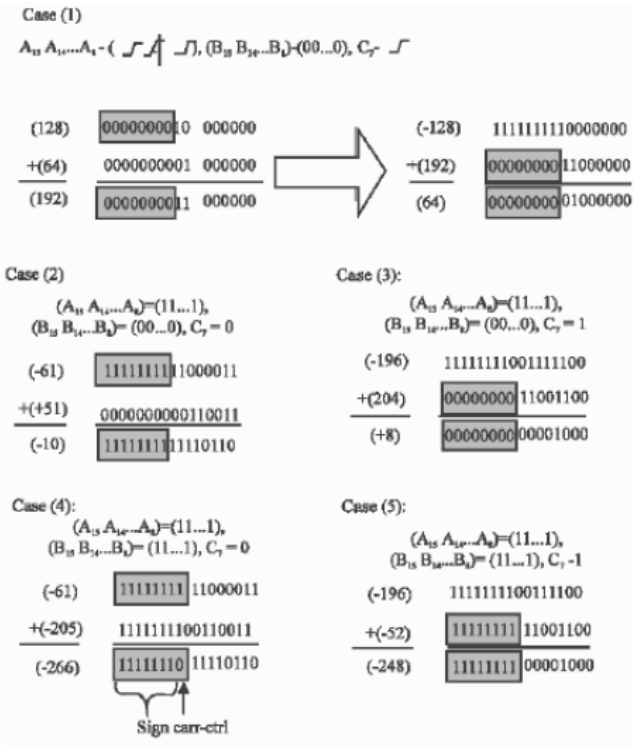

Fig.2.

From the above fives cases we can design the pre computation logic circuit (Detection Logic) as shown in Fig.3 which will avoid the useless computations so that the useless power has been reduced.

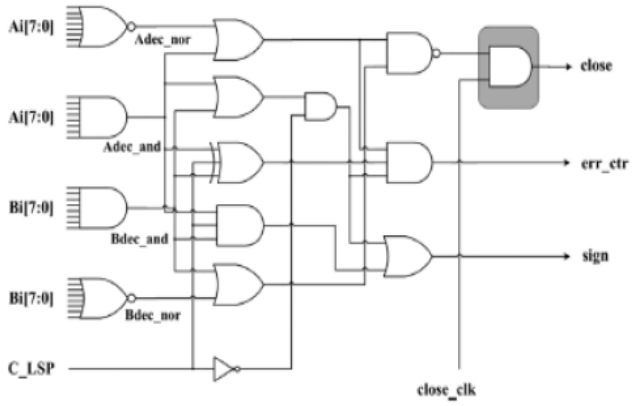

Fig.3.

In this paper the above detection logic is used to detect the unwanted MSB calculations, so that unwanted power dissipations were avoided. The SPST adder can be designed by using this detection logic to achieve power efficiency while adding Partial products, such a SPST adder is shown in Fig.4 below.

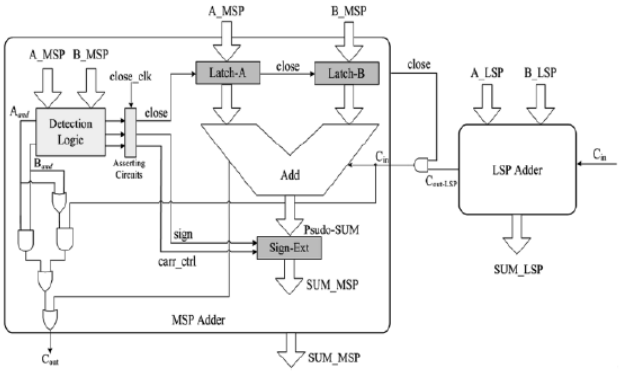

Fig.4.

III. LOW POWER MULTIPLIER DESIGN USING SPST

The Modified Booth algorithm is used for Multiplication with SPST technique in this paper.

A. Applying SPST on Modified Booth Encoder

While multiplying two 16 bit numbers through booth algorithm eight partial products produced, but some of the partial product may contain all the bits as zero, so saving those computations can significantly reduce the power consumption caused by the transient signals. We propose the SPST-equipped modified-Booth encoder, which is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. As shown in Fig. 5, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero, to reduce the transition power dissipation. Such cases occur frequently in e.g., FFT/IFFT, DCT/IDCT, and Q/IQ which are adopted in encoding or decoding multimedia data.

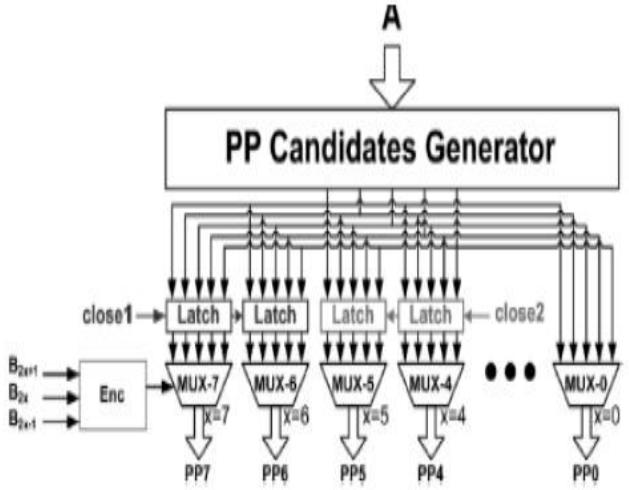

Fig.5.

B. Applying SPST on Compression Tree

The proposed SPST-equipped multiplier is illustrated in Fig.6. The PP generator generates five candidates of the partial products, i.e., {-2A; -A; 0; A; 2A}, which are then selected according to the Booth encoding results of the operand B. Moreover, when the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPST-equipped adders, which are marked with oblique lines in Fig. 6. The bit-widths of the MSP and LSP of each SPST-equipped adder are also indicated in fraction values nearing the corresponding adder in Fig. 6.

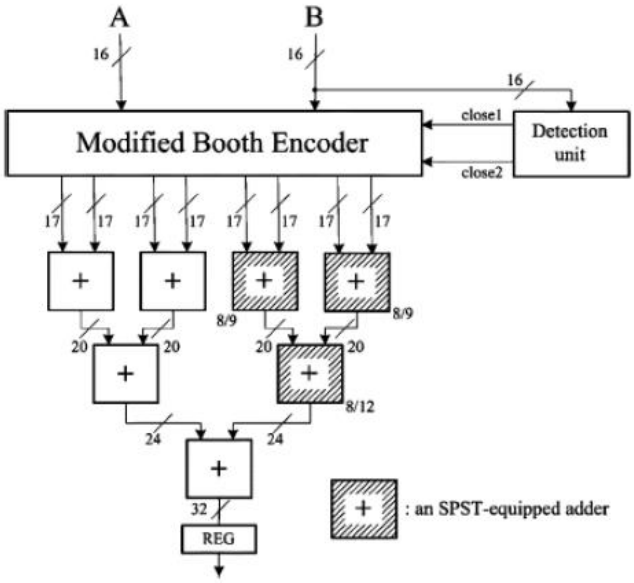

Fig.6

IV. PERFORMANCE EVALUATION AND COMPARISON

Comparing the proposed SPST adder/subtractor designs with the existing pre-computation techniques, we can start from two points of view. From the quantitative point of view, the performance comparison of the SPST ETD shall represent the trend of the performance comparison of the SPST adder/subtractor, since all the computations are simplified into additions/subtractions and shift operations in the integer transform of H.264. From the qualitative point of view, the concept of proposed SPST adder/subtractor is similar to the PGC design [8]. Both of these two techniques use a detection-logic unit to determine the effective ranges of the input data, a SE unit to compensate for the correct sign signals, and data latches to block the input data. However, the proposed SPST has a critical improvement in filtering out the glitches inside the adders/subtractor using only three 1-bit registers to control the assertion of the close, sign, and carr-ctrl signals, respectively. The realizing approaches of the data latches and the SE units are also different from [8]. The designs in [9] and [10] present another realizing approach based on the similar concept with the PGC designs. Never the-less, their applications on multipliers may not gain power saving because the input data flows are switched frequently when the input operands with a smaller effective dynamic range often exchange between operands A and B.

This problem will not occur in this paper. The design it presents two low-power techniques, i.e., the most significant bit (MSB) rejection (MSBR) and the row–column classification (RCC). The MSBR method, a kind of pre-computation technique, uses a circuit to determine whether the most significant bits of an operand are the same or not. This circuit is conceptually analogous to the detection-logic unit in the PGC and SPST. The MSBR circuit outputs a mask signal to control the activation of the ROM and accumulator (RAC) unit in the DCT core using gated clocks. Hence, there is no SE unit in the MSBR approach. The RCC method, on the other hand, trades off image quality with power dissipation.

TABLE I: Measuring Results Of The Proposed Spst-Equipped Etd With 1.8-V Supply Voltage, Where "Spst Off" Denotes That The Spst Function Is Turned Off And "Spst On" Denotes That The Spst Function Is Turned On

Freq. (MHz)	Applications	Power (P, mW)		Reduction of P. (%)
		SPST ON	SPST OFF	
22	HD 720p	5.49	7.57	27.48
50	HD 1080i	12.05	16.59	27.37
100	Digital cinema	24.18	33.25	27.28

A. Evaluation and Comparison of the SPST-Equipped ETD

The measuring results of the proposed SPST-equipped ETD chip are listed in Table I, where "SPST off" and "SPST on," respectively, denote turning off and on the SPST function. By turning on the SPST function, 27.48%/ 27.37%/27.28% power reductions are, respectively, gained when the SPST-equipped ETD is operated at 22/50/100 MHz with 1.8-V supply voltage. This indicates that the proposed SPST technique can certainly reduce the power dissipation of transform coding for H.264. Table V compares the performance of the proposed SPST-equipped ETD with some existing H.264 transform designs. The design offers a hardware implementation for the transform and quantization of H.264. This design adopts a parallel architecture to unfold the 2-D transform to avoid using a transpose memory; thus, it achieves a high throughput of 16 pixels per cycle. However, it is hard for the parallel-transform design to process in full speed because the input and output data are seldom transmitted in such a high-parallelism way due to practical constraints. The design presents an H.264 transform realization that contains two 1-D transform PEs and 16 registers served as the transpose memory with hardware cost of 6538 gates. This design has a rather low throughput of only four pixels per cycle. Further- more, the design uses only one 1-D transform PE, in a recursive manner, and 16 registers, served as the transpose memory, with the hardware cost of 3524 gates to realize the transform coding of H.264. The throughput of this design is even lower as one pixel per cycle.

In both the design, the transpose register array occupies a crucial portion of the total hardware expense. In Table II, we adopt an index named data Throughput rate Per Unit Area (TPUA), which is computed from dividing the throughput rate of each design listed in the fourth column by the corresponding area cost listed in the second column, to objectively evaluate the hardware efficiency of the SPST-equipped ETD. The TPUA index shows that the proposed design is at least 1.6 times more efficient than the existing designs.

TABLE II: Hardware Efficiency Comparisons Of The Spst-Equipped Etd And The Existing H.264 Transform Designs. "Tpua" Stands For Data Throughput Rate Per Unit Area

Designs	Area (gate)	Freq. (MHz)	Throughput (M pixels /sec)	TPUA (pixels/sec/gate)
Kordasiewicz [20]	77280	107	1712	22.15 k
Wang [21]	6538	80	320	48.94 k
Wang [21] redesigned	6274	100	400	63.76 k
Liu [22]	3524	129	129	36.61 k
SPST-equipped ETD	7839	100	800	102.05 k

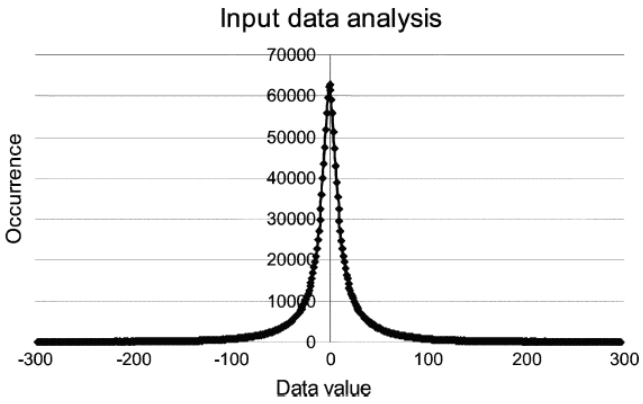

Fig.7. Data analysis of the input data of the texture coding in H.264 where the video sequence is "Foreman," the quantization step is 20, and the total data number is over two million.

B. Evaluation and Comparison of the SPST-Equipped VMFU

The data analysis of the input data of multiplications in H.264 texture coding is shown in Fig.7. The video sequence is "Foreman," and the quantization step is 20. The total number of the input data is more than two million. From the quantitative analysis of Fig.7, we can tell that 95% of the input data are concentrated in the range between -95 and +95 among the total range between -2^{14} and $+2^{14}$. The improvement in applying the SPST on the VMFU, classified into two phases, is shown in Fig.8. In the first phase, the SPST is applied only on the compression tree of the VMFU which results in an 8% power reduction at the cost of a 9% area increment. In the second phase, the SPST is further applied on the modified Booth encoder which consumes considerable power dissipation, enlarging the power reduction to 24%. In addition, Fig.9 shows the power results of the VMFU without and with the SPST, respectively. On the VMFU, the SPST can achieve a 24% power reduction at the cost of only a 10% area increment when compared with the original VMFU without equipping the SPST. This reveals that the SPST can save obvious power consumption of the VMFU at a rather tiny area cost, and we may extend the applications of the SPST to other circuits by finding a niche for the SPST in the target circuit.

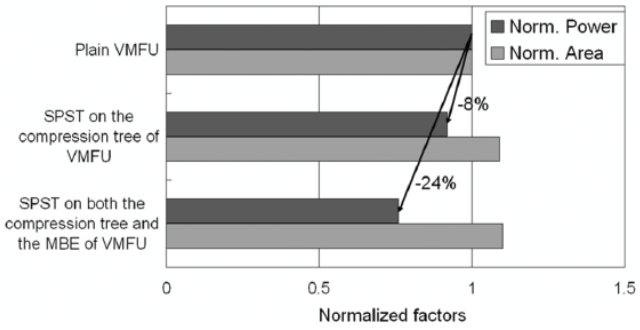

Fig.8. Power improvements using the SPST.

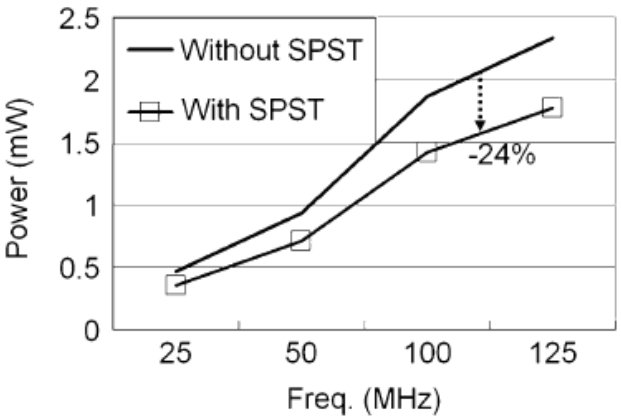

Fig.9. Power reduction of the SPST for the VMFU.

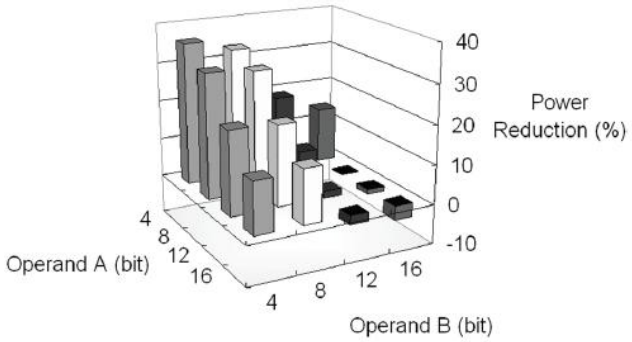

Fig.10. Power reduction of the proposed SPST on multiplication A*B for different effective ranges of Normal distribution of the operands using VMFU.

Besides measuring the power dissipation in terms of multimedia applications, we provide the power analysis in terms of the inputs of different effective ranges using the normal distribution. Fig. 10 shows the power reduction of the proposed SPST on multiplication for different effective

ranges, i.e., 4-, 8-, 12-, and 16-bit, of the operands using the VMFU. The figure reveals the following conditions.

- The power reduction can reach up to 31%–36% if both the effective data ranges of operands A and B are smaller than or equal to 8 bit, by using the proposed SPST.
- When the effective data range of operand B is smaller than or equal to 8 bit and that of operand A is 12 or 16 bit, the SPST also obviously saves power consumption for VMFU, e.g., around 21% or 13% power savings for 12- or 16-bit wide operand A, respectively. This achievement mainly results from operand B being Booth encoded and the pro-posed SPST being able to reduce the power dissipation of the Booth encoder apparently.
- Moreover, the proposed SPST can reduce the power consumed in the compression tree besides the Booth encoder. When operand B is 12-bit wide, the power reduction is 19% or 8%, respectively, for the 4- or 8-bit wide operand A. Additionally, there is a 14% power saving in the case of multiplying 4-bit wide operand A with 16-bit wide operand B.

Furthermore, this paper examines some modern multiplier or MAC designs because the basic architecture of VMFU is similar to them. The design includes three techniques, i.e., the signal flow optimization (SFO), left-to-right leapfrog (LRLF) structure, and upper/lower split structure, to optimize the array multipliers. The SFO and LRLF techniques are used for signal balancing of the PPR section in a multiplier. While the upper/lower split structure is used to shorten the path of the PPR section to prevent the snowballing glitch effect. The design turns off some columns in the multiplier array whenever their outputs are known, thus, saving 10% power consumption at the cost of 20% area overhead under a 0.35-µm CMOS technology. The design uses a DRD unit to detect the dynamic range of the inputs and adopts three separate Wallace trees for the 4×4, 8×8, and 16×16 multiplications. Both methods adopted in the design certainly increase the area and capacitance overheads. The design proposes a 32-bit single-instruction–multiple-data MAC unit which is a co-processor to the Intel X Scale microprocessor. Under a 0.18-µm CMOS technology, dissipates 450 mW at 600 MHz with 1.3-V supply voltage. The design a vector MAC unit that can perform one 64×64, two 32×32, four 16×16, or eight 8×8 signed/unsigned multiply accumulations and is fabricated using the 0.13-µm bulk and 90-nm silicon-on-insulator silicon technology. The design it involves a fixed-width 32-bit left-to-right multiplier which obtains 8% speed improvement, 14% power reduction, and 13% area saving. Meanwhile, the design explores a design methodology for high-speed modified Booth multipliers. Finally, design adopts an advanced 90-nm dual V_t CMOS technology to implement a 16 16-bit multiplier that consumes 9mWat 1 GHz with 1.3 V.

Table III lists the performance of some representative existing multipliers and the proposed SPST-VMFU. For the sake of a fairer comparison in a time-economic way, we scale the power results to the same technology, i.e., the 0.18-µm technology with 1.8 V, according to the geometric feature and the well-known power approximation $P = \sum_i \alpha_i C V^2 f$[5], where P, α_i, C, V, and f denote power dissipation, switching activity, capacitance, voltage, and frequency, respectively. Under the situation that all the multiplier designs including the compared ones and the proposed one can meet the performance requirements, the factor of frequency, i.e., f, of all the designs can be assumed to be the same to avoid the frequency-scaling effects. Besides, switching activity, i.e., α_i, is also the same when all the designs are computing for the same applications. Thus, power consumption P is proportional to the product of capacitance and supply voltage only. The capacitance is assumed to be proportional to the silicon area which is proportional to the square of the line width in the technology scaling. Therefore, we can obtain the scaling

TABLE III: Performance Comparison of Existing Multipliers And The Proposed VMFU

Design	Feature	Tech.	Power (mW)	Delay (ns)	Area
Huang [22]	(1) 32b × 32b	0.18-µm	(1) 19.65 for Djpeg (2) 40.65 for Random data @ 100MHz	7.25	74598 (tr.)
Liao [25]	(1) Coprocessor (2) SIMD (3) 32b MAC	0.18-µm	900@1.6V, 800MHz	1.25	N.A.
Wang [27]	(1) 32b × 32b (2) Fixed-width	0.35-µm /3.3V	79.86	14.01	19743 (gate)
Chen [9]	(1) 16b × 16b	0.25-µm	17.30 for *Normal distribution* inputs	8.3	0.337 (mm^2)
Lee [24]	Scalable length of 4b, 8b, 16b	0.13-µm /1.2V	1.04@100MHz for random data	N.A.	6388 (gate)
Hsu [29]	(1) 16b × 16b (2) Sleep mode (3) Duel V_T	90nm	(1) 9@1.3V, 1GHz (1) 7.9×10^{-2} @50MHz, 0.57V	1	0.03 (mm^2)
Proposed	(1) 16b × 16b (2) Versatile functions	0.18-µm	(1) 4.2@100MHz,1.8V (2) 1.25×10^{-1}@25MHz, 0.7V for H.264 IQ (3) 6.3@125MHz,1.8V for *Normal distribution* inputs	8	5232 (gate) or 0.178 (mm^2)

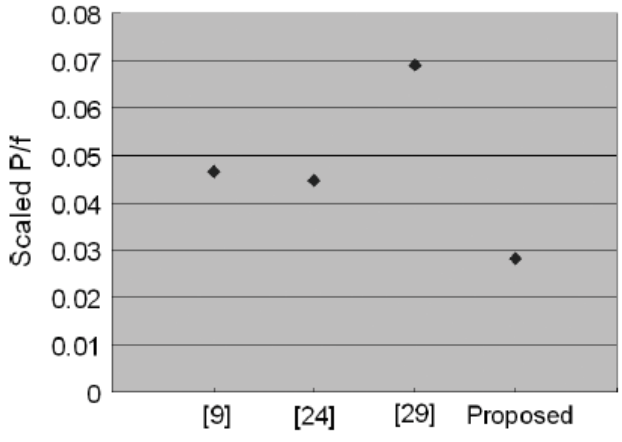

Fig.11. Power comparison of the proposed VMFU.

$$\text{Formulation } P_{sca} = (P_{org}) / \left((Tech_{org}/0.18)^2 * (V_{org}/1.8)^2 \right) \quad \textbf{(1)}$$

where P_{sca}, P_{org}, $Tech_{org}$ and V_{org} denote the scaled power dissipation, original power dissipation, line width in the

original technology, and the original voltage, respectively. Similar scaling approaches are adopted in the design. The scaled results in terms of power per unit frequency are shown in Fig. 10. Because the designs are basically 32-bit multipliers, they are considered as reference indexes only. From Fig. 10, we can find that the proposed VMFU has better power efficiency than the existing multipliers although it involves the augmented circuits for versatile functions.

V. CONCLUSION

The high speed low power multiplier adopting the new SPST is designed. The Multiplier is designed by equipping SPST on a modified Booth encoder which is controlled by a detection unit using AND gate. The modified Booth encoder will reduce the number of partial products generated by a factor two. The SPST adder will avoid the unwanted addition and thus minimize the switching power dissipation. The SPST implementation with AND gate have an extremely high flexibility on adjusting the data asserting time. This facilitates the robustness of SPST can attain significant speed improvement and power reduction when compared with the conventional tree multipliers. This design verified using Xilinx 9.1 using Verilog HDL coding and successfully synthesized.

VI. REFERENCES

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