POST LAB :

module alu\_8bit (

input [7:0] a,

input [7:0] b,

input [2:0] alu\_op,

output reg [7:0] result,

output reg zero

);

always @\* begin

case (alu\_op)

3'b000: result = a + b; // Addition

3'b001: result = a - b; // Subtraction

3'b010: result = a & b; // AND

3'b011: result = a | b; // OR

3'b100: result = a ^ b; // XOR

default: result = 8'b00000000; // Default case, you can choose to assign it to 0 or handle it differently

endcase

zero = (result == 8'b00000000); // Set zero flag

end

endmodule

OUTPUT

