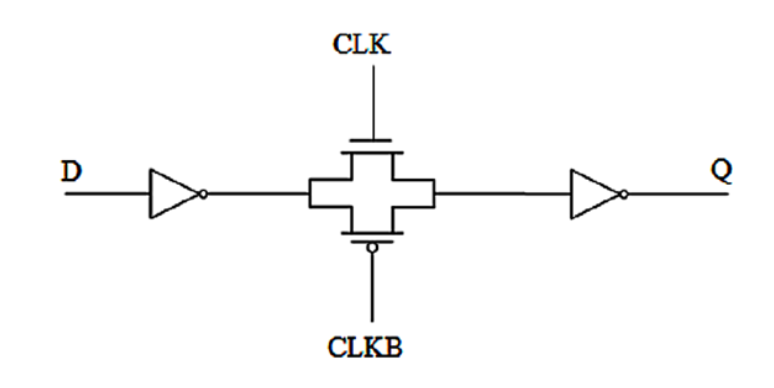
level\_sensitive\_CMOS\_latch



module level\_sensitive\_latch (

input wire D, // Data input

input wire CLK, // Clock input

output reg Q // Output

);

always @ (posedge CLK)

if (D)

Q <= 1'b1;

else

Q <= 1'b0;

Endmodule

TESTBENCH

module TB\_v;

// Inputs

reg D;

reg CLK;

// Outputs

wire Q;

// Instantiate the Unit Under Test (UUT)

level\_sensitive\_latch uut (

.D(D),

.CLK(CLK),

.Q(Q)

);

// Clock generation

always #((PERIOD / 2)) CLK = ~CLK;

initial begin

// Initialize Inputs

D = 0;

CLK = 0;

// Wait 100 ns for global reset to finish

#100;D = 1; #100;D = 0; #100;D = 1; #100;D = 0;

end

endmodule

OUTPUT

