EXP 8 POSTLAB

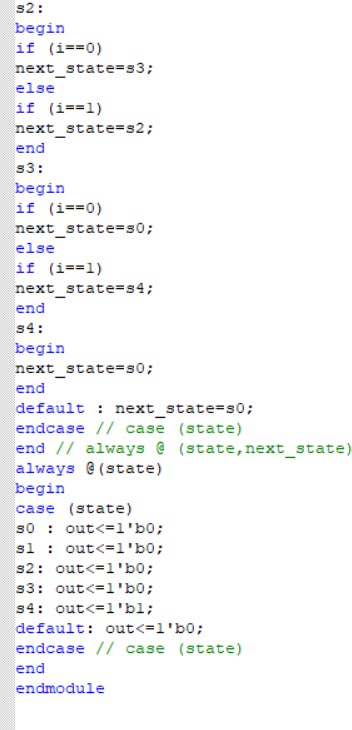
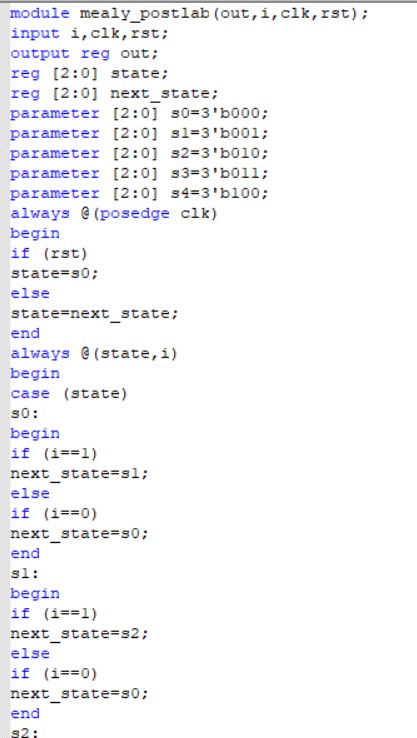


Fig 8.1 Verilog Code

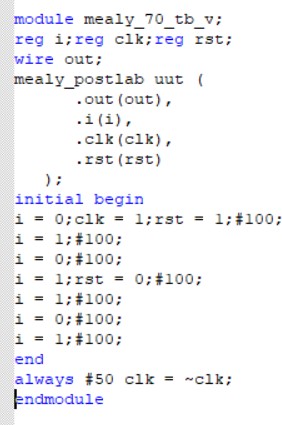


Fig 8.2 Testbench

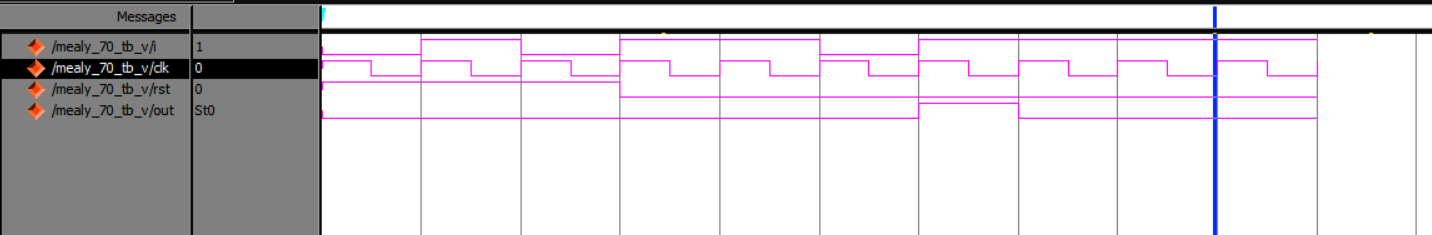


Fig 8.3 Output Waveform