VISVESVARAYA TECHNOLOGICAL UNIVERSITY

MINI PROJECT REPORT ON

“SPEED CONTROLLED DC MOTOR”

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CERTIFICATE

Certified that the mini project work entitled "**SPEED CONTROLLED MOTOR**" carried out by **C.ABHINAY KUMAR REDDY(1NH18EC026)** bonafide students of Electronics and Communication Department , New Horizon College of Engineering, Bangalore.

The mini project report has been approved as it satisfies the academic requirements in respect of mini project work prescribed for the said degree.

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ACKNOWLEDGEMENT

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ABSTRACT

The speed control of direct **current (DC)** motor for various applications is very important. In particular requirement, setting a speed DC motor as the driving equipment must be performed remotely. Under that **condition,** conduHed a research on a DC motor speed control with pulse width modulation **(PWM)** method of the infrared remote control. **PWM** is method that may be used as an efficient DC motor speed control.

Pube width modulation (PWM), or pulse-duration modulation (PDM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage (and Current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate.

PWM is particularly suited for running inertial loads such as motors, which a not as easily affected by this discrete switching, because ey have inertia to react slow. The PWM switching frequency has to be high enough not to affect the load, which is to say that the resuKant waveform perceived by the load must be as smooth as possible.

CHAPTER 1

INTRODUCTION

Today's industries are increasingly demanding process automation in all sectors. Automation results into better quality, increased prod ion an reduced costs. The variable speed drives, which can control the speed of A.C/D.C motors, are indispensable controlling elements in automation systems. Depending on the applications, some of them are fixed speed and some of the variable speed drives.

The variable speed drives, till a couple of decades back, had various limitations, such as poor efficiencies, larger space, lower speeds, etc., Howev the advent power electronic devices such as power MOSFETs, IGBTs etc., and today we have variable speed drive systems which are not only in the smaller in size but also very efficient, highly reliable and meeting all the stringent demands of various industries of modern era.

Direct currents (DC) moths have been used in variable speed drives for a long time. The versatile characteristics of dc motors can provide high starting torques which is required for traction drives. Control over a wide speed range, both below and above the rated speed can be very easily achieved. The methods of speed control are simpler and less expensive than those of alternating current motors.

There are different techniques available for the speed control of DC motors. The phase control method is widely adopted in which ac to dc converters are used to supply the dc motors, but has certain I Imitations mainly it generates harmonics on the power line and it also has poor p.f. when operated at lower speeds. The second method is pwm technique, which has got better advantages over the phase control.

CHAPTER 2

LITERATURE SURVEY

The DC motors a re In general much more adaptable speed drives than AC motors which are associated with a constant speed rotating field. Indeed one of the p rimary reasons for the strong competitive position of DC motors in modern industrial drives is the wide range of specified afforded we know the equation

N= K ( )

=K (V—la Ra / q)

Where V=supply voltage (volts)

la = armature current (amps)

Ra=armature resistance (ohms)

O=fux per pole (Weber)

This equation gives two methods of effective speed changes i.e.

a) The variation of field excitation, if this causes in the flux per pole @ and is known as the field control.

b) The variation of termi nal voltage (V).this method is known as armatu re control.

a) FLUX CONTROL METHOD:

It is known that N a 1/ @ by decreasing the flux, thus speed can be increased and vice versa. Hence, name flux or field control method.

e flux of DC motor can be changed by changing with help of a she field rheostat. Since in relatively small, shunt field rheostat has to carry only a small, so that rheostat is small in size. This method therefore very efficient in non-interpolar mach s the speed can be increased by this method in the ratio 2:1 any further weakening of flux @ adversely affect the communication

And hence puts a limit to the maximum speed obtainable with this method in machines fitted with interloper in ratio of maximum to minimum speeds of 6:1 is fairly common.

b) ARMATURE OR RHEOSTAT CONTROL METHOD:

This method is used why speeds below the no load speed are required. As the supply voltage is rmally constant, the voltage across the armature is varied by inserting a variable rheostat or controller resistance in series with the armature circuit as shown in fig1.3 as controller resistance is increased, potential difference across the armature is decreased, thereby decreasing the armature speed. For a load of constant torque, speed is approximately proportional to the potential difference.

CHAPTER 3

PROPOSED METHODOLOGY

In our proposed project, a 5 H.P DC shunt motor circuitry is designed, and developed usi ng pulse with modulation (PWM).The pulse width modulation can be achieved in several ways. In the present project, the PWM generation is done using timer IC.

In order to have better open loop speed control as demand varies frequently like In traction system and many operations in industry must be control manually, PWM is most efficient and cheap speed control method for dc drives. By varying resistor pot only we can control the speed of motor states that simple and easy method.

Fig 1

CHAPTER 3.1

COMPONENTS REQUIRED

S.No.	Re9u ired Components	Remarks	Quantity
1	IC's	NE555	1
2	Transistor	IRF540 MOSFET	1
3	Diode	1NH4001 1N5819	1 2
4	Water pump	3-6 V 80-120 L/H	1

		DC Magnetic driving	
5	Resistor	Quarter watt	10k ohm - 3 100k Ohm(POT) — 1
6	Capacitor	Ceramic	100nF —1 100pF - 1

CHAPTER 4

PROJECT DESCRIPTION

Pi n 1 of 555 is connected to GND. Pi ns 8 and 4 are connected to +12V Su pply.

Pins 6 and 2 are short and a 100nF Capacitor is connected between Pin 2 and GND. The wiper pin of the POT is connected to Pin 3 of 555. Two Schottky diodes (1N5819) are connected to the other two pins of the POT as shown in the circuit diagram.

The common point of the diodes 1s connected to Pin 2. Pin 7 is pulled high with the help of a 10KCl Resistor. The Gate terminal of the MOSFET is connected to Pin 7 of 555. The motor is connected between +12V Supply and Drain of MOSFET while the Source of MOSFET is connected to GND.

A PN Junction Diode is connected across the Motor terminals to prevent the back emf.

In this circuit, the DC motor is operated by a 555 i ntegrated circuit. The IC 555 in this circuit is being operated in astable mode, which produces a continuous HIGH and LOW pulses.

In this mode, the 555 IC can be used as a pulse width modulator with a few small adjustments to the circuit. The frequency of operation of the circuit is provided by the passive parameters of resistances and capacitors attached to it.

CHAPTER 4.1

HARDWARE DESCRIPTION

NE555 IC pin diagram :

This IC contains an SR flip flop as shown in the figure

Fig 2

Some important features of the 555 timer:

555 timer is used in almost everv electronic circuit todav For a 555 timer working as a flip flop or as a multi-vibrator, it has a particular set of configurations. Some of the major features of the 555 timer would be,

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
- Sinking or sourcing 2D0 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohenz.
- The output of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 5D parts per million (ppm) per degree Celsius change in temperature which is equivalent to D.005 %/ °C.
- The duty cycle of the timer is adjustable.
- Also, the maximum power dissipation per package is 6D0 mW and its trigger and reset inputs has logic compatibility.

Pin diagram and description

Pin	Name	**Purpose**
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 V'cc, CTRL being 2/3 V'cc by default if CTRL is left open). In other words, OUT is high as long as the trigger low. Output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.
3	OUT	This output is driven to approximately 1.7 V below +V'cc, or to GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides threshold.
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 dcc).
6	THR	The timing (OUT high) interval ends when the voltage at threshold is greater than that at CTRL (2/3 dcc if CTRL is open).
7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with out put.

8	dcc	Positive supply voltage, which is usually between 3 and 15 V depending is variable

The timer IC 555 was introduced around 1971 by the company Signetics under the name SE555 / NE555 and was called "The Time Machine IC". It offered circuit designers a relatively inexpensive, stable and easy-to-use integrated circuit for monostable and astable applications. Since this device was first marketed, many unique and innovative circuits have been developed and presented in various commercial, professional and leisure publications. Over the past decade, some manufacturers have stopped making these timers for reasons of competition or other reasons. However, other companies, such as NTE (a sub-division of Philips) have resumed their activities where some have left.

Although the CMOS version of this IC, such as the Motorola MC14S5, is primarily used, the standard type is still available, but many enhancements and variations have been made to the circuits. But all types are compatible with pin plugs. In this tutorial, the 555 timer is examined in detail, as are its uses, either alone or in combination with other semiconductor devices. This timer uses a labyrinth of transistors, diodes and resistors and, for this complex reason, a more simplified (but precise) block diagram is used to explain the internal organization of 555. The 555, in fig. 1 and FIG. 2 above, is available in two cases, either the round metal housing called "T", or the 8-pin DIP housing better known, "V". About 20 years ago, t type of canister was almost standard (SE / NE types). The 556 timer is a 5 dual version and comes in a 14-pin DIP package, the 558 is a quad version with four 5S5s also Tn a 14-pin DIP package.

Pin 1 (ground): The ground (or common) pin is the most negative power potential of the device, which is normally connected to the common (ground) circuit when operating from positive supply voltages.

Pin 2 (trigger): This pin is the input of the lower comparator and is used to adjust the latch, which makes the output high. This is the beginning of the time sequence in the monostable operation. The shot is obtained by taking the pin up and down with a voltage of 1/3 V + (or, in general, half of the voltage appearing on pin 5). The action of the activation input is level sensitive, allowing the use of slow change rate waveforms, as well as pulses, as activation sources. The trigger pulse must be shorter than the time interval determined by external R & C. If this pin remains low longer, the output will remain high until the trigger input increases again. A caution to observe with the trigger input signal is that it should not be less than 1/3 V + for a longer period than the synchronization cycle. If allowed, the timer wi ll be reactivated at the end of the first output pulse. Therefore, when the timer is used in monostable mode with input pulses longer than the desired output pulse width, the input trigger must be effectively shortened by differentiation. The minimum pulse width allowed for activation depends to some extent on the pulse level, but in general if greater than 1uS (micro-second), the activation will be reliable. A second precaution concerning the trigger input refers to the storage duration in the lower comparator. This part of the circuit may have normal stopping delays of several microseconds after activation; that is, the lock may still have an activation input during this peri od after the activation pulse. In practice, this means that the minimum monostable output pulse width must be of the order of 10 in order to avoid possible double activation due to this effect. The voltage range that can safely be applied to the trip pin is between V + and ground. A DC current, called the tripping current, must also flow from this terminal to the external circuit. This current is usually 500nA (nano-amp) and will set the upper limit of allowable resistance of pin 2 to earth. For an astable configuration operating at V + = 5 volts, this resistance is 3 megaohms; It can be higher for a higher level of V +.

Pin 3 (output)I output 555 is from a high current totem stage consisting of transistors Q20 to Q24. Transistors Q21 and Q22 provide a drive for source-type loads, and their Darlington connection provides a high output voltage of about 1.7 volts less than the V + power level used. Transistor Q24 offers the possibility of absorbing the current for low state loads called V + (as typical TTL inputs). The transistor Q24 has a low saturation voltage, which allows it to interact directly with a good noise margin when it performs the current reduction logic. However, the exact output saturation levels vary considerably with the sup ply voltage, for both high and low states. At a V + of 5 volts, for example, the low state Vce (sat) is typically 0.25 volts at 5 mA. However, when running at 15 volts, it can absorb 200 mA if a 2 volt output voltage level is allowed (the power dissipation must be taken into account in this case, of course). The high state level is typically 3.3 volts at V + = 5 volts; 13.3 volts at V + = 15 volts. The rise and fall times of the output waveform are quite fast, the typical switching times are 100nS. The state of the output pin will always reflect the opposite of the logic state of the latch, which can be seen by examining FIG. 3. Since the lock itself is not directly accessible, this relation can be better explained in terms of the activation activation lock conditions. To activate the output in the high state, the activation input is momentarily taken from a higher level to a lower level. [see "Pin 2 - Trigger”]. This causes locking and high output. The performance of the lower comparator is the only way to set the output high. The output can return to a low state by raising the threshold from a lower level to a higher level [see "Pin 6 - Threshold"], which resets the latch. The output can also be reduced by bringing the reset to alovv state near the ground [see "Pin 4 Reset"] The output voltage avaiIabIeonthispinisapproxmatelyequaItotheVccappIiedto pin8 minus1.7Vs.

Pin 4 (reset): This pin is also used to reset the latch and return the output to a low state. The threshold level of the reset voltage is 0.7 volts and a 0.1 mA dissipation current of this pin is required to restart the device. These levels a re relatively independent of the V + level of operation; Thus, the reset input is compatible with TTL for any supply voltage. The reset input is a primary function. that is, it will force the output to a low state regard less of the state of the other inputs. Therefore, it can be used to prematurely terminate an output pulse, to block oscillations from "on" to "off", etc. The delay time between the restart and the output is generally of the order of 0.5 uS and the minimum width of the reset pulse is 0.5 . However, none of these numbers are guaranteed and may vary from manufacturer to manufacturer. In summary, the reset pin is used to reset the latch that controls the state of output pin 3. The pin is activated when a voltage level between 0 and 0.4 volts is applied to the pin. The reset pin will force the output to a low level, regardless of the state in which the other inputs of the flip-flop are located. When not in use, it is recommended to connect the reset input to V + in order to avoid the possibility of false restart.

Pin 5 (control voltage): This pin allows direct access to the 2/3 V + voltage division point, the reference level of the upper comparator. It also allows indirect access to the lower comparator because there is a 2: 1 splitter (R8 R9) from this point to the lower comparator reference input, Q13. The use of this terminal is a user option, but it allows extreme flexibility by allowing the modification of the period, the restart of the comparator, etc. When timer SSS is used in a voltage controlled mode, its voltage operation varies from about 1 volt less than V + to 2 volts of mass (although this is not guaranteed). Voltages may safely be applied outside these limits, but must be limited within the V + and ground limits for reasons of reliability. By applying a voltage to this pin, it is possible to vary the duration of the device independently of the RC network. The control voltage can vary from 45 to 90% of the Vcc in monostable mode, which allows the output pulse width to be controlled independently of RC. When used in astable mode, the control voltage can vary from 1.7 V to full VDC. Variable voltage in astable mode will produce a modulated frequency (FM) output. If the control voltage pin is not used, it is recommended to ground it with a capacitor of about 0.01uF (10n F) for noise immunity because it is an input comparison. This fact is not evident in many 555 circuits since I have seen many circuits with "no-pin-5" connected to anything, but this is the proper procedure. The small ceramic lid can eliminate false activations.

Pin 6 (threshold): Pin 6 is an input of the upper comparator (the other is pin 5) and is used to reset the latch, resulting in low output. The reset through this terminal is made by taking the bottom terminal to a voltage of 2/3 V + (the normal voltage on pin S). The action of the threshold pin is level sensitive, which allows slow rate of change waveforms. The voltage range that can safely be applied to the threshold pin is between V + and ground. A direct current, called the current threshold, must also reach this terminal from the external circuit. This current is generally 0.1 pA and will define the upper limit of total resistance allowed from pin 6 to V +. For any synchronization setting that operates at V + = 5 volts, this resistance is 16 MCI. For operation at 15 volts, the maximum resistance value is 20 MCI.

Pin 7 (discharge): this pin is connected to the open collector of an NPN transistor (Q14), whose emitter is grounded, so that when the transistor is activated, pin 7 is actually short-circuited to the mass. Generally, the sync capacitor is connected between pin 7 and ground and is discharged when the transistor is turned on. The state of attack of this transistor has a synchronization identical to that of the output stage. It is "on" (low resistance to earth) when the output is low and "off" (high resistance to earth) when the output is high. In the monostable and astable time modes, this transistor switch is used to ground the appropriate nodes of the synchronization network. The saturation voltage is generally less than 100 mV (millivolts) for currents of 5 mA or less, and the leakage in the off state is approximately 20 nA (however, these parameters are not specified by all manufacturers) . The maximum collector current is internally limited by design, thus eliminating capacitor size restrictions due to the maximum discharge of the pulse current. In some applications, this open-collector output can be used as an auxiliary output terminal, with a current-dissipating capacity similar to that of the output (pin 3).

Pin 8 (V +): Pin V + (also called Vcc) is the positive power supply terminal of the timer CI 555. The operating voltage supply range of the SSS is between +4.S volts (minimum) and +16 volts (maximum). It is specified for operation between +5 volts and +15 volts. The device will operate essentially in the same way in this voltage range without changing the period. In fact, the most significant operating difference is the capacity of the output inverter, which increases for both the current and voltage ranges as the supply voltage increases. The sensitivity of the time interval to the variation of the supply voltage is low, typically 0.1% per volt. There are special and military devices operating at voltages up to 18 V.

Diode:

Diode, an electrical component that allows the flow of current in only one direction. In circuit diagrams, a diode is represented by a triangle with a line across one vertex. The most common type of diode uses a p n junction. In this type of diode, one material \ *n)* 'in which electrons are charge carriers a buts a second material *p)* in which holes (p laces depleted of electrons that act as positively charged particles) act as charge carriers. At their interface, a depletion region is formed across which ctrons diffuse to fill holes in the p-side. This stops the further flow of electrons. When this jun n is forward biased (that is, a positive voltage is applied to the *p*-side), elect s can easily move across the junction to fill the holes, and a current flows through the diode. When the junction is reverse biased (that is, a negative voltage is applied to the *p*-side), the depletion region widens and e lectrons cannot easily move across. The current remains very small until a certain voltage (the breakdown voltage) is reached and the current suddenly increases.

Fig 3

The Schottky diode, also known as Schottky barrier diode or hot-carrie iode, is a semiconductor diode formed by the junction of a semiconductor with a metal. It has a low forward voltage drop and a very fast switching action. The cat's-whisker tectors used in the early days of wireless and metal rectJfiers used in early power applications can be considered prTmitTve Schottky diodes.

When sufficient forward voltage is applied, a current flows in the forward direction. A silicon diode has a typical forward voltage of 600—700 mV, while the Schottky's forward voltage is 150—450 mV. This lower forward voltage requirement allows higher switching speeds and better system efficiency.

Fig 4

WATER PUMP MOTOR:

Micro DC 3-6V Micro Submersible Pump Mini water pump For Fountain Garden Mini water circulation System DIY project. This is a low cost, small size Sub mersi ble Pump Motor which can be operated from a 3 - 6V power supply. It can

current consumption of 220mA. Just connect tube pipe to the motor outlet, submerge it in water and power it. Make sure that the water level is always higher than the motor. Dry run may damage the motor due to heating and it will also produce noise.

Specifications:-

Operating Voltage : 3 - 6V

Operating Current : 130 ” 220mA

Flow Rate : 80 " 120 L/H

Maximum Lift : 40 " 110mm

Continuous Working Life : 500 hours

Driving Mode : DC, Magnetic Driving

Material : E ngi veering Plastic

Outlet Outside Diameter : 7.5 mm

Outlet Inside Diameter : 5 mm

Fig 5

POWER SUPPLY:

A power supp ly is a device that sup plies electric power to a electric load .The term is most common ly referred to electric power converts that converts one form of electrical energy to another ,though it may also refer to that convert another form of energy (mechanical chemical, solar) to e lectrical energy . The regulated power supply is that controls the output voltage or current to a specific value ;the controlled val ue is held nearly .

Fig 6

BREADBOARD:

A breadboard is a sol derless device for temporary prototype with electronics and test circuit designs. Most electronic components in electronic circuits can be interconnected by inserting their leads or terminals into the holes and then making connections through wires where ap proprJate.

Fig 7

RESULT

Under Progress

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

- One of the best things about this circuit is that you can make it work as an astable multivibrator with little hardware and little cost, which can save both the cost involved in making it as well as the space on the printed circuit board (PCB).

- If you want a sophisticated pulse width modulator which works more accurately and which can have more adjusting capabilities, then it is better to use a microcontroller based pulse width modulator than the one which we are using now.
- However, the circuit or the application for which we are using a pulse width modulator is not so sensitive and hence does not demand so much of accuracy. In such a case, the circuit which we are using with a bare IC 555 is better as it saves our monetary as well as space resources in building the circuit.
- The duty cycle of the circuit can be changed by changing the value of the potentiometer. If we increase the duty cycle, the speed of the motor increases and if we decrease the duty cycle, the speed of the motor decreases.

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