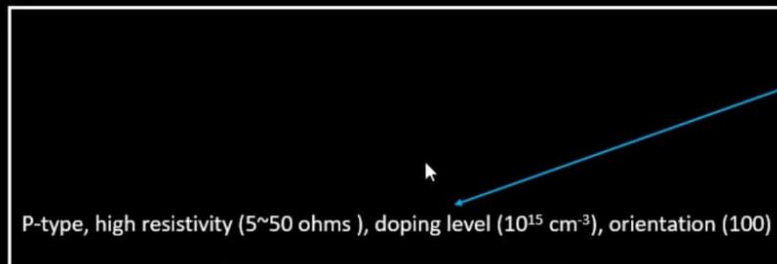


## CHIP FABRICATION PROCESS

### 16-mask CMOS process

#### 1) Selecting a substrate



P-type, high resistivity (5~50 ohms), doping level ( $10^{15} \text{ cm}^{-3}$ ), orientation (100)

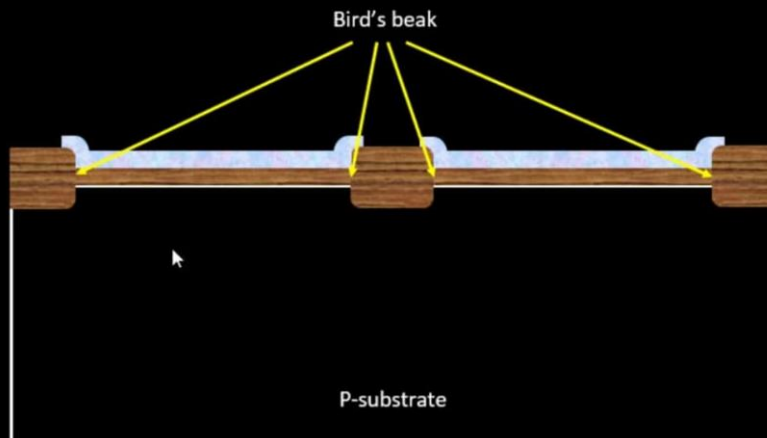
Substrate doping should be less than 'well' doping. Coming in further sections

### 16-mask CMOS process

#### 2) Creating active region for transistors

Mask1

Field oxide is grown  
This process is called  
"LOCOS"  
"Local Oxidation of Silicon"

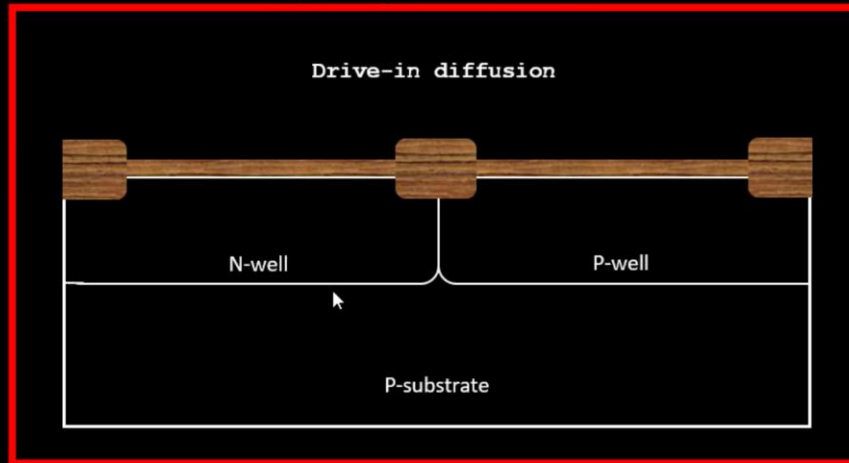


~1 $\mu\text{m}$  photoresist  
~80nm of  $\text{Si}_3\text{N}_4$   
~40nm of  $\text{SiO}_2$

## 16-mask CMOS process

### 3) N-Well and P-Well formation

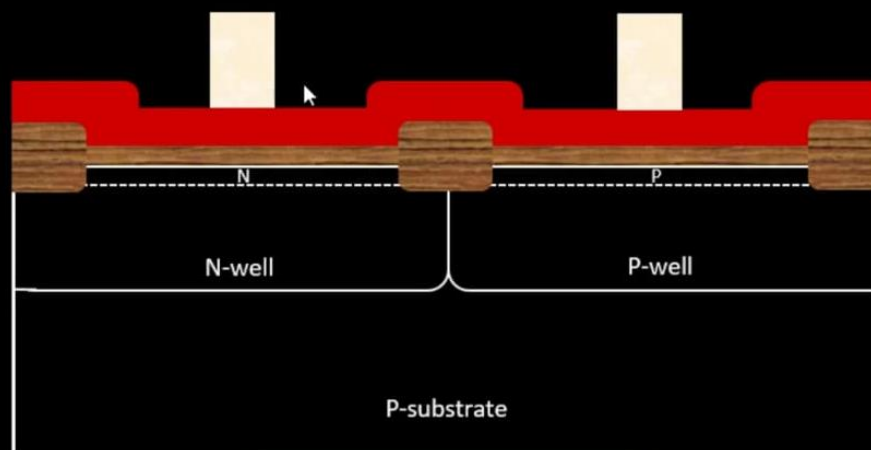
High temperature furnace



udemy

## 16-mask CMOS process

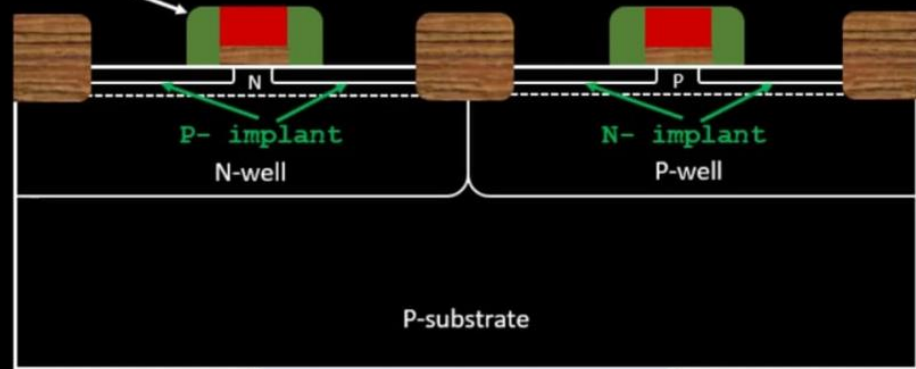
### 4) Formation of 'gate'



## 16-mask CMOS process

### 5) Lightly doped drain (LDD) formation

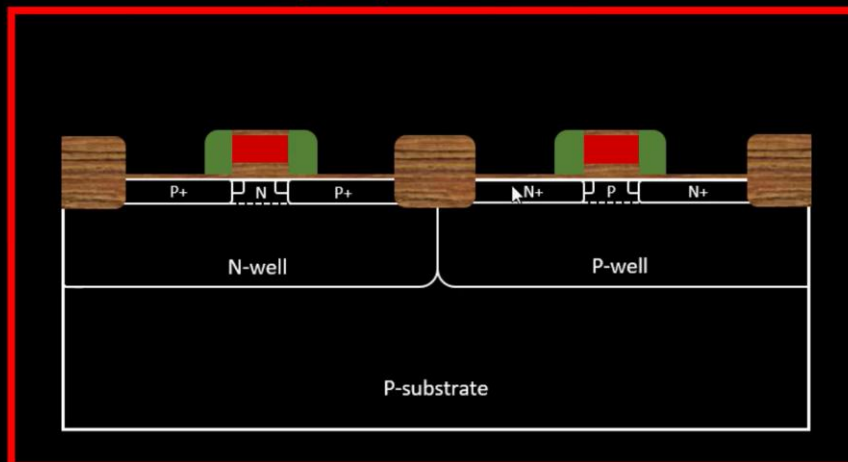
Side-wall spacers



## 16-mask CMOS process

### 6) Source and drain formation

High temperature furnace



## 7) Steps to form contacts and interconnects(local)

