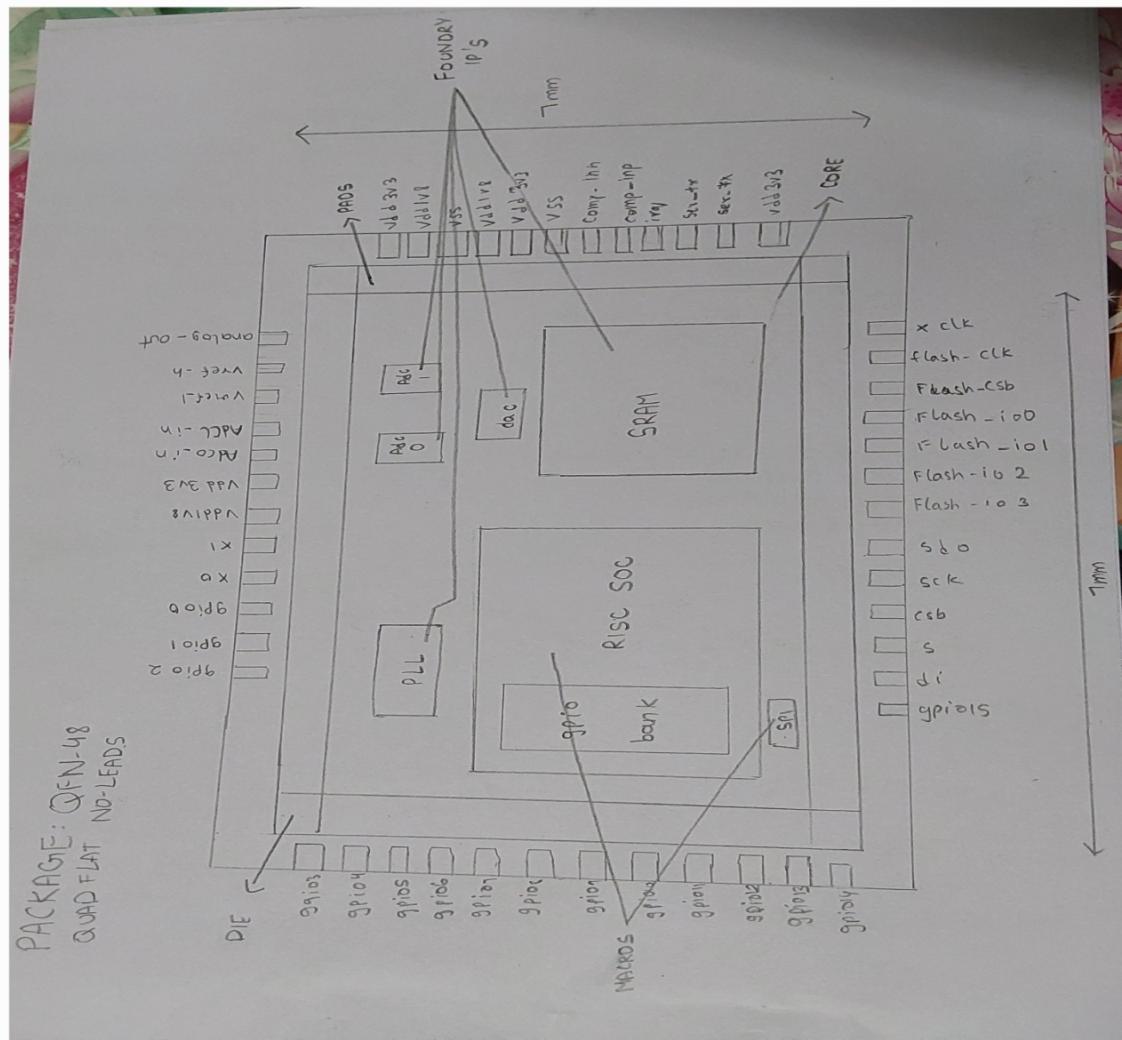


Chip :-

Pads- means through which the message is sent inside and vice-versa.

IP. The full form of IP is Intellectual property.

Macros- Macros basically means a pure digital logic.



RISC-V Architecture:-

Implementation

Layout

Application :-

System Software

• Operating System (OS)

C, C++, Java

• Compiler

Exe file

• Assembler

Binary number (Machine Language)

Hardware

instr 1
instr 2

Abstra-
ct
interface.

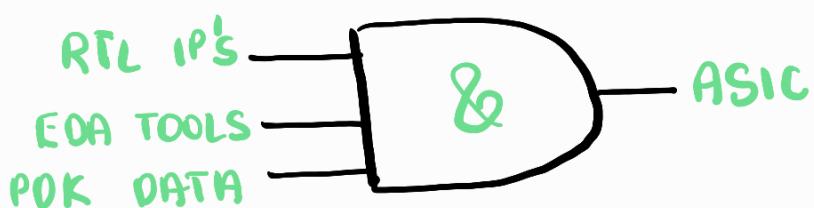
instruction
set archite-
cture.

Architecture of
computer.

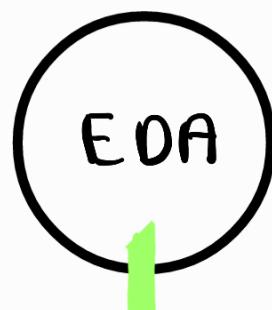
Other Works of System Software :-

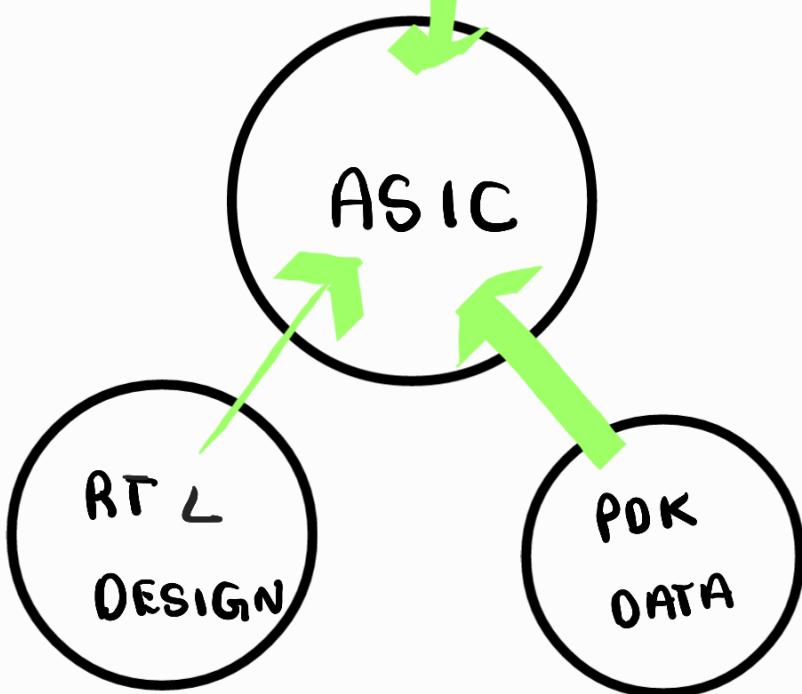
- Handle I/O operation
- Allocate memory
- Low level system function

DIGITAL ASIC DESIGN :-



OPEN SOURCE DIGITAL ASIC DESIGN





What is PDK :-

- Process Design
- Collection of files used to model a fabrication process for the EDA tools used to design an IC.
- Process design C,L,V,S ,PEX.
- Device Models
- Digital standard cell libraries.
- I/O libraries.

Simplified RTL-to-GDSI, Flow:-

- Synthesis
- Floor / power planning
- Placement
- clock tree synthesis
- Routing
- Sign off

Synthesis:-

- * Converts RTL to a circuit out of components

- * from the standard cell library SCL.
- * Standard cells have regular layout.
- * Each has different views / models.
- * Electrical, HDL, SPICE
- * Layout (abstract and detailed)

Floor / power planning :-

- * Chip floor planning : Partition the chip lie between different system building blocks and place the I/O pads.
- * Macro floor planning : Dimensions , pin location , row definition
- * Power planning

Placement :-

- * Place the cells on the floor plans rows, aligned with the sites
- * Usually done in 2 steps : Global and detailed

Clock tree synthesis :-

- * Create the clock distribution network .
 - To deliver the clock to all sequential elements
 - Minimum skew (zero is hard to achieve)
 - And widoor shape
 - Usually a tree (H,X,.....)

Routing :-

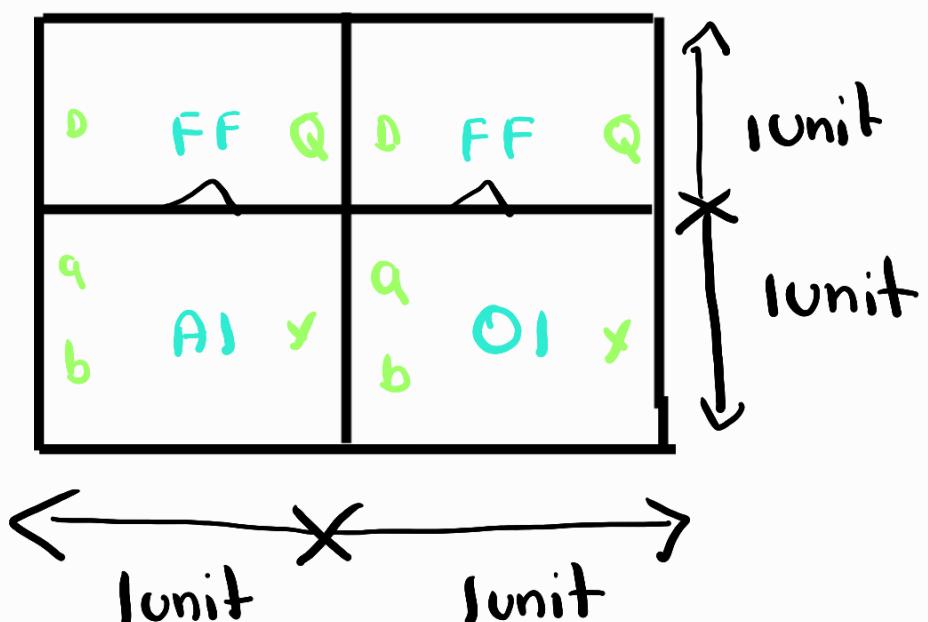
- * Implement the interconnect using the available metal layers .
- * Metal tracks from grid .
- * Routing grid is huge .

- * Routing grid is huge
- * Divide and conquer
- Global routing - Generates routing guides
- Detailed routing - Uses the routing guides to implement the actual wiring.

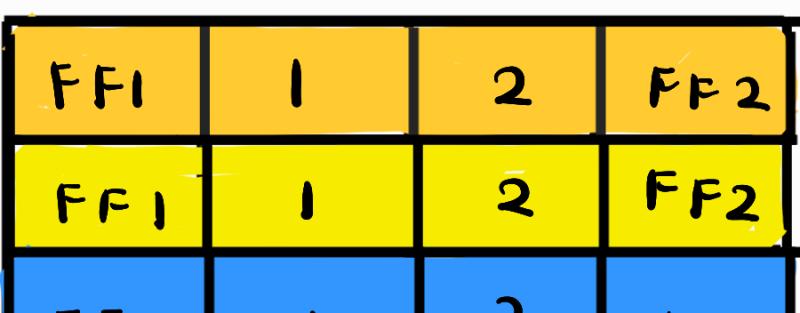
Sign off :-

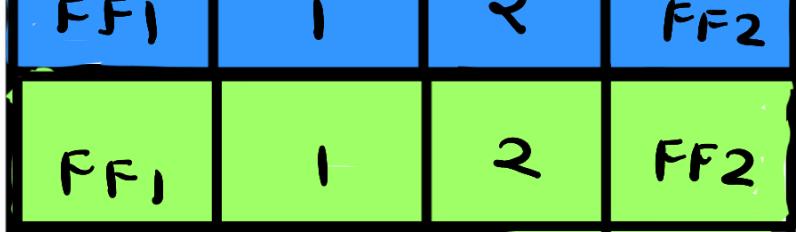
- * Physical Verifications
- * Design Rules checking (DRC)
- * Layout vs schematic (LVS)
- * Timing Verification
 - Static Timing Analysis (STA)

AREA OF A NETLIST :-



① Bind netlist with Physical cells :-





Block A

Block b

Block C

- All the cells are kept in a shelf and it is called a library.

LIBRARY CONTENTS:-

- AND GATE
- OR GATE
- BUFFER
- INVERTER
- DFF
- LATCH
- ICG
-

* The Standard cells :-

- Buffer
- Gate
- FF2, FF1

* the standard cells are placed in library.

* Cell design flow are divided into inputs, design steps and outputs.

* Space model parameters
Eg: V_{TO}, Y, K_{N1}, T_{OX}

