A Low Cost High Performance VLSI Architecture for Image Scaling in Multimedia Application

Navin Kumar S (RA2211004010543), Vishwa K (RA2211004010554), Abishek C (RA221100401056)
GUIDE: Dr. Selvakumar J (Professor, Department of Electronic & Communication Engineering)
Department of Electronics and Communication Engineering, SRM Institute of Science and Technology, Kattankulathur

INTRODUCTION/ABSTRACT

Real-time image scaling is vital in multimedia and vision applications. This project proposes a novel VLSI architecture for scaling images with high performance and low area. The design supports interpolation methods such as nearest-neighbor, bilinear, and bicubic. Implemented on an FPGA using Verilog and verified using simulation and hardware testing, the architecture achieves <15% resource utilization and processes each pixel in <13µs, suitable for real-time deployment.

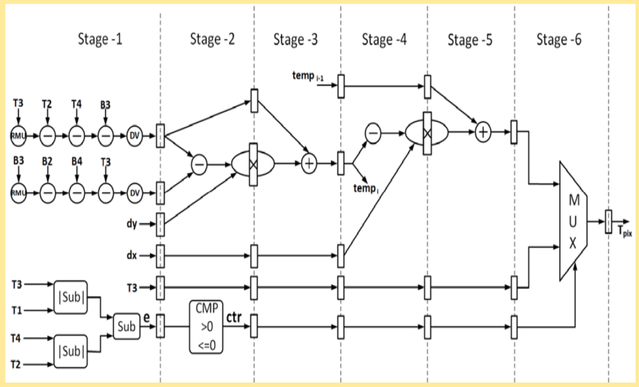
PROBLEM STATEMENT

In multimedia and computer vision applications, real-time image scaling is essential for resizing images to fit various display resolutions and processing requirements. However, conventional image scaling techniques, when implemented on general-purpose processors or inefficient hardware architectures, often result in high latency, excessive power consumption, and increased silicon area. There is a pressing need for a low-cost, high-performance VLSI architecture that can perform efficiently that can perform efficient image scaling using standard interpolation techniques using standard interpolation techniques while meeting the strict constraints of speed, power, and resource utilization in embedded systems.

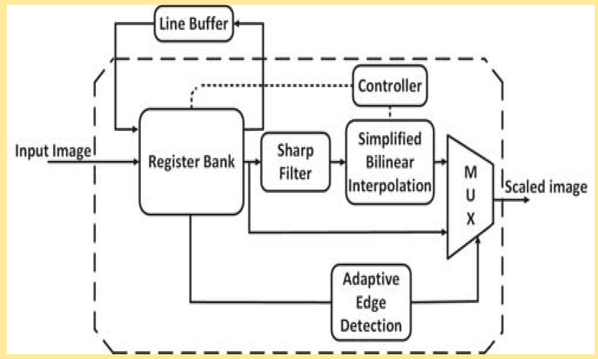
OBJECTIVE

- Design a low-cost and high-speed VLSI architecture for image scaling.
- Implement nearest-neighbor, bilinear, and bicubic interpolation.
- Achieve optimized performance on FPGA(PYNQ-Z2).
- Validate functionality via simulation and hardware testing

METHODOLOGY



DESIGN



RESULTS & INFERENCE

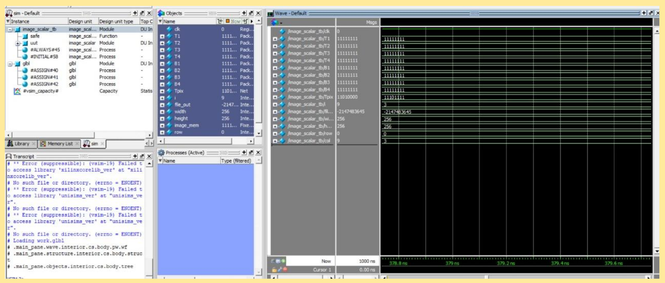
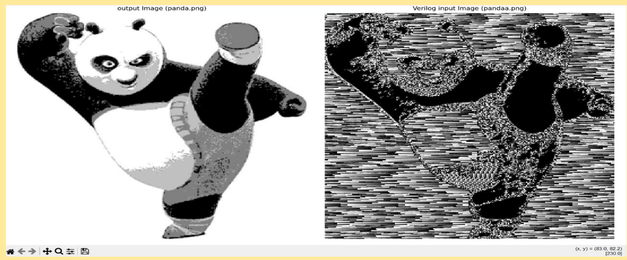
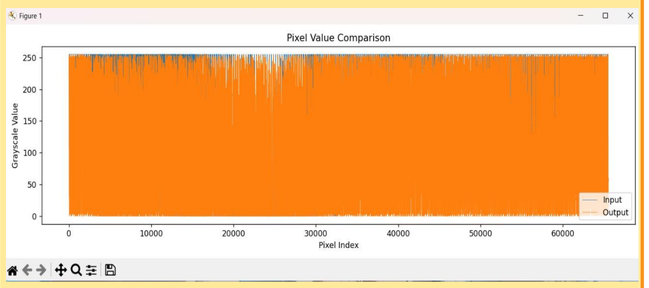


Image scaling is a fundamental operation in multimedia systems and digital image processing, where an image is resized to a different resolution while attempting to preserve visual quality. Scaling is essential in applications such as video conferencing, real-time video playback, image preview, and hardware-based multimedia rendering.





REALISTIC CONSTRAINTS

- Limited logic blocks, DSPs, and memory on the FPGA restricted complex algorithm implementation
- Real-time processing requires low-latency operation for each frame or image.
- Higher interpolation accuracy increases resource usage, creating trade-offs between quality and efficiency.
- Power consumption must be minimized for use in portable or embedded systems.
- The design should adapt to different image sizes and scaling ratios without performance loss.

CONCLUSION

The proposed low-cost, high-performance VLSI architecture for image scaling effectively addresses the challenges of real-time processing in multimedia applications. By leveraging efficient interpolation techniques like bilinear interpolation and optimizing the hardware design for minimal power consumption and area utilization, the system provides a practical solution for embedded devices with limited resources. The use of Python for algorithm validation ensured that the scaling logic was accurately modeled before hardware implementation. Testing on FPGA platforms demonstrated the feasibility and performance of the design, proving it to be both efficient and scalable for various image resolutions. This work contributes to the advancement of multimedia processing in resource-constrained environments, offering a balance between computational efficiency, image quality, and costeffectiveness, making it well-suited for modern portable devices.

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