Software Requirements Specification (SRS)

For projects

1526

Version: 1.0

RESTRICTION OF USE, DUPLICATION, OR DISCLOSURE OF PROPRIETARY INFORMATION

This document contains proprietary information that is the sole property of DSIT. The document is submitted to the recipient for his use only. By receiving this document, the recipient undertakes not to duplicate the document or to disclose in part, or in whole any of the information contained herein to any third party without receiving beforehand written permission from DSIT.

B.A. Microwaves LTD.

10 Marconi St. P.O.B. 25482, Haifa 3125401

Tel. +972-4-8202715 Fax. +972-4-8202716

bamw@bamicrowaves.co.il www.bamicrowaves.co.il

Table of Contents

1 Changes

Name	Change	Version	Date
Roee Zinoue	First Edition.	1.0	07/01/18

2 *Project 1526*:

2.1 Introduction:

This document describes the SW operation of the SFC unit.

The SFC main goal is to output two signals frequencies at frequency of:

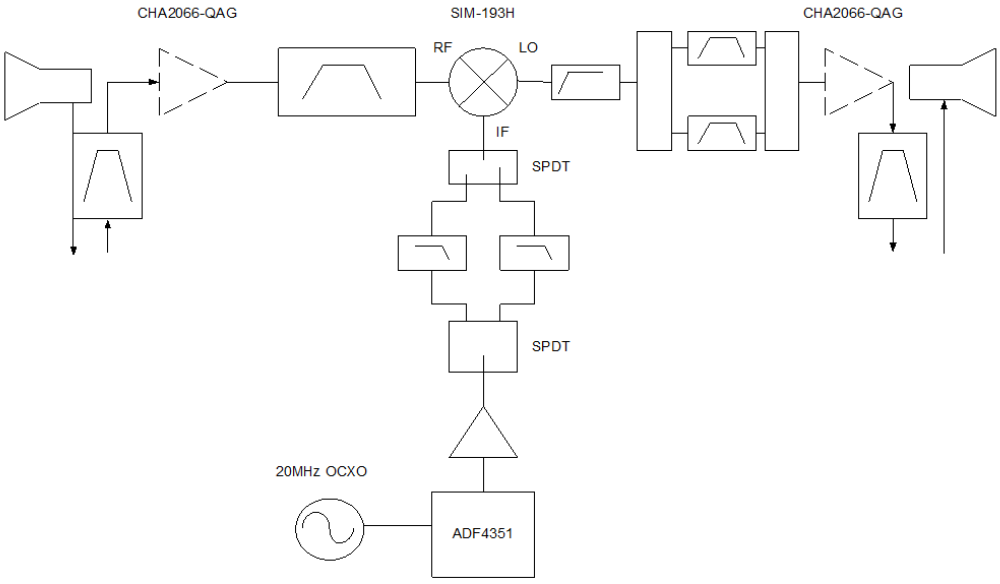
a. 1.95 GHz.
b. 2.8 GHz.

This achieved by written digital configuration words that exit from on board MCU (PIC16LF1823) and already stored by the MCU to synthesizer (ADF-4351) unit.

The system user will able to choose the desire output frequency signal by external switch that connected to the MCU.

The MCU will also have LEDs indication of the synthesizer operation (that indicate about the frequency that selected and if the frequency is latched). The opposite results of the above can also be viewed by 2 GPIO that exit from the MCU.

2.2 System block diagram



2.3 Objective

Main object of the MCU is two configure synthesizer ADF-4351 to output 2 frequencies RF signals at frequencies: a. 1.95 GHz b. 2.8 GHz according to user selection.

Beside that the system will able to:

a. Operate immediate after system power on or system reset. (In case of system boot failure the LEDs will blinks which in a way that it indicate an issue to the system user).
b. Will indicate to the system user the state of synthesizer mode (if the output RF signal is latched or there is an issue in the synthesizer unit).
c. Will output the synthesizer values by 2 GPIO pins that are connected to the MCU.

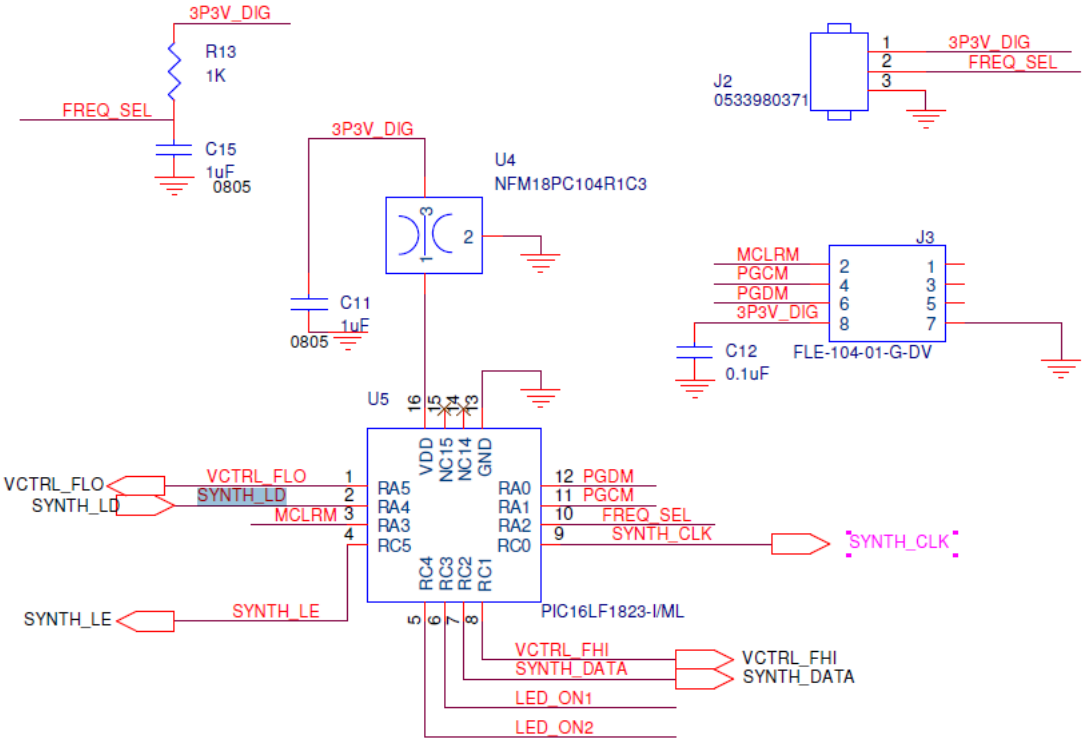
2.4 Synthesizer registers values

Note: Please check Appendix A on this document describe to learn about the way of frequency in the sensitizer unit.

Register name	Register possible data range	Register data value		Register bits size
		$f_{out} = 1.95\ GHz$	$f_{out} = 2.8\ GHz$	
FRAQ	$0 \div 0\text{xFFF}$	TBD	TBD	12
Prescaler (PR1)	$0 \div 1$ 0: 4/5 prescaler 1: 8/9 prescaler	TBD	TBD	1
INT	$\text{PR1} = 0 \rightarrow 0\text{x17} \div 0\text{xFFFF}$ $\text{PR1} = 1 \rightarrow 0\text{x4B} \div 0\text{xFFFF}$	TBD	TBD	16
MOD	$0 \div 0\text{xFFF}$	TBD	TBD	12
D (Reference Doubler) – multiple by 2 REFIN value	$0 \div 1$ 0: disable. 1: Enable.	TBD	TBD	1
T (reference divide-by-2 bit)	$0 \div 1$	TBD	TBD	1
R (reference division factor)	$1 \div 1023$	TBD	TBD	10

3 Hardware

3.1 MCU Schematic



3.2 Microcontroller

Recommended PIC	PIC16LF1823 – 8 bit core
Operating voltage	3.3V
Inputs (TTL / converter)	TBD
Outputs (TTL / converter)	TBD
POR	Available
Internal clock	8MHz and up to 32MHz
Pin count	14

- Flash Memory
  - The PIC microcontroller has 3.5KB (2K x 14) of internal flash memory. This memory will be used for store the internal synthesizer registers data.
- RAM Memory
  - The PIC microcontroller has 128 bytes of internal RAM, the system will use this memory for its software stack & heap.
- Peripherals support:
  - Connectivity: 1-UART, 1-SPI, 1-I2C1-MSSP(SPI/I2C).
  - ADC: 8 ch, 10-bit.

3.3 GPIO and Analog Pin Assignments

Name in document	PIN Name	Net Name	Type
MCU power and programing pins			
3.3 VDC Enable	VDD	VDD	Input Analog
Digital ground	GND	GND	Input Analog
Program data Enable	RA0	PGDM	Bi-directional Discrete
Program clock Enable	RA1	PGCM	Input Discrete
System reset	RA3	MCLRM	Input Discrete
synthesizer			
SYNTH_CLK	RC0	SYNTH_CLK	Output Discrete
SYNTH_LE	RC5	SYNTH_LE	Output Discrete
SYNTH_LD	RA4	SYNTH_LD	Input Discrete
SYNTH_DATA	RC2	SYNTH_DATA	Output Discrete
System indication			
VCTRL_FHI	RC1	VCTRL_FHI	Output Discrete
VCTRL_FLO	RA5	VCTRL_FLO	Output Discrete
LED_ON1	RC3	LED_ON1	Output Discrete
LED_ON2	RC4	LED_ON2	Output Discrete
User selection			
FREQ_SEL	RA2	FREQ_SEL	Input Discrete

4 Appendix A – How to set the registers values of sensitizer ADF-4351

** Please refer to unit datasheet for full details.

The Sensitizer ADF-4351 is software programmable unit which mean that each of the unit registers data is given and controlled by 4 registers that each one have control buffer of 32-bit. This registers configuration values will output from the on board MCU unit.

The synthesizer is also calibrated by the VCO (voltage controlled oscillator) and the frequency that comes after the VCO circuit can be calculated using the formula:

$$RF_{out} = f_{PDF} * (INT + \frac{FRAC}{MOD})$$

When:
RFOUT: is the output frequency of the voltage controlled oscillator (VCO).
INT: is the preset divide ratio of the binary 16-bit counter.
FRAC: is the numerator of the fractional division (0 to MOD − 1).
MOD: is the preset fractional modulus (2 to 4095).
fPEF: is a frequency parameter that calculated from inputs parameters:

$$f_{PDF} = REF_{in} * \left[\frac{1 + D}{R * (1 + T)}\right]$$

When:
REFIN: is the reference input frequency.
D: is the REFIN doubler bit (0 or 1).
R: is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).
T: is the REFIN divide-by-2 bit (0 or 1).

Example of frequency calculation:

As an example, a UMTS system requires a 2112.6 MHz RF frequency output (RFOUT); a 10 MHz reference frequency input (REFIN) is available and a 200 kHz channel resolution (fRESOUT) is required on the RF output.
Note that the ADF4351 VCO operates in the frequency range of 2.2 GHz to 4.4 GHz. Therefore, the RF divider of 2 should be used (VCO frequency = 4225.2 MHz, RFOUT = VCO frequency/ RF divider = 4225.2 MHz/2 = 2112.6 MHz).
It is also important where the loop is closed. In this example, the loop is closed before the output divider (see Figure 30). fPFD PFD VCO N DIVIDER ÷2 RFOUT 09800-027 Figure 30.
Loop Closed before output Divider Channel resolution (fRESOUT) of 200 kHz is required at the output of the RF divider.
Therefore, the channel resolution at the output of the VCO (fRES) needs to be

2 × fRESOUT,

that is, 400 kHz. MOD = REFIN/fRES MOD = 10 MHz/400 kHz = 25 From Equation 4, fPFD = [10 MHz × (1 + 0)/1] = 10 MHz (5) 2112.6 MHz = 10 MHz × [(INT + (FRAC/25))/2] (6) where: INT = 422. FRAC = 13.