

Software Requirements Specification (SRS)

For projects

1533 (CORAL VER2)

Version: 1.0

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1 Changes

Name	Change	Version	Date
Roe Zinoue	First Edition.	1.0	18/01/18

2 Project 1533:

2.1 Introduction:

This document describes the SW operation of the CORAL VER2 unit.

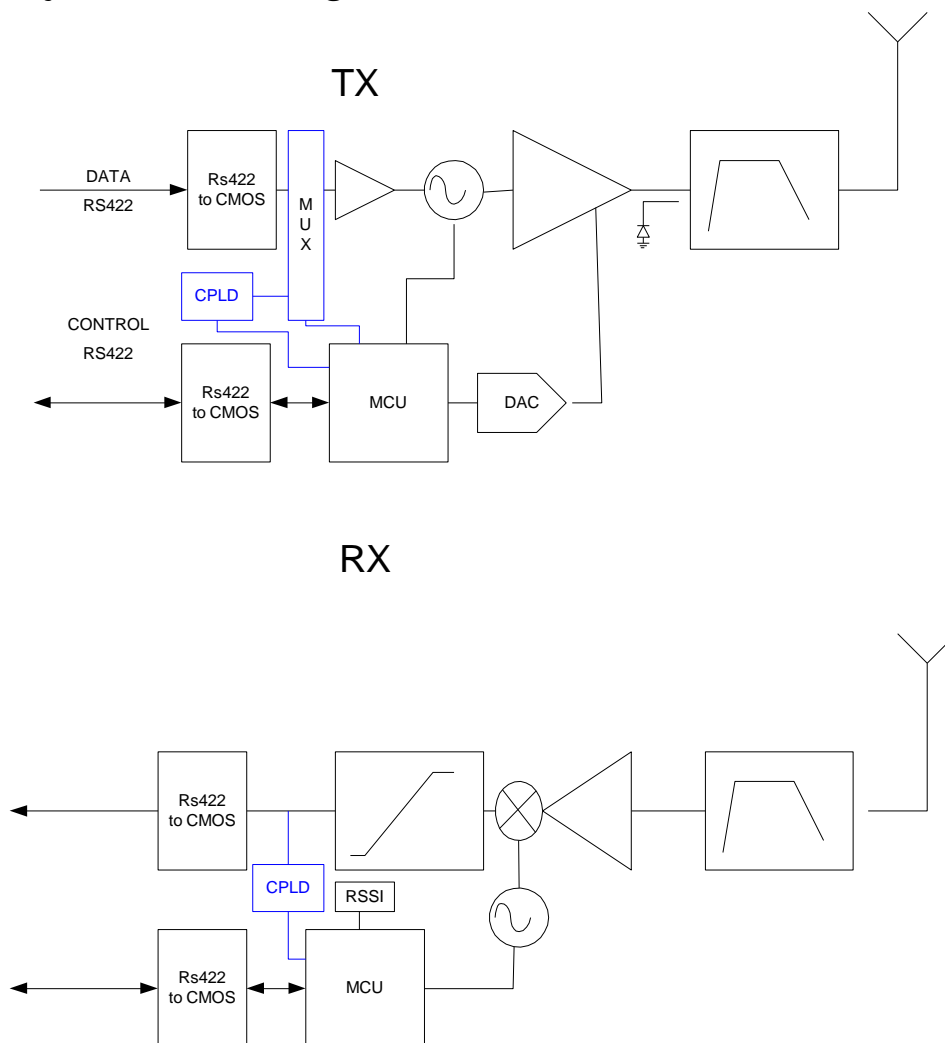
The system will consist two RF channels:

Transmit channel: will output RF signal with unique pattern that generated by the on board CPLD unit.

Receive channel: Will receive RF signal, if the signal match by his pattern to what expected the CPLD unit will indicate it to the on board MCU (which in final blink a connected LED to indicate about it).

Via serial connection we will able to control state of the transmitting / receiving and transmitting pattern. The system also have connect to MCU LEDs to indicate about the state of the system.

2.2 System block diagram



2.3 Objective

Main object of the MCU is collection data and indicate the user system about the RF signals states.

Goals of the Tx channel:

- a. To configure synthesizer unit (ADF4113) to output RF signal in parameters of:
 - Frequency of output signal: the Tx RF signal work at two ranges:
 - Low frequency: at range of: 5.75 – 5.85 GHz.
 - High frequency: at range of: 5.15 – 5.25 GHz.
 - Both ranges have step size of: 1 MHz.
 - Frequency of PLL signal: the PLL will receive signals at range of:
 - Low frequency: 2.575 – 2.625 GHz.
 - High frequency: 2.8625 - 2.9125 GHz.
 - Both are divided by factor of 2.
 - Both ranges have step size of: 0.5 MHz.
 - Advance power.
 - If the signal latched by the receiving unit.
 - Return power.
- b. Transfer Tx channel to stand-by mode (at this mode no transmission will occur).
- c. Turn on and off the power sensor.

Goals of the Rx channel:

- a. Transfer Rx channel to stand-by mode (at this mode the system will not listen to any income RF signals).
- b. Change working frequency mode of the frequency RF signal.
- c. Turn on and off the RSSI sensor.

The above operation modes set by serial communication channel (using user inputs commands that set by terminal application).

The on board MCU unit also will collect samples data from on board ADC unit, write them to internal flash and will output them to user via serial channel at user request.

2.4 Errors indications and system failures treatment

The system have two connected LEDs that indicate about the following system states:

- a. Green led:

This led indicate that certain system operation is set correctly. It indicate about:

- a. If system is initialize ok and ready to operate – the led will be stable for 3 seconds.
- b. If frequency is latched on the on board synthesizer – the led will blink 3 times (the MCU at this state will stop sending the configuration word to the on board synthesizer).

b. Red led:

This LED indicate that certain system have failure on one of the requested operation. It indicate about:

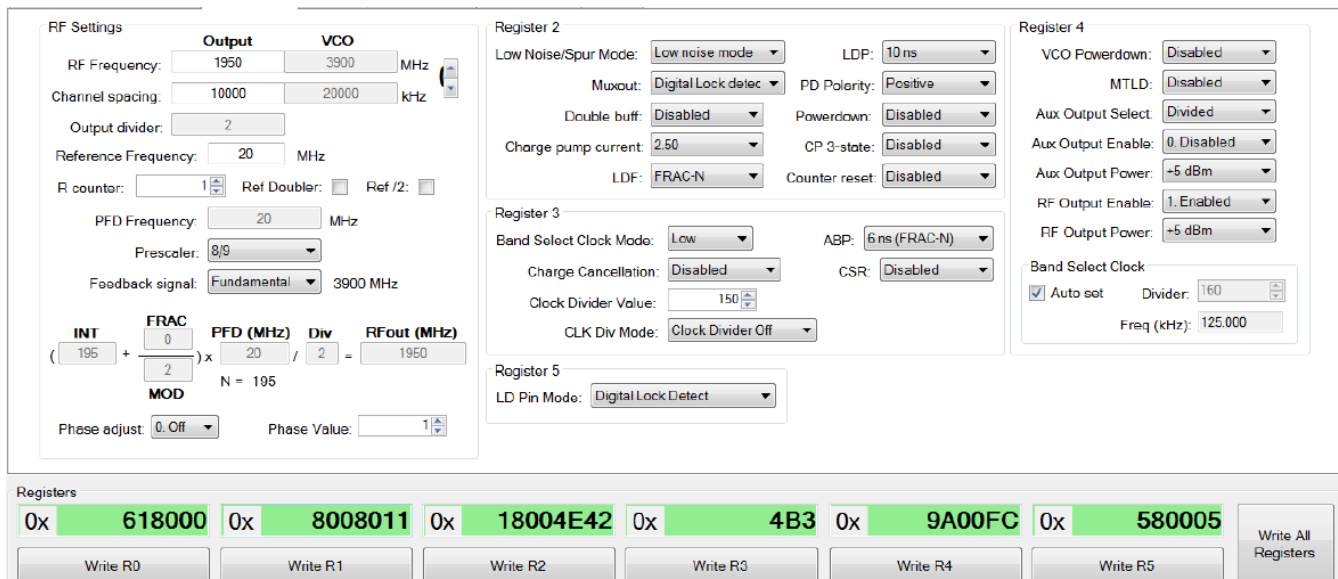
- If system is not success in initialize state– the led will be stable till system reset.
- If the on board MCU don't success to latch the selected frequency, the MCU will try to configure and send the digital words more 2 times. If after 3 times the frequency still not latched the red led will blink 5 times.

2.5 Synthesizer registers values

Note: Please check [Appendix A](#) on this document describe to learn about the way of frequency in the sensitizer unit.

The following registers configurations will be set on the on board synthesizer:

a. Frequency: 1.95 GHz:



RF Settings

Output VCO
 RF Frequency: 1950 3900 MHz
 Channel spacing: 10000 20000 kHz
 Output divider: 2
 Reference Frequency: 20 MHz
 R counter: 1 Ref Doubler: ☐ Ref /2: ☐
 PFD Frequency: 20 MHz
 Prescaler: 8/9
 Feedback signal: Fundamental 3900 MHz
 INT 195 + FRAC 0 PFD (MHz) 20 Div 2 RFout (MHz) 1950
 MOD N = 195
 Phase adjust: 0. Off Phase Value: 1

Register 2

Low Noise/Spur Mode: Low noise mode LDP: 10 ns
 Muxout: Digital Lock detect PD Polarity: Positive
 Double buff: Disabled Powerdown: Disabled
 Charge pump current: 2.50 CP 3-state: Disabled
 LDF: FRAC-N Counter reset: Disabled

Register 3

Band Select Clock Mode: Low ABP: 6 ns (FRAC-N)
 Charge Cancellation: Disabled CSR: Disabled
 Clock Divider Value: 150
 CLK Div Mode: Clock Divider Off

Register 4

VCO Powerdown: Disabled
 MTLD: Disabled
 Aux Output Select: Divided
 Aux Output Enable: 0 Disabled
 Aux Output Power: -5 dBm
 RF Output Enable: 1 Enabled
 RF Output Power: +5 dBm
 Band Select Clock
☒ Auto set Divider: 160
 Freq (kHz): 125.000

Register 5

LD Pin Mode: Digital Lock Detect

Registers

0x 618000	0x 8008011	0x 18004E42	0x 4B3	0x 9A00FC	0x 580005
Write R0	Write R1	Write R2	Write R3	Write R4	Write R5

Write All Registers

b. Frequency: 2.8 GHz:

RF Settings

Output

VCO

RF Frequency: 2800 2800 MHz

Channel spacing: 20000 20000 kHz

Output divider: 1

Reference Frequency: 20 MHz

R counter: 1 Ref Doubler: Ref /2:

PFD Frequency: 20 MHz

Prescaler: 6/9

Feedback signal: Fundamental 2800 MHz

INT

FRAC

140

0

+

2

MOD

N = 140

PFD (MHz) Div RFout (MHz)

20 1 = 2800

Phase adjust: 0 Off Phase Value: 1

Register 2

Low Noise/Spur Mode: Low noise mode LDP: 10 ns

Muxout: Digital Lock detec PD Polarity: Positive

Double buff: Disabled Powerdown: Disabled

Charge pump current: 2.50 CP 3-state: Disabled

LDF: FRAC-N Counter reset: Disabled

Register 3

Band Select Clock Mode: Low ABP: 6 ns (FRAC-N)

Charge Cancellation: Disabled CSR: Disabled

Clock Divider Value: 150

CLK Div Mode: Clock Divider Off

Register 4

VCO Powerdown: Disabled

MTLD: Disabled

Aux Output Select: Divided

Aux Output Enable: 0 Disabled

Aux Output Power: +5 dBm

RF Output Enable: 1 Enabled

RF Output Power: +5 dBm

Band Select Clock

☒ Auto set Divider: 160

Freq (kHz): 125,000

Register 5

LD Pin Mode: Digital Lock Detect

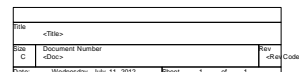
Registers

0x 460000	0x 8008011	0x 18004E42	0x 4B3	0x 8A00FC	0x 580005
Write R0	Write R1	Write R2	Write R3	Write R4	Write R5

Write All Registers

The configuration above taken from Analog devices ADF435x simulator.

3.1 MCU Schematic



3.2 Microcontroller

Recommended PIC	PIC16LF1823 – 8 bit core
Operating voltage	3.3V
Inputs (TTL / converter)	TBD
Outputs (TTL / converter)	TBD
POR	Available
Internal clock	8MHz and up to 32MHz
Pin count	14

- Flash Memory
 - The PIC microcontroller has 3.5KB (2K x 14) of internal flash memory. This memory will be used for store the internal synthesizer registers data.
- RAM Memory
 - The PIC microcontroller has 128 bytes of internal RAM, the system will use this memory for its software stack & heap.
- Peripherals support:
 - Connectivity: 1-UART, 1-SPI, 1-I2C1-MSSP(SPI/I2C).
 - ADC: 8 ch, 10-bit.

3.3 GPIO and Analog Pin Assignments

Name in document	PIN Name	Net Name	Type
MCU power and programing pins			
3.3 VDC Enable	VDD	VDD	Input Analog
Digital ground	GND	GND	Input Analog
Program data Enable	RA0	PGDM	Bi-directional Discrete
Program clock Enable	RA1	PGCM	Input Discrete
System reset	RA3	MCLRM	Input Discrete
synthesizer			
SYNTH_CLK	RC0	SYNTH_CLK	Output Discrete
SYNTH_LE	RC5	SYNTH_LE	Output Discrete
SYNTH_LD	RA4	SYNTH_LD	Input Discrete
SYNTH_DATA	RC2	SYNTH_DATA	Output Discrete
System indication			
VCTRL_FHI	RC1	VCTRL_FHI	Output Discrete
VCTRL_FLO	RA5	VCTRL_FLO	Output Discrete
LED_ON1	RC3	LED_ON1	Output Discrete
LED_ON2	RC4	LED_ON2	Output Discrete
User selection			
FREQ_SEL	RA2	FREQ_SEL	Input Discrete



4 Appendix A – How to set the registers values of sensitizer ADF-4351

** Please refer to unit datasheet for full details.

The Sensitizer ADF-4351 is software programmable unit which mean that each of the unit registers data is given and controlled by 4 registers that each one have control buffer of 32-bit. This registers configuration values will output from the on board MCU unit.

The synthesizer is also calibrated by the VCO (voltage controlled oscillator) and the frequency that comes after the VCO circuit can be calculated using the formula:

$$RF_{out} = f_{PDF} * (INT + \frac{FRAC}{MOD})$$

When:

RFOUT: is the output frequency of the voltage controlled oscillator (VCO).

INT: is the preset divide ratio of the binary 16-bit counter.

FRAC: is the numerator of the fractional division (0 to MOD – 1).

MOD: is the preset fractional modulus (2 to 4095).

fPEF: is a frequency parameter that calculated from inputs parameters:

$$f_{PDF} = REF_{in} * \left[\frac{1 + D}{R * (1 + T)} \right]$$

When:

REFIN: is the reference input frequency.

D: is the REFIN doubler bit (0 or 1).

R: is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

T: is the REFIN divide-by-2 bit (0 or 1).

Example of frequency calculation:

As an example, a UMTS system requires a 2112.6 MHz RF frequency output (RFOUT); a 10 MHz reference frequency input (REFIN) is available and a 200 kHz channel resolution (fRESOUT) is required on the RF output.

Note that the ADF4351 VCO operates in the frequency range of 2.2 GHz to 4.4 GHz. Therefore, the RF divider of 2 should be used (VCO frequency = 4225.2 MHz, RFOUT = VCO frequency/ RF divider = 4225.2 MHz/2 = 2112.6 MHz).

It is also important where the loop is closed. In this example, the loop is closed before the output divider (see Figure 30). fPFD PFD VCO N DIVIDER ÷2 RFOUT 09800-027 Figure 30.

Loop Closed before output Divider Channel resolution (fRESOUT) of 200 kHz is required at the output of the RF divider.

Therefore, the channel resolution at the output of the VCO (fRES) needs to be

$$2 \times fRESOUT,$$

that is, 400 kHz. MOD = REFIN/fRES MOD = 10 MHz/400 kHz = 25 From Equation 4, fPFD = [10 MHz × (1 + 0)/1] = 10 MHz (5) 2112.6 MHz = 10 MHz × [(INT + (FRAC/25))/2] (6) where: INT = 422. FRAC = 13.