Software Requirements Specification (SRS)

For projects

1533 (CORAL VER2)

Version: 1.0

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1 Changes

Name	Change	Version	Date
Roee Zinoue	First Edition.	1.0	25/01/18

2 *Project 1533*:

2.1 Introduction:

This document describes the SW operation of the CORAL VER2 unit.

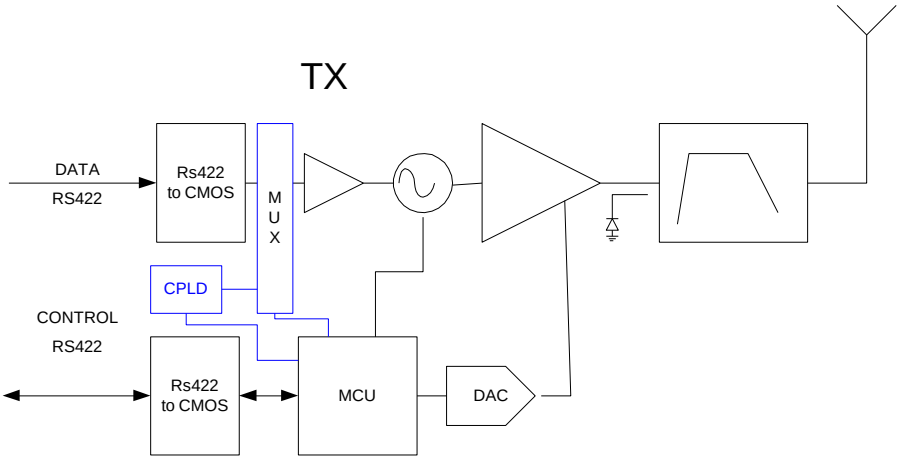
The system will consist two RF channels:

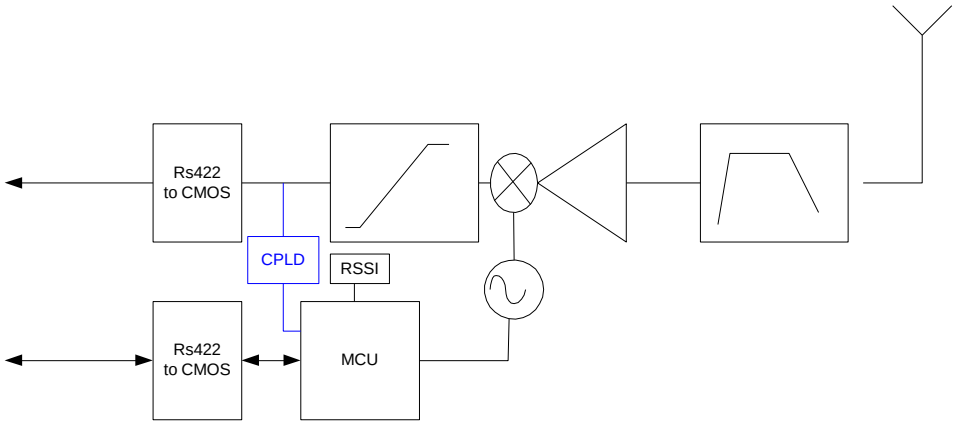
Transmit channel: will output RF signal with unique pattern that generated by the on board CPLD unit.

Receive channel: Will receive RF signal, if the signal match by his pattern to what expected the CPLD unit will indicate it to the on board MCU (which in final blink a connected LED to indicate about it).

Via serial connection we will able to control state of the transmitting / receiving and transmitting pattern. The system also have connect to MCU LEDs to indicate about the state of the system.

2.2 System block diagram





2.3 Objective

Main object of the MCU is collection data and indicate the user system about the RF signals states.

Goals of the Tx channel:

a. To configure synthesizer unit to transmit RF signals according to "PLL – configurations" section.
b. To indicate the system user about:
    - Advance power.
    - If the signal latched by the on board synthesizer.
    - Return power.
c. Transfer Tx channel to stand-by mode (at this mode no transmission will occur).
d. Turn on and off the power sensor.

Goals of the Rx channel:

a. To receive RF signals according to "PLL – configurations" section.
b. Transfer Rx channel to stand-by mode (at this mode the system will not listen to any income RF signals).
c. Change working frequency mode of the frequency RF signal.
d. Turn on and off the RSSI sensor.

The above operation modes set by serial communication channel (using user inputs commands that set by terminal application).

The on board MCU unit also will start to collect samples data from on board ADC unit immediate after system initialize
Those samples will be written to MCU internal flash and will output them to user via serial channel at user request.

On system initialize the Rx / Tx frequencies will set on default values.

2.4 PLL configurations

The on board MCU need to configure on board PLL-Synthesizers to the following configurations:

Tx signals:
PLL parameters:
PLL type: ADF4113
RF reference to PLL = 10 MHz
PRESCALER: 64
Frequencies steps: 10 kHz
Registers values:
prog = 0b110010010000000010010011 = 0xC90093
prog = 0b000000000000111110100000 = 0x000FA0

Tx signals		
Description	Range	Step size
RF_{out} – Low	5.75 – 5.85 GHz	1 MHz
RF_{out} – High	5.15 – 5.25 GHz	1 MHz
$\mathrm{PLL}_{\text{receive signal}} = \frac{RF_{out}}{2}$		
PLL – receive signal (Low)	2.575-2.625 GHz	0.5 MHz
PLL – receive signal (High)	2.8625-2.9125 GHz	0.5 MHz

Rx signals:
PLL parameters:
PLL type: ADF4350
RF reference to PLL = 10 MHz
PRESCALER: 8
Frequencies steps: 10 kHz
IF FREQ=480MHz
Registers values:
R1 = 0x08008321 R2 = 0x18005EC2 R3 = 0x000004B3 R4 = 0x0085003C
R5= 0x00580005

Rx signals		
Description	Range	Step size
RF_{in} – Low	5.15-5.25 GHz	1 MHz
RF_{in} – High	5.75-5.85 GHz	1 MHz
$\mathrm{PLL}_{\text{receive signal}} = \frac{(RF_{in} - 480\ MHz)}{2}$		
PLL – receive signal (Low)	2.335-2.385 GHz	0.5 MHz
PLL – receive signal (High)	2.6225-2.6725 GHz	0.5 MHz

2.5 Errors indications and system failures treatment

The system have two connected LEDs that indicate about the following system states:

Green led:

This led indicate that certain system operation is set correctly. It will indicate about

a. System initialize: the system initialize ok and ready to operate at stable state if the following tests will be pass:
   - Serial communication test: the on board MCU will send to host "start frame" and suppose to receive ACK.
   - The Flash on the MCU free space not reach to quarter of his limit size.
   - Connection to CPLD unit test: the on board MCU will send to the on board CPLD unit unique frame and suppose to receive ACK.

   If all off the above tests will pass ok the green led will blink 3 times.

b. System operation – Advance power: Advanced power have received in the system transmitter. Green led will blink for 5 times.
c. System operation – synthesizer letch: the transmit synthesizer latched the configuration signals ok. Green led will blink for 7 times.
d. System operation – return power: the transmitter receive return power. The green led will blink for 9 times.
e. Rx signals latch – the Rx synthesizer receive RF signal that match the pattern of the sanded RF signal. Green led will blink for 11 times.

Red led:

This led indicate that certain system have failure on one of the requested operation. It will indicate about:

a. Serial communication failure: The MCU sent to host "start frame" and not receive ACK for 30 seconds. Red led will blink 2 times.
b. Flash memory failure: The Flash on the MCU free space reached to quarter or more of his limit size – at this case the system will not store data at the flash until user will select to empty the flash space throw host serial application. Red led will blink 4 times.
c. Connection to CPLD unit test failure: The MCU sent to CPLD unit "start frame" and not receive ACK for 30 seconds. Red led will blink 6 times.
d. Synthesizer latch failure: If the on board MCU don’t success to latch the selected frequency, the MCU will try to configure and send the digital words more 2 times. If after 3 times the frequency still not latched the red led will blink 8 times.

2.6 Synthesizer registers values

Note: Please check Analog devices datasheet to learn about the way of frequency in the sensitizer unit.

In order to configure the registers of both ADF4113 and ADF4350 we use Analog devices simulator (Int N-PLL software).

3 Host PC serial control protocol

The on board MCU unit will be controller by serial communication channel (based on RS-485) and via hyper terminal application. The following table will configure that commands that the host can send to the MCU.

Frame description:
Each sending request command will begin with $ char delimiter and end with <cr> (carriage return).
On each request the MCU will send ACK response command that start with "OK <cr>$" and end with carriage return.

#	Description	Command	Example
1	Frequency change on both RX and TX.	$F XXXX <cr> XXXX = Frequency in MHz	$F 1234 <cr>
2	Insert Tx and Rx units to full operation mode.	$ON 1/0 < cr> 1: ON 0: OFF Default: 0	$ON 1
3	Turn on / off the power amplifier.	$PS 1/0 <cr> 1: ON 0: OFF Default: 0	$PS 1
4	Turn on / off the RSSI / advance power sensors	$LD 1/0<cr> 1: ON 0: OFF Default: 1	$LD 1
5	Receive the system info, a. FREQ=XXXX b. POWER OR RSSI=± XX dBM c. REV POWER = OK / FAIL d. LOCK = OK / FAIL e. UNIT ID = XXXXX format (5 signs) f. SW VERSION = XXXXX format (5 signs) g. UNIT S/N = XXXXX format (5 signs) h. UNIT DC = XXXXX format (5 signs) Note: The parameters will be show at single row when parameters will be separate by comma and after that will be carriage return.	$Q<cr>	

4 Software Update Session

The MFE software update component is a piece of software that is responsible for checking the integrity of the operational software, loading it and running it.
The software update component is also responsible for getting a new software image from the host, verify its integrity and saving it to internal flash.

To start the software update process, a power up should be performed with the PROG_EN discrete line set to ‘0’. When PROG_EN equals ‘0’ the software update process does not load the operational software from flash but instead waits for configuration data from the host.
The software update process will sample the PROG_EN discrete line for approx. TBD milliseconds. If while sampling the PROG_EN discrete its value does not equal ‘0’ the software update process will load the operational software (if it exists) and jump to it.

As in the operational application, the communication channel is an RS422 Half Duplex, 1Mb/s communication channel as described in section 5.1.
Also, the software update component also uses the RFFC1662 framing as described in section 5.3 and the message / response packet structure is the same.

To verify that the software update component has indeed loaded correctly, the host should request the version string from the MFE. The Version string form the MFE software update component is in the form of B.x where B denotes that this is a software update component version.

When starting a new flash programming operation, the software update process will start by erasing the flash sections affected by the data received, this step is destructive and data saved on that sector will be lost.

The software update component cannot update itself, in case that the software update component needs to be updated a physical access to the MFE will be needed (a PICit3 or similar debugger will be needed to program the MFE controller via ICSP).

Calibration parameters are not programmed via the software update process, and will not be effected by a software upgrade.

4.1 Software Update Messages

As stated above, the software update component uses the same communication channel, framing and message format as the operational software, this allows the host to use the same codebase for communicating with the MFE software update component .

The MFE software update component can receive the following messages:

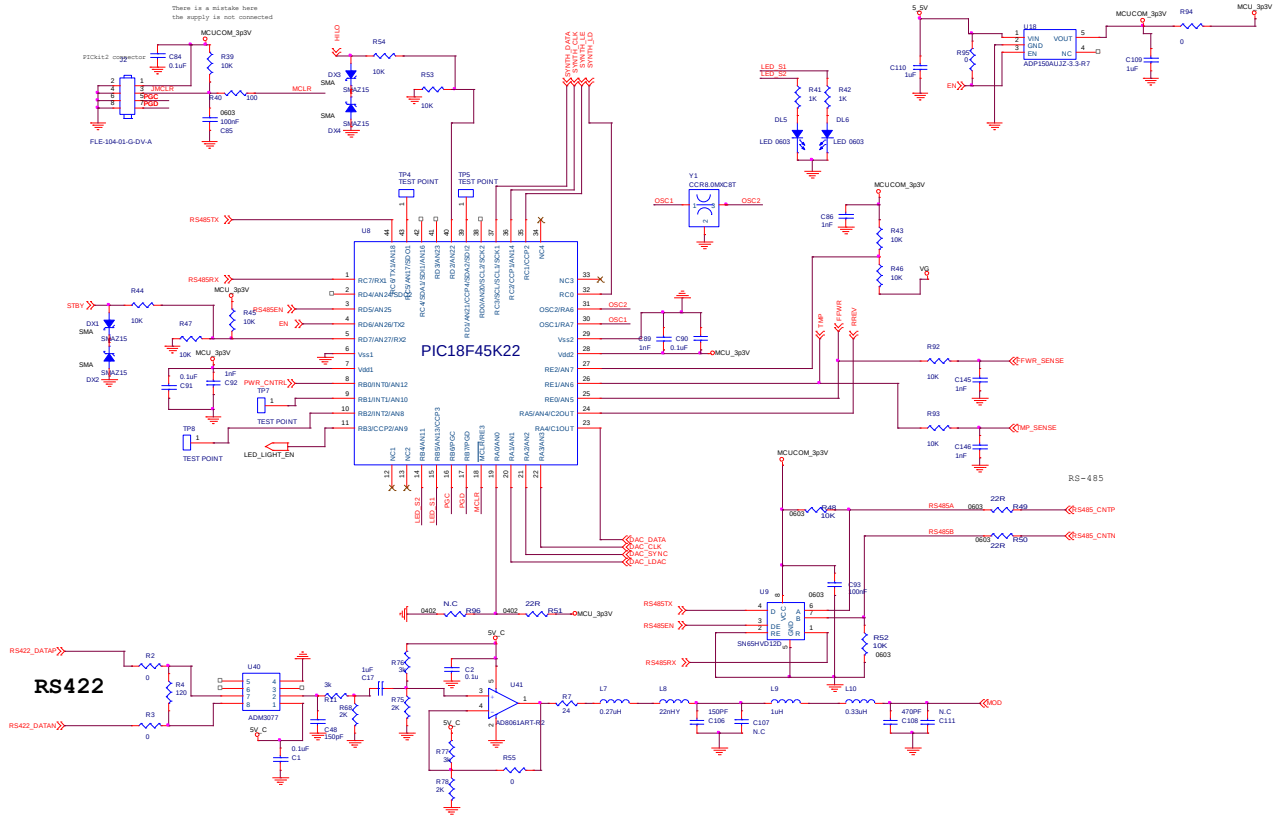
- Version Request.
- Set Data Line.
- Get Data Line.
- Finished Update Process.

The MFE will respond with the following responses:

- Version Response.
- Data Line Status.
- Data Line Data.
- Ack.

5 Hardware

5.1 MCU Schematic



5.2 Microcontroller

Recommended PIC	PIC18F45K22 – 8 bit core
Operating voltage	**3.3V**
Inputs (TTL / converter)	**TBD**
Outputs (TTL / converter)	**TBD**
POR	**Available**
Internal clock	**8MHz and up to 64Mhz**
Pin count	**40**

- Flash Memory
  - The PIC microcontroller has 32Kbytes of internal flash memory. This memory will be used for both the software update component software and for the operational software.
- RAM Memory
  - The PIC microcontroller has 1536 bytes of internal RAM, the software will use this memory for its stack & heap.
- Peripherals support:
  - Connectivity: 2-UART, 2-SPI, 2-I2C2-MSSP(SPI/I2C).
  - ADC: 28 ch, 10-bit.

5.3 GPIO and Analog Pin Assignments

MCU NET	I/O	SCHEMATIC NET	TX FUNCTION	RX FUNCTION	EXPLAIN
RC7/RX1	I	RS485RX	RS422_RX	RS422_RX	RS422 Control RX
RD4/AN24/SDO2			NC	NC	
RD5/AN25		RS485EN	NC	NC	
RD6/AN26/TX2	O	EN	POWER_EN	POWER_EN	
RD7/AN27/RX2	I	N16785247	STBY_IN	STBY_IN	When HI unit goes into STBy (EN=0) . If Low the according to Software word)
Vss1		GND_POWER			
Vdd1		MCU_3p3V			
RB0/INT0/AN12	O	PWR_CNTRL	PA_ON		operating when negative power supply is ok and when software control used
RB1/INT1/AN10		N16949169	NC	NC	
RB2/INT2/AN8		N16920411	NC	NC	
RB3/CCP2/AN9	O	LED_LIGHT_EN	MET_EN	MET_EN	when Hi enables EXTERNAL METER BACKLIGHT
NC1					
NC2					
RB4/AN11	O	LED_S2	LED_S2	LED_S2	Blinks when not locked , Lights up when PLL locked

RB5/AN13/CCP3	O	LED_S1	LED_S1	LED_S1	IN TX : on in full power . Blinks in low power mode , IN RX : Blinks when below RSSI THRESHHOLD, Lights above
RB6/PGC		PGC	PGC	PGC	
RB7/PGD		PGD	PGD	PGD	
M\C\L\R\/RE3		MCLR	MCLR	MCLR	
RA0/AN0		N16785239	NC	NC	
RA1/AN1	O	DAC_LDAC	DAC_LDAC	DAC_LDAC	Controls DAC AD5312ARMZ for :
RA2/AN2	O	DAC_SYNC	DAC_SYNC	DAC_SYNC	TX: PORT A : analog voltage according to measured output power
RA3/AN3	O	DAC_CLK	DAC_CLK	DAC_CLK	TX: PORT B: Set negative voltage according to software control . HI /LO only
RA4/C1OUT	O	DAC_DATA	DAC_DATA	DAC_DATA	RX: PORT A: analog voltage according to measured RSSI , outputs 1,11,111,1111 , PORT B: Not used
RA5/AN4/C2OUT	IAN	RREV	RREV	RSSI	TX: Analog input detecting REV power for reading through

					software .RX : RSSI
RE0/AN5	IAN	FFWR	FFWR	FFWR	TX : Analog input for FWD power to show on meter and in software.RX: not used
RE1/AN6	IAN	TMP	TMP	TMP	Reads Temperature parameters , reads in status .
RE2/AN7	IAN	N16785439	VG_MONITOR	NC	Monitors voltage , if Above ?Thereshhold , PA_ON is off
Vdd2		MCU_3p3V			
Vss2		GND_POWER			
OSC1/RA7		OSC1	OSC1	OSC1	8MHZ EXTERNAL CRYSTAL
OSC2/RA6		OSC2	OSC2	OSC2	
RC0	I	SYNTH_LD	SYNTH_LD	SYNTH_LD	IN TX: ADF 4113 , IN RX : ADF4350 (Need to decrease 480MHz IF)
NC3					
NC4					
RC1/CCP2	O	SYNTH_LE	SYNTH_LE	SYNTH_LE	
RC2/CCP1/AN14	O	SYNTH_CLK	SYNTH_CLK	SYNTH_CLK	
RC3/SCL/SCL1/SCK1	O	SYNTH_DATA	SYNTH_DATA	SYNTH_DATA	
RD0/AN20/SCL2/SCK2					
RD1/AN21/CCP4/SDA2/SDI2		N1678585842			
RD2/AN22	I	N16785806	HILO		TX ONLY, When "1" the

					tx power is set to low . When "0" Controlled by software
RD3/AN23					
RC4/SDA1/SDI1/AN16					
RC5/AN17/SDO1		N1678585824			
RC6/TX1/AN18	I	RS485TX	RS422_TX	RS422_TX	RS422 Control TX