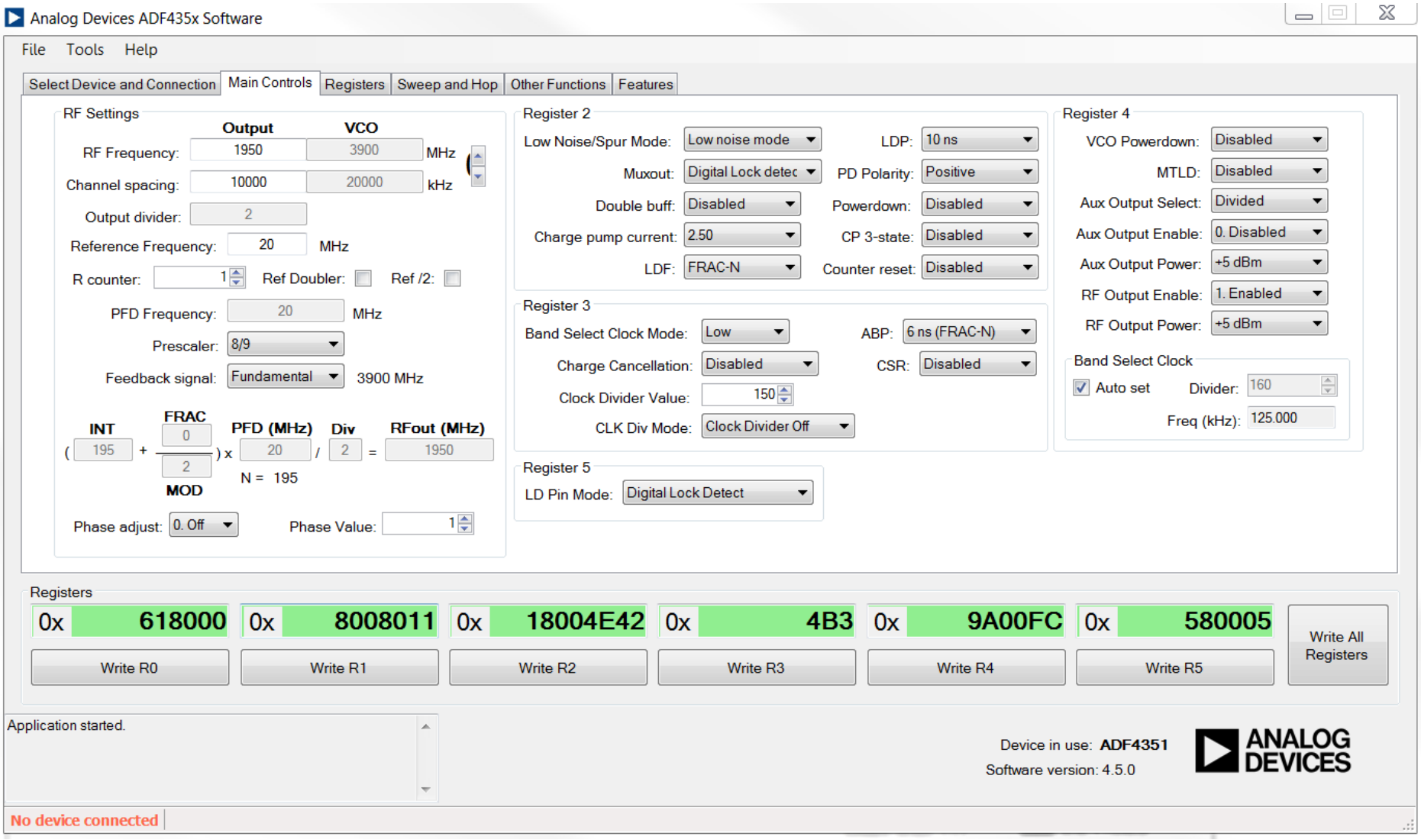
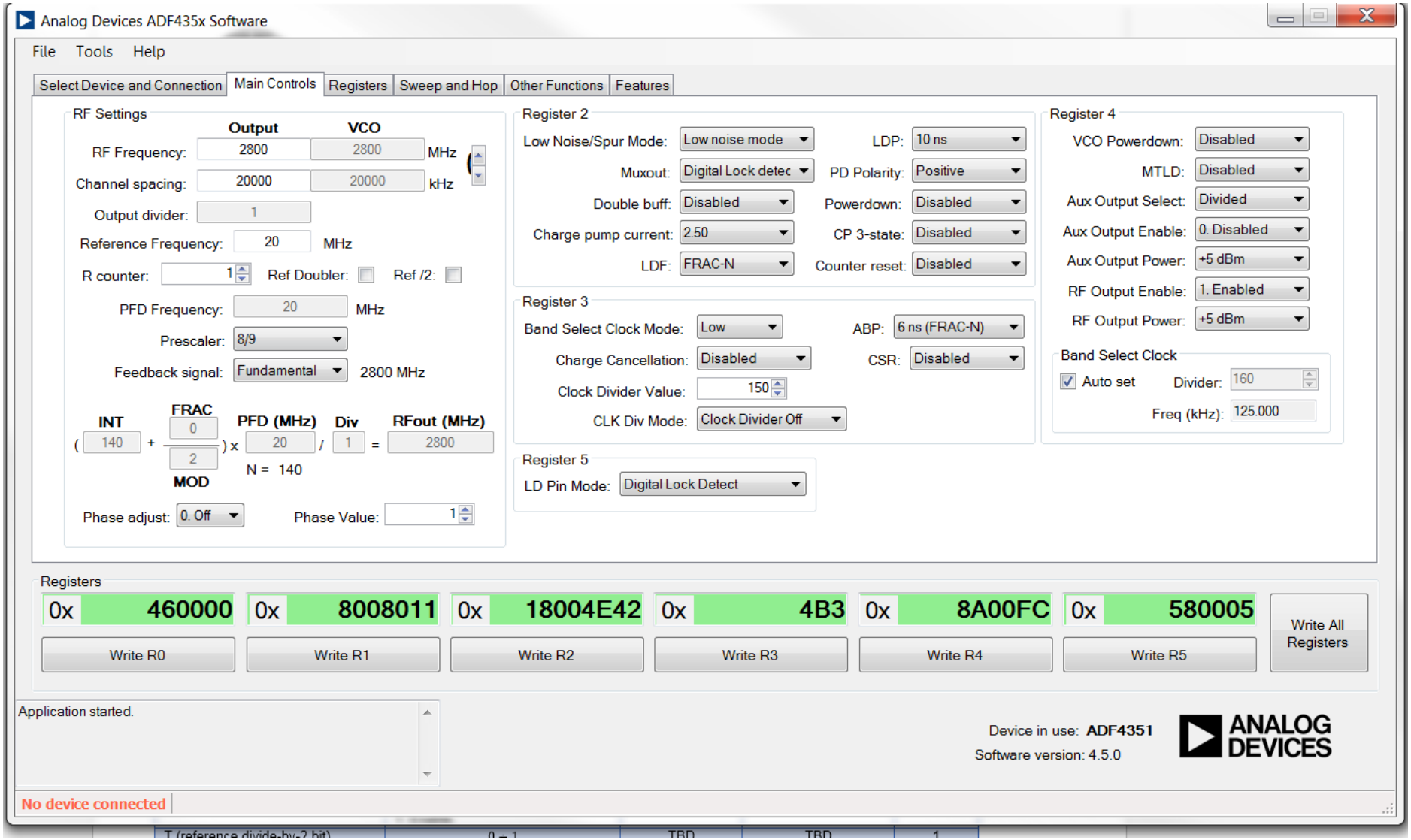

Analog Devices ADF435x Software
File
Tools
Help
Select Device and Connection
Main Controls
Registers
Sweep and Hop
Other Functions
Features
RF Settings
Output
VCO
RF Frequency:
1950
3900
MHz
Channel spacing:
10000
20000
kHz
Output divider:
2
Reference Frequency:
20
MHz
R counter:
1
Ref Doubler:
Ref /2:
PFD Frequency:
20
MHz
Prescaler:
8/9
Feedback signal:
Fundamental
3900 MHz
INT
FRAC
MOD
195
0
2
PFD (MHz)
Div
RFout (MHz)
20
2
1950
N = 195
Phase adjust:
0. Off
Phase Value:
1
Register 2
Low Noise/Spur Mode:
Low noise mode
LDP:
10 ns
Muxout:
Digital Lock detec
PD Polarity:
Positive
Double buff:
Disabled
Powerdown:
Disabled
Charge pump current:
2.50
CP 3-state:
Disabled
LDF:
FRAC-N
Counter reset:
Disabled
Register 3
Band Select Clock Mode:
Low
ABP:
6 ns (FRAC-N)
Charge Cancellation:
Disabled
CSR:
Disabled
Clock Divider Value:
150
CLK Div Mode:
Clock Divider Off
Register 5
LD Pin Mode:
Digital Lock Detect
Register 4
VCO Powerdown:
Disabled
MTLD:
Disabled
Aux Output Select:
Divided
Aux Output Enable:
0. Disabled
Aux Output Power:
+5 dBm
RF Output Enable:
1. Enabled
RF Output Power:
+5 dBm
Band Select Clock
Auto set
Divider:
160
Freq (kHz):
125.000
Registers
0x 618000
0x 8008011
0x 18004E42
0x 4B3
0x 9A00FC
0x 580005
Write R0
Write R1
Write R2
Write R3
Write R4
Write R5
Write All Registers
Application started.
Device in use: ADF4351
Software version: 4.5.0
ANALOG DEVICES
No device connected


Analog Devices ADF435x Software
File
Tools
Help
Select Device and Connection
Main Controls
Registers
Sweep and Hop
Other Functions
Features
RF Settings
Output
VCO
RF Frequency:
2800
2800
MHz
Channel spacing:
20000
20000
kHz
Output divider:
1
Reference Frequency:
20
MHz
R counter:
1
Ref Doubler:
Ref /2:
PFD Frequency:
20
MHz
Prescaler:
8/9
Feedback signal:
Fundamental
2800 MHz
INT
FRAC
MOD
140
0
2
PFD (MHz)
Div
RFout (MHz)
20
1
2800
N = 140
Phase adjust:
0. Off
Phase Value:
1
Register 2
Low Noise/Spur Mode:
Low noise mode
LDP:
10 ns
Muxout:
Digital Lock detec
PD Polarity:
Positive
Double buff:
Disabled
Powerdown:
Disabled
Charge pump current:
2.50
CP 3-state:
Disabled
LDF:
FRAC-N
Counter reset:
Disabled
Register 3
Band Select Clock Mode:
Low
ABP:
6 ns (FRAC-N)
Charge Cancellation:
Disabled
CSR:
Disabled
Clock Divider Value:
150
CLK Div Mode:
Clock Divider Off
Register 5
LD Pin Mode:
Digital Lock Detect
Register 4
VCO Powerdown:
Disabled
MTLD:
Disabled
Aux Output Select:
Divided
Aux Output Enable:
0. Disabled
Aux Output Power:
+5 dBm
RF Output Enable:
1. Enabled
RF Output Power:
+5 dBm
Band Select Clock
Auto set
Divider:
160
Freq (kHz):
125.000
Registers
0x 460000
0x 8008011
0x 18004E42
0x 4B3
0x 8A00FC
0x 580005
Write R0
Write R1
Write R2
Write R3
Write R4
Write R5
Write All Registers
Application started.
Device in use: ADF4351
Software version: 4.5.0
ANALOG DEVICES
No device connected