康芯科技

HX1006A
User 's manual

杭州康芯电子有限公司

Hangzhou Kangxin Electronic Co., Ltd

Contents

一、Introduction to Development Board

(一) Features and Design Characteristics

1. HX1006 board carries Intel Cyclone 10 LP device;

2. USB cable for power supply;

3. USB Blaster (on board) for programming and user API control;

4. HX1006 containing: pushbutton switches, toggle switches, buzzer, digital tube, user LEDs, SDRAM, EPCS16, serial Flash W25Q64, PS/2 and VGA Interface;

5. Two 40-pin external expansion ports, including 5V pin, 3.3V pin and 36-pin I/O ports which is compatible with most expansion boards on the market;

6. Rich and advanced expansion modules.

(二) Introduction

1. The core FPGA chip is 10CL006YU256C8G, Intel Cyclone 10 LP Devices. Its package is FBGA; it has 6772 logic elements, 2 PLL, 256 pins and at most 176 IO. The resource counts of this FPGA chip are shown on Table One.

Table One: Resource Counts for Intel Cyclone 10 LP Devices

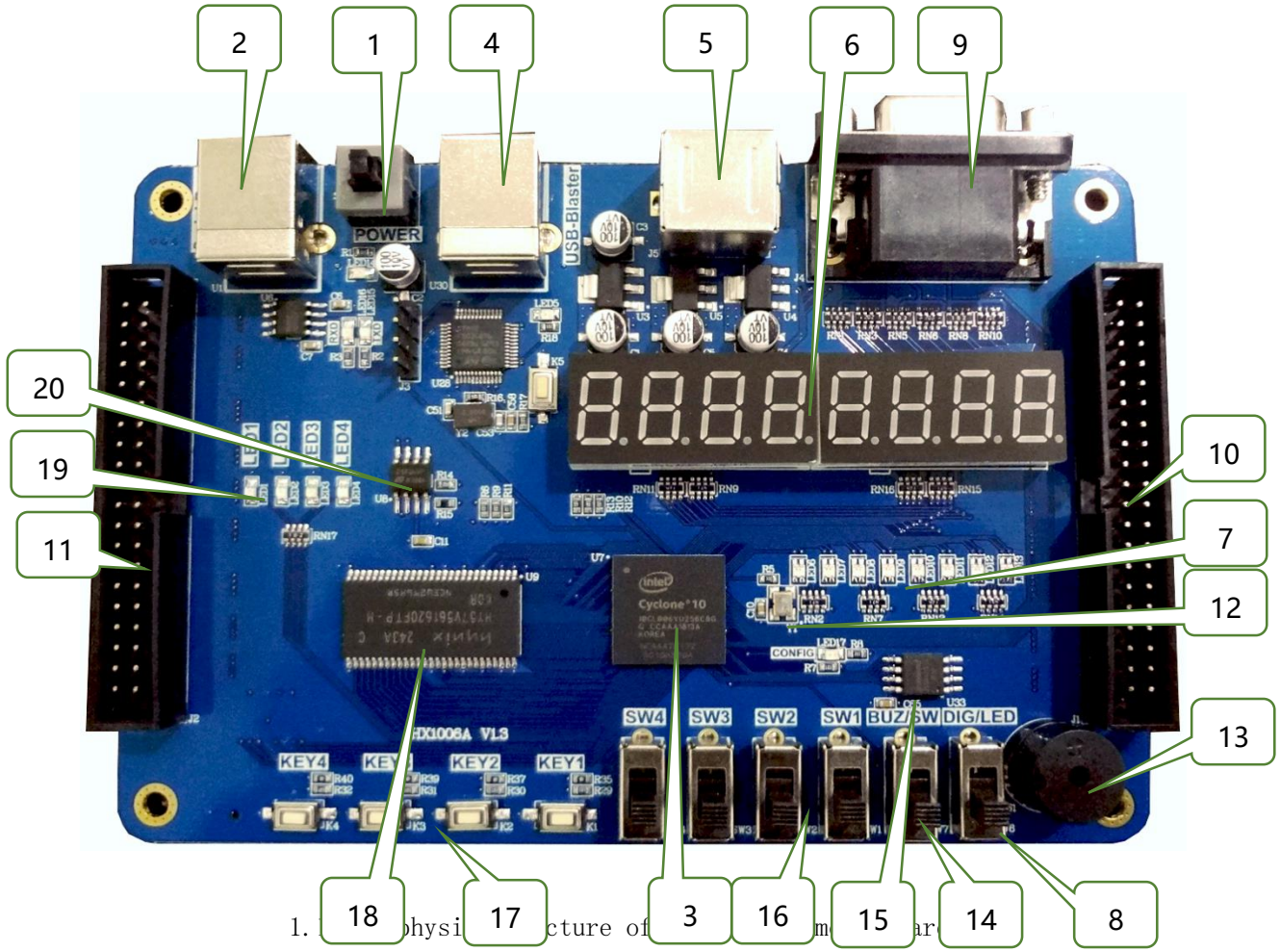
资源		器件							
		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
逻辑单元(LE)		6,272	10,320	15,408	24,624	39,600	55,856	81,264	119,088
M9K 储存器	模块	30	46	56	66	126	260	305	432
	容量(Kb)	270	414	504	594	1,134	2,340	2,745	3,888
18 × 18 乘法器		15	23	56	66	126	156	244	288
PLL		2	2	4	4	4	4	4	4
时钟		20	20	20	20	20	20	20	20
最大 I/O 数		176	176	340	150	325	321	423	525
最大 LVDS 数		65	65	137	52	124	132	178	230

Table Two: Intel Cyclone 10 LP Package Plan

器件	封装											
	类型	M164 164-pin MBGA		U256 256-pin UBGA		U484 484-pin UBGA		E144 144-pin EQFP		F484 484-pin FBGA		F780 780-pin FBGA	
	尺寸	8 mm × 8 mm		14 mm × 14 mm		19 mm × 19 mm		22 mm × 22 mm		23 mm × 23 mm		29 mm × 29 mm	
	球间距	0.5 mm		0.8 mm		0.8 mm		0.5 mm		1.0 mm		1.0 mm	
	I/O 类型	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS
10CL006		—	—	176	65	—	—	88	22	—	—	—	—
10CL010		101	26	176	65	—	—	88	22	—	—	—	—
10CL016		87	22	162	53	340	137	78	19	340	137	—	—
10CL025		—	—	150	52	—	—	76	18	—	—	—	—
10CL040		—	—	—	—	325	124	—	—	325	124	—	—
10CL055		—	—	—	—	321	132	—	—	321	132	—	—
10CL080		—	—	—	—	289	110	—	—	289	110	423	178
10CL120		—	—	—	—	—	—	—	—	277	103	525	230

Table Two shows the package plan for Intel Cyclone 10 LP devices. For more detailed information, refer to the device manual.

二、Package Contents



1. Physical picture of the front panel area

The following hardware is provided on the HX1006 board. We can learn what can be done with the development platform from figure 1.1.

1. Power switch, USB-powered operation;
2. USB to serial port, also used as a power source;
3. FPGA chip: 10CL006Y256C8, Intel Cyclone 10 LP devices;
4. USB-Blaster port, also used as a power source;
5. PS/2 port, used for connecting keyboards and mice;
6. 8 seven-segment displays;
7. 8 bicolor LED for flowing water light, also multiplexed with seven-segment displays;
8. Control switches of 8 seven-segment displays and 8 bicolor LEDs;
9. VGA port, 12-bit RGB444 color depth;
10_11. Two 40-pin GPIO, including 5V pin, 3.3 pin, GND pin and 36 I/O ports which are compatible with expansion boards;
12. The onboard 50 MHz oscillator;
13. Buzzer;
14. Buzzer switch;
15. W25Q64 (64M-bit) serial flash memory for FPGA;
16. 4 toggle switches, also used as input port;
17. 4 pushbuttons;
18. 256Mb ×16 SDRAM;
19. 4 LEDs;
20. SPI FLASH MP16 used to realize power fail protection and store FPGA configuration files and user data;
21. Micro SD connector located on the back of the board;

1. Power Source

（1）Three different voltages are supplied on the development board

Connect the USB cable from the host computer to the USB connector on the

development board. Turn the power on by pressing the ON/OFF switch on the board. The power supply chips transmit the input power to three power lines, 3.3V, 2,5V and 1.2V, which meet the I/O, PLL and kernel voltage requirements of FPGA.

Schematic diagram of power supply design is shown in figure 1-1.

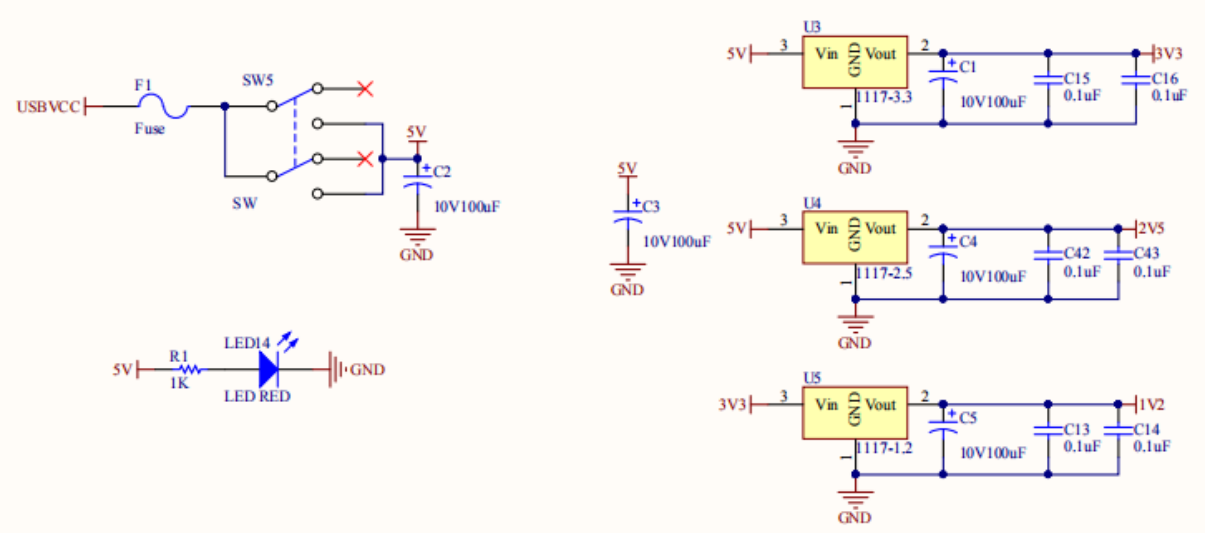


Figure 1-1 Three power lines on the development board

（2）Power Supply and Ground Pins of FPGA

There are there power supplies for FPGA, I/O bank voltage, core voltage, analog voltage and PLL power supply.

1. FPGA core needs independent working power supply. VCCINT is the power supply pin of FPGA and its supply voltage is 1.2V. Two PLL provides convenience for development projects that require different clock sources. VCCD_PLL is the power supply pin of the digital part of the PLL and its supply voltage is also 1.2V.

2. The peripheral I/O port voltage of FPGA is 3.3V and FPGA pins are 3.3V input and output. VCCIO 0-VCCIO 3 are respectively the power supply pins of FPGA BANK 0-BANK 3. On the development board, the voltage of VCCIO are all 3.3V.

3. VCCA is the analog power supply of FPGA and its supply voltage is 2.5V. The analog part of PLL and the configuration circuit voltage of FPGA are both 2.5V.

4. Note that in order to ensure a smooth reference ground inside the FPGA, a lot of pins are connected to GND. The power connection diagram is shown in figure 1-2.

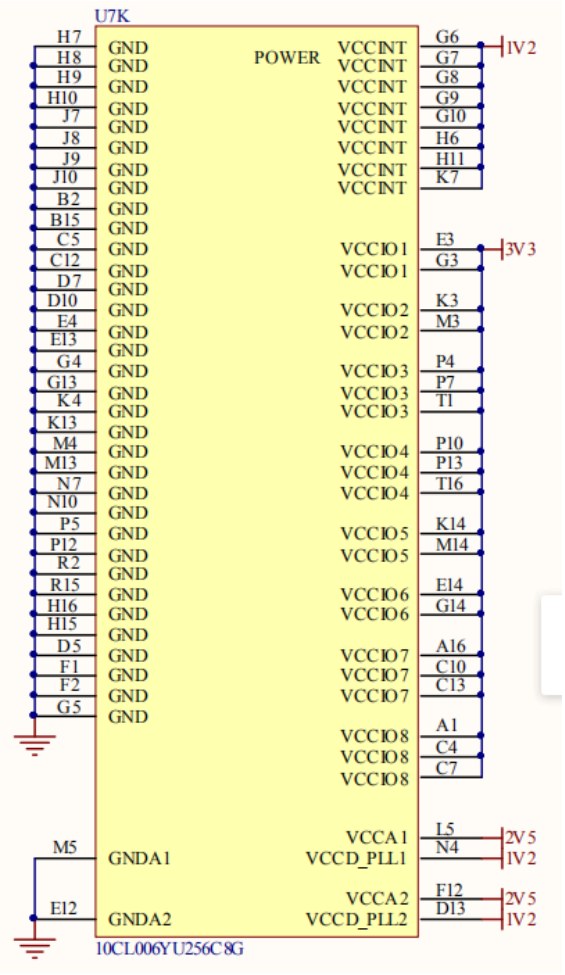


Figure 1-2 Power supply and ground pins of FPGA

2. USB to UART Serial Convertor

The development board carries a USB to serial chip, CH330. This chip has two features: (1) supports 5V and 3.3V supply voltage; (2) can communicate with the computer end with a USB cable. The schematic diagram is shown in figure 2-1.

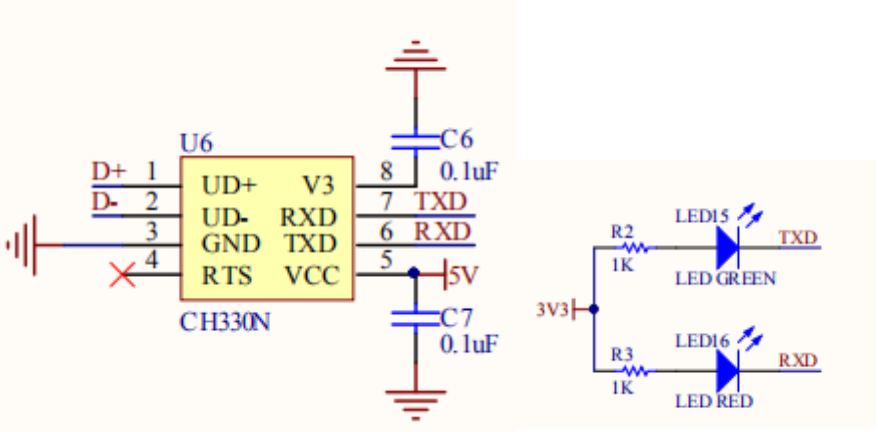


Figure 2-1 The schematic diagram of USB to UART Serial

Serial Port Pin and Signal Assignments:

Signal Name	Pin
RXD	B7
TXD	A7

3. FPGA

The FPGA chip is 10CL006 in the Intel Cyclone 10 LP series. Its package is ball grid array (BGA) with 256 pins, which is smaller and denser when compared with the previous package. If the FPGA is QFP package, 144 pins or 208 pins, its pin name is pure number, 1 to 144 or 1 to 208 respectively; when the FPGA is BGA package, its pin name is the combination of letters and numbers, such as H4 and J13. Thus, when the pin name of schematic diagram is the combination of digit and number, we will know this FPGA chip is BGA package. Figure 3-1 is the physical picture of FPGA on the development board.

Figure 3-1 The FPGA physical figure

4. USB-Blaster

The USB-Blaster download cable interfaces a USB port on a host computer to an Intel FPGA mounted on a printed circuit board. Connection specifications can be found in the USB-Blaster Download Cable User Guide.

The JTAG interface of the FPGA is used to download the compiled program (.sof) into the FPGA, or to load the prof file into the power-drop protected FLASH (EPCS)

through the AS mode. If the development board has no AS mode, we can transfer the sof file to the jic file through Quartus, and then download the jic file to the flash. Thus, after recharging, the FPGA will automatically read and run the jic configuration file in flash.

Figure 4-1 is the schematic diagram of JTAG port. TCK, TDO, TMS and TDI are four associated ports on FPGA and each signal port connects with the diode as an overvoltage protection circuit.

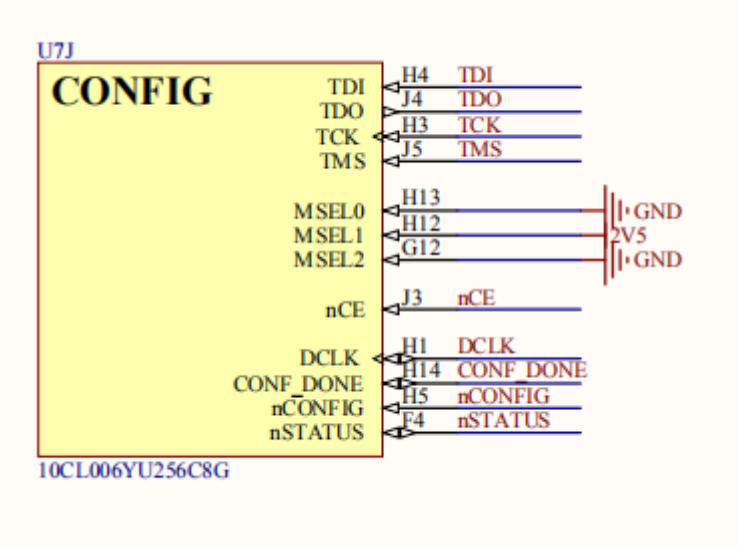
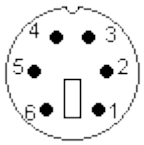


Figure 4-1 Schematic diagram of JTAG port

5、PS/2

The PS/2 port is a 6-pin mini-DIN connector, shown in figure 5-1, used for connecting keyboards and mice. As shown in figure 5-2, Pin 1 Data and Pin 5 CLK can be controlled by FPGA I/O. Pin 4 is VCC and Pin 3 is GND.



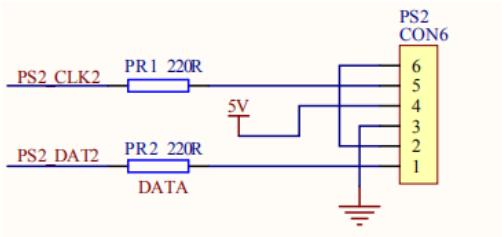


Figure 5-1 PS/2 interface diagram

Figure 5-2 The schematic diagram of PS/2

Figure 5-3 The physical picture of PS/2

PS/2 Pin and Signal Assignments:

Signal Name	Pin
P_CLK	B9
P_DATA	A9

6、7-Segment Displays

The 7-segment display is a form of electronic display device for displaying decimal numerals. It consists of eight LEDs arranged in a rectangular fashion as shown in figure 6-1. In this package, all of the anodes of the segment LEDs are connected and brought out to a common pin; this is also referred to as a "common anodes". It means when the pin corresponding to a segment is low level, the corresponding segment is lit.

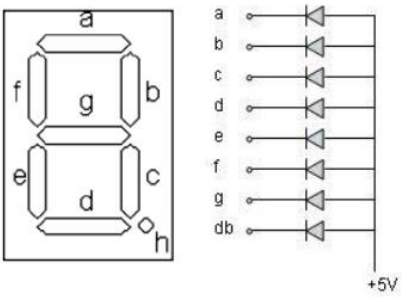


Figure 6-1 The individual segments of a seven-segment display

To operate any particular segment of any digit, the controlling integrated circuit would turn on the cathode driver for the selected digit, and the anode drivers for the desired segments; then after a short blanking interval the next digit would be

selected and new segments lit, in a sequential fashion. Because of the visual staying phenomenon, we will not see flickering.

Two multiplexed 4-digit, 7-segment displays are placed together with only 16 pins. As shown in figure 6-1, DIG [0…7] corresponds to segment a, b, c, d, e, f, g, h and DP; SEL [0…7] corresponds to control pins for 7-segment display with active high enable input. Schematic diagram is shown in figure 6-2; physical figure is shown in figure 6-3.

Note: As shown in figure 7-1, pin SW6 is connected a selector switch to choose whether 8 bicolor LED or 7-segment display works. Choose the different display mode by turn ON/OFF the selector on the board.

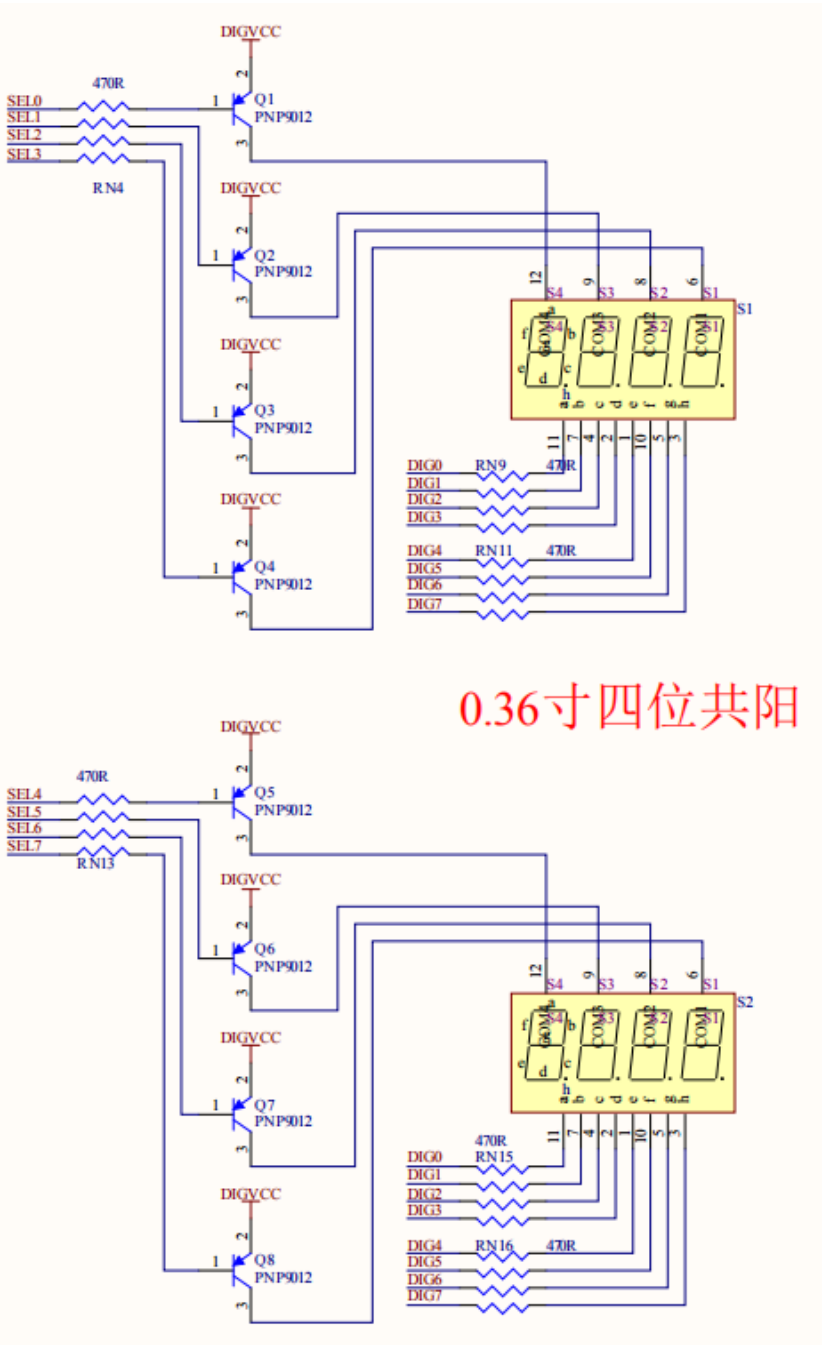


Figure 6-2 The schematic diagram of two multiplexed 4-digit, 7-segment displays

Figure 6-3 The physical diagram of two multiplexed 4-digit, 7-segment displays

7. Bicolor LEDs

There are 8 bicolor LEDs with red and green on the development board. They are actually two different LEDs in one case; thus, it needs 16 pins to control 8 bicolor LEDs as shown in figure 7-1. When the pin is logic 0, the LED goes out; when the pin

is logic 1, the LED is lit. Figure 7-2 is a physical figure.

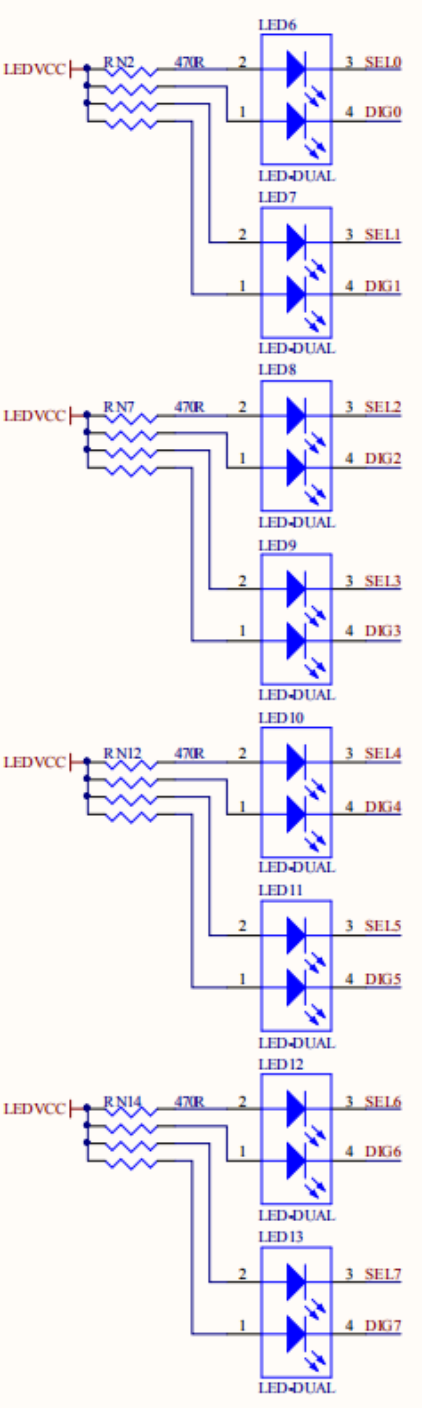


Figure 7-1 The schematic diagram of bicolor LEDs

Figure 7-2 The physical picture of bicolor LEDs

The Corresponding Pins between LEDs, 7-segment Displays and FPGA pin

LEDs Pin	7-segment displays pin	FPGA Pin

LED6 red	DIG0 (a)	D15
LED6 green	SEL0 (Left First)	D16
LED7 red	DIG1 (b)	C15
LED7 green	SEL1 (Left Second)	C16
LED8 red	DIG2 (c)	A15
LED8 green	SEL2 (Left Third)	B16
LED9 red	DIG3 (d)	A14
LED9 green	SEL3 (Left Fourth)	B14
LED10 red	DIG4 (e)	A13
LED10 green	SEL4 (Left Fifth)	B13
LED11 red	DIG5 (d)	A12
LED11 green	SEL5 (Left Sixth)	B12
LED12 red	DIG6 (g)	A11
LED12 green	SEL6 (Left Seventh)	B11
LED13 red	DIG7 (h)	A10
LED13 green	SEL7 (Left Eighth)	B10

8. Selector Switch for LEDs and 7-segment Displays

In chapter 6 and chapter 7, we have mentioned that control pins for LEDs and 7-segment are multiplexed pins. The selector switch SW6 under the development board is to choose whether 8 bicolor LEDs or 7-segment displays works. Choose the different display mode by turn ON/OFF the selector on the board. Figure 8-1 is the schematic diagram and figure 8-2 is the physical picture.

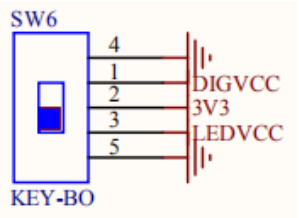


Figure 8-1 The schematic diagram for selector switch
Figure 8-2 The physical picture for selector switch

9. VGA Interface

A Video Graphics Array (VGA) connector is a three-row 15-pin DE-15 connector. VGA connectors and cables carry analog component video signals, including RGB video signal, HSYNC (horizontal sync) and VSYNC (vertical sync). FPGA can only output digital signals, but RGB signals required by VGA are analog signals. In the development board, transferring FPGA digital signal to analog signal is realized by a simple resistance circuit. The circuit can produce 32 gradations of RGB analog signals (RGB 565). The schematic circuit of VGA interface is shown in figure 9-1; and the physical picture is shown in figure 9-2.

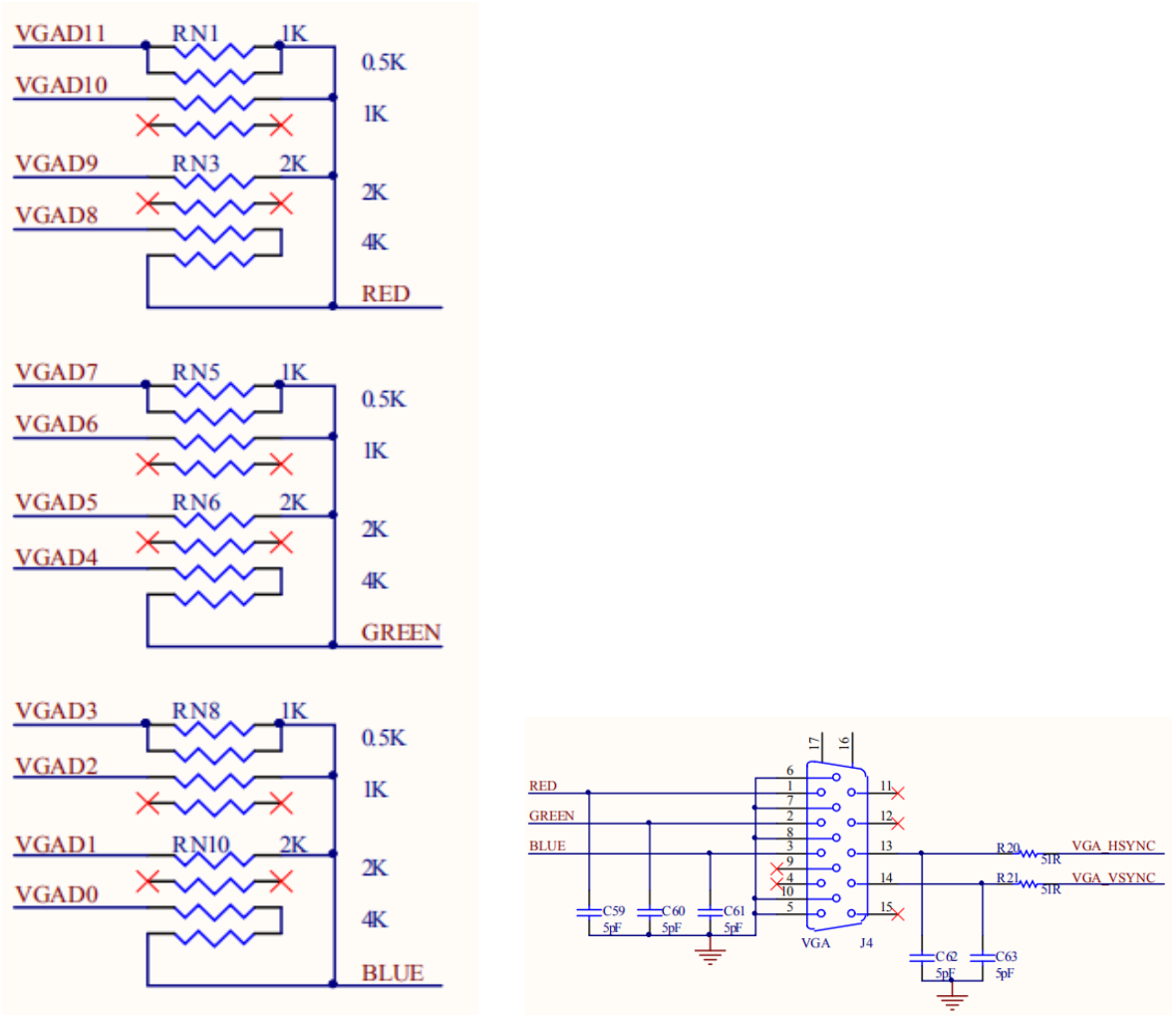


Figure 9-1 The schematic circuit of RGB444 (left) The schematic circuit of VGA interface (right)

Figure 9-2 The physical picture of VGA cable

VGA Interface Pin and Signal Assignments

Pin Name	FPGA PIN	Description
VGA_D[0]	N16	BLUE[0]
VGA_D[1]	L15	BLUE[1]
VGA_D[2]	L16	BLUE[2]
VGA_D[3]	K15	BLUE[3]
VGA_D[4]	K16	GREEN[0]
VGA_D[5]	J15	GREEN[1]
VGA_D[6]	J16	GREEN[2]
VGA_D[7]	J11	GREEN[3]
VGA_D[8]	G16	RED[0]
VGA_D[9]	G15	RED[1]
VGA_D[10]	F16	RED[2]
VGA_D[11]	F15	RED[3]
VGA_HS	P16	Horizontal Sync
VGA_VS	N15	Vertical Sync

10_11、Two Expansion Port

The development board reserves two 40-pin expansion ports, including 5V pin, 3.3V pin and 36-pin I/O ports. On the right side, I/O ports of J1 are all independent ports; on the left side, I/O ports of J2 multiplexed I/O ports with character LCD display, lattice LCD display and selector switch. Thus, we cannot use the LCD display and extension module on J2 at the same time. Since the I/O voltage tolerance of FPGA is 3.3V, it is worth noting that two expansion ports cannot connect with the device with an output voltage of 5V. For avoiding damage to the FPGA by external voltage and current, the FPGA, 47-Ohm resistor packs and the expansion port are connected in series. The schematic circuit of two expansion ports are shown in figure 10-1 and 10-2.

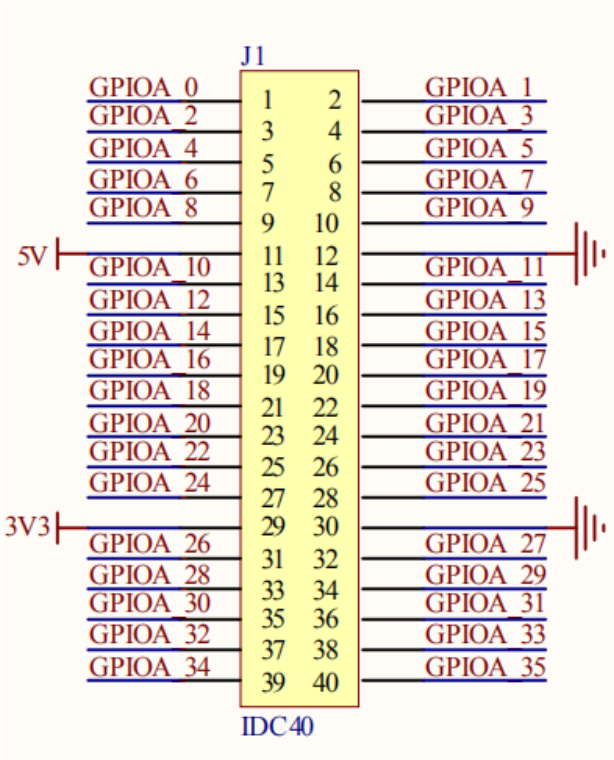


Figure 10-1 J1 expansion port (right side)

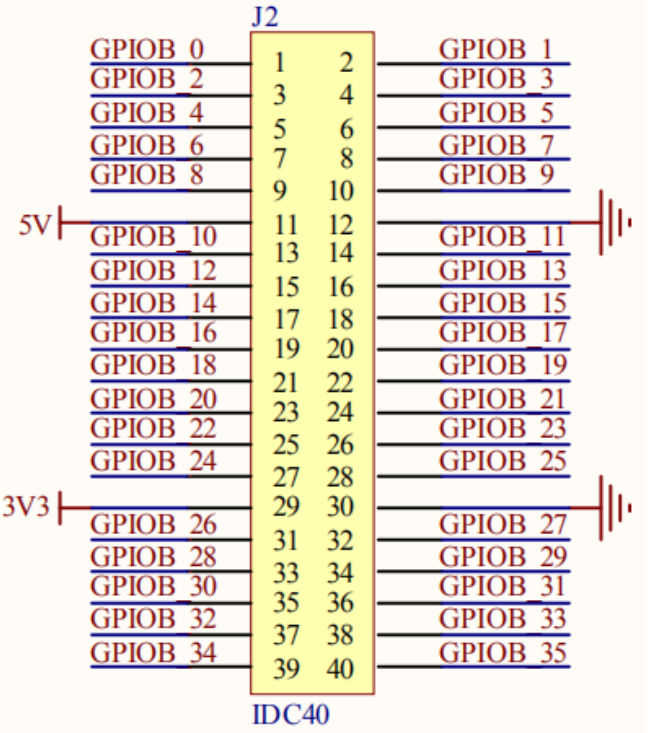
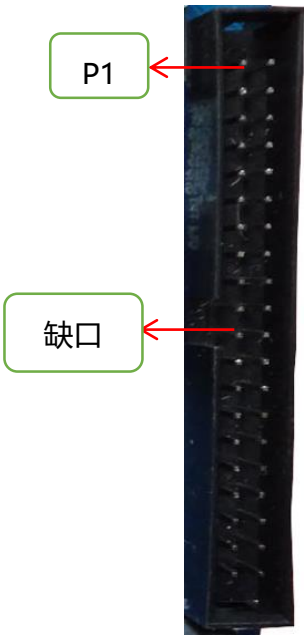


Figure 10-2 J2 expansion port (left side)



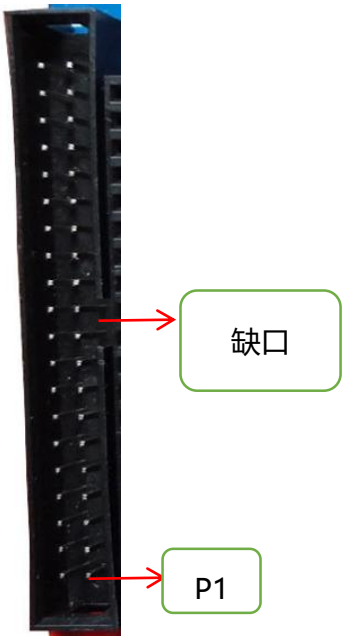


Figure 10-3 Physical picture of J1 port (right) Figure 10-4 Physical picture of J2 port

Note: When locking the expansion port, the direction of the notch should be followed. Figure 10-3 and 10-4 shows the physical picture of J1 and J2, respectively.

J1 Expansion Port Pin and Signal Assignments

Number	FPGA Pin	Number	FPGA Pin
1	F5	**2**	D3
3	C3	**4**	D4
5	E5	**6**	E6
7	C6	**8**	D6
9	D8	**10**	R10
11	VCC5V	**12**	GND
13	E7	**14**	E8
15	F6	**16**	F8
17	F7	**18**	D9
19	C9	**20**	E9
21	E10	**22**	C11
23	D11	**24**	E11
25	C14	**26**	D12
27	D14	**28**	F9
29	3.3V	**30**	GND
31	F13	**32**	F14
33	F11	**34**	G11
35	F10	**36**	L10
37	K11	**38**	L11
39	J12	**40**	J14

J1 Expansion Port Pin and Signal Assignments

Number	FPGA Pin	Number	FPGA Pin
1	J13	**2**	K12
3	L14	**4**	L13
5	M12	**6**	N14
7	N13	**8**	P14
9	N12	**10**	L12
11	VCC5V	**12**	GND
13	N11	**14**	P11
15	M11	**16**	M10
17	P9	18	N9
19	M9	**20**	L9
21	M8	**22**	N8
23	P8	**24**	L7
25	M7	**26**	P6
27	N6	**28**	N5
29	M6	**30**	P3
31	3.3V	**32**	GND
33	L6	**34**	N3
35	K6	**36**	L4
37	L3	**38**	K5
39	L8	**40**	K9

12. 50M Oscillator

The schematic circuit of oscillator on the development board is shown in figure 12-1. The clock input pin (CLK1, E15) is driven with an external oscillator. The clock signal can be divided or multiplied into a desired frequency by configuring the PLL inside the FPGA. The physical picture of 50M oscillator is shown in figure 12-1.

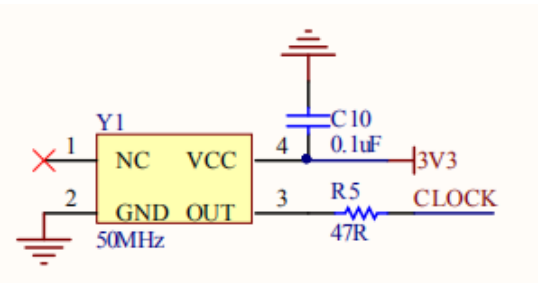


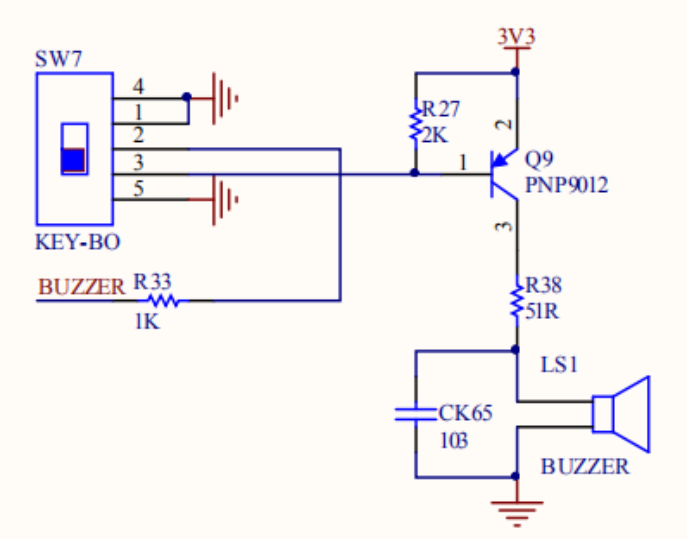
Figure 12-1 Schematic diagram of oscillator connection Figure 12-2 Physical picture of oscillator

Clock Pin and Signal Assignments

Pin Name	FPGA Pin
CLK	E15

13_14. Buzzer and Control Switch

The buzzer connects with a transistor. When input signal BUZZER is low level, the transistor conducts and the buzzer rings; when input signal BUZZER is high level, the buzzer sound stops. To control the noise of buzzer, the control switch SW7 is connected between the transistor and the buzzer. The schematic diagram is shown in figure 13-1.



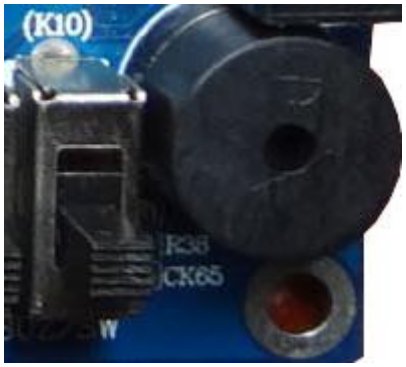


Figure 13-1 Schematic diagram of buzzer and control switch Figure 13-2 Physical picture of buzzer and control switch

Buzzer Pin and Signal Assignments:

Pin Name	FPGA Pin
BUZ	K10

15. Serial FLASH W25Q64

The development board contains a 64M-bit serial SPI flash memory, W25Q64. It has more than 100,000 erase/program cycles and more than 20-year data retention. It supports single 2.7 to 3.6V supply. The W25Q64 supports standard/dual/quad SPI clocks, and its clock can up to 80Mhz. The schematic diagram is shown in figure 15-1; the physical picture is shown in figure 15-2.

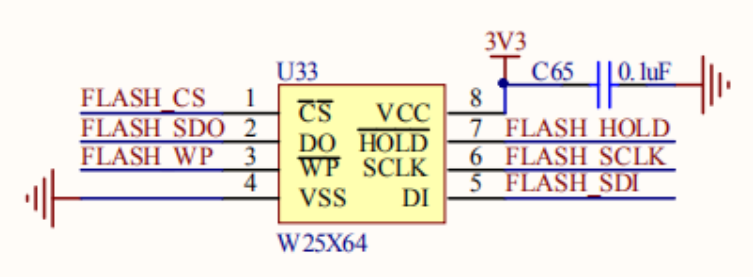


Figure 15-1 The schematic diagram SPI Flash

图 15-2 The physical Picture SPI Flash

W25Q64 Pin and Signal Assignment

Pin Name	FPGA Pin
FLASH_CS	R13
FLASH_SDO	R14
FLASH_WP	R16
FLASH_HOLD	T14
FLASH_SCLK	T15
FLASH_SDI	P15

16. Toggle Switch

The development board contains four toggle switches. The schematic diagram is shown in figure 16-1; the physical picture is shown in 16-2.

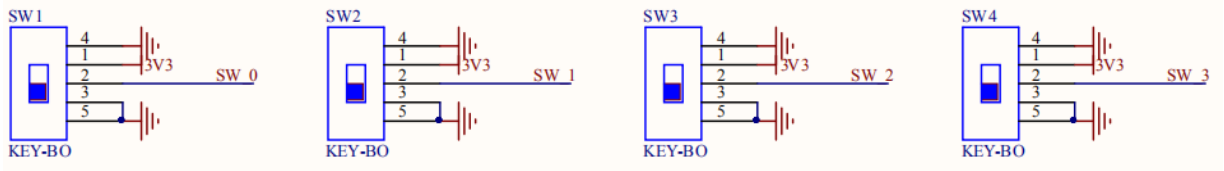


Figure 16-1 The schematic diagram of toggle switch

Figure 16-2 Physical picture of toggle switches

Toggle Switch Pin and Signal Assignments:

Pin Name	FPGA Pin
SW1	E16
SW2	M16
SW3	M15
SW4	M2

17. Pushbutton

The development board contains 4 pushbutton, KEY1-KEY4. The signal is low level when keeps the pushbutton pressed; the signal is high level when releases the pushbutton. The schematic diagram is shown in figure 17-1 and the physical picture is shown in figure 17-2.

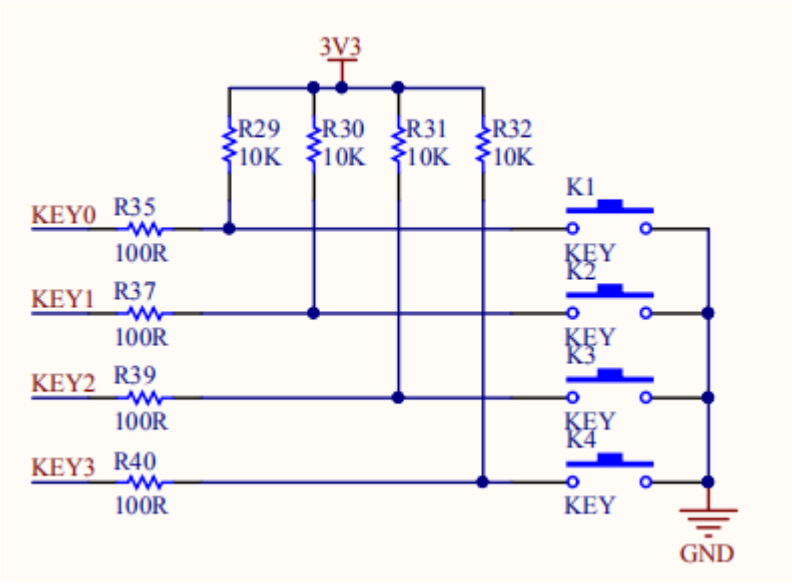


Figure 17-1 The schematic diagram of four pushbuttons

Figure 17-2 The physical picture of four pushbuttons

Pushbutton Pin and Signal Assignments

Key Name	FPGA Pin
K1	M1
K2	F3
K3	E1
K4	E2

18. SDRAM

The development board carries a SDRAM chip, HY57V2562GTR. It is 256Mbit CMOS Synchronous DRAM and it is organized as 16-bit bus. SDRAM can temporarily store image data and then display it through it through the interface. The schematic diagram is shown in figure 18-1 and the physical picture is shown in figure 18-2.

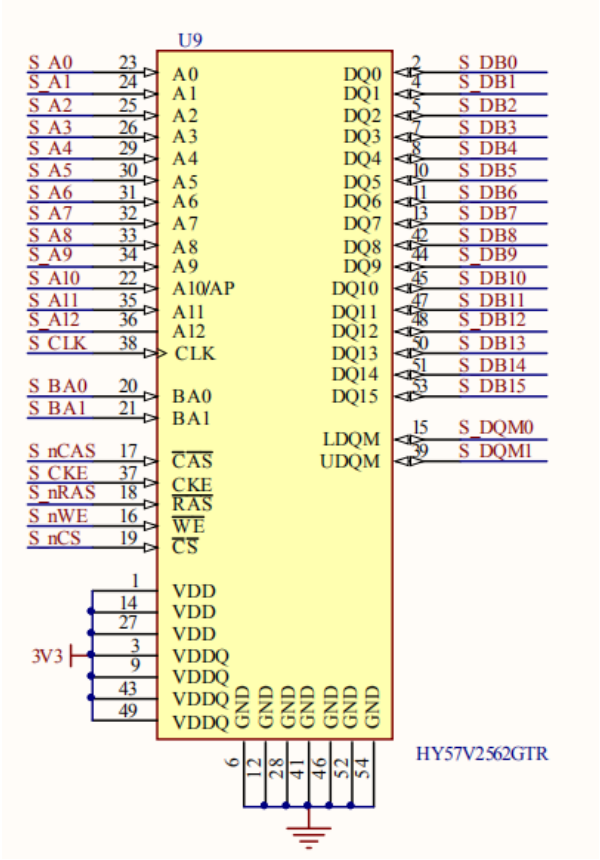


Figure 18-1 The schematic diagram of SDRAM

Figure 18-2 The physical picture of SDRAM

SDRAM Pin and Signal Assignments:

Pin Name	FPGA Pin
S_CLK	R4
S_CKE	T4
S_nCS	G2
S_nWE	B1
S_nCAS	C2
S_nRAS	D1
S_DQM0	A2
S_DQM1	T3
S_BA0	G1
S_BA1	J6
S_A0	J2
S_A1	K1
S_A2	K2
S_A3	L1
S_A4	T8
S_A5	R8
S_A6	T7
S_A7	R7
S_A8	T6
S_A9	R6
S_A10	J1
S_A11	T5
S_A12	R5
S_DQ0	B5
S_DQ1	A5
S_DQ2	B6
S_DQ3	A6
S_DQ4	A4
S_DQ5	B4
S_DQ6	A3
S_DQ7	B3
S_DQ8	R3

S_DQ9	T2
S_DQ10	L2
S_DQ11	N1
S_DQ12	N2
S_DQ13	P1
S_DQ14	P2
S_DQ15	R1

19. 4 LEDs

The development board carries 4 LEDs, (LED1-LED4). The schematic diagram of 4 LEDs is shown in figure 19-1 and the physical picture is shown in figure 19-2.

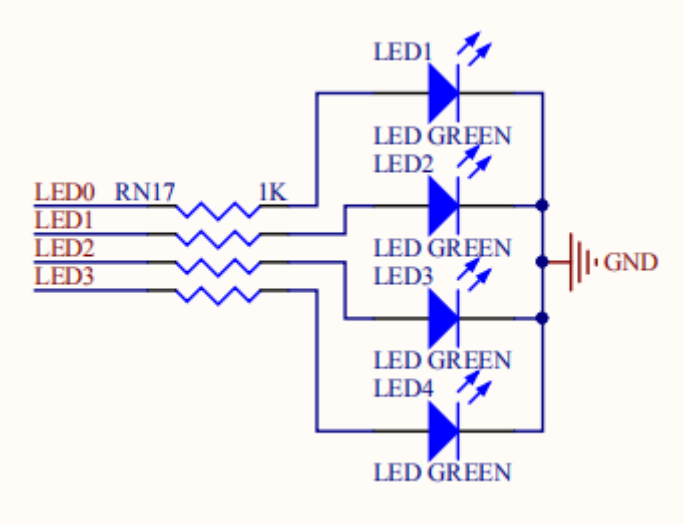


Figure 19-1 The Schematic diagram of 4 LEDs

Figure 19-2 The physical picture of 4 LEDs

LEDs Pin and Signal Assignments:

Pin Name	FPGA Pin
LED0	T10
LED1	R9
LED2	T9
LED3	K8

20. SPI Flash

The development board carries a 16Mbit SPI FLASH, M25P16. To configure a system using an SRAM-based device, each time you power on the device, you must load the configuration data. M25P16 is a flash memory device that can store configuration data that you use for FPGA configuration purpose after power on. For more information about M25P16 and its parameters, refer to the Table 20.1. The

schematic diagram of SPI Flash is shown in figure 20-1 and the physical picture of figure 20-2 is shown in figure 20-2.

Table 20.1 SPI Flash

Bit number	Chip	Capacity	Manufacturer
U8	M25P16	16M bit	ST

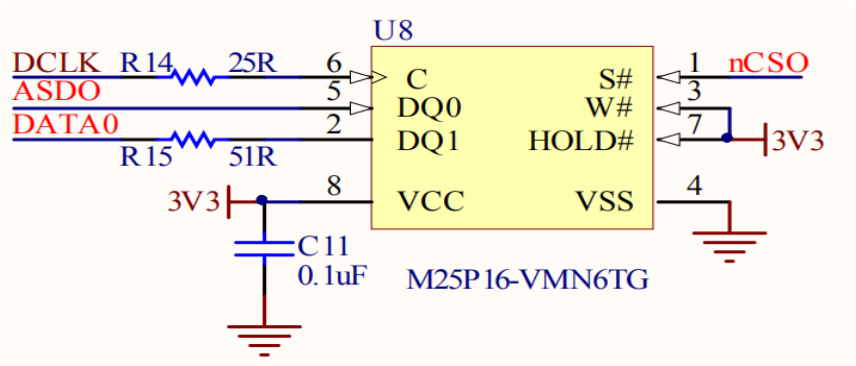


Figure 20-1 Schematic diagram of SPI Flash

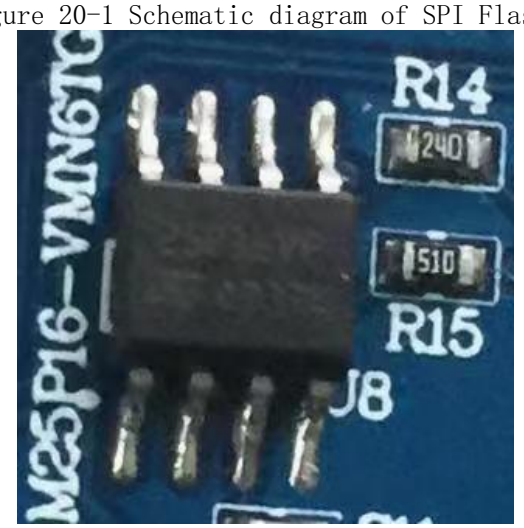


Figure 20-2 Physical picture of SPI Flash

Flash Pin and Signal Assignments

Pin Name	FPGA Pin
DCLK	H1
nCSO	D2
DATA0	H2
ASDO	C1

21. SD Card Slot

The SPI bus mode and one-bit SD bus mode are mandatory for all SD families.

The development board uses the more comprehensive SD card mode. Pin diagram is shown in figure 21-1 and the schematic diagram is shown in figure 21-2.

TF Card (SD mode) : 1-data2; 2-data3; 3-cmd; 4-vdd; 5-clk; 6-vss; 7-data 0; 8-data1.

TF Card (SPI mode): 1-rsv; 2-cs; 3-di; 4-vdd; 5-sclk; 6-vss; 7-do; 8-rsv.

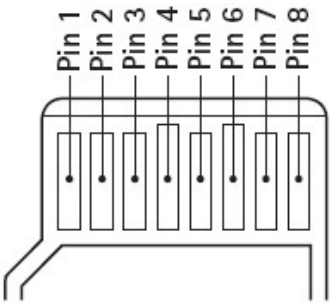


Figure 21-1 Pin diagram

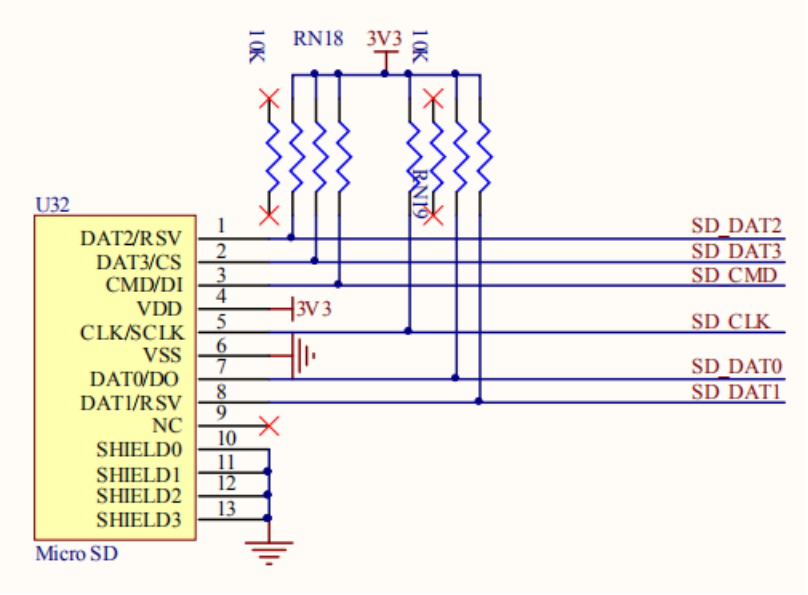


Figure 21-2 The schematic diagram of SD card

SD card slot is on the back of the development board. Figure 21-3 is the physical picture of SD card slot.

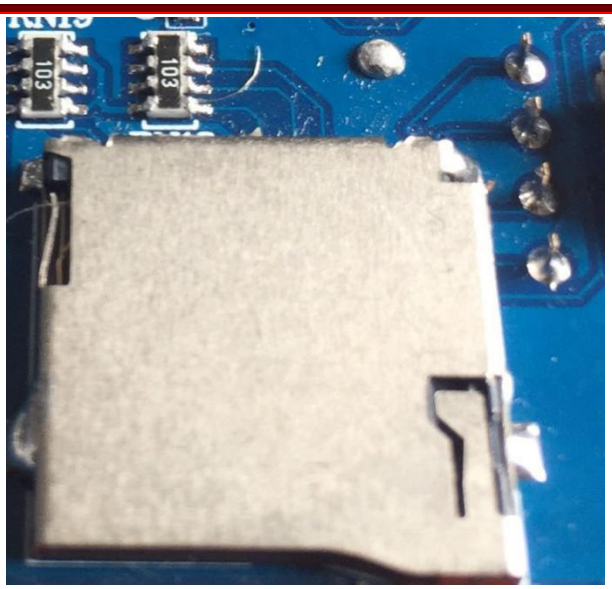


Figure 21-3 The physical picture of SD card slot

SD Card Slot Pin and Signal Assignments:

Pin Name	FPGA Pin
SD_DAT3	R12
SD_DAT2	T13
SD_DAT1	R10
SD_DAT0	T11
SD_CLK	R11
SD_CMD	T12

三、 Introduction to Extension Module

1. Extension Module for 4×4 Matrix Keypad

Figure 1-1 is the physical picture of matrix keypad. It has 16 built-in pushbutton contacts connected to 4 row and 4 column lines. The pushbuttons of each row and column are connected through the pin outside. The matrix keypad can be connected to the development board through J1 extension port or J2 extension port. The connecting method is shown in figure 1-3. For more information about locking the expansion port, please refer to “Chapter Two, Introduction to Development Board” ->” 10_11 Two Expansion Port”. The pin locking mode of other modules is the same. Detailed information and experiments related to matrix keypad module

are in the folder “DEMO/20_SCAN_4X4KEY”.

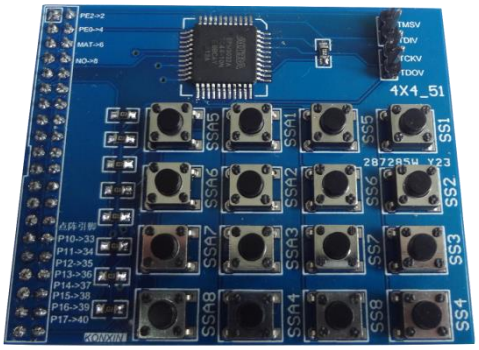


Figure 1-1 The physical picture of 4X4 matrix keypad

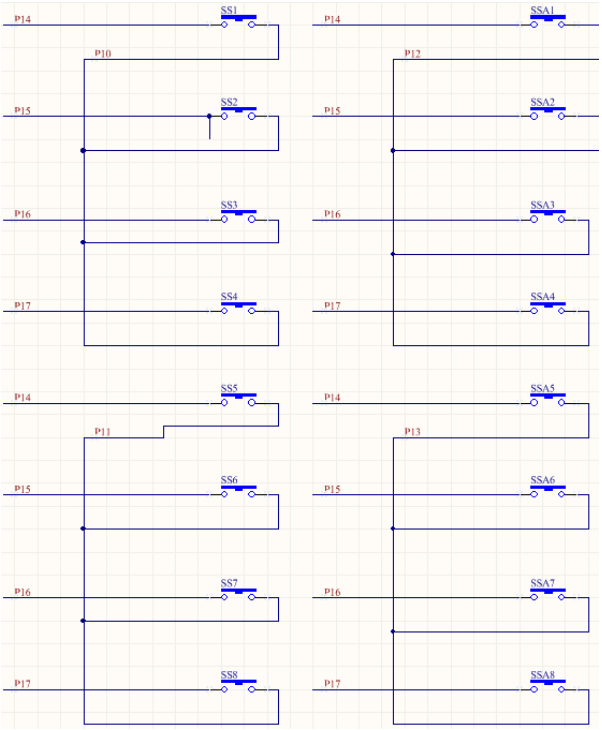


Figure 1-2 The schematic diagram of matrix keypad

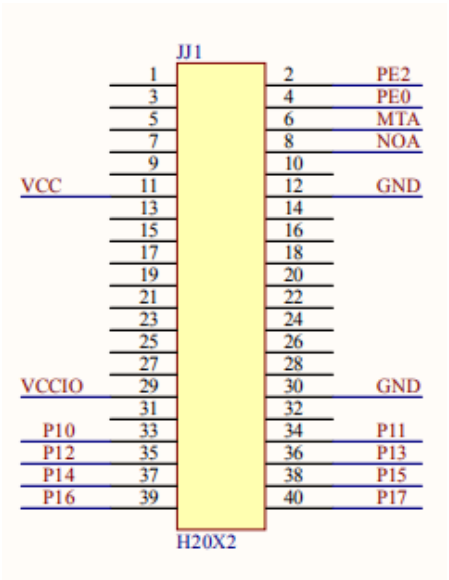


Figure 1-3 The interface diagram of matrix keypad

It is worth noting that pin 2, 4, 6 and 8 corresponds to PE2, PE0, MIA and NOA, which are four pins on CPLD 3032. Thus, before we use the chip CPLD3032, we need to lock those four pins first.

2. Extension Module for WIFI

Figure 2-1 is the physical picture of WIFI module, XLW-210. Detailed information and experiments related to WIFI module are in the folder “DEMO/24_8051_R2WiFi_XLW210A”. Figure 2-2 is the interface diagram

connecting with WIFI module and extension port. Pin TXD_B and RTD_B are used for data communication. In addition, there is a 10-pin female header on the right side of expansion port, as shown in figure 2-1. It can be used for connecting external ultrasonic module. The manual materials and experiments are also provided, and users can order by themselves.

Figure 2-1 WIFI

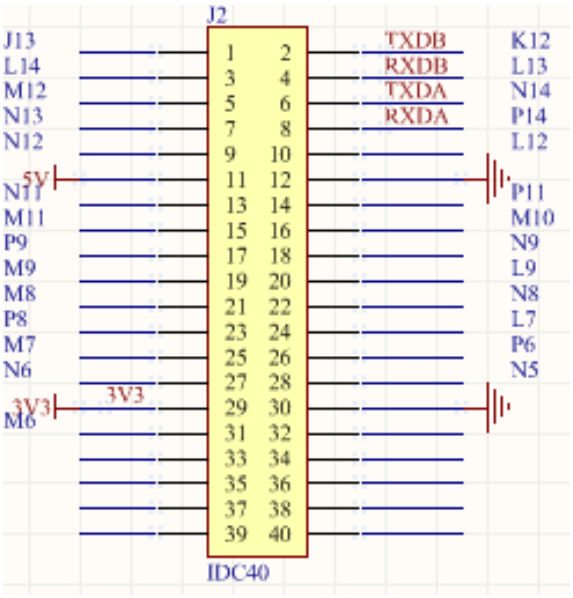


Figure 2-2 The interface diagram of WIFI

3. Extension Module for Network Interface Card

Figure 3-1 is the physical picture of network interface card (NIC). It carries controller chip W5200, and the schematic diagram is shown in figure 3-3. Detailed information and experiments related to network interface card are in the folder "DEMO/23_8051Core_W5200". As shown in the interface diagram of figure 3-2, pin MISO, MOSI, SCLK, INT, PWDN, SCS and RST corresponds to signal pin on the chip W5200.

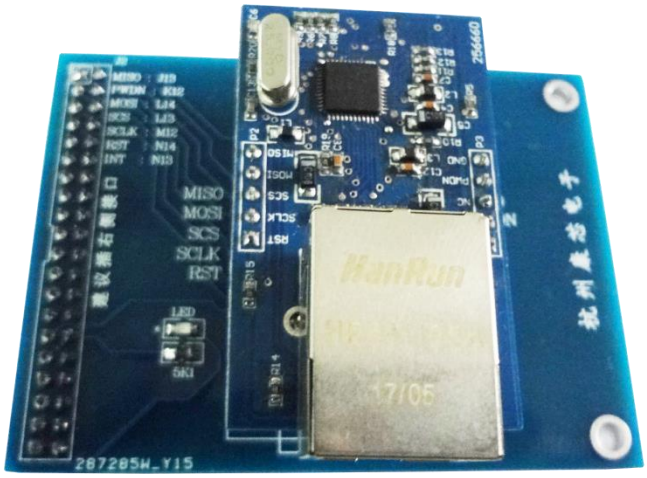


Figure 3-1 The physical picture of NIC

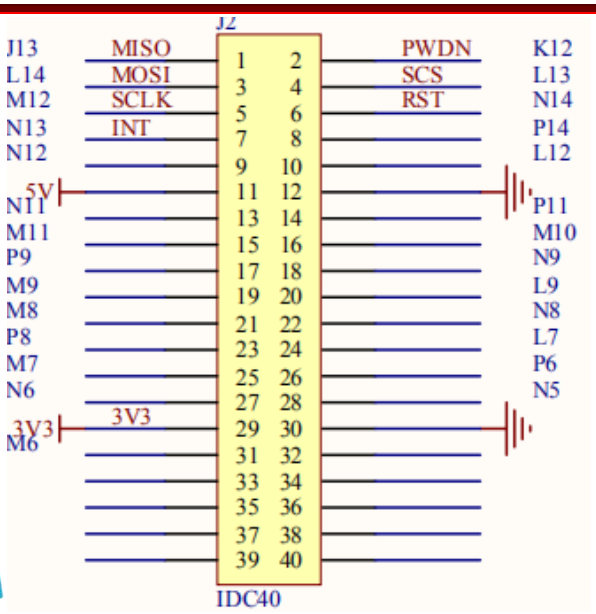


Figure 3-2 The interface diagram of NIC

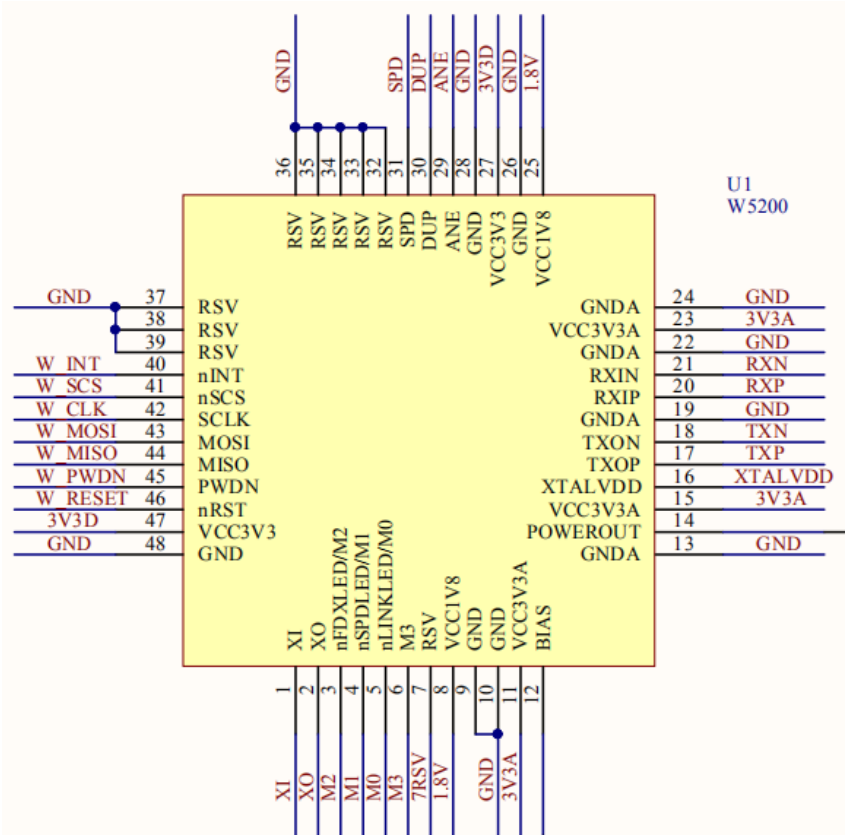
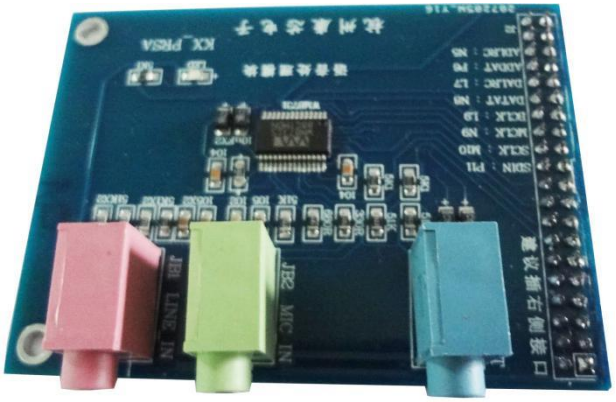


Figure 3-3 The schematic diagram of W5200

4. Extension Module for Speech Processing

Figure 4-1 is the physical picture of speech processing module. It carries an integrated headphone driver WM8731. On the development board, blue interface is the speech outlet, green interface is the microphone inlet, and pink interface is the speech inlet. Figure 4-2 is the interface diagram of speech processing module, and

figure 4-3 is the schematic diagram of WM8731. Pin SDIN, SCLK, MCLK, BCLK, DADAT, DALRC, ADDAT and ADLRC corresponds to signal pin on the chip WM8731.



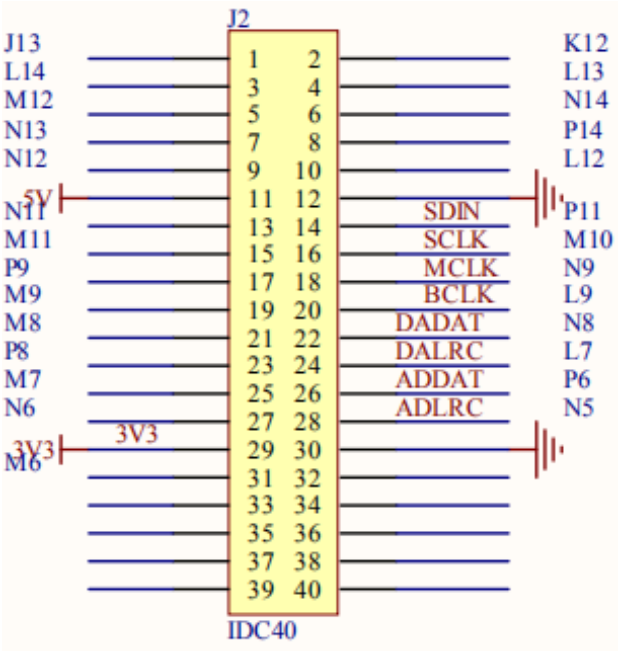


Figure 4-1 The speech processing module

Figure 4-2 The interface diagram of speech processing module

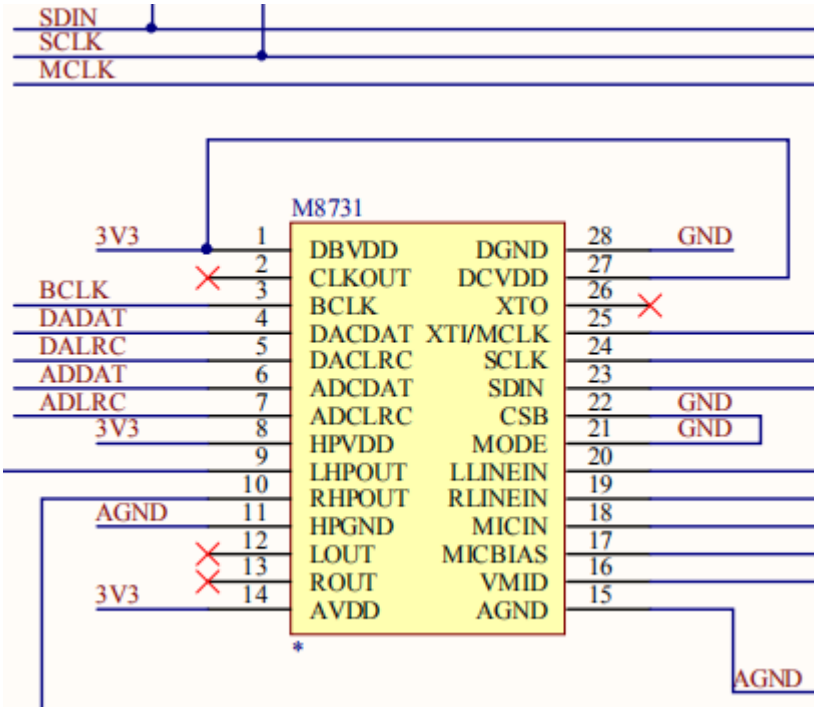


Figure 4-3 The schematic diagram of WM8731

5. Extension Module for HDMI Input

The HDMI input module carries the chip ADV7611, as shown in figure 5-1, to support all mandatory video formats. Since the user need not to configure the resolution, the difficulty of developing application programs is reduced. After

receiving the video signal through the HDMI input extension module, we can output the processed image signal through VGA port on the development board.

The resolution format supported by the extension module is shown as below:

720 × 480 (480P) Refresh Rate: 60Hz

640 × 480 (VGA) Refresh Rate: 60Hz

800 × 600 (SVGA) Refresh Rate: 60Hz

1024 × 768 (XGA) Refresh Rate: 60Hz

1280 × 720 (720P) Refresh Rate: 60Hz

1920 × 1080 (1080i) Refresh Rate: 60Hz

Detailed information and experiments related to the HDMI input module are in the folder "DEMO/19_HDMI_IN_OUT". Figure 5-2 is the interface diagram of HDMI input module.

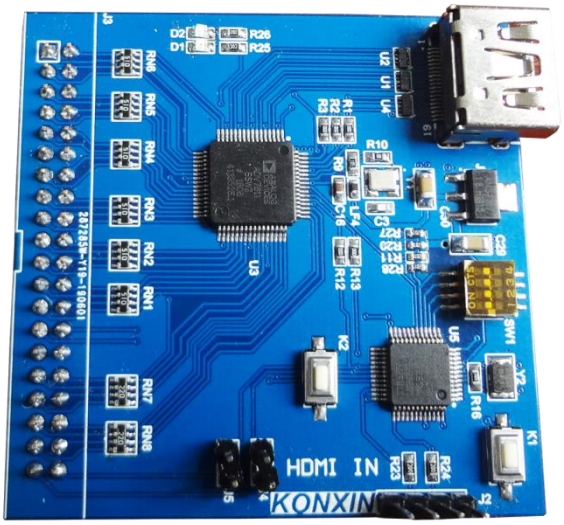


Figure 5-1 The physical picture of HDMI input module

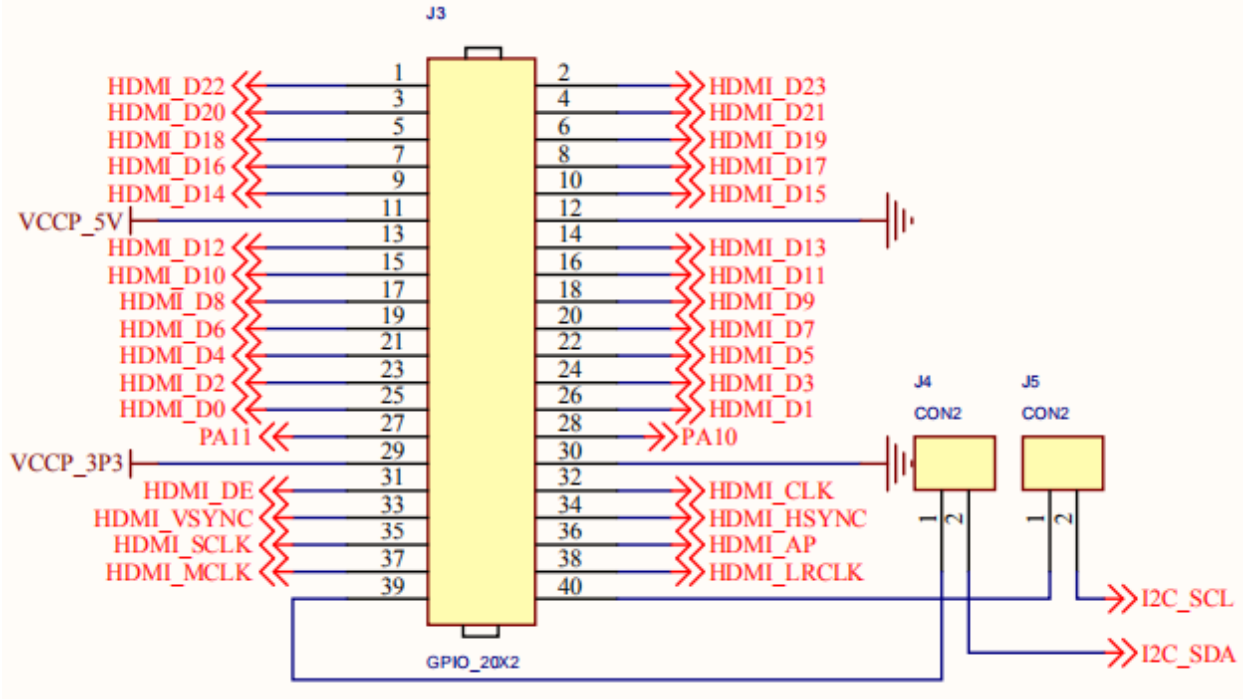


Figure 5-2 The interface diagram of HDMI input extension module

6. Extension Module for HDMI Output

The HDMI output module carries the chip Sil9022 to control the output mode, as shown in figure 6-1. Since the user need not to configure the resolution, the difficulty of developing application programs is reduced. The HDMI output module is responsible for

The resolution format supported by the extension module is shown as below:

720 × 480 (480P) Refresh Rate: 60Hz

640 × 480 (VGA) Refresh Rate: 60Hz

800 × 600 (SVGA) Refresh Rate: 60Hz

1024 × 768 (XGA) Refresh Rate: 60Hz

1280 × 720 (720P) Refresh Rate: 60Hz

1920 × 1080 (1080i) Refresh Rate: 60Hz

Detailed information and experiments related to the HDMI output module are in the folder "DEMO/19_HDMI_IN_OUT". Figure 602 is the interface diagram of HDMI output module.

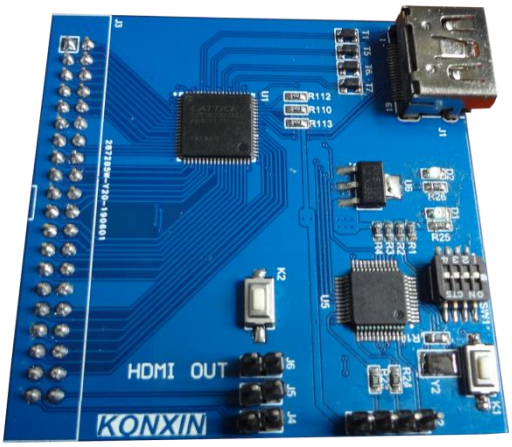


Figure 6-1 The physical picture of HDMI output module
Figure 6-2 The interface diagram of HDMI output module

7. Extension Module for 12 Bit Parallel ADC/DAC

The ADC extension module carries 12-bit AD807 and its sampling rate is 50MHz. The analog output port is on the position of red cap, as shown in figure 7-1, the pin AD_IN indicates the collection port and the pin AGND is the ground plane port. The DAC extension module carries 12-bit DA902 and its transferring rate is 165MHz. The analog input port is on the position of red cap, as shown in figure 7-2, the pin DA_OUT indicates the output port and the pin AGND is the ground plane port. As shown in figure 7-3, the ADC module and the DAC module can be stacked together to connect one side of extension port. Figure 7-4 is the schematic diagram of AD807 and figure 7-5 is the schematic diagram of DA902. As shown in figure 7-6, pin AD_D0-AD_D11, DA_D0-DA_D11 and AD_CLK, DA_CLK are data pins and clock pins respectively. Detailed information and experiments related to this extension module are in the folder “DEMO/18_adda_direct”.

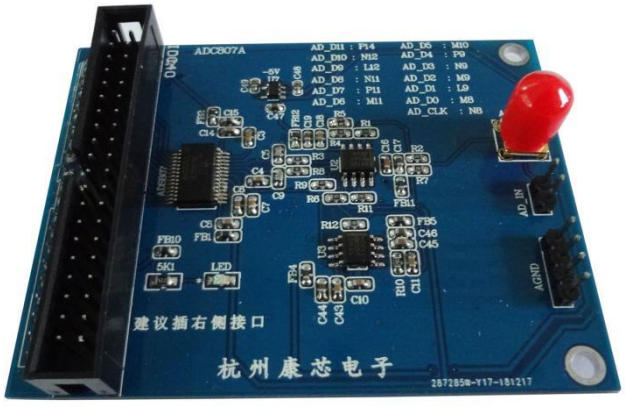


Figure 7-1 The physical picture of AD807

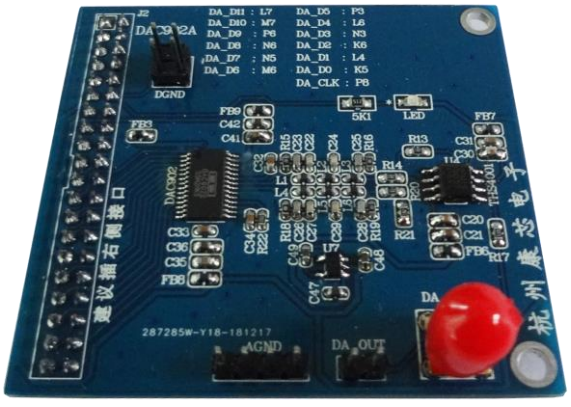


Figure 7-2 The physical picture of DAC902

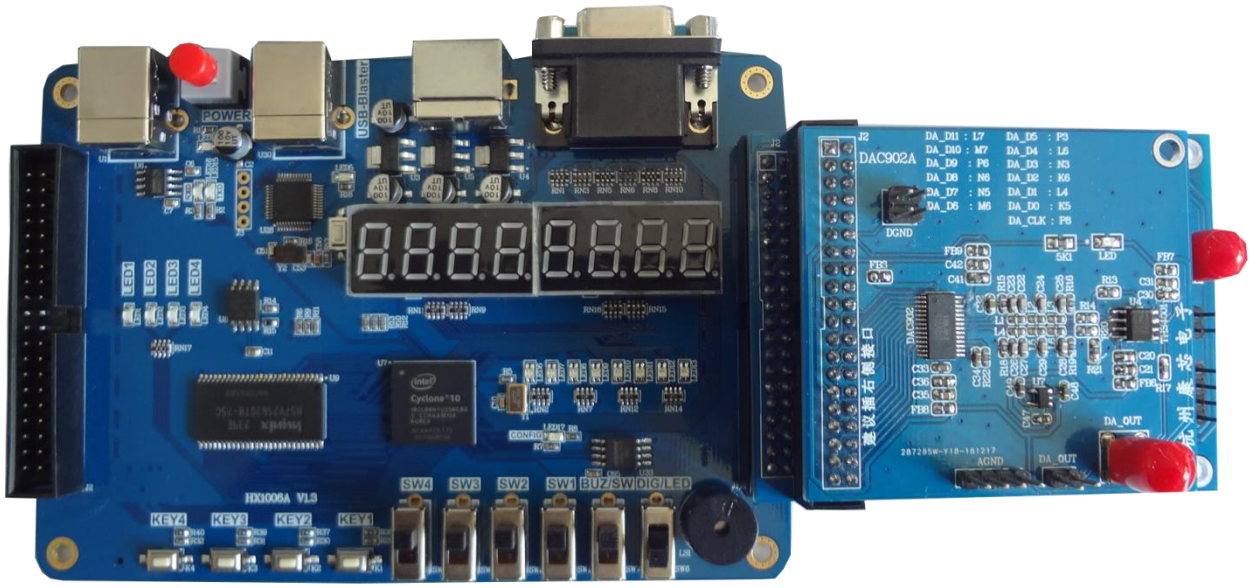


Figure 7-3 The physical picture of two extension module superimposed

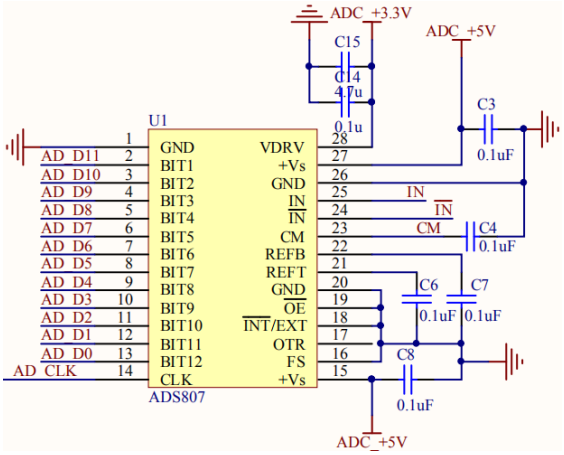


Figure 7-4 The schematic diagram of AD807

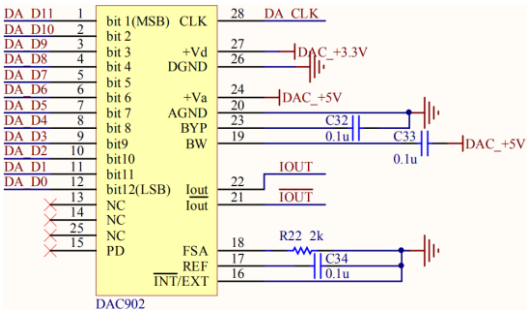


Figure 7-5 The schematic diagram of DA902

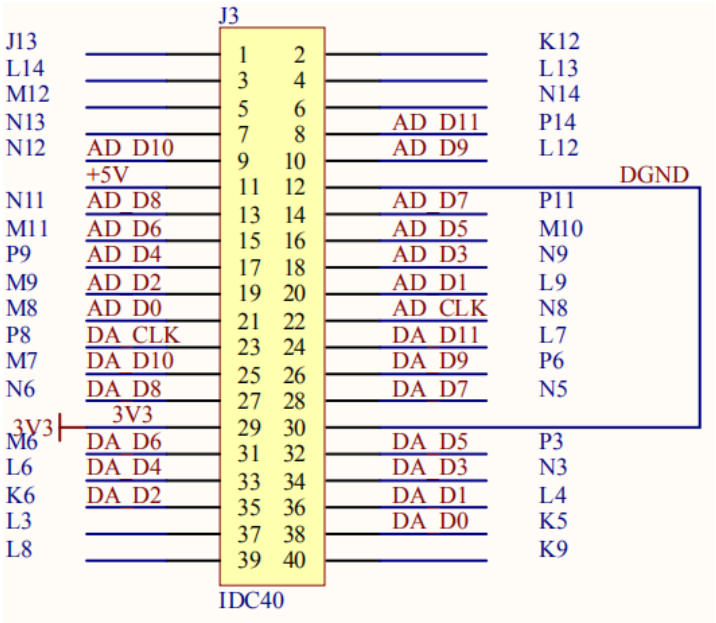


Figure 7-6 The interface diagram of DAC/ADC extension module

康芯科技

名称：杭州康芯电子有限公司
地址：杭州市拱墅区祥茂路16号
网址：WWW.KX-SOC.COM
电话：0571-88914587
邮编：310010