CSCI 2500 Homework 6

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November 29, 2021

1. Problem 4.7

a) Data path of R-type instruction: Register Read $\rightarrow$ $I-Mem$ $\rightarrow$ $Register\ File$ $\rightarrow$ MUX $\rightarrow$ ALU $\rightarrow$ MUX $\rightarrow$ $Register\ Setup$
Latency of R-type of instruction $= 30 + 250 + 150 + 25 + 200 + 25 + 20 = \boxed{700\ ps}$

b) Data path of lw instruction : $Register\ Read$ $\rightarrow$ $I-Mem$ $\rightarrow$ $Register\ File$ $\rightarrow$ MUX $\rightarrow$ ALU $\rightarrow$ $D-Mem$ $\rightarrow$ MUX $\rightarrow$ $Register\ Setup$
Latency of lw instruction $= 30 + 250 + 150 + 25 + 200 + 250 + 25 + 20 = \boxed{950\ ps}$

c) Data path of sw instruction : $Register\ Read$ $\rightarrow$ $I-Mem$ $\rightarrow$ $Register\ File$ $\rightarrow$ ALU $\rightarrow$ MUX $\rightarrow$ $D-Mem$
Latency of sw instruction $= 30 + 250 + 150 + 200 + 25 + 250 = \boxed{905\ ps}$

d) Data path of beq instruction : $Register\ Read$ $\rightarrow$ $I-Mem$ $\rightarrow$ $Register\ File$ $\rightarrow$ MUX $\rightarrow$ ALU $\rightarrow$ $Single\ gate$ $\rightarrow$ MUX $\rightarrow$ $Register\ Setup$
Latency of beq instruction $= 30 + 250 + 150 + 25 + 200 + 5 + 25 + 20 = \boxed{705\ ps}$

e) Data path of arithmetic, logical, or $shift-I-type\ (non-load)$ *instruction* : $Register\ Read$ $\rightarrow$ $I-Mem$ $\rightarrow$ $Register\ File$ $\rightarrow$ MUX $\rightarrow$ ALU $\rightarrow$ MUX $\rightarrow$ $Register\ Setup$
Latency of arithmetic, logical, or shift-I-type (non-load) instruction $= 30+250+150+25+200+5+25+20 = \boxed{700\ ps}$

f) The minimum clock period for this CPU is the longest latency needed to compute a type of instruction. In this case, it is for lw instructions.
Clock cycle for this CPU $= \boxed{950\ ps}$

2. Problem 4.10

a) Increasing the registers from 32 to 64 will reduce load and store instruction execution time by 12 percent. Given that lw (25 percent) and sw (11 percent) take up 36 percent, 0.12(0.36) = 4.32 percent. As we solved in problem 4.7 part f, the clock cycle is 950 ps. Increasing the registers from 32 to 64 will add an additional 10 ps latency (as the latency of the register file increases from 150 to 160 ps), resulting in an overall 960 ps clock cycle for the improved processor prior to factoring in the improvement for load and store instructions.
960 * 0.9568 = 918.528 ps
Speedup = 950/918.528 = $\boxed{1.03}$

b) The cost of the original CPU factors in I-Mem (1), register file (1), MUX (4), ALU (1), adder (2), D-Mem (1), sign extend (1), single gate (1), and control (1). The improved CPU costs 200 more as the register file cost increases from 200 to 400.
Original CPU cost = 1*1000 + 1*200 + 4*10 + 1*100 + 2*30 + 1*2000 + 1*100 + 1*1 + 1*500 = 4001
Improved CPU cost = 1*1000 + 1*400 + 4*10 + 1*100 + 2*30 + 1*2000 + 1*100 + 1*1 + 1*500 = 4201
200/4001 = 5 percent more expensive than the old CPU
$\boxed{\textit{For a 3 percent improvement in CPU performance, the cost of the CPU goes up by 5 percent}}$

c) If a client waits 1 minute on average to receive their queries and does not mind waiting a couple extra seconds using the slower CPU but really wants to save money, then it does not make sense to increase the registers. In contrast, if another client like Google really wants the best performance to make their search engine give results as fast as possible and will pay more for a better CPU, then it makes sense to build a better CPU with more money.

3. Problem 4.16

a) A non-pipelined processor's clock cycle is the sum of all the latencies in the table.
Non-pipelined clock cycle = IF + ID + EX + MEM + WB = 250 + 350 + 150 + 300 + 200 = $\boxed{1250\ ps}$
A pipelined processor's clock cycle is equal to the longest latency in the table, which in this case is the ID stage.
Pipelined clock cycle = ID = $\boxed{350\ ps}$

b) The lw instruction goes through all five stages. Each cycle in the non-pipelined processor executes one instruction.
Non-pipelined processor latency = $\boxed{1250\ ps}$
Pipelined processor latency = 5 cycles = 5(350) = $\boxed{1750\ ps}$

c) **We will split the stage with the longest latency, which is** $\boxed{ID}$ **in this case. Our new clock cycle for the pipelined processor is now from the MEM stage, which is** $\boxed{300\ ps}$**.**

d) Data memory is only utilized by lw and sw instructions.
Utilization of the data memory = 20 percent + 15 percent = $\boxed{35\ percent}$

e) The write-register port of the registers unit is used by the ALU and lw instruction.
Utilization of the write register port of the registers unit = 45 percent + 20 percent = $\boxed{65\ percent}$