7-Channel Relay and Inductive Load Sink Driver

Check for Samples: ULN2003V12

FEATURES

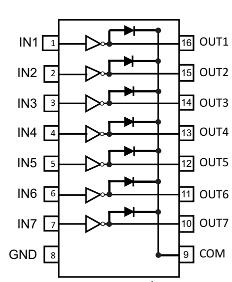
- **7-Channel High Current Sink Drivers**
- **Supports up to 20V Ouput Pull-up Voltage**
- **Supports Wide Range of Low and High Voltage Relays and Inductive Coils**
- **Low Output VOL of 0.6V (Typical) with**
  - **100mA (Typical) Current Sink per Channel at 3.3V Logic Input(1)**
  - **140mA (Typical) Current Sink per Channel at 5.0V Logic Input(1)**
- **Compatible to 3.3V and 5.0V Micro-controllers and Logic Interface**
- **Internal Free-wheeling Diodes for Inductive Kick-back Protection**
- **Input Pull-down Resistors Allows Tri-stating the Input Driver**
- **Input RC-Snubber to Eliminate Spurious Operation in Noisy Environment**
- **Low Input and Output Leakage Currents**
- **Easy to use Parallel Interface**
- **ESD Protection Exceeds JESD 22**
  - **2kV HBM, 500V CDM**
- **Available in 16-pin SOIC and TSSOP Packages**

(1) Total current sink may be limited by the internal junction temperature, absolute maximum current levels etc - refer to the Electrical Specifications section for details.

APPLICATIONS

- **Relay and Inductive Load Driver in Various Telecom, Consumer, and Industrial Applications**
- **Lamp and LED Displays**
- **Logic Level Shifter**

Functional Diagram



DESCRIPTION

The ULN2003V12 is a low power upgrade of TI's popular ULN2003 family of 7-channel Darlington transistor array. The ULN2003V12 sink driver features 7 low output impedance drivers that minimize on-chip power dissipation. When driving a typical 12V relay coil a ULN2003V12 will dissipate up to 12 times lower power than an equivalent ULN2003A. The ULN2003V12 driver is pin-to-pin compatible with ULN2003 family of devices in similar packages.

The ULN2003V12 supports 3.3V to 5V CMOS logic input interface thus making it compatible to a wide range of micro-controllers and other logic interfaces. The ULN2003V12 features an improved input interface that minimizes the input DC current drawn from the external drivers. The ULN2003V12 features an input RC snubber that greatly improves its performance in noisy operating conditions. The ULN2003V12 channel inputs feature an internal input pull-down resistor thus allowing input logic to be tri-stated. The ULN2003V12 also supports other logic input levels, e.g. TTL and 1.8V; see typical characteristics section for details.

As shown in the Functional Diagram, each output of the ULN2003V12 features an internal free-wheeling diode connected in a common-cathode configuration at the COM pin.

The ULN2003V12 provides flexibility of increasing current sink capability through combining several adjacent channels in parallel. Under typical conditions the ULN2003V12 can support up to 1.0A of load current when all 7-channels are connected in parallel.

The ULN2003V12 can also be used in a variety of other applications requiring a sink drivers. The ULN2003V12 is available in 16-pin SOIC and 16-pin TSSOP packages.

Table 1. ULN2003V12 Function Table(1)

INPUT (IN1 – IN7)	OUTPUT (OUT1–OUT7)
L	$H^{+(2)}$
H	L
Z	$H^{+(2)}$

(1) L = Low-level (GND); H= High-level; Z= High-impedance;
(2) H^+ = Pull-up-level

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PART NUMBER	PACKAGE		TOP-SIDE MARKING
–40°C to 125°C	ULN2003V12DR	16-Pin SOIC	Reel of 2500	U2003V12
	ULN2003V12PWR	16-Pin TSSOP	Reel of 2000	U2003V12

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Specified at T_J = –40°C to 125°C unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
V_{IN}	Pins IN1- IN7 to GND voltage		–0.3	5.5	V
V_{OUT}	Pins OUT1 – OUT7 to GND voltage			20	V
V_{COM}	Pin COM to GND voltage			20	V
I_{GND}	Max GND-pin continuous current (100ºC < T_J < +125°C)			700	mA
	Max GND-pin continuous current (T_J < +100°C)			1.0	A
P_D	Total device power dissipation at T_A = 85°C	16 Pin - SOIC		0.86	W
		16 Pin - TSSOP		0.68	W
ESD	ESD Rating – HBM			2	kV
	ESD Rating – CDM			500	V
T_J	Operating virtual junction temperature		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)(2)

BOARD	PACKAGE	θ_{JC}	θ_{JA}(3)	DERATING FACTOR ABOVE T_A = 25ºC	T_A < 25°C	T_A = 70°C	T_A = 85°C	T_A = 105°C
High-K	16-Pin SOIC	46°C/W	75°C/W	13.33 mW/ºC	1.66 W	1.06 W	0.86 W	0.59 W
High-K	16-Pin TSSOP	49°C/W	95°C/W	10.44 mW/ºC	1.31 W	0.84 W	0.68 W	0.47 W

(1) Maximum dissipation values for retaining device junction temperature of 150°C
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
(3) Operating at the absolute $T_{J\text{-}max}$ of 150°C can affect reliability– for higher reliability it is recommended to ensure T_J < 125°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
V_{OUT}	Channel off-state output pull-up voltage				16	V
V_{COM}	COM pin voltage				16	V
$I_{OUT(ON)}$	Per channel continuous sink current	VINx = 3.3V			100(1)	mA
		VINx = 5.0V			140(1)	mA
T_J	Operating junction temperature		–40		125	ºC

(1) 1) Refer to ABSOLUTE MAXIMUM RATINGS for T_J dependent absolute maximum GND-pin current

ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range T_J = –40°C to 125°C and over recommended operating conditions unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUTS IN1 THROUGH IN7 PARAMETERS						
$V_{I(ON)}$	IN1–IN7 logic high input voltage	$V_{pull\text{-}up}$ = 3.3 V, $R_{pull\text{-}up}$ = 1 kΩ, I_{OUTX} = 3.2 mA	1.65			V
$V_{I(OFF)}$	IN1–IN7 logic low input voltage	$V_{pull\text{-}up}$ = 3.3 V, $R_{pull\text{-}up}$ = 1 kΩ, (I_{OUTX} < 20 µA)			0.6	
$I_{I(ON)}$	IN1–IN7 ON state input current	$V_{pull\text{-}up}$ = 12 V, VIN_x = 3.3 V		12	25	uA
$I_{I(OFF)}$	IN1–IN7 OFF state input leakage	$V_{pull\text{-}up}$ = 12 V, VIN_x = 0 V			250	nA
OUTPUTS OUT1 THROUGH OUT7 PARAMETERS						
$V_{OL(VCE\text{-}SAT)}$	OUT1–OUT7 low-level output voltage	V_{INX} = 3.3 V, I_{OUTX} = 20 mA		0.12	0.15	V
		V_{INX} = 3.3 V, I_{OUTX} = 100 mA		0.60	0.75	
		V_{INX} = 5.0 V, I_{OUTX} = 20 mA		0.09	0.11	
		V_{INX} = 5.0 V, I_{OUTX} = 140 mA		0.60	0.75	
$I_{OUT(ON)}$	OUT1–OUT7 ON-state continuous current(1) (2) at V_{OUTX} = 0.6V	V_{INX} = 3.3 V, V_{OUTX} = 0.6 V	80	100		mA
		V_{INX} = 5.0 V, V_{OUTX} = 0.6 V	95	140		
$I_{OUT(OFF)(ICEX)}$	OUT1–OUT7 OFF-state leakage current	V_{INX} = 0 V, V_{OUTX} = V_{COM} = 16 V		0.5		µA
SWITCHING PARAMETERS(3) (4)						
t_{PHL}	OUT1–OUT7 logic high propagation delay	V_{INX} = 3.3V, $V_{pull\text{-}up}$ = 12 V, $R_{pull\text{-}up}$ = 1 kΩ		50	70	ns
t_{PLH}	OUT1–OUT7 logic low propagation delay	V_{INX} = 3.3V, $V_{pull\text{-}up}$ = 12 V, $R_{pull\text{-}up}$ = 1 kΩ		121	140	ns
$t_{CHANNEL}$	Channel to Channel delay	Over recommended operating conditions and with same test conditions on channels.		15	50	ns
R_{PD}	IN1–IN7 input pull-down Resistance		210k	300k	390k	Ω
ζ	IN1–IN7 Input filter time constant			9		ns
C_{OUT}	OUT1–OUT7 output capacitance	V_{INX} = 3.3 V, V_{OUTX} = 0.4 V		15		pF
FREE-WHEELING DIODE PARAMETERS(5) (4)						
VF	Forward voltage drop	$I_{F\text{-}peak}$ = 140 mA, VF = V_{OUTx} – V_{COM}		1.2		V
$I_{F\text{-}peak}$	Diode peak forward current			140		mA

(1) The typical continuous current rating is limited by V_{OL}= 0.6V. Whereas, absolute maximum operating continuous current may be limited by the Thermal Performance parameters listed in the Dissipation Rating Table and other Reliability parameters listed in the Recommended Operating Conditions Table.
(2) Refer to the Absolute Maximum Ratings Table for T_J dependent absolute maximum GND-pin current.
(3) Rise and Fall propagation delays, t_{PHL} and t_{PLH}, are measured between 50% values of the input and the corresponding output signal amplitude transition.
(4) Guaranteed by design only. Validated during qualification. Not measured in production testing.
(5) Not rated for continuous current operation – for higher reliability use an external freewheeling diode for inductive loads resulting in more than specified maximum free-wheeling. diode peak current across various temperature conditions

DEVICE INFORMATION

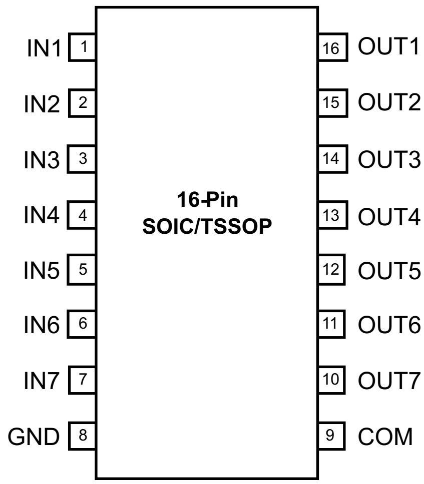


Figure 1. ULN2003V12 PINOUT

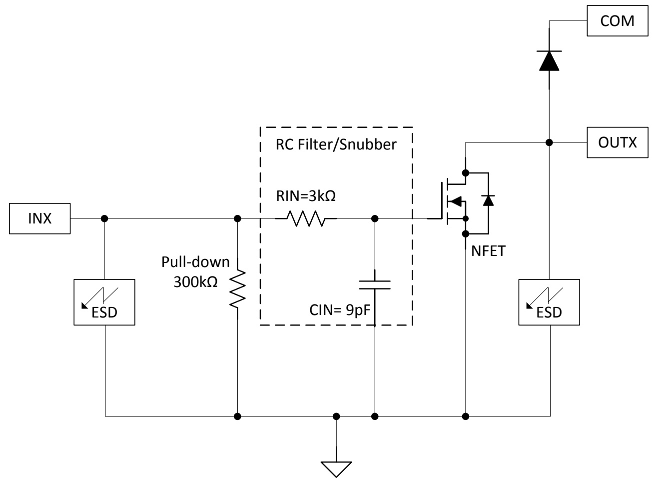


Figure 2. Channel Block Diagram

ULN2003V12 PIN DESCRIPTION

NAME	PIN NUMBER		DESCRIPTION
	16-SOIC	16-TSSOP	
IN1 – IN7	1–7	1–7	Logic Input Pins IN1 through IN7
GND	8	8	Ground Reference Pin
COM	9	9	Internal Free-Wheeling Diode Common Cathode Pin
OUT7 – OUT1	10–16	10–16	Channel Output Pins OUT7 through OUT1

APPLICATION INFORMATION

TTL and other Logic Inputs

ULN2003V12 input interface is specified for standard 3V and 5V CMOS logic interface. However, ULN2003V12 input interface may support other logic input levels as well. Refer to Figure 10 and Figure 11 to establish VOL and the corresponding typical load current levels for various input voltage ranges. Application Information section shows an implementation to drive 1.8V relays using ULN2003V12.

Input RC Snubber

ULN2003V12 features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1kΩ to 5kΩ resistor in series with the input to further enhance ULN2003V12's noise tolerance.

High-impedance Input Drivers

ULN2003V12 features a 300kΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the ULN2003V12 detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

On-chip Power Dissipation

Use the below equation to calculate ULN2003V12 on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. (1)

Thermal Reliability

It is recommended to limit ULN2003V12 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (2)

Improving Package Thermal Performance

The package θ_{JA} value under standard conditions on a High-K board is listed in the DISSIPATION RATINGS. θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

Application Examples

Inverting Logic Level Shifter

To use ULN2003V12 as an open-collector or an open-drain inverting logic level shifter configure the device as shown in Figure 3. The ULN2003V12's each channel input and output logic levels can also be set independently. When using different channel input and output logic voltages connect the ULN2003V12 COM pin to the maximum voltage.

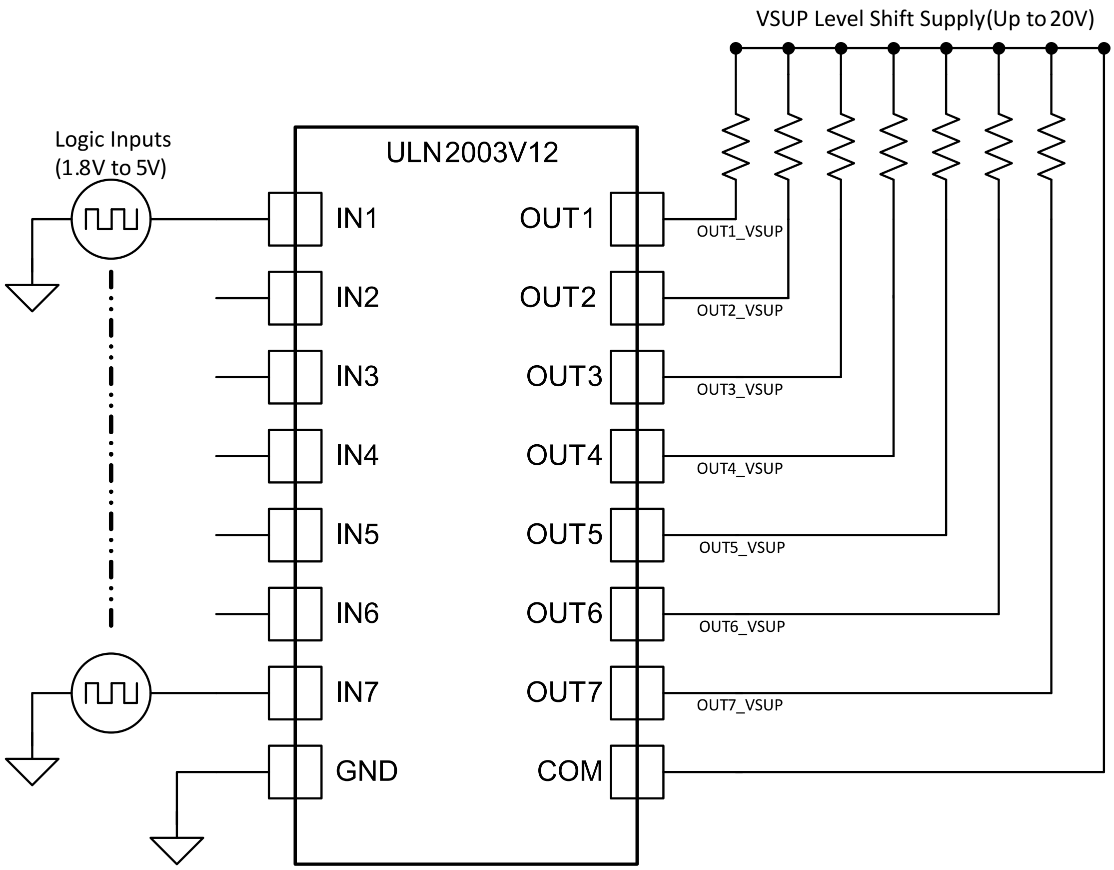


Figure 3. ULN2003V12 as Inverting Logic Level Shifter

Max Supply Selector

Figure 4 implements a max supply selector along with a 4-channel logic level shifter using a single ULN20003V12. This setup configures ULN2003V12's channel clamp diodes OUT5 – OUT7 in a diode-OR configuration and thus the maximum supply among VSUP1, VSUP2 and VSUP3 becomes available at the COM pin. The maximum supply is then used as a pull-up voltage for level shifters. Limit the net GND pin current to less than 100mA DC to ensure reliability of the conducting diode. The unconnected inputs IN5-IN7 are pulled to GND potential through 300kΩ internal pull-down resistor.

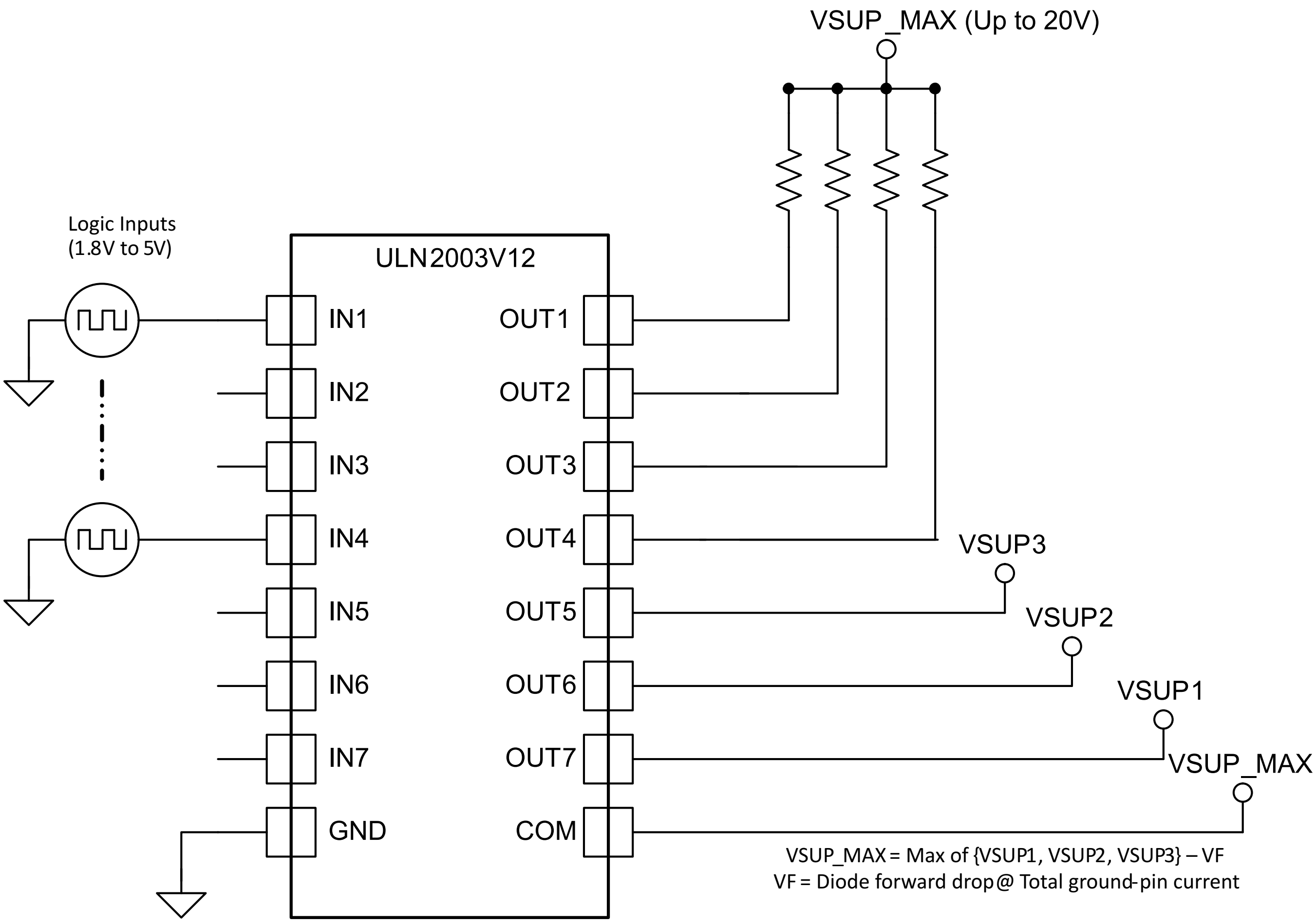


Figure 4. ULN2003V12 as Max Supply Selector

Constant Current Generation

When configured as per Figure 5 the ULN2003V12 outputs OUT1-OUT6 act as independent constant current sources. The current flowing through the resistor R1 is copied on all other channels. To increase the current sourcing connect several output channels in parallel. To ensure best current copying set voltage drop across connected load such that VOUTx matches to VOUT7.

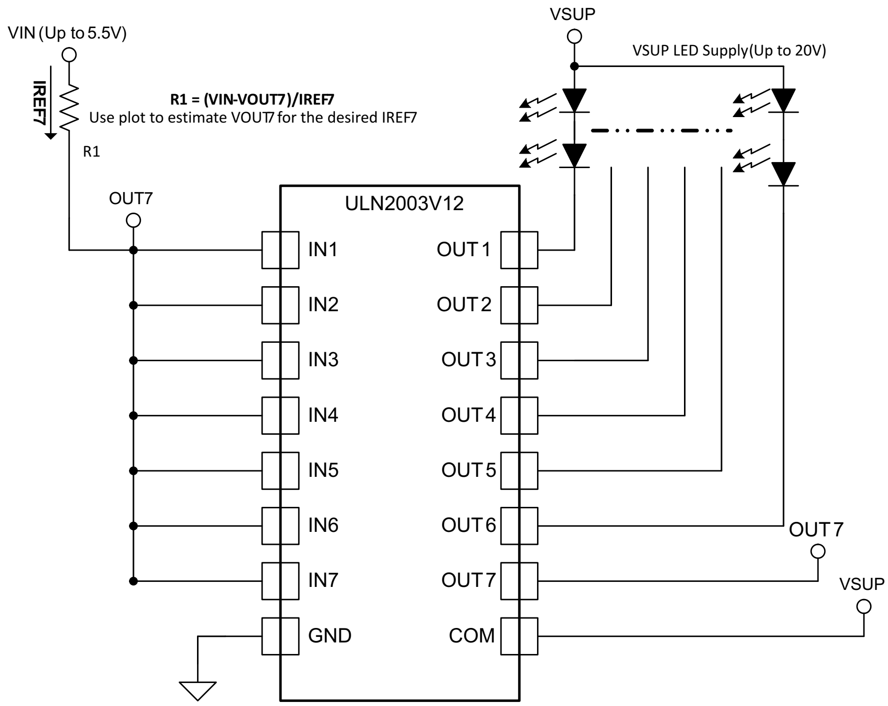


Figure 5. ULN2003V12 as a Constant Current Driver

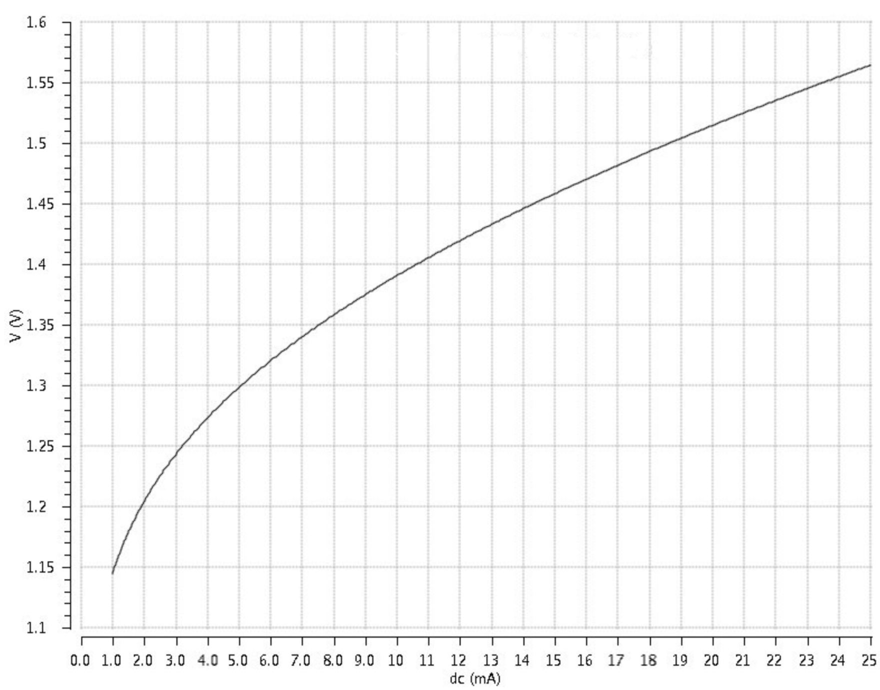


Figure 6. ULN2003V12 VOUT vs IREF

Unipolar Stepper Motor Driver

Figure 7 shows an implementation of ULN2003V12 for driving a uniploar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 300kΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins.

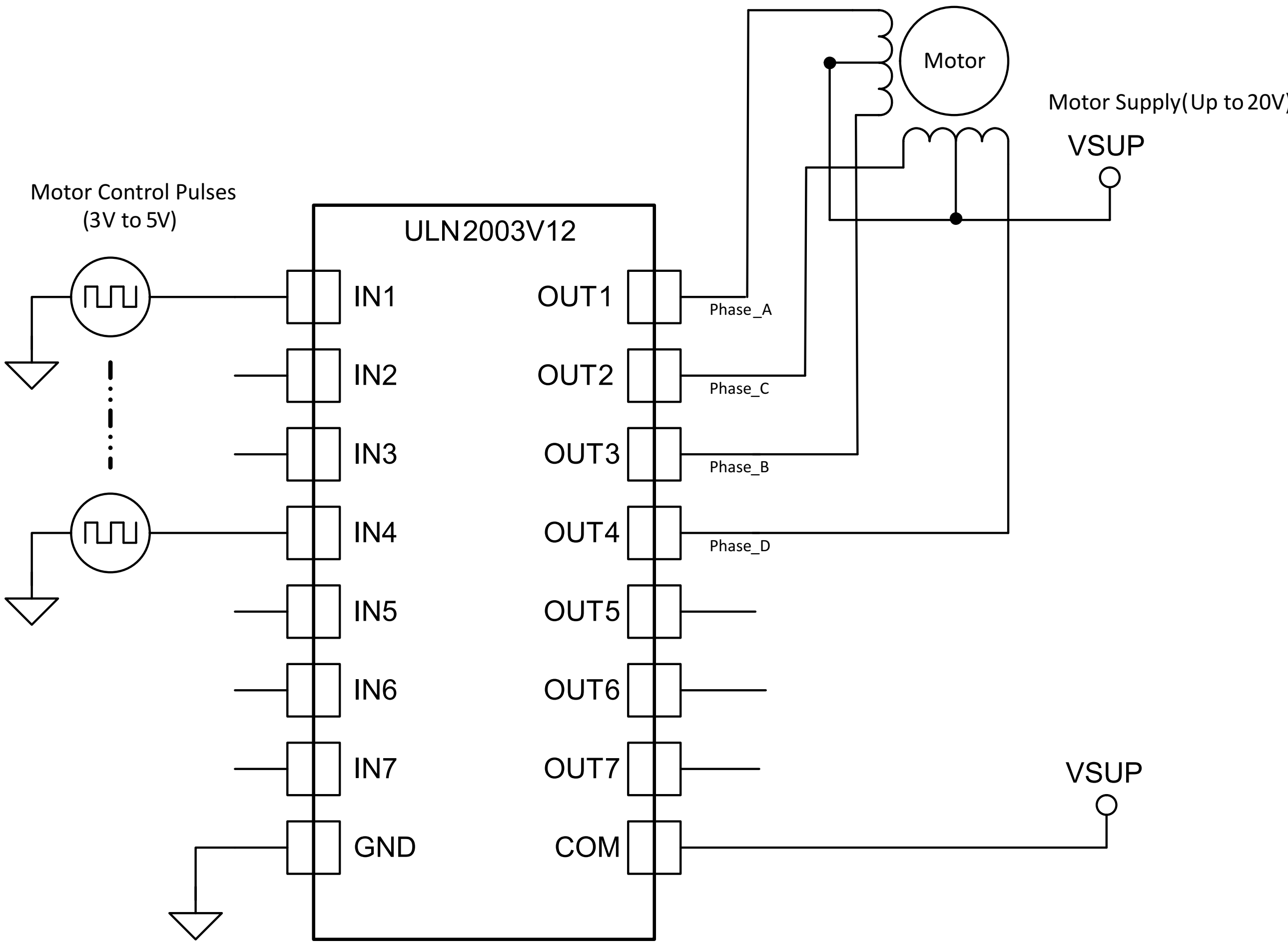


Figure 7. ULN2003V12 as a Stepper Motor Driver

NOR Logic Driver

Figure 8 shows a NOR Logic driver implementation using ULN2003V12. The output channels sharing a common pull-up resistor implement a logic NOR of the respective channel inputs. The LEDs connected to outputs OUT5-OUT7 light up when any of the inputs IN5-IN7 is logic-high (> VIH).

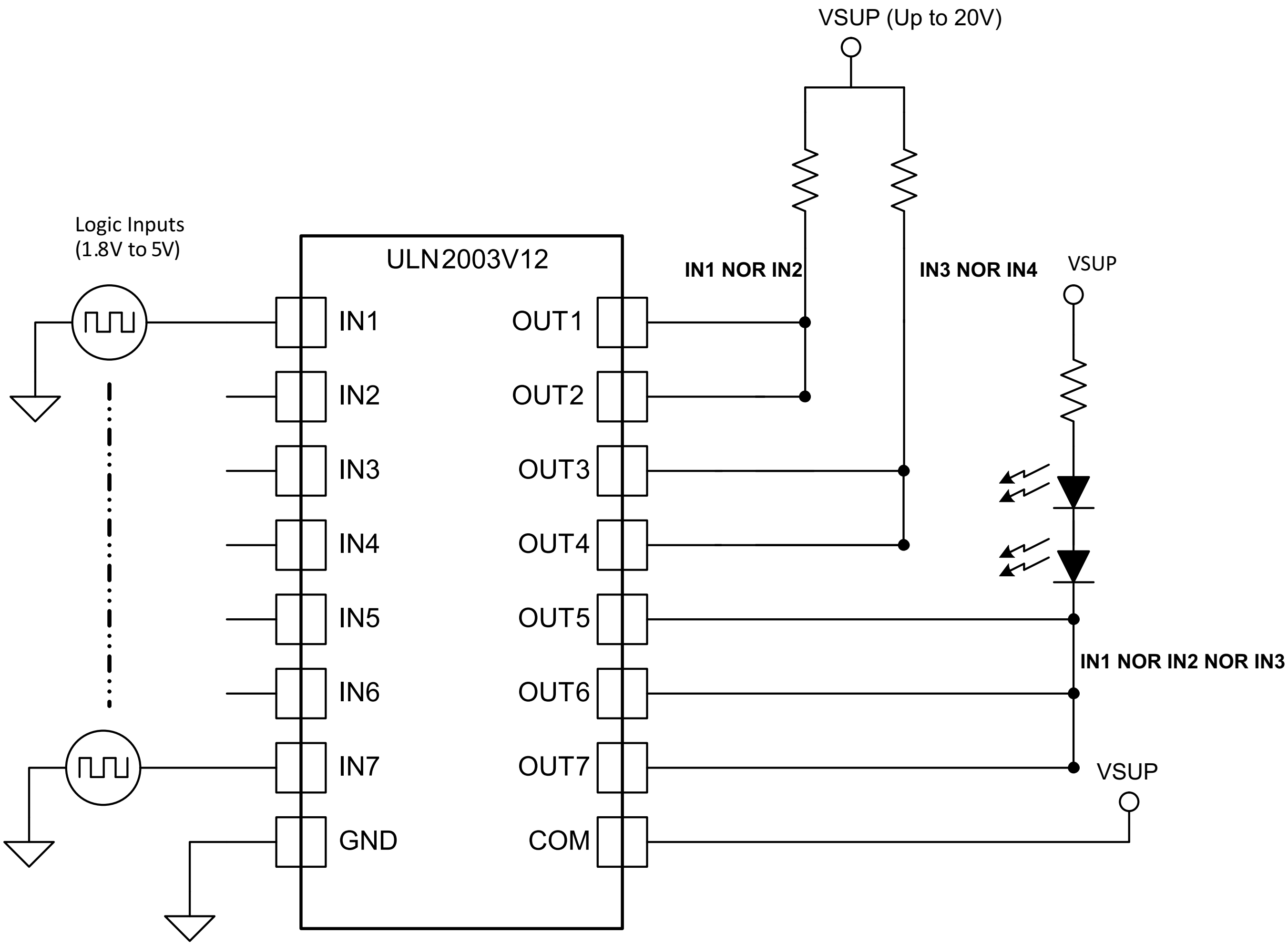


Figure 8. ULN2003V12 as a NOR driver

TYPICAL CHARACTERISTICS

T_A = +25ºC

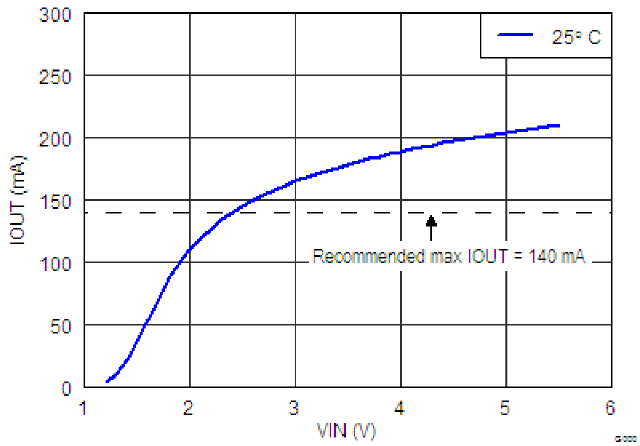


Figure 9. Load Current 1-Channel; VOL=0.6V

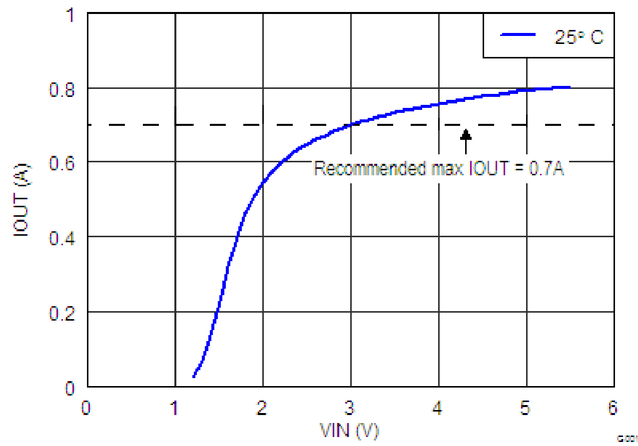


Figure 10. Load Current 7-Channels in parallel; VOL=0.6V

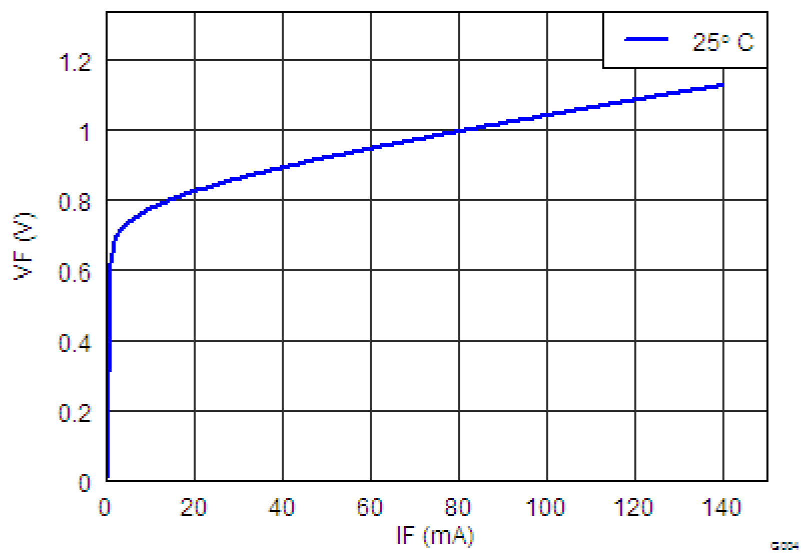


Figure 11. Freewheeling Diode VF versus IF

REVISION HISTORY

Changes from Revision A (July 2012) to Revision B **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ULN2003V12DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	Samples
ULN2003V12PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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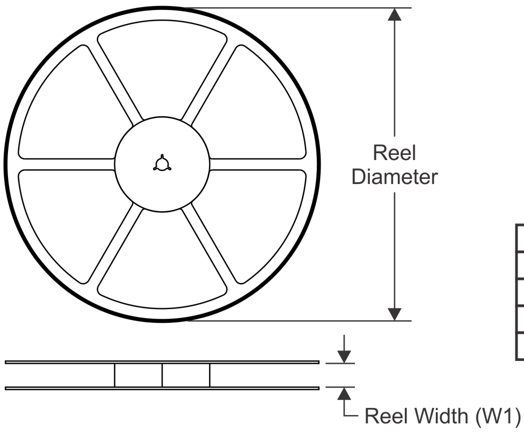
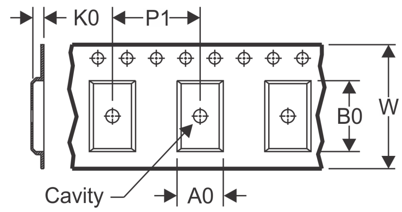
TAPE AND REEL INFORMATION

REEL DIMENSIONS

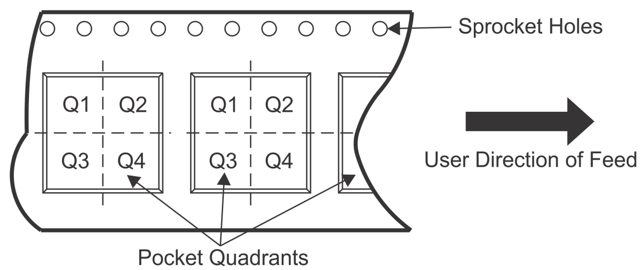


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

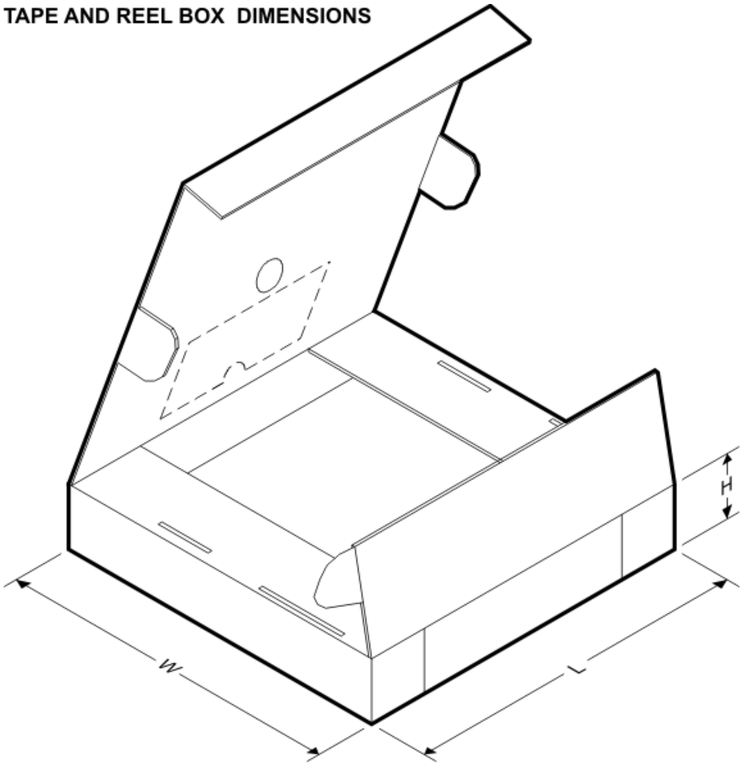
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003V12DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003V12PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

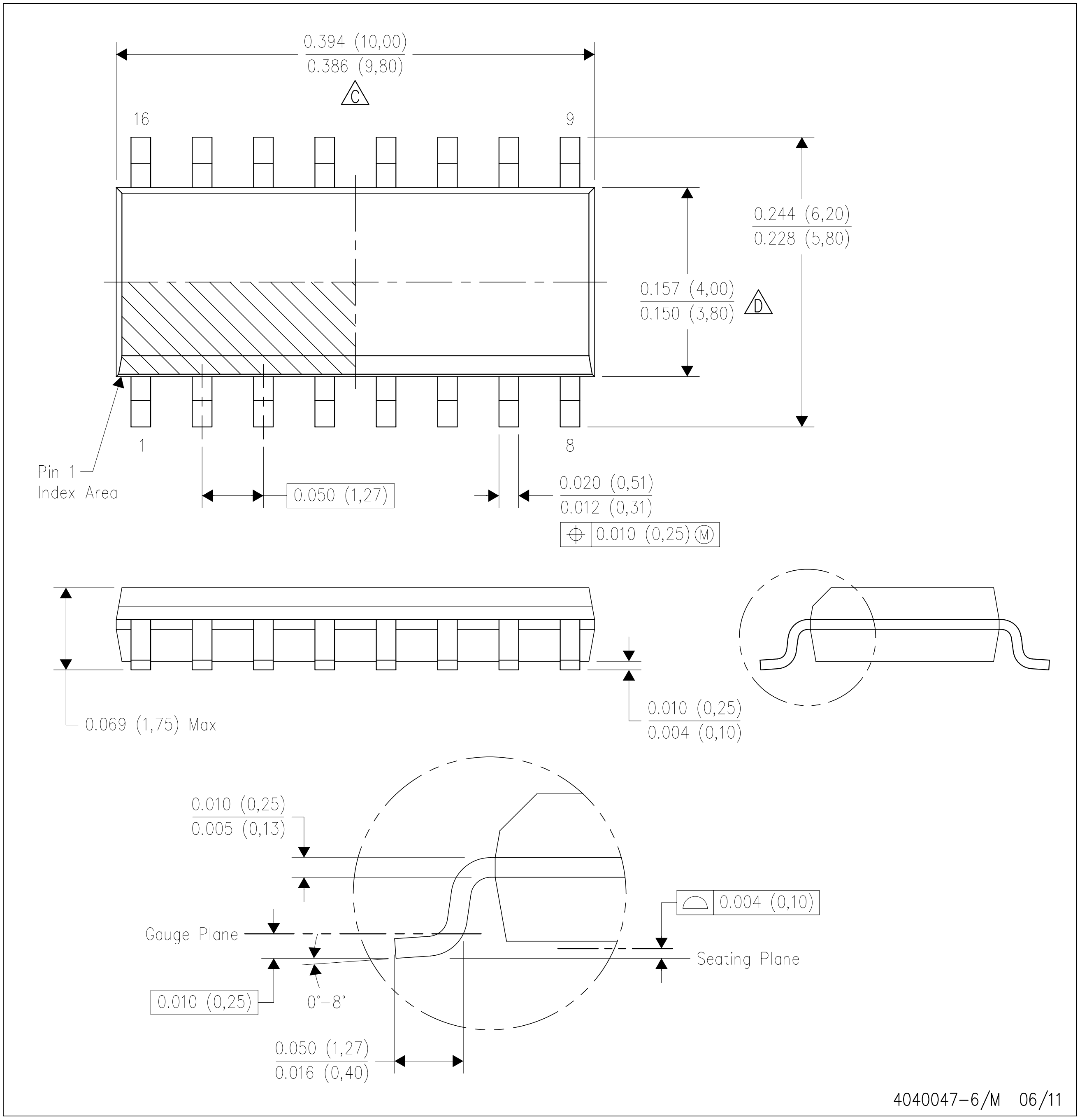
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

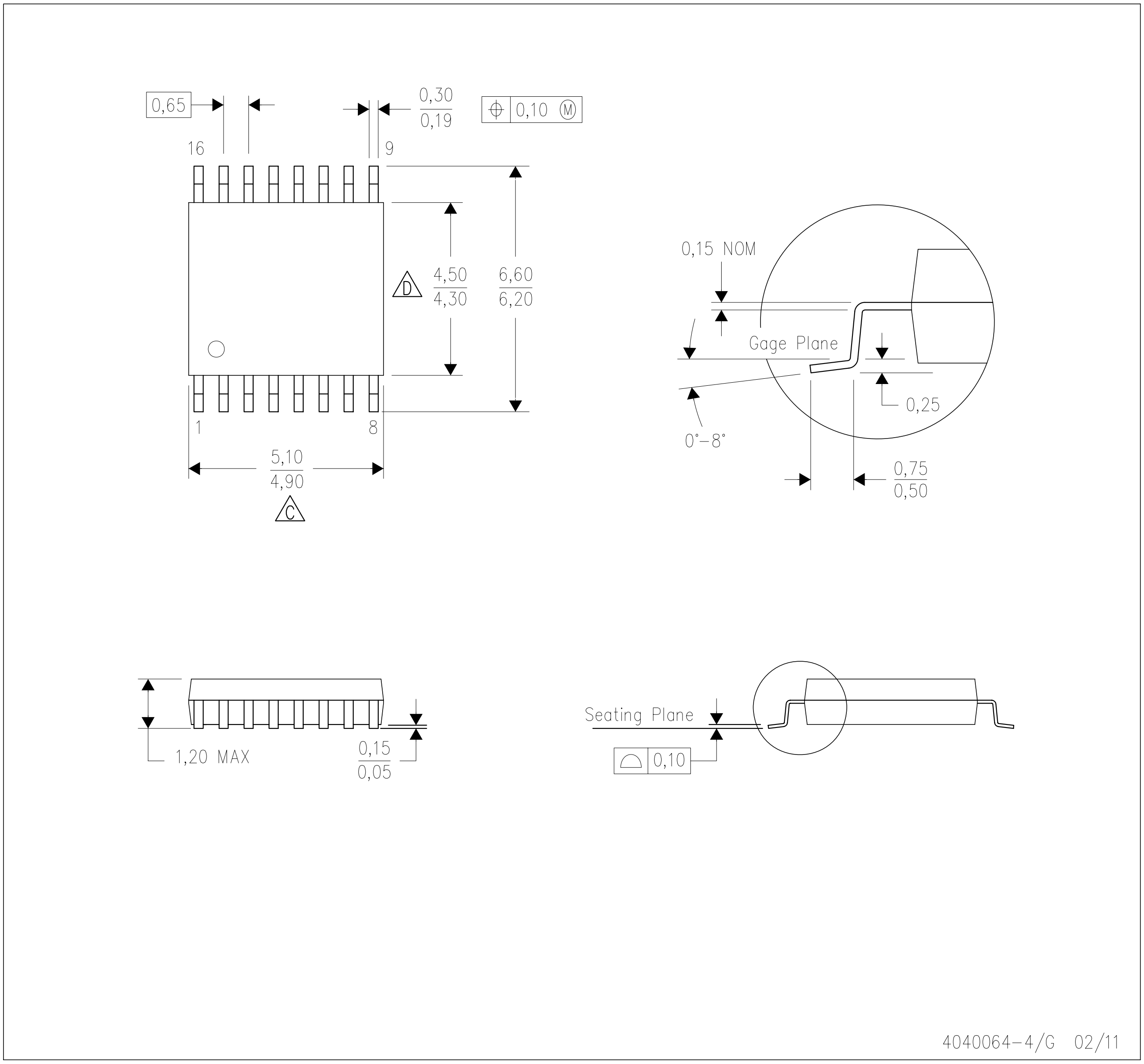
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003V12DR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003V12PWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



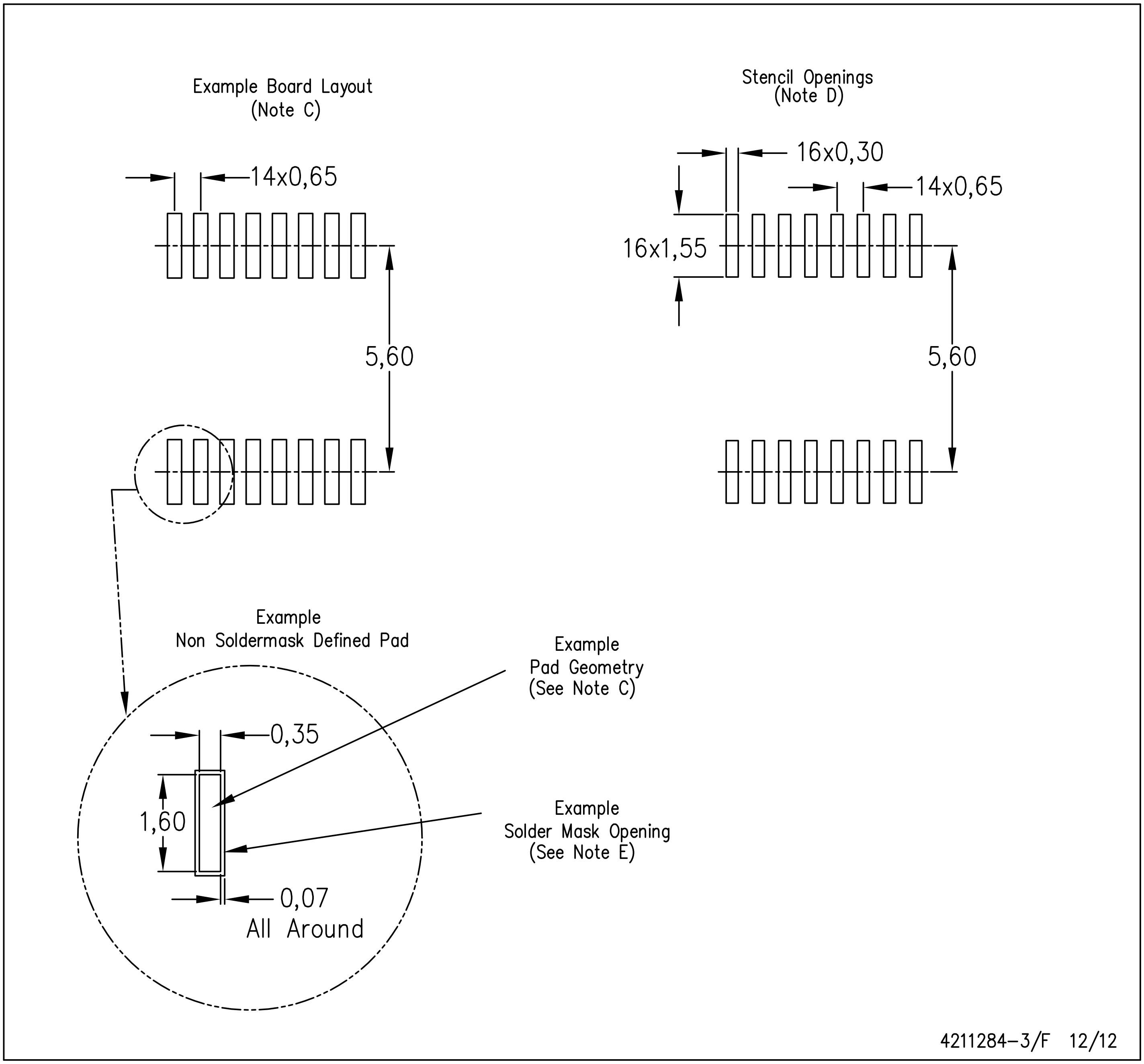
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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