Hermes Lite J16 Filter Control Proposal

This document will outline the current J16 implementation in the HPSDR server for ghpsdr3-alex, and make some proposals that enhance the capability to control different hardware from a common code base.

Document Version 1.2

Version Control

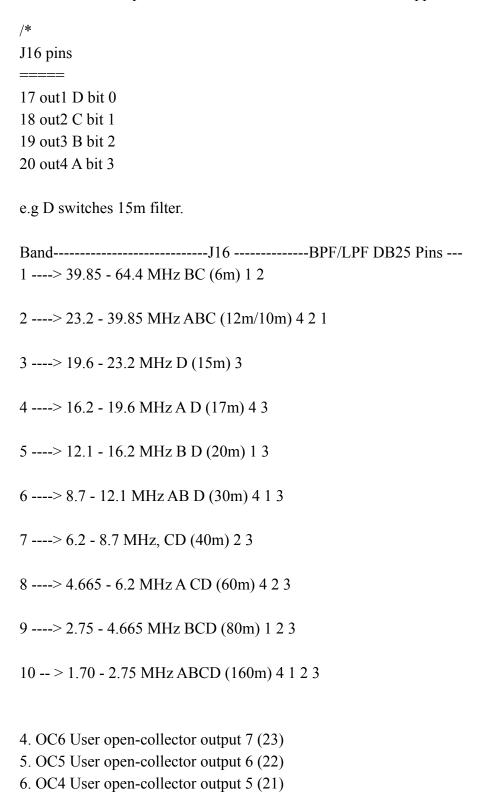
- 1.0 Initial document
- 1.1 update Superband data structure values
- 1.2 added Appendix A

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1.0 Comments and code from ozy.c

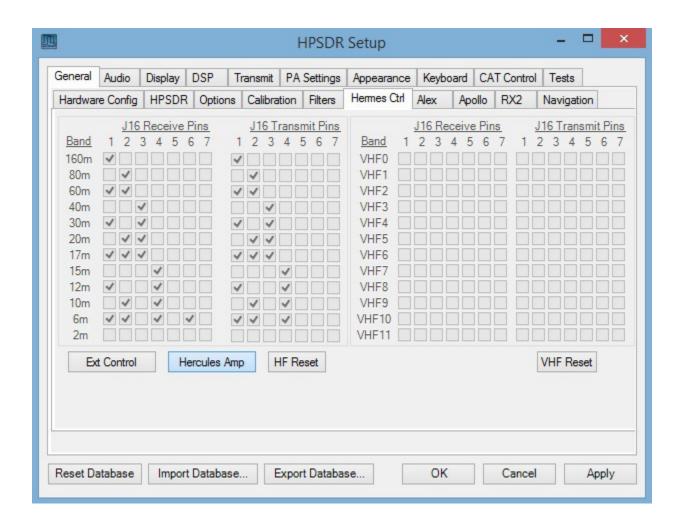
Here are some snips of code from the recent commit of J16 support into master at ghpsdr3-alex.



```
7. OC3 User open-collector output 4 (20)
8. OC2 User open-collector output 3 (19)
9. OC1 User open-collector output 2 (18).
 10. OC0 User open-collector output 1 (17)
*/
typedef struct filter j16 {
long f1;
long f2;
unsigned char j16;
 } filter_j16;
filter j16 fltj16 tbl [] =
  { 1700000, 2750000, 0x0f },
  \{2750000, 4665000, 0x07\},\
 { 4665000, 6200000, 0x0b },
  \{6200000, 8700000, 0x03\},\
  { 8700000, 12100000, 0x0d },
  \{12100000, 16200000, 0x05\},\
  \{ 16200000, 19600000, 0x09 \},
  \{19600000, 23200000, 0x01\},\
  { 23200000, 39850000, 0x0e },
  \{39850000, 64400000, 0x06\},\
#define ARRAY_SIZE(x) (sizeof(x)/sizeof(x[0]))
int get j16 from freq (long f)
int i;
for (i = 0; i < ARRAY SIZE(fltj16 tbl); ++i) {
if((f \ge flt_116_tbl[i].fl) && (f \le flt_11) & (f \le
fltj16_tbl[i].f2))
return fltj16 tbl[i].j16;
 }
return -1;
```

Note about implementation differences

Andrea implemented a fixed array that is the same for both TX and RX. PowerSDR provides 2 tables of values in a configuration dialog that provides flexible control of filters for both RX and TX as shown here:



The first 2 Hermes Lite PA designs do not need this feature. However we should consider implementing this to remain functionally compatible with other radio control applications. Otherwise we risk causing QtRadio to be excluded from controlling some future design that implements unique different encoding values for RX vs. TX.

2.0 Megaband Filter Design Overview

Here is a filter design overview for Megaband, the 160M to 10M 5W Power amplifier.

The filters are driven from an open collector BCD decoder. We use signals USEROUT0 thru USEROUT3 for the decode. This corresponds to the OC0 thru OC3 signals on J16. The board does not latch the filter data as is done in the Alex protocol. J16 has the capability of providing different filter encodes for receive and transmit enabled by the state of PTT. This is not necessary for Megaband. We designed the logic to use the same encoding values for receive and transmit to avoid having relays chattering between TX and RX.

This would be the data needed for Megaband.

```
Code Band
0000
     160
0001
     80
0010 60
0011
     40
0100 30
0101 20
0110
     17
0111
     15
1000 12
1001
    10
1010 - 1111 = Bypass
```

There are 6 LPFs for TX. We wire-OR the open collector outputs of the BCD decoder to select the appropriate LPF thru a relay switch circuit. Presenting an invalid (bypass) BCD encode causes all of the relays banks to be off, resulting in a bypass in the 160M relay to be active.

There are 5 BPFs for RX. We wire-OR the open collector outputs of the BCD decoder to select the appropriate BPF thru a diode switch circuit. Presenting an invalid (bypass) BCD encode causes all of the filter banks to be off, resulting in a bypass circuit comprised of a diode OR array to activate a bypass.

Thus, the array needs to look like this after being loaded by whatever schema we determine. The frequency values are chosen to align roughly with the RX BPF filter passbands, with some arbitrary splitting to enforce groupings by individual bands. Note that the 10M frequency span is larger than the actual band. This is to allow the use of a transverter for 2M to 10M to be used without causing a filter issue within mid-band.

```
{ 12100000, 17500000, 0x05 },

{ 17500000, 19600000, 0x06 },

{ 19600000, 23200000, 0x07 },

{ 23200000, 27500000, 0x08 },

{ 27500000, 32000000, 0x09 },

};
```

3.0 Superband Filter Design Overview

Here is a filter design overview for Superband, the 5W Power amplifier that provides user select-able BPFs to build at user discretion.

The BPFs cover 160, 80/75, 60/40, 30/20, 17/15 and 12/10 and the BPFs are shared for both RX and TX. These can be built and grouped in any combination, however the most likely groupings will be 160 with 80/75, 60/40 with 30/20 and 17/15 with 12/10. Those will be the groupings that I will document here.

The filters are driven from a single FPGA signal called USEROUT0. There is no open collector decoder provided since the board attaches directly into the PCI-E connector on Hermes Lite. The board does not latch the filter data as is done in the Alex protocol. J16 has the capability of providing different filter encodes for receive and transmit enabled by the state of PTT. This is not necessary for Superband. We designed the logic to use the same encoding values for receive and transmit.

This would be the data needed for Superband. Bank denotes the filter group as defined on the Superband schematic.

```
Code Band Bank #
0000 160
             1
             0
0001 80
0000 60
             1
0001
     40
             1
0000 30
             0
0001
     20
             0
0000 17
             1
     15
0001
             1
             0
0000
     12
0001
1010 - 1111 = none provided, will follow the state of the least significant bit.
```

Thus, the array needs to look like this after being loaded by whatever schema we determine.

```
filter j16 fltj16 tbl [] =
```

Appendix A - J16 Pin Numbering Confusion

**** High Performance Software Defined Radio Discussion List ****

J16 pin numbering confusion.

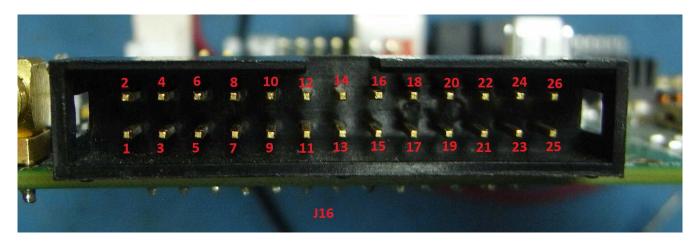
I still hear from users confused by the J16 schematic numbering scheme on both the Hermes, Angelia board KEYED IDC connectors and the Apache Labs ANAN-100 and ANAN-100D DB25 accessory port. Many of these users are using breakout boards with KEYED 26 pin IDC connectors and they cannot understand why the pinout on these boards differs from the J16 pinout found on the Hermes and Angelia schematics.

Both the assembled TAPR and Apache Labs Hermes boards were built with a 26 pin KEYED IDC connector installed on board, designated J16 on the schematics. IDC Pin 1 is clearly indicated on the top of the installed KEYED 26 pin IDC connector. Unfortunately, J16 KEYED IDC pin 1 actually corresponds with J16 pin 26 on the Hermes and Angelia schematics, hence the confusion for users who use KEYED industry standard IDC connectors for interconnection purposes.

Some time ago Kjell explained how the pin numbering confusion occurred, Nuff said about that. Hopefully, the following will lessen some confusion. BTW, much of the following information is from the ANAN-10 and ANAN-100 user docs. RTFM for more details.

Hermes_User_Manual_V1.17.pdf includes the following J16 note on page 14: IMPORTANT NOTE: The pin numbers may NOT correspond to individual cables within an IDC

ribbon cable. In particular, ex PC IDC cables do NOT match the pin-outs shown in the photo.



Clearly, the J16 pin numbers on the schematic WILL NOT correspond to pin numbers of any KEYED 26 pin IDC connector a user may install in J16.

The following information details the correlation between the J16 pin numbers on the Hermes and Angelia schematics and pin numbers found on a standard 26 pin KEYED IDC connector.

Note: The ANAN-100 and ANAN-100D further confuse the issue by using a DB25 female connector for the Accessory port (J16) and this changes the pinout yet again! See listing below the Hermes/Angelia J16 pinout for details.

Hermes/Angelia J16 pinout for 26 pin KEYED IDC ribbon cable. (Numbers in parentheses are J16 Pinout shown on Hermes and Angelia schematics)

- 1. User Digital input 3: Connected to 3.3V via 1K pullup resistor (26)
- 2. Open-drain PTT output (25).
- 3 OCREF Open-Collector reference/flyback diodes (24)
- 4. OC6 User open-collector output 7 (23)
- 5. OC5 User open-collector output 6 (22)
- 6. OC4 User open-collector output 5 (21)
- 7. OC3 User open-collector output 4 (20)
- 8. OC2 User open-collector output 3 (19)
- 9. OC1 User open-collector output 2 (18).
- 10. OC0 User open-collector output 1 (17)
- 11 User Digital input 2: Connected to 3.3V via 1K pullup resistor (16)
- 12 Right channel speaker balanced (ROUT+) pair with pin 13 (15)
- 13 Right channel speaker, balanced (ROUT-) pair with pin 12 (14).
- 14 User Digital input 4: connnected to 3.3V via 1K pullup resistor (13)

```
15 User Analogue input 2: 0-3V max (12)
```

- 16 User Analogue input 1: 0-3V max (11)
- 17 Analogue Ground (10)
- 18 User Digital input 1: Connected to 3.3V via 1K pullup resistor (9)
- 19 Right channel line Out (unbalanced) (8)
- 20 Left channel line Out (7)
- 21 Left channel phones output (6)
- 22 Right channel phones output(5)
- 23 Right channel line-level audio input (unbalanced) (4)
- 24 Left channel line-level audio input* (unbalanced) (3)
- 25 Analogue Ground (2)
- 26 PTT: connected to 3.3V via 1k pullup resistor(1) (same as Mic PTT,
- J2 if JP6 used)

The PowerSDR Setup, ANAN Ctrl tab numbering scheme for the J16 Receive and transmit pins does not represent the actual keyed IDC pin numbers.

PowerSDR

As shown IDC ribbon cable Hermes Schematic

- 1 10 17
- 2918
- 3 8 19
- 4720
- 5 6 21
- 6 5 22
- 7 4 23
- 3 OCRef. 24

The Apache Labs ANAN-100 and ANAN-100D Accessory Port/J16/DB25 numbering confusion:

The Hermes/Angelia schematic detail J16 pin numbering does not correspond to KEYED IDC ribbon cable numbering conventions. An IDC to DB25 adapter cable further re-arranges the pin numbers available on the rear panel Accessory Port of the ANAN-100 and ANAN-100D. J16-26 ANALOG 3 user input is lost, but it is not presently supported by PowerSDR in any case.

Pin out and connections between 26 pin J16, Modified (shifted) 26 pin KEYED IDC ribbon cable and DB 25.

J16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 IDC 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5

```
4 3 2 1
DB25 13 25 12 24 11 23 10 22 9 21 8 20 7 19 6 18 5 17 4 16 3
15 2 14 1
```

DB25 Acc Port pinout. Number in parentheses is the J16 pin number shown on the schematic.

- 1. Open-drain PTT output (25)
- 2. OC6 User open-collector output 7 (23)
- 3. OC4 User open-collector output 5 (21)
- 4. OC2 User open-collector output 3 (19)
- 5. OC0 User open-collector output 1 (17)
- 6. Right channel speaker balanced pair (ROUT+) with pin 19 (15)
- 7. User Digital input 4: connected to 3.3V via 1K pullup resistor (13)
- 8. User Analogue input 1: 0-3V max (11)
- 9. User Digital input 1: Connected to 3.3V via 1K pullup resistor (9)
- 10. Left channel line Out (unbalanced) (7)
- 11. Right channel phones output(5)
- 12. Left channel line-level audio input* (unbalanced) (3)
- 13. PTT input, connected to 3.3V via 1K pullup resistor (1)
- 14. OCREf Open-Collector reference/flyback diodes (24)
- 15. OC5 User open-collector output 6 (22)
- 16. OC3 User open-collector output 4 (20)
- 17. OC1 User open-collector output 2 (18)
- 18. User Digital input 2: Connected to 3.3V via 1K pullup resistor (16)
- 19. Right channel speaker, balanced pair (ROUT-) with pin 6 (14)
- 20. User Analogue input 2: 0-3V max (12)
- 21. Analogue Ground (10)
- 22. Right channel line Out (unbalanced) (8)
- 23. Left channel phones output (6)
- 24. Right channel line-level audio input (unbalanced) (4)
- 25. Analogue Ground (2)

The PowerSDR Setup, ANAN Ctrl tab numbering scheme for the J16 Receive and transmit pins does not represent the actual pin numbers.

PowerSDR Acc Port

As shown DB25 cable Hermes/Angelia Schematic J-16

1 5 17 OC0

2 17 18 0C1

3 4 19 OC2

4 16 20 OC3

5 3 21 OC4

6 15 22 OC5

7 2 23 OC6

14 OC REF 24 OC REF

HTH, Bill KC9XG