Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Libre Silicon process design rules

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June 3, 2018

1 Layer Definitions

Name	GDSII	CIF	Description
PWELL	41	CWP	p-well
NWELL	42	CWN	n-well
ACTIVE	43	CAA	active area
PPLUS	44	CSP	p^+ implant
NPLUS	45	CSN	n^+ implant
POLY	46	CPG	poly silicium
CONTACT	25	CCC	contact (connects METAL1 to POLY)
METAL1	49	CM1	lowest metal layer
VIA1	50	CV1	via layer (connects METAL2 to METAL1)
METAL2	51	CM2	second metal layer
VIA2	61	CV2	via layer (connects METAL3 to METAL2)
METAL3	62	CM3	third metal layer
GLASS	52	COG	passivation / isolation

2 General Requirements

1.1 All scaled dimensions are specified in Lambda λ.
1.2 All fixed dimensions are specified in Microns μm.
1.3 All geometries must be drawn on grid. The grid size is 1λ.
1.4 Polygones should be rectangles with 90 degree angles only.
1.5 The die size should be an integer multiple of $10\mu m$.

3 Process Layer Overview

Name	Minimum Width	Minimum Spacing
PWELL	10 λ	10 λ
NWELL	10 λ	10 λ
ACTIVE	3 λ	3 λ
POLY	2 λ	2 λ
CONTACT	2 λ	2 λ
METAL1	4 λ	4 λ
VIA1	2 λ	3 λ
METAL2	4 λ	4 λ
VIA2	2 λ	3 λ
METAL3	6 λ	4 λ

4 Structure Rules

4.1 PWELL Rules

- reserved for future use -

4.2 NWELL Rules

2.2.1 Minimum Width of NWELL is 10λ.
2.2.2 Spacing to NWELL at different potential is 9λ.
2.2.3 Spacing to NWELL at same potential is 6λ.

4.3 ACTIVE Rules

2.3.1	Minimum Width of ACTIVE is	3λ.
2.3.2	Spacing to ACTIVE is	3λ.
2.3.3	Source/Drain surround by PWELL/NWELL is	6λ.
2.3.4	Substrate/NWELL contact sourround by PWELL/NWELL is	3λ.
2.3.5	Spacing to ACTIVE of opposite type is	4λ.

4.4 POLY Rules

2.4.1	Minimum Width of POLY is	2λ.
2.4.2	Spacing to POLY over ACTIVE is	2λ.
2.4.3	Gate extension beyond ACTIVE is	2λ.
2.4.4	ACTIVE extension beyond POLY is	3λ.
2.4.5	Spacing of POLY to ACTIVE is	1λ.

4.5 CONTACT Rules

2.5.1	Exact Width of CONTACT is	$2x2\lambda$.
2.5.2	Overlap by POLY or ACTIVE is	1λ.
2.5.3	Spacing to CONTACT is	2λ.
2.5.4	Spacing to Gate is	2λ.
2.5.5	Spacing of POLY CONTACT to other POLY is	4λ.
2.5.6	Spacing of ACTIVE CONTACT to POLY CONTACT is	4λ.

4.6 METAL1 Rules

2.6.1	Minimum Width of METAL1 is	4λ.
2.6.2	Spacing of METAL1 is	4λ.
2.6.3	Overlap of CONTACT or VIA is	1λ.
2.6.4	Spacing to METAL1 for lines wider than 10λ is	6λ.

4.7 VIA1 Rules

2.7.1	Exact Width of VIA1 is	$2x2\lambda$.
2.7.2	Spacing to VIA1 is	3λ.
2.7.3	Spacing to CONTACT is	2λ.
2.7.4	Spacing to POLY or ACTIVE is	2λ.

4.8 METAL2 Rules

2.8.1	Minimum Width of METAL2 is	4λ.
2.8.2	Spacing to METAL2 is	4λ.
2.8.3	Overlap to VIA1 is	1λ.
2.8.4	Spacing to METAL2 for lines wider than 10λ is	6λ.

4.9 VIA2 Rules

2.9.1	Exact Width of VIA2 is	$2x2\lambda$.
2.9.2	Spacing to VIA2 is	3λ.

4.10 METAL3 Rules

4.10.1	Minimum Width of METAL3 is	6λ.
2.10.2	Spacing to METAL3 is	4λ.
2.10.3	Overlap to VIA2 is	1λ.
2.10.4	Spacing to METAL3 for lines wider than 10λ is	6λ.

4.11 GLASS Rules

2.11.1	Minimum Width of GLASS opening is	$60\mu m$.
2.11.2	METAL3 Overlap of GLASS opening is	$6\mu m$.
2.11.3	Spacing of pad METAL3 to unrelated METAL is	$30\mu m$.
2.11.4	Spacing of pad METAL3 to ACTIVE or POLY is	$15\mu m$.

5 Lithographic limitations

When looking at the mask making module "Intertech ISI-2808 Laser Direct Write System" from HKUST (**??**) we see the following limitations for the lithographic masks:

- The Minimum Feature Size of the Laser system is $1.5\mu m$. Any pattern size less than $1.5\mu m$ may not come out.
- The grid of the Laser system is $0.25\mu m$, any off grid pattern will be round off or up to the grid location

So the smallest structure **on the mask** shall be bigger than $1.5\mu m$
If we look at the stepper "ASML Stepper (PHT-S1)" from HKUST(**??**) we see it has a resolution of $0.5\mu m$ and a reduction ratio of 5:1
This mean that our feature sizes **on the wafer** can be around $0.5\mu m$ (for sizes below $0.5\mu m$ it will require some trickery with multiple overlapping masks in the future)

6 Etching limitations

We have established in section 5 that our lithographic lower limit is $0.5\mu m$. Now in this chapter we look at the different etching machines used for determining their minimum line spacing.

6.1 Poly etching

Because the "Poly Etcher (DRY-Poly)"(**??**) has minimum line space of $0.5\mu m$ we are not limited any further beyond what the lithographic limits are. The poly layer as well requires a minimum line space of $0.5\mu m$

6.2 Oxide etching

Because the "Trion RIE Etcher (DRY-Trion)"(**??**) has no minimum line space defined we are not limited any further beyond what the lithographic limits are. This means that the oxide etching as well requires a minimum line space of $0.5\mu m$.
This plays into the construction design rules for vias and the like.