Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Libre Silicon process design rules

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In overall the lambda rules from MOSIS are sufficient for keeping it manufacturable but just for completion we accumulate all the edge parameters arising from using the HKUST equipment which we are using for this open process in this chapter.

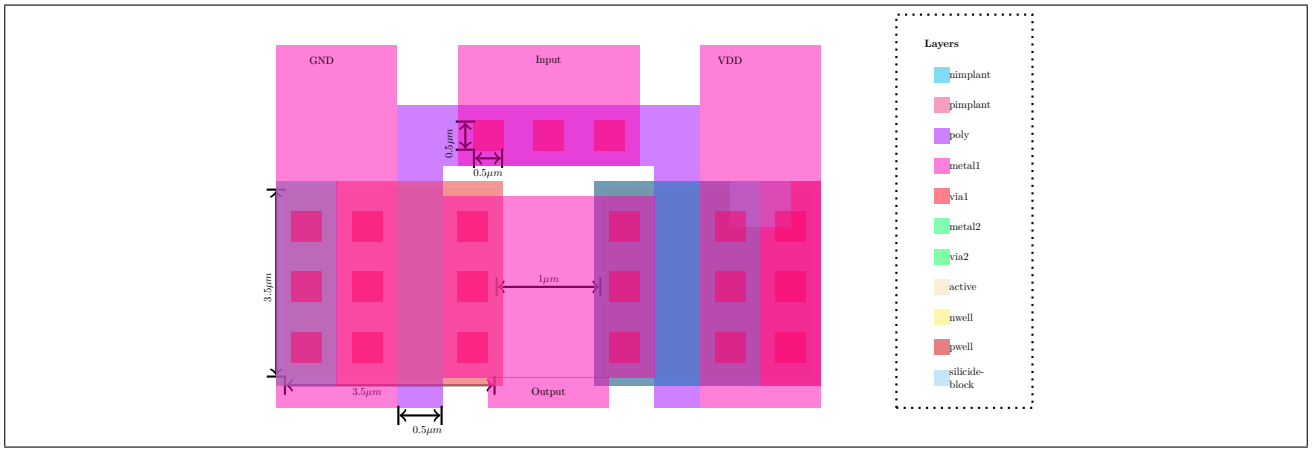

Figure 1: Example inverter

The layout shown in Figure 1 is for demonstration purposes only and shows a circuit at the limit of our resolution with $\lambda = 0.5\mu m$.
This process however will, as already stated so many times through out this document, only be tested with a λ of $1.0\mu m$ for now.
Please have a look at the LS1U technology standard logic cells in our repository.

1 Lithographic limitations

When looking at the mask making module "Intertech ISI-2808 Laser Direct Write System" from HKUST (**??**) we see the following limitations for the lithographic masks:

- The Minimum Feature Size of the Laser system is $1.5\mu m$. Any pattern size less than $1.5\mu m$ may not come out.
- The grid of the Laser system is $0.25\mu m$, any off grid pattern will be round off or up to the grid location

So the smallest structure **on the mask** shall be bigger than $1.5\mu m$
If we look at the stepper "ASML Stepper (PHT-S1)" from HKUST(**??**) we see it has a resolution of $0.5\mu m$ and a reduction ratio of 5:1
This mean that our feature sizes **on the wafer** can be around $0.5\mu m$ (for sizes below $0.5\mu m$ it will require some trickery with multiple overlapping masks in the future)

2 Etching limitations

We have established in subsection 0.1 that our lithographic lower limit is $0.5\mu m$. Now in this chapter we look at the different etching machines used for determining their minimum line spacing.

2.1 Poly etching

Because the "Poly Etcher (DRY-Poly)"(**??**) has minimum line space of $0.5\mu m$ we are not limited any further beyond what the lithographic limits are. The poly layer as well requires a minimum line space of $0.5\mu m$

2.2 Oxide etching

Because the "Trion RIE Etcher (DRY-Trion)"(**??**) has no minimum line space defined we are not limited any further beyond what the lithographic limits are. This means that the oxide etching as well requires a minimum line space of $0.5\mu m$.
This plays into the construction design rules for vias and the like.