

# Generic LibreSilicon process HKUST (NFF)

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## Abstract

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This is the specification of the free silicon manufacturing standard for manufacturing the ls180nm<sup>1</sup> standard logic cells and related free technology nodes from the LibreSilicon project.

For further clarification consult the complete documentation of the process.

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<sup>1</sup><https://github.com/leviathanch/ls180nm>

Process Flow of Lanceville Technologies LibreSilicon 180nm

- Project: LibreSilicon 180nm
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer <100>
- Date: January 28, 2018

SiO2						
Si (p-type)	<b>Wafer Cleanliness</b>	<b>Step Number</b>	<b>Equipment</b>	<b>Location</b>	<b>Cleanliness</b>	<b>Process</b>
	Clean	0.1	A3: Sulfuric Cleaning	P201000	Clean	Initial Clean
	Clean	0.2	A2: HF:H2O (1:50)	P201000	Clean	HF dip
	Clean	0.3	Spin Dryer-A	P201000	Clean	Dry the wafer automatically
	Clean	0.4	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Sacrificial Oxide Growth
						Requirements
						H2SO4 + H2O2, 10mins, 120C
						1 min
						200A