Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Libre Silicon process steps

David Lanzendörfer

May 8, 2018

The general flow chart of the overall process flow can be seen in Figure 1. These process steps will be discussed within the following sections.

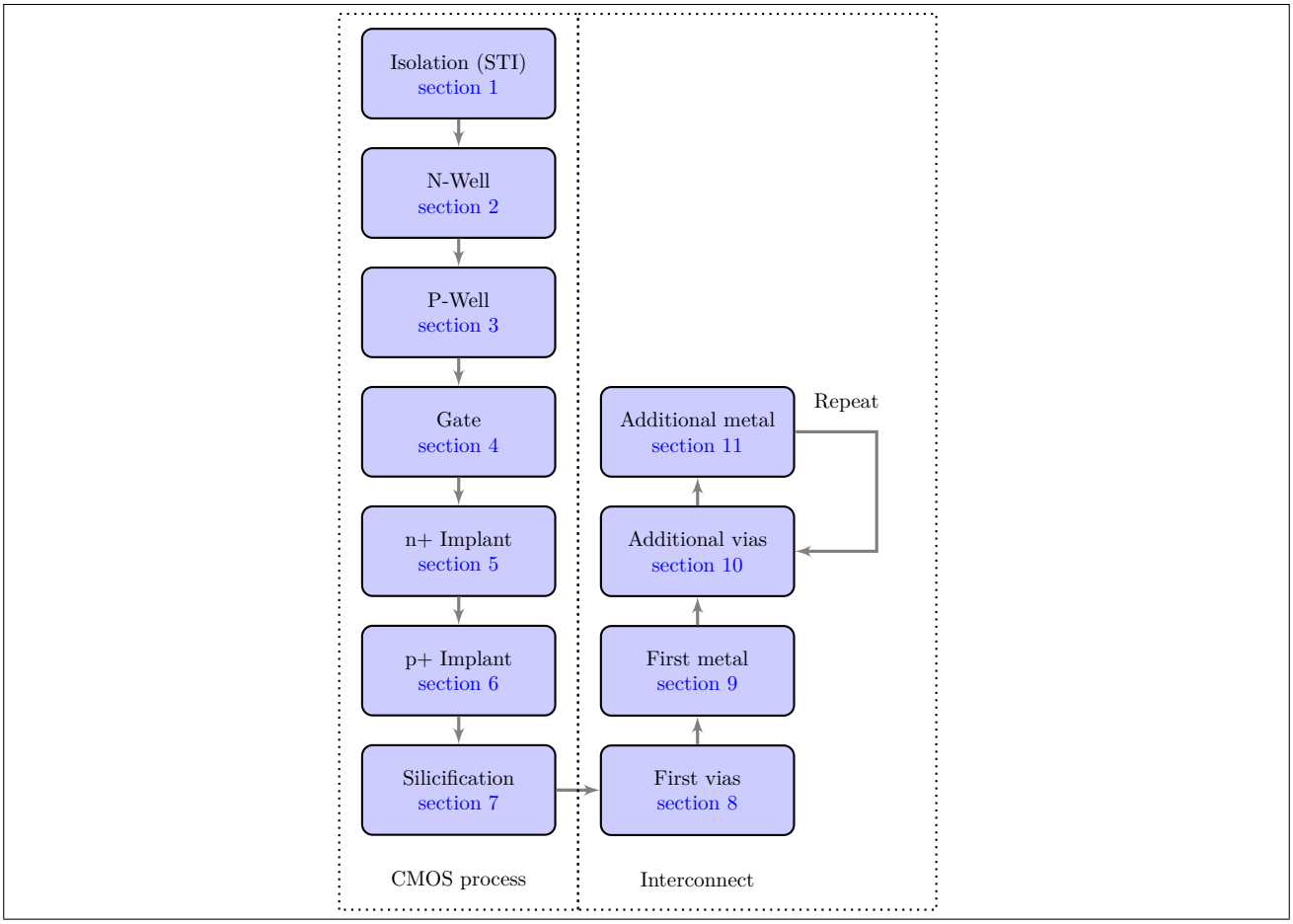

Figure 1: Frontend and backend process flow

The six overall process steps are part of an active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world.
For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

1 Shallow trench isolation

The geometry of a substrate with STI implemented can be seen in Figure 2.

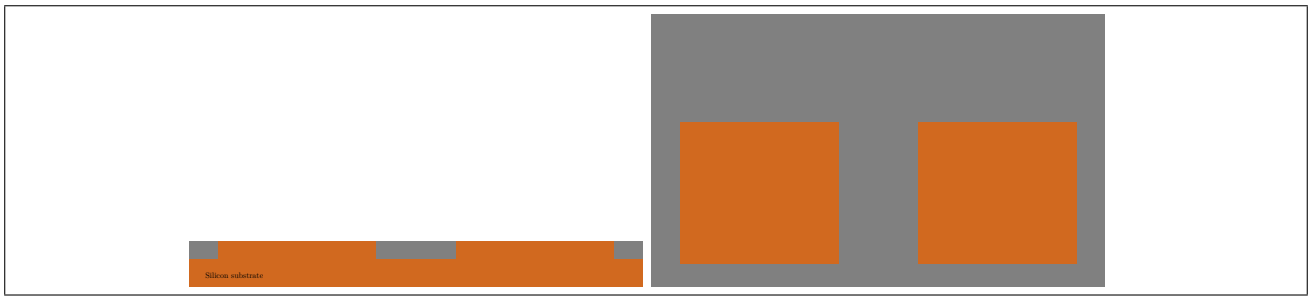

Figure 2: Shallow trench isolation target geometry

As can be seen in Figure 12, the n-well and the STI trench are supposed to have approximately the same depth but the n-well and p-well go down a little bit further. Because the n-well will be $\approx 4\mu m$ in depth we have to match this with our trench depth. I order to allow a sufficiently low resistance of the ESD diode but at the same time a sufficient isolation of between the standard cells a trade-ff has been done. The targeted depth of the box isolation is $\approx 2\mu m$.

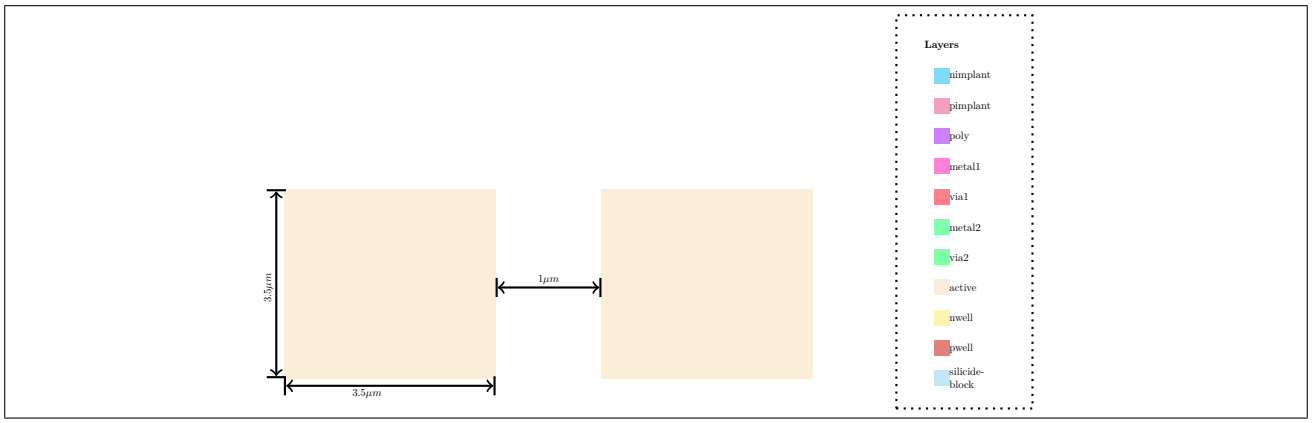

Figure 3: Shallow trench isolation layout

In Figure 3 we can see the layout for the STI area. The STI area will be everywhere, where no active areas are. The deep isolating oxide needs to be grown out of trenches which can't been etched out of the silicon by using resist as a mask. For that reason we will have to resort to a protective mask made from a silicon dioxide layer which has to be etched before hand. So the mask will be exposed onto positive resist on top of the nitride in order to form a protective mask covering the active areas from having etched trenches into them as show in **??**. After that we will use a dry etching method for cutting into the silicon substrate and making the active area become islands with trenches in between, as shown in subsection 1.8. After these steps we have to remove the hard mask.
Our minimum width and height as well as the space between the active areas comes from the line space constrain of the silicon etcher (**??**) and of course the optical limitations of the stepper which are as well $0.5\mu m$.

1.1 Initial cleaning

In order to remove the initial naturally grown silicon dioxide from the wafer, acid is being applied to the wafer which leads to a pure silicon substrate wafer as in the process illustration shown in Figure 4.

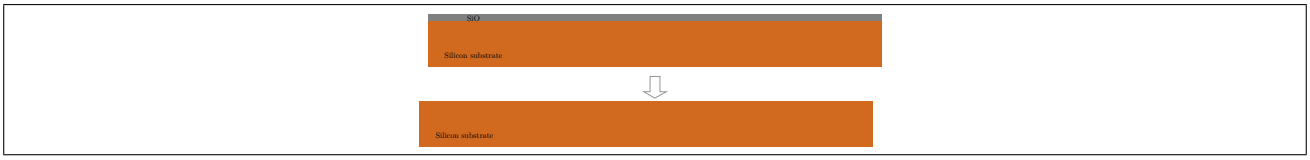

Figure 4: Initial cleaning

This needs to be done because the naturally grown initially existing silicon oxide is not pure and may contain contamination which may render the final product unusable.

1.2 Sulfuric Cleaning

The sulfuric acid mixture, $H_2SO_4 + H_2O_2$ is being applied to the wafer for 10 minutes at a temperature of 120 °C.

1.3 HF dip

After the sulfuric cleaning a HF (HF:H_2O,1:50) dip is being performed for one minute.
Hydrofluoric acid (HF) is used to remove native silicon dioxide from wafers. Since it acts quickly, one needs to only expose the wafer for a short time ("dip").
After that the wafer needs to be dried and quickly processed further before new uncontrolled natural oxide can build up on the wafer through the contact with air.

1.4 Hard mask (oxide)

We need a thick layer of oxide as protective hard mask to etch the trenches into the silicon.

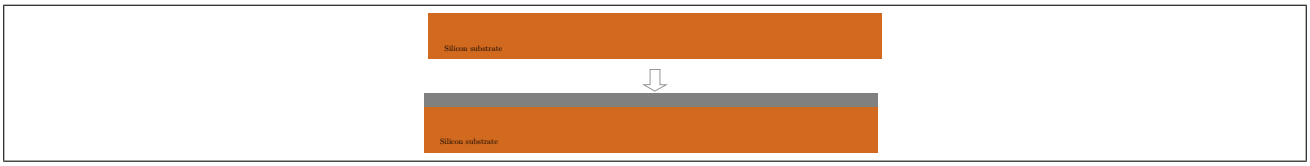

Figure 5: Hard mask growth

The machine "DRIE Etcher #1 (DRY-Si-1)" (**??**) which we're going to use to etch the trenches has a selectivity of >80:1 which means we have to be at least $\frac{1}{80} \cdot 2\mu m = 25nm$ thick.
To be safe 500nm is a good approach (TODO: Needs to experimentally verified!)
The layer of silicon dioxide of around 500nm thickness is grown in wet ambient for 56 minutes at 1050°C [1] in the diffusion furnace (**??**).

1.5 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist.

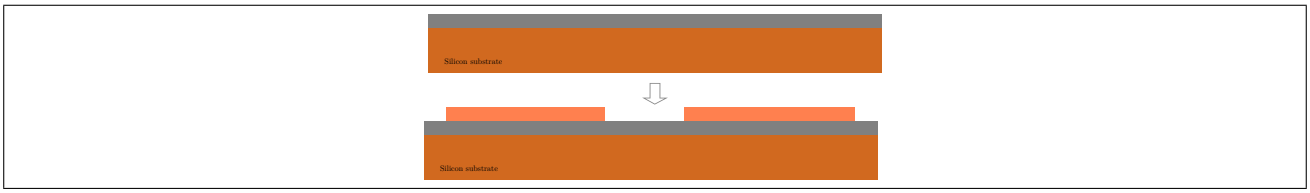

Figure 6: Patterning with positive resist

The layout for being exposed onto the resist is being extracted from the "active" layer within the GDS2 file onto a dark field mask. A dark field mask can be used because alignment doesn't play a role yet because it's the first layer, however the alignment crosses need to be included into the mask.

[1] `http://cleanroom.byu.edu/OxideTimeCalc`

1.6 Hard mask etching

We open the access to the silicon outside of the active areas in order to etch the trenches.

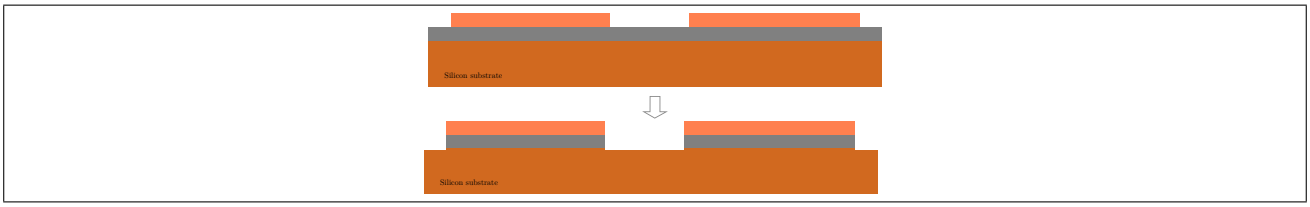

Figure 7: Nitride mask etching

We use anisotropic plasma etching for sharper borders. We etch for roughly 30 seconds. The machine properties are described in **??**. It has to be verified whether 30 seconds etch time are enough.

1.7 Resist removal

Now we come out of the last step which means we are Semi clean. Now we need to remove the contaminants for further processing.

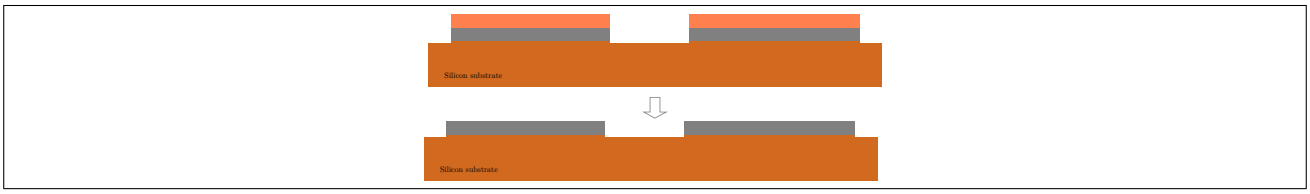

Figure 8: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

1.8 Silicon etching

Silicon can only be etched by a very aggressive chemical cocktail of KOH and TMAH (25%) or by plasma etching.

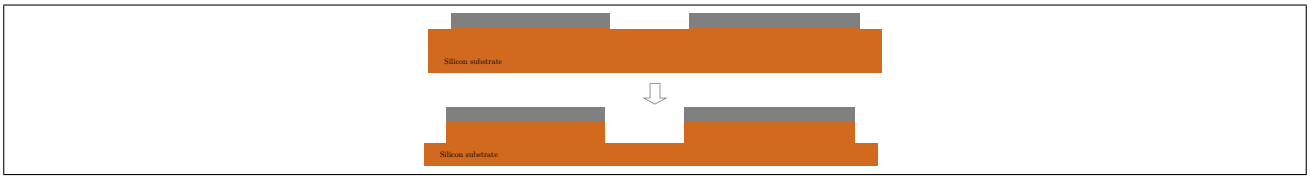

Figure 9: Trench etching

Possible approaches:

- **"DRIE Etcher #1" from HKUST(??)**
  Has a normal etching rate of up to $2\frac{\mu m}{min}$. This means we etch for 10 minutes with a reduced etch speed of $200\frac{nm}{min}$ in order to be clearly deep enough and to compensate for different etch depths in different places. This way we have a good chance of having proper isolation everywhere on the wafer.
- **Chemical solution**
  Using a KOH solution of 20% at $60°C$ gives us an etch rate of roughly $25\mu m$ per hour[2]. With a desired depth of $2\mu m$ we will have to etch around 3 minutes in order to reach the desired depth. The disadvantage of this approach is the imprecision and possible under-etch of the mask.

[2] `https://cleanroom.byu.edu/KOH`

1.9 Oxide deposition

Now we need to fill up the trenches with silicon dioxide and even it out afterwards.

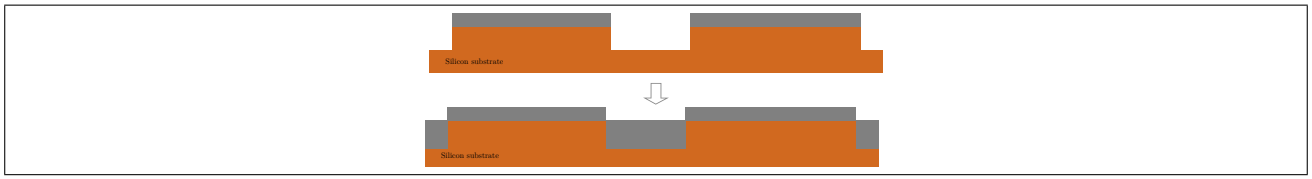

Figure 10: Oxide deposition

For this reason we put it into the furnace (**??**) and run a wet oxidation for roughly two days (roughly 48 hours) at $1150°C$. The timing here isn't that critical because excess oxide will be evened out anyway by the CMP process.

1.10 Hard mask removal

Now we have to remove the nitride mask for further processing and need to even out the oxide layer.

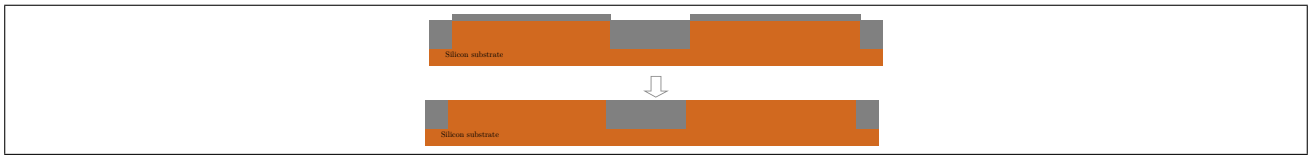

Figure 11: Trench etching

We use a CMP machine. The HKUST lab provides multiple "Buehler Polisher" machines(**??**), which allow polishing away the hard mask **and** evening out the uneven oxide deposition in one single step!
We polish away around 100nm of material. This makes sure we have an even surface at the end.

2 N-well

In order to build CMOS on the same substrate, an n-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The cross section as well as the top view of the targeted geometry are shown in Figure 12

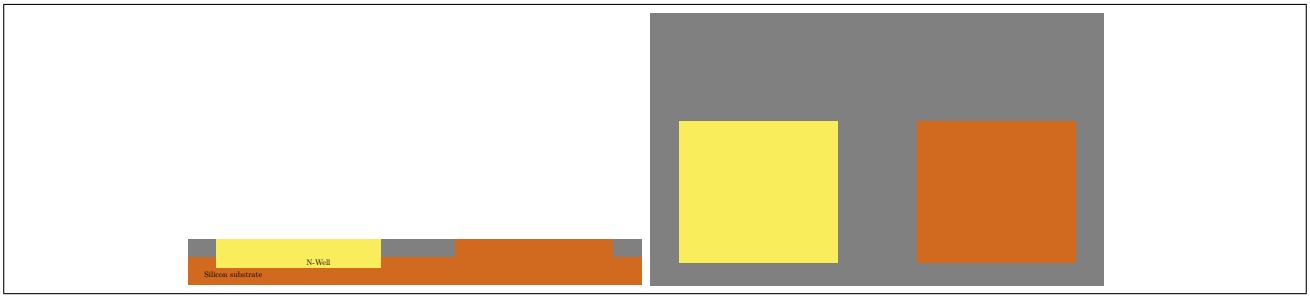

Figure 12: N-well target geometry

The n-well will serve us as an island of n-doped substrate within the p-doped basis substrate.
The dopant dose will be $2.5 \times 10^{12} cm^{-2}$ as calculated in **??**.

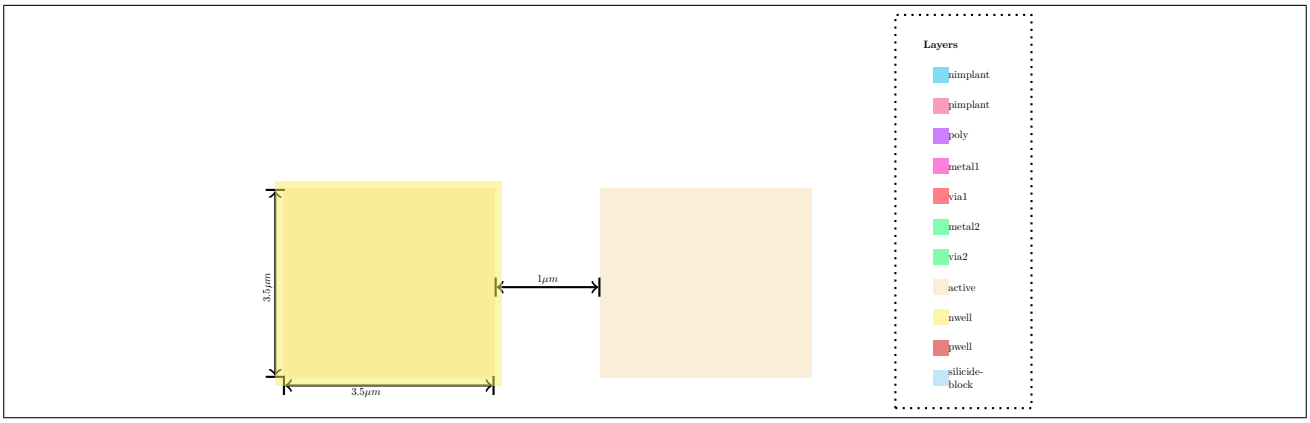

Figure 13: N-Well layout

In Figure 13 the layout of the n-well region on top of the active area region can be seen.
The n-well is being fit into the active area. It should even be a little bit bigger than the active area, because of possible alignment offsets

2.1 Mask dioxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

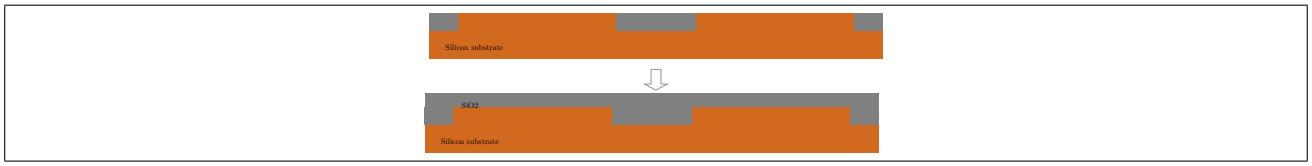

Figure 14: Dioxide layer growth

The industrial best practice is a layer of around (500nm≈5000Å) thickness or more. For this purpose the wafer is being oxidized for at least 90 minutes at 1000°C using wet oxidation which results in a dioxide layer at least 500nm(≈5000Å) in thickness.

2.2 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”nwell” layer within the GDS2 file.

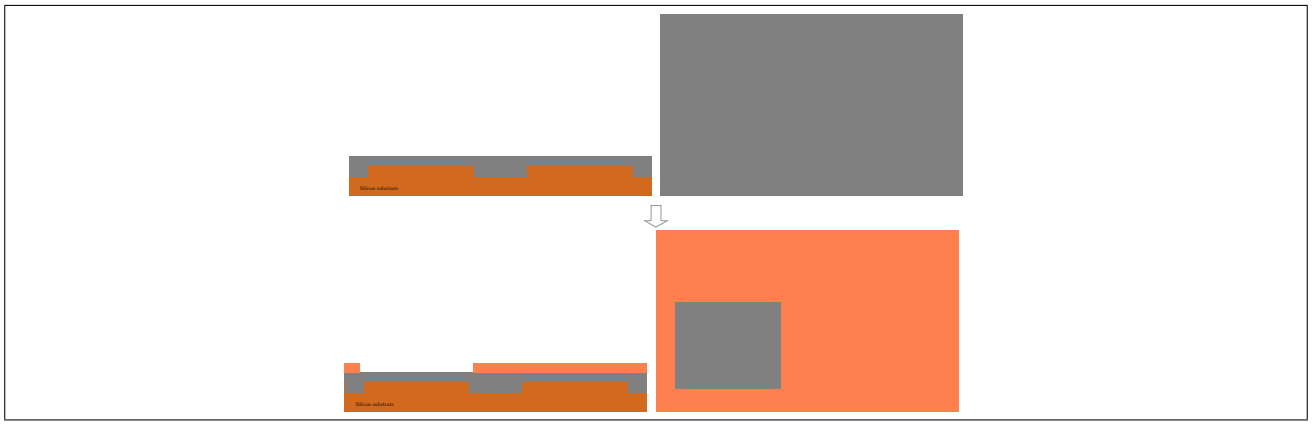

Figure 15: Cross/top view of n-well layout on resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with.

2.3 Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

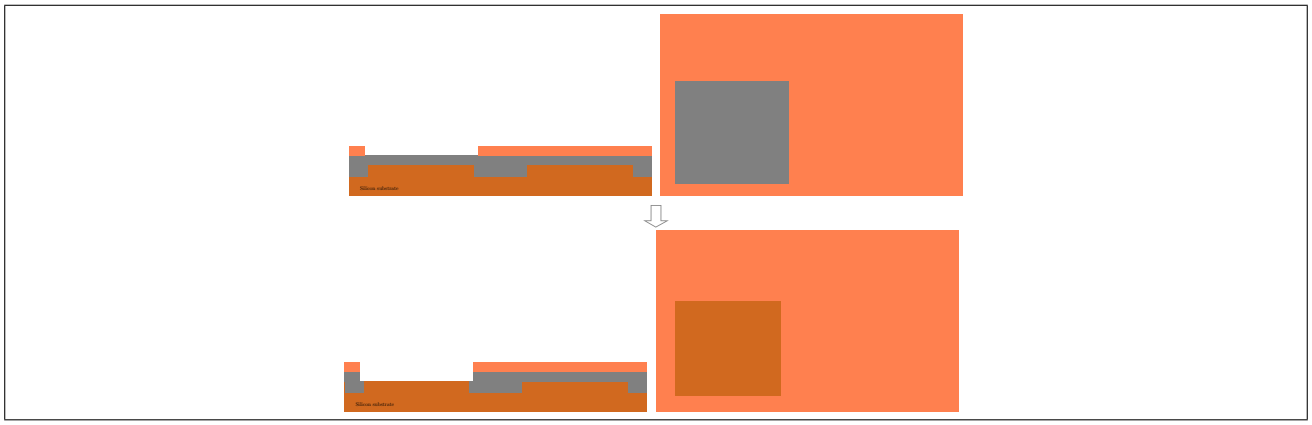

Figure 16: Cross/top view of n-well oxide window

Since the silicon dioxide layer is 500nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) (**??**) we can etch with a speed of approximately 2 nm/s at

25 °C, we can calculate the etching time to be $\frac{500nm}{2nm/s}$=250s=4 minutes 10 seconds (or make it rather 30 seconds instead of 10)

2.4 Cleaning

In order to avoid contamination of the machines we need to make sure all the resist has been stripped off from the wafer.

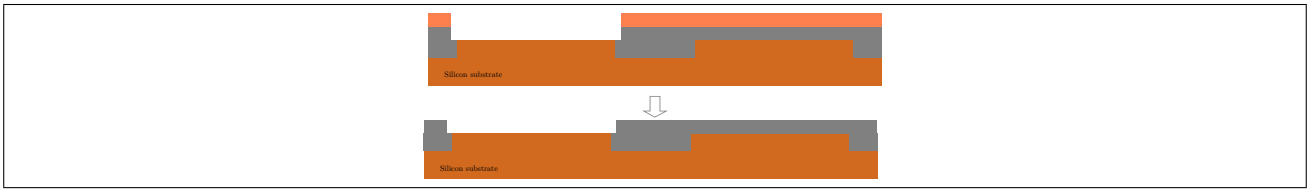

Figure 17: Resist removal

Please just use the solvent for the specific resist.

2.5 Injection

We now need to inject the carriers into the upper level of the n-channel area so that we can later on drive them into the crystal during the drive-in step.

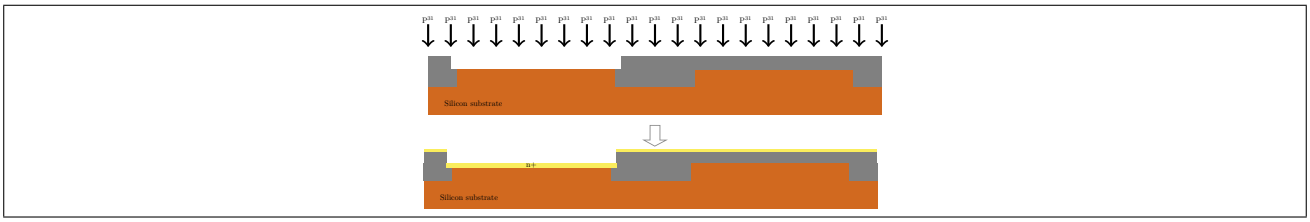

Figure 18: Doping process

The n-well is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 KeV. The n-well is then annealed.

2.6 Oxide for drive-in

Now we need to cover the now doped and annealed areas with an oxide layer for the drive-in phase.

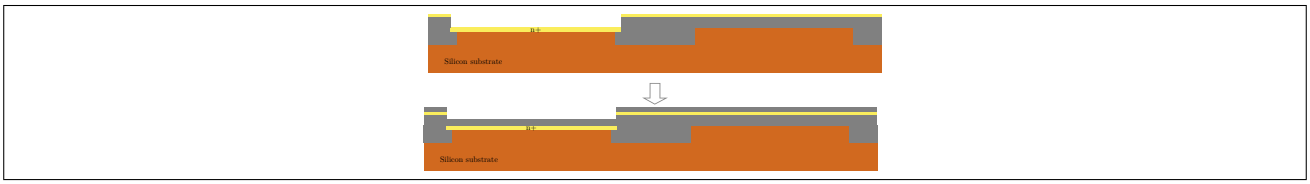

Figure 19: Oxide growth

The wafer is being oxidized for 32 minutes at 1000°C in order to achieve a cover silicon layer of 250nm thickness (≈2500Å).

2.7 Drive-in

In order to drive the carrier atoms deeper into the crystalline structure the wafer needs to be driven in after predeposition.

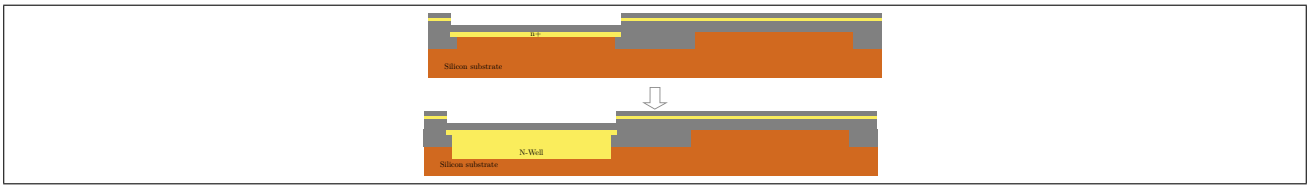

Figure 20: Drive-in process

In this step the wafer is driven-in for 96 minutes at 1150°C in an inert ambient.

2.8 Oxide mask removal

We want to remove the silicon mask from the wafer so that the n-well becomes accessible for the further process steps but we don't want to etch "way too much" of the trench material.

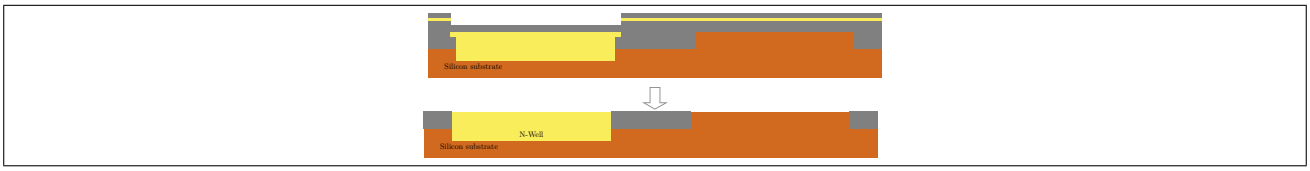

Figure 21: Oxide removal

Since the silicon dioxide layer is 750nm (500nm+250nm) thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) (**??**) we can etch with a speed of approximately 2 nm/s at 25 °C. We can calculate the etching time to be $\frac{750nm}{2nm/s}$=375s=6 Minutes and 15 Seconds.
Etching away a "little bit too much" of the oxide isn't that bad, because the oxide within the trenches will be "filled up" again during the later steps.

3 P-well

In order to build CMOS on the same substrate, an P-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The cross section as well as the top view of the targeted geometry are shown in Figure 12

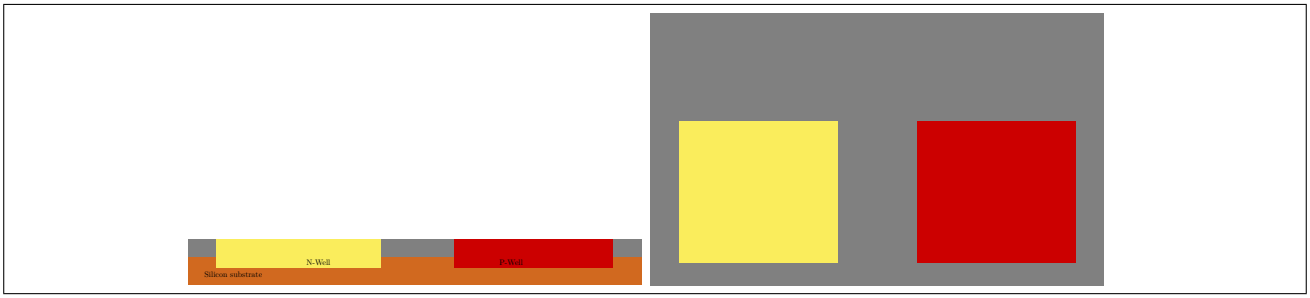

Figure 22: P-well target geometry

The P-well will serve us as an island of higher p-doped substrate within the slightly p-doped basis substrate. The dopant dose will be: $2.5 \times 10^{12} cm^{-2}$

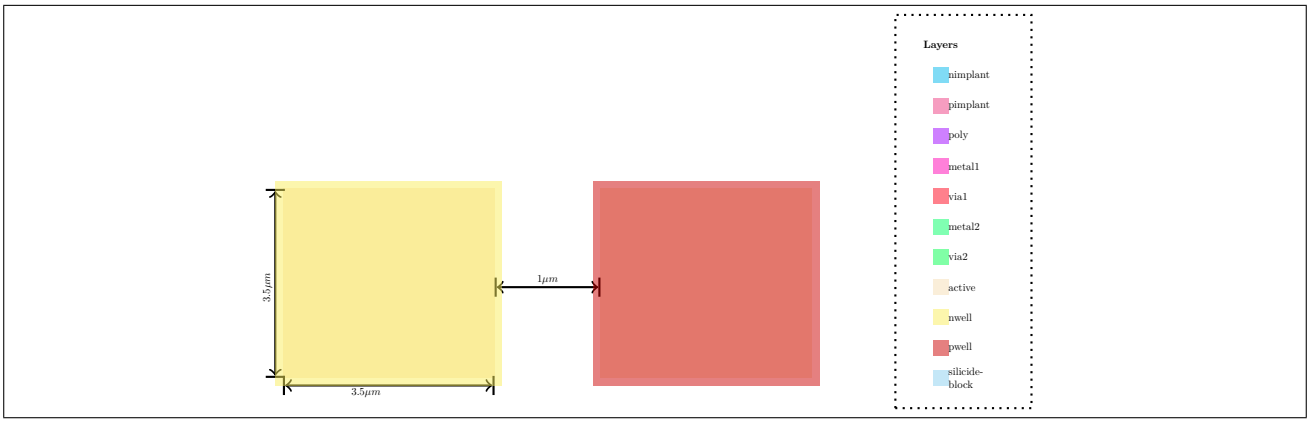

Figure 23: P-Well layout

In Figure 23 the layout of the P-well region on top of the active area region can be seen.
The p-well is being fit into the active area.
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3.1 Mask dioxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

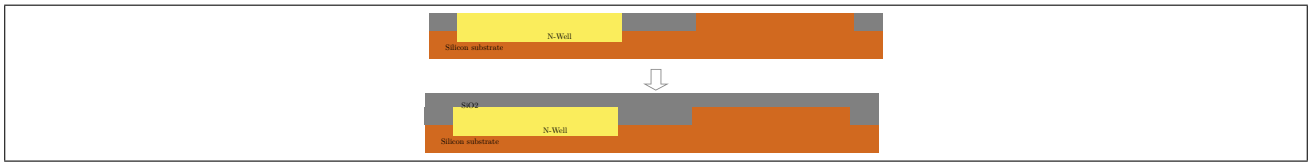

Figure 24: Dioxide layer growth

The industrial best practice is a layer of around (500nm≈5000Å) thickness or more. For this purpose the wafer is being oxidized for at least 90 minutes at 1000°C using wet oxidation which results in a dioxide layer at least 500nm(≈5000Å) in thickness.

3.2 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”pwell” layer within the GDS2 file.

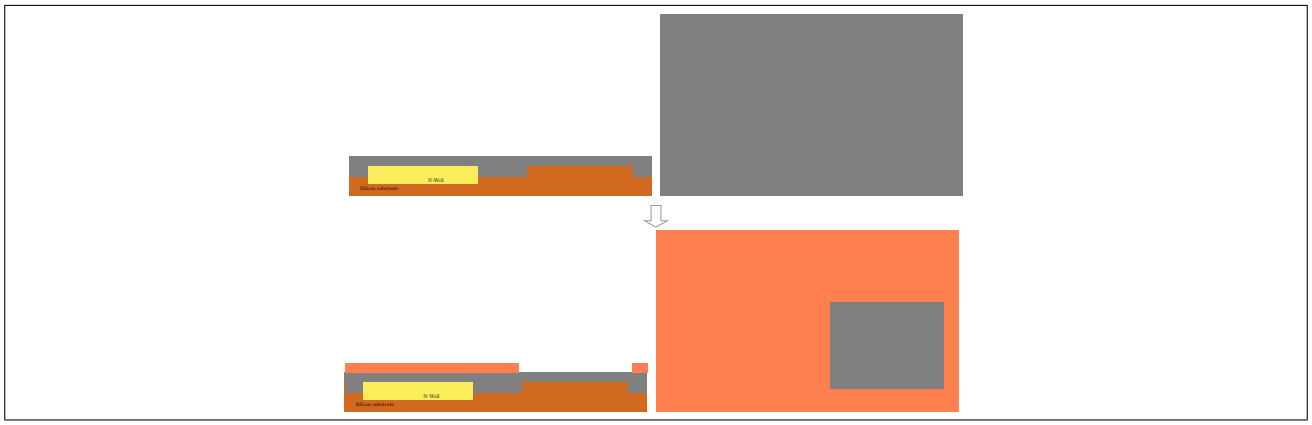

Figure 25: Cross/top view of P-well layout on resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with.

3.3 Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

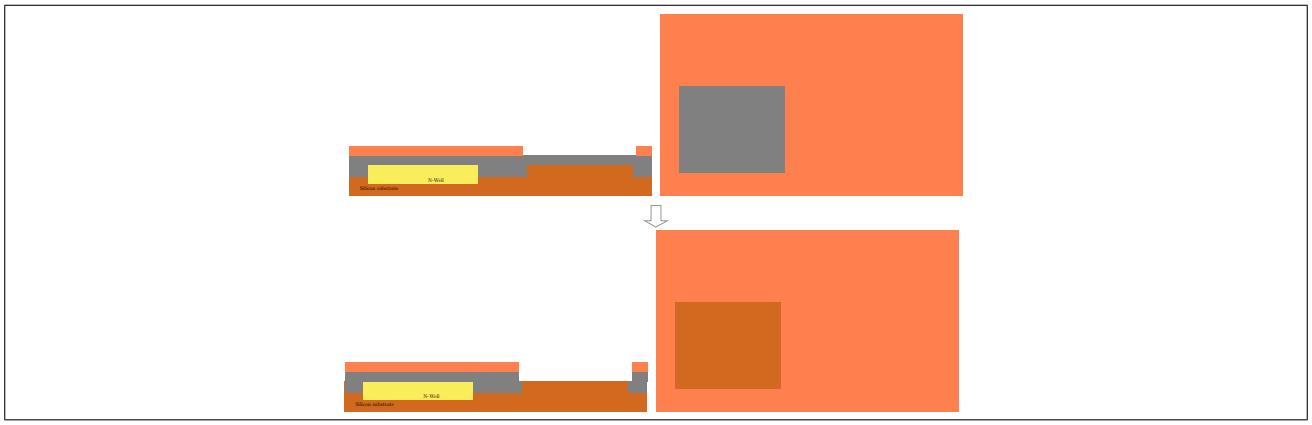

Figure 26: Cross/top view of P-well oxide window

Since the silicon dioxide layer is 500nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) (**??**) we can etch with a speed of approximately 2 nm/s at

25 °C, we can calculate the etching time to be $\frac{500nm}{2nm/s}$=250s=4 minutes 10 seconds (or make it rather 30 seconds instead of 10)

3.4 Cleaning

In order to avoid contamination of the machines we need to make sure all the resist has been stripped off from the wafer.

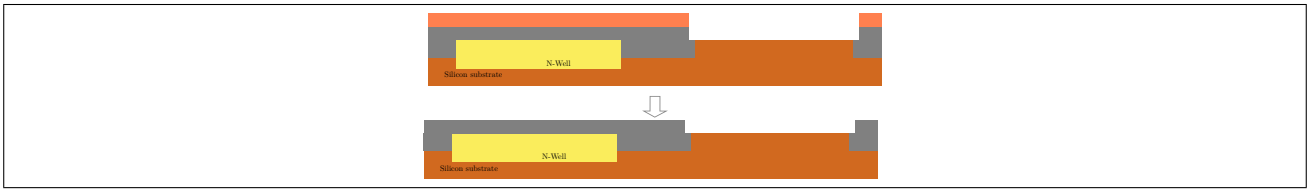

Figure 27: Resist removal

Please just use the solvent for the specific resist.

3.5 Injection

We now need to inject the carriers into the upper level of the n-channel area so that we can later on drive them into the crystal during the drive-in step.

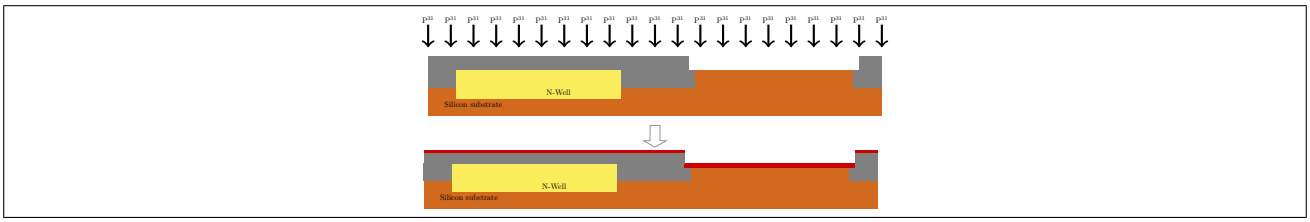

Figure 28: Doping process

The P-well is implanted with a Boron (B^{11}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 KeV. The P-well is then annealed.

3.6 Oxide for drive-in

Now we need to cover the now doped and annealed areas with an oxide layer for the drive-in phase.

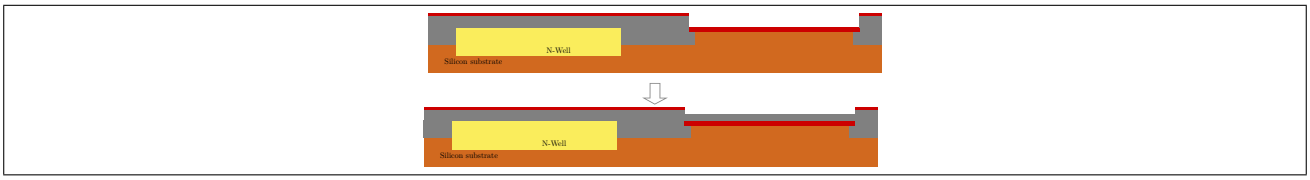

Figure 29: Oxide growth

The wafer is being oxidized for 32 minutes at 1000°C in order to achieve a cover silicon layer of 250nm thickness (≈2500Å).

3.7 Drive-in

In order to drive the carrier atoms deeper into the crystalline structure the wafer needs to be driven in after predeposition.

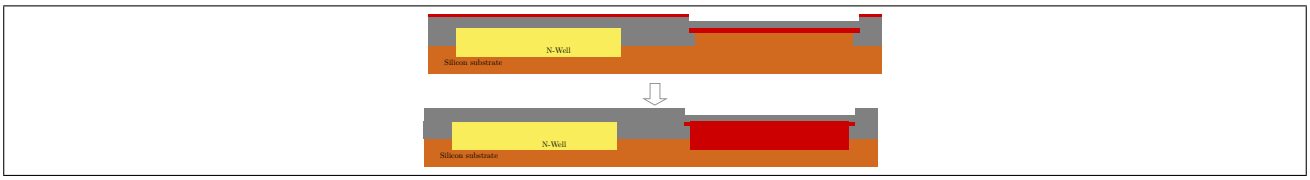

Figure 30: Drive-in process

In this step the wafer is driven-in for 96 minutes at 1150°C in an inert ambient.

3.8 Oxide mask removal

We want to remove the silicon mask from the wafer so that the P-well becomes accessible for the further process steps but we don't want to etch "way too much" of the trench material.

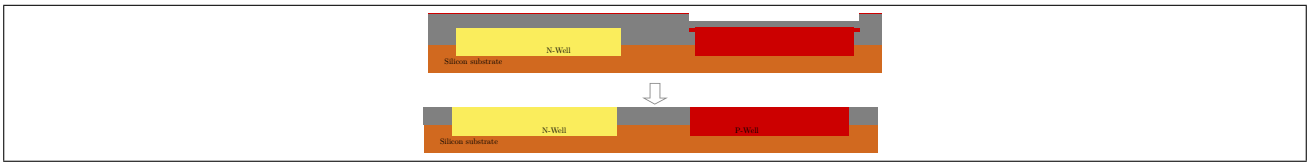

Figure 31: Oxide removal

Since the silicon dioxide layer is 750nm (500nm+250nm) thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) (**??**) we can etch with a speed of approximately 2 nm/s at 25 °C. We can calculate the etching time to be $\frac{750nm}{2nm/s}$=375s=6 Minutes and 15 Seconds.
Etching away a "little bit too much" of the oxide isn't that bad, because the oxide within the trenches will be "filled up" again during the later steps.

4 Gate

Now we have to build the initial gate structure which contains of the 40nm thick dielectric (in our case just silicon dioxide) and the polysilicon electrode.

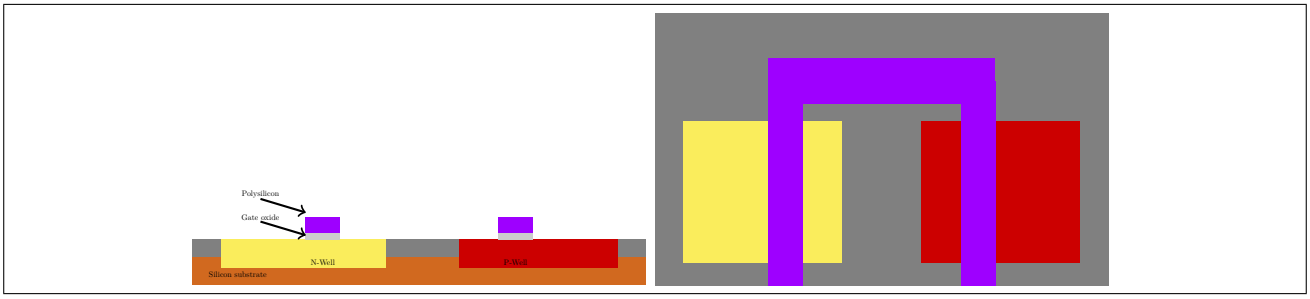

Figure 32: Aluminum gate contacts with gate oxide

The line spacing of the polysilicon electrode shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.

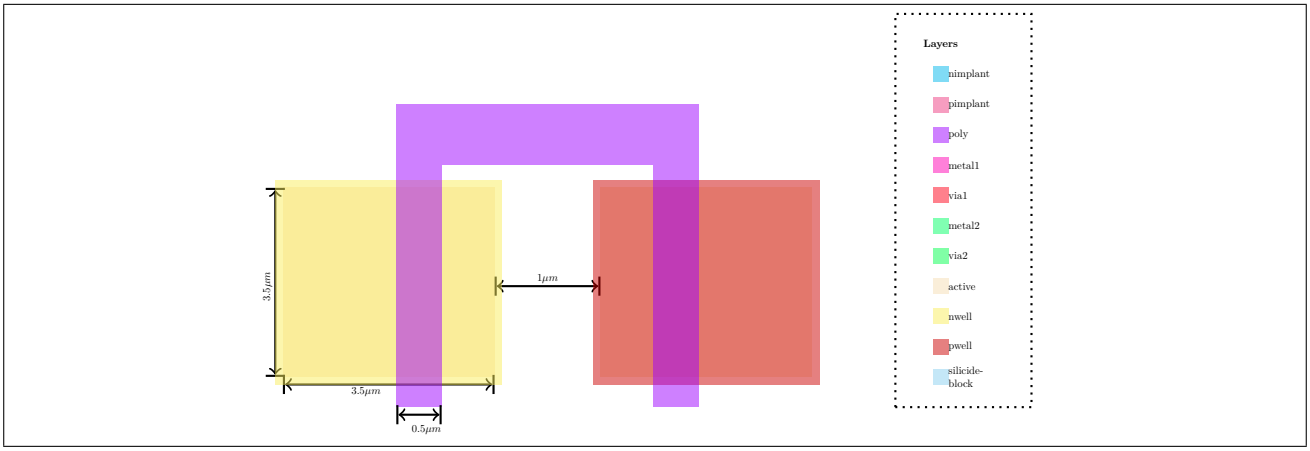

Figure 33: Gate layout

In Figure 33 we can see the layout honoring the $0.5\mu m$ spacing design rule for the gate structure shape and poly-layer interconnect between NMOS and PMOS.

4.1 Gate oxide deposition

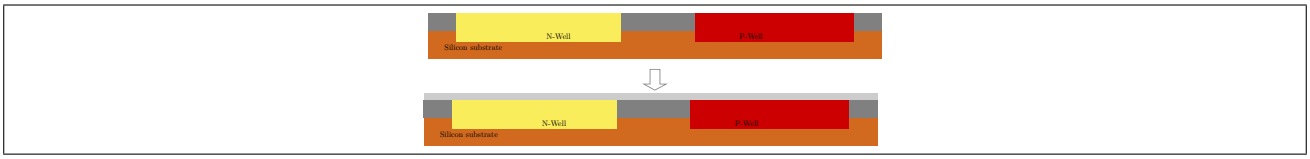

Figure 34: Thin oxide

4.2 Polysilicon deposition

Now we need to add the polysilicon layer for forming the gate structure after etching.

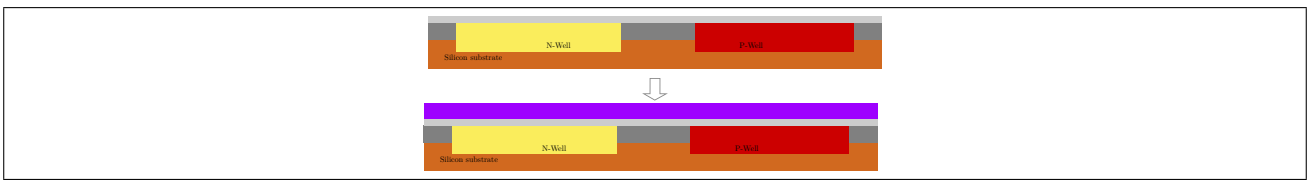

Figure 35: Polysilicon

We use the LPCVD machine(**??**) and deposit a layer of around 600nm polysilicon[3].

[3] `https://people.rit.edu/lffeee/LPCVD_Recipes.pdf`

We set the temperatue to $650°C$, the gas will be Silane (SiH_4 ($Si + 2H_2$)), the pressure will be set to 300 mTorr with a flow of 90sccm.
This will give us a growth rate of roughly 23.5 nm per minute, so for 600nm we let it grow half an hour.

4.3 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”poly” layer within the GDS2 file onto a bright field mask.

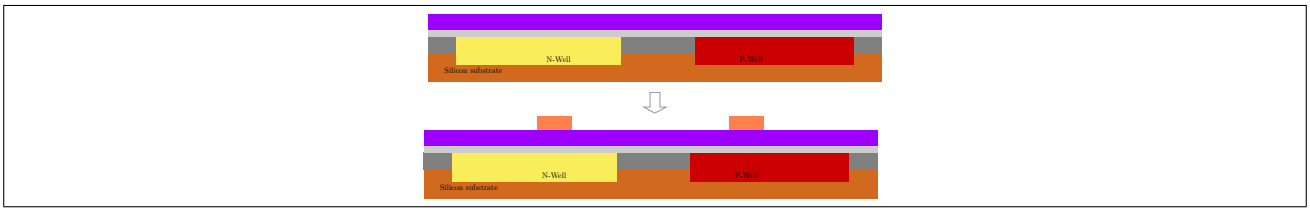

Figure 36: Resist

4.4 Etching

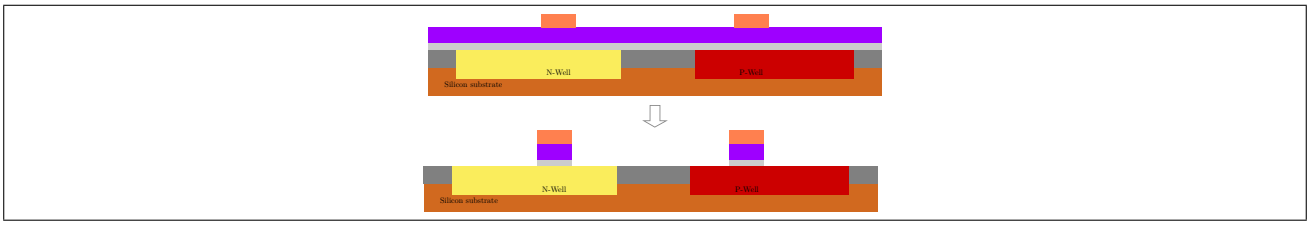

Figure 37: Resist

4.5 Cleaning

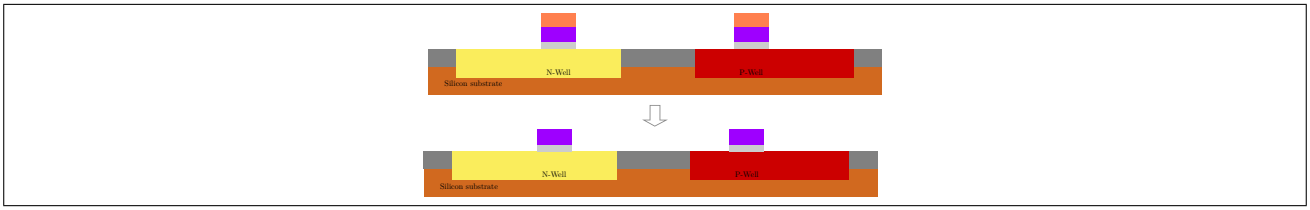

Figure 38: Resist

5 n+ Implant

For the bulk of the PMOS transistors and for the source and drain of the NMOS transistors highly doped n+ areas are required. In this step we're going to build these.

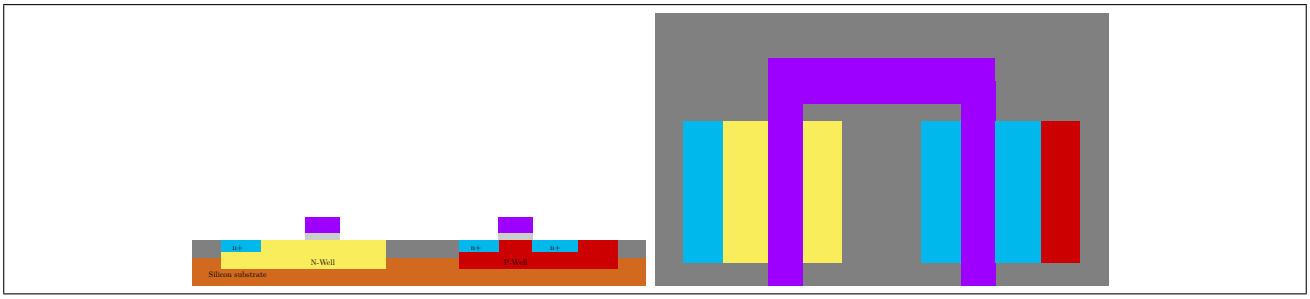

Figure 39: N+ implant geometry target

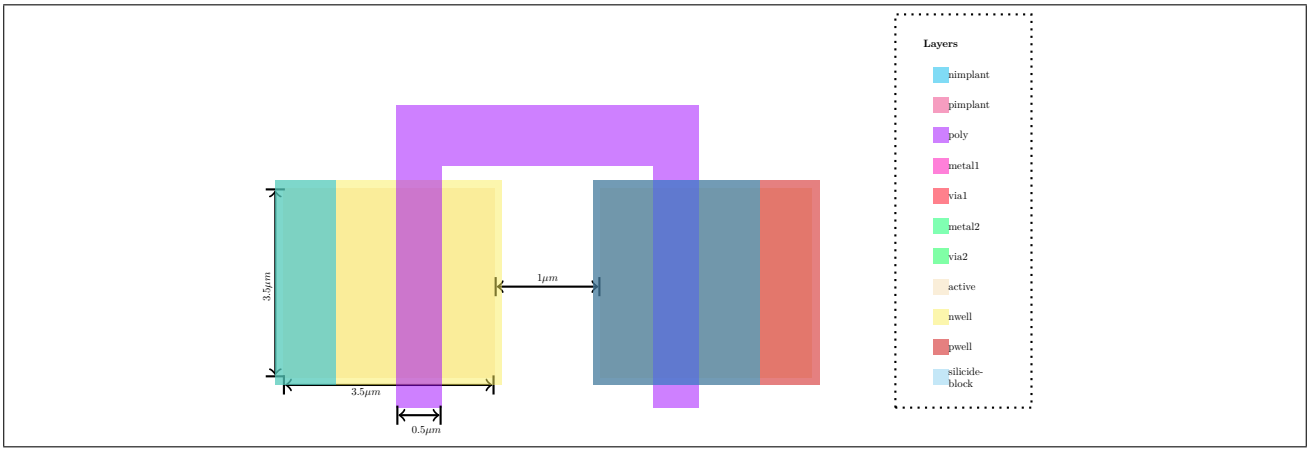

Figure 40: N+ layout

5.1 Mask dioxide layer

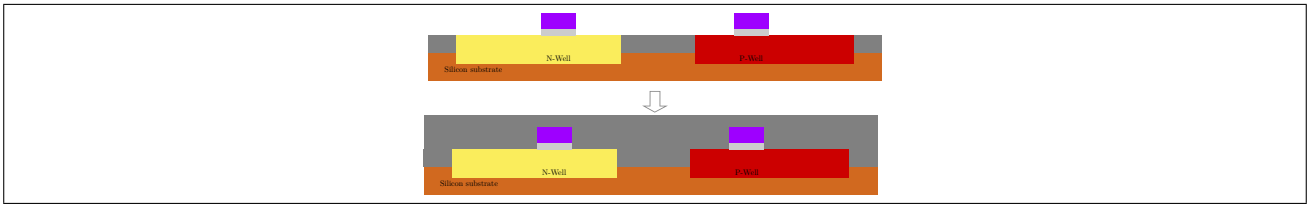

Figure 41: Oxide layer

5.2 Pattering

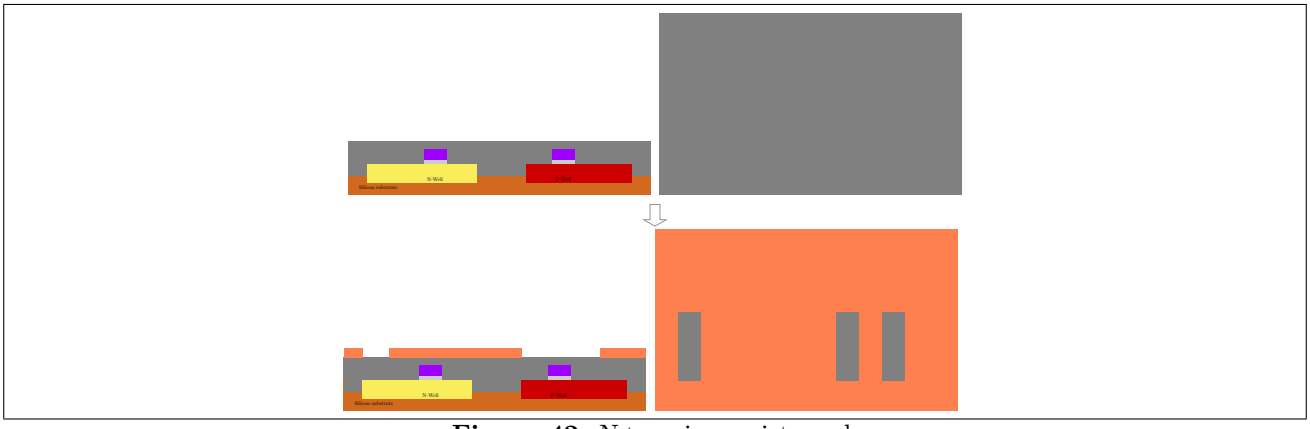

Figure 42: N+ region resist mask

5.3 Etching

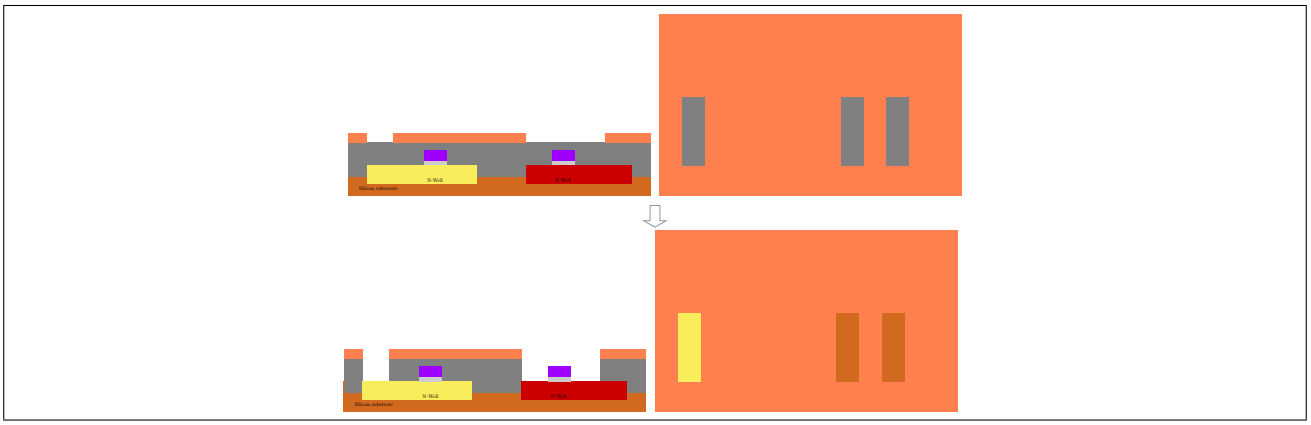

Figure 43: N+ region opened

5.4 Cleaning

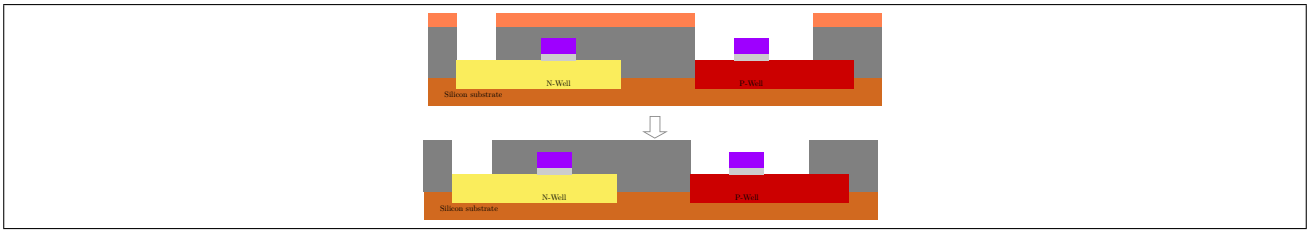

Figure 44: Resist removal

5.5 Injection

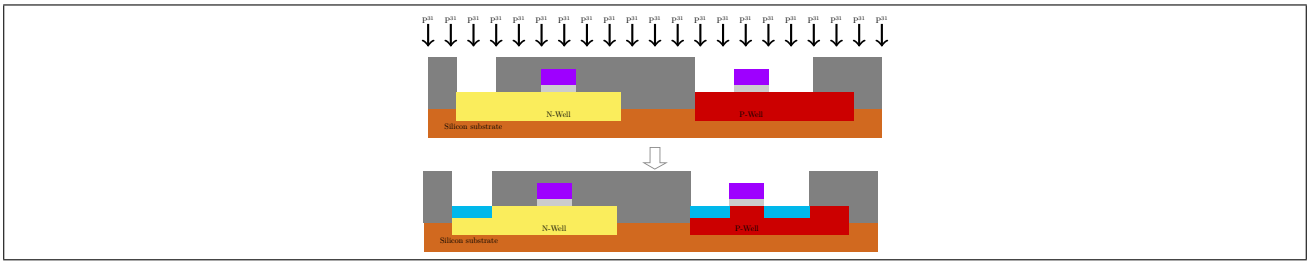

Figure 45: N+ injection process

5.6 Oxide removal

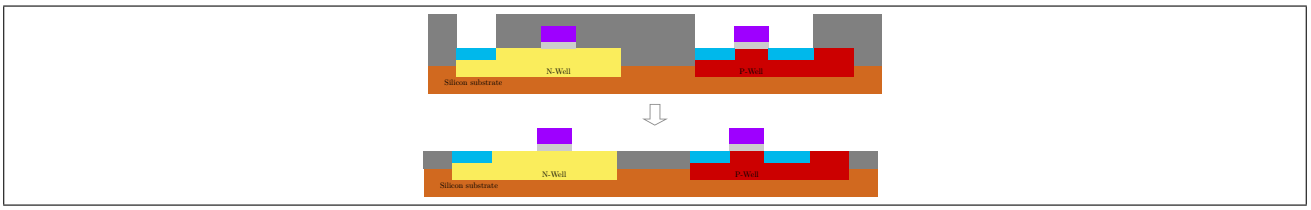

Figure 46: Oxide removal

6 p+ Implant

For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required. In this step we're going to build these.

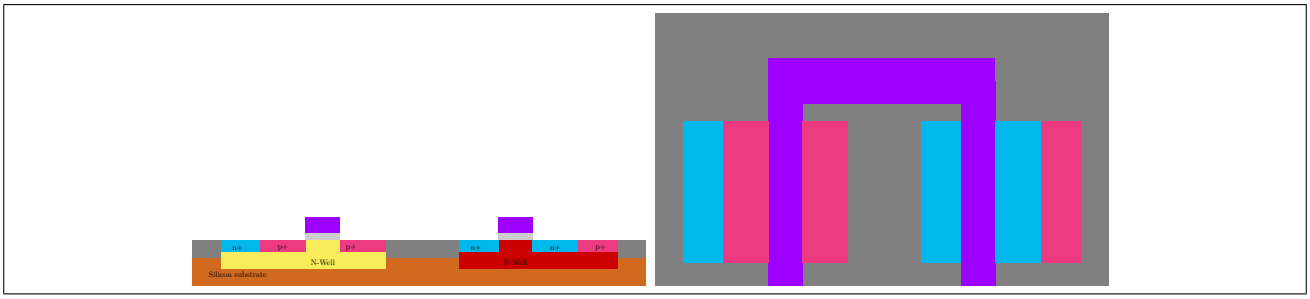

Figure 47: P+ implant geometry target

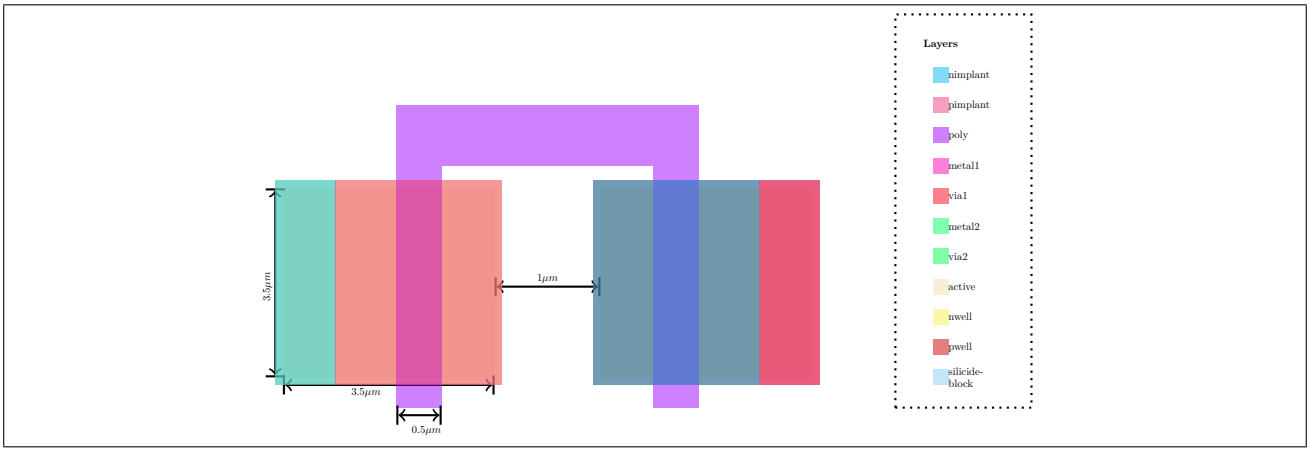

Figure 48: P+ layout

6.1 Mask dioxide layer

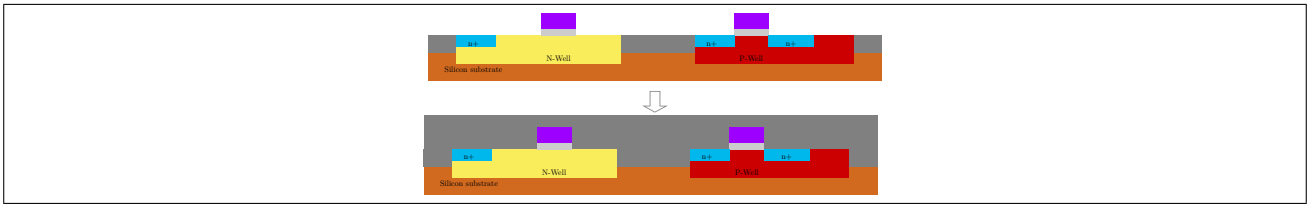

Figure 49: Oxide layer

6.2 Pattering

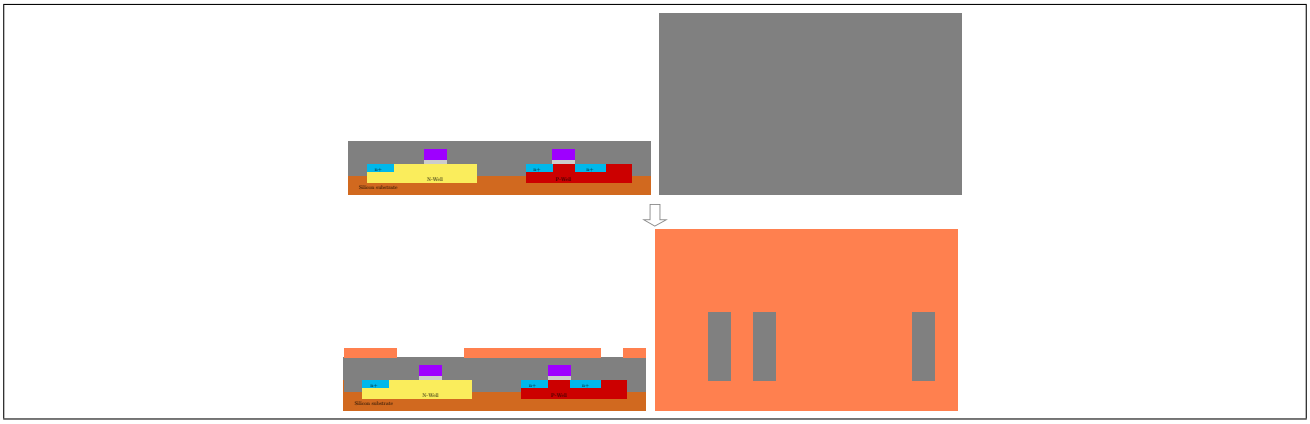

Figure 50: P+ region resist mask

6.3 Etching

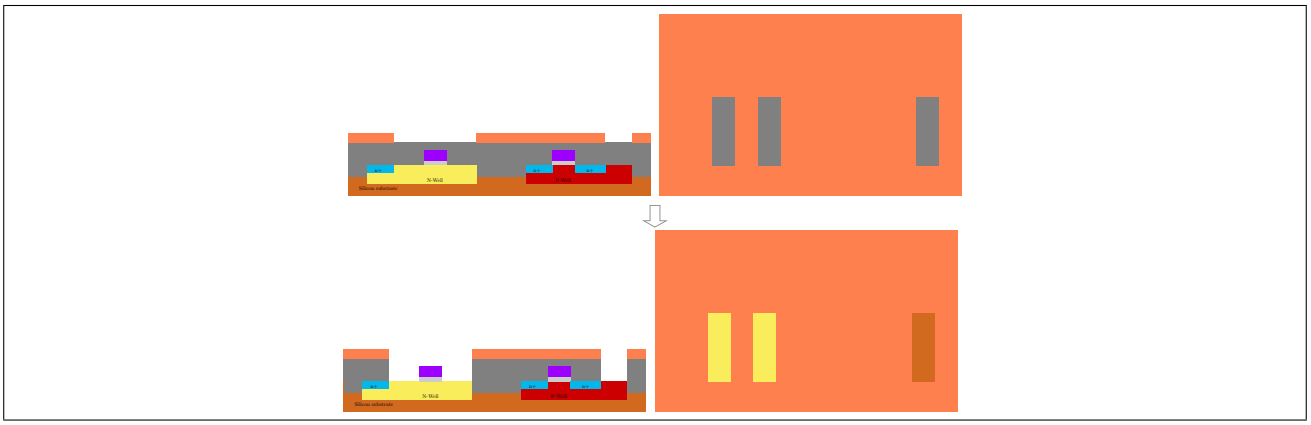

Figure 51: P+ region opened

6.4 Cleaning

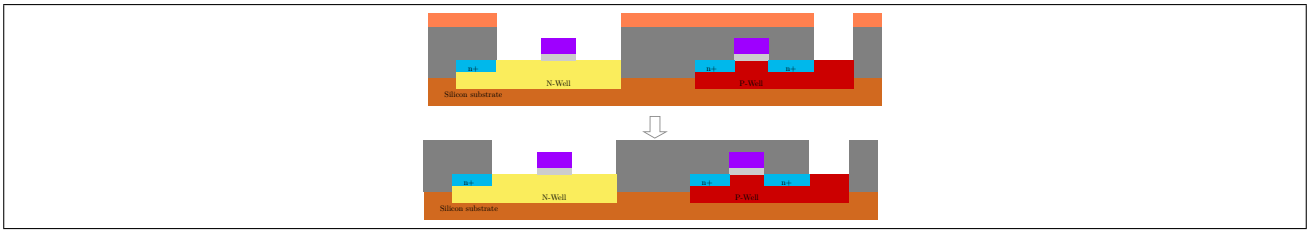

Figure 52: Resist removal

6.5 Injection

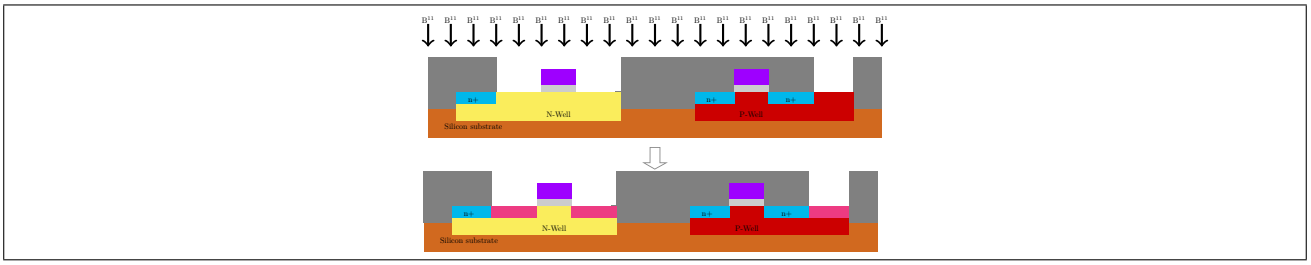

Figure 53: P+ injection process

6.6 Oxide removal

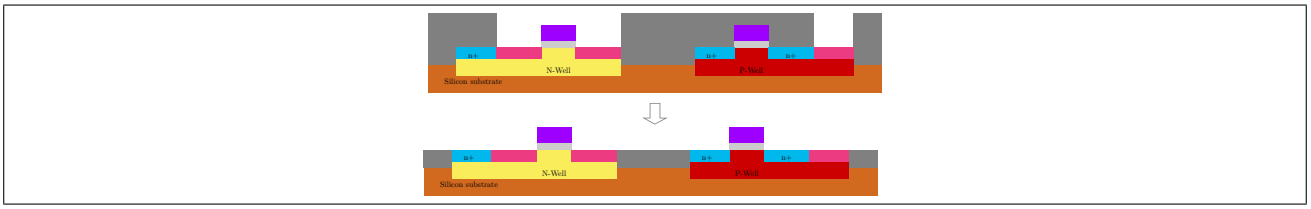

Figure 54: Oxide removal

7 Silicification

Titanium silicide is one of the first SALICIDE material introduced in ULSI devices owing to its low resistivity, high thermal stability, ease in deposition and compatibility with silicon processes. Titanium has been one of the familiar materials in ULSI productions, which is also an important advantage in practical use of titanium SALICIDE.[4]

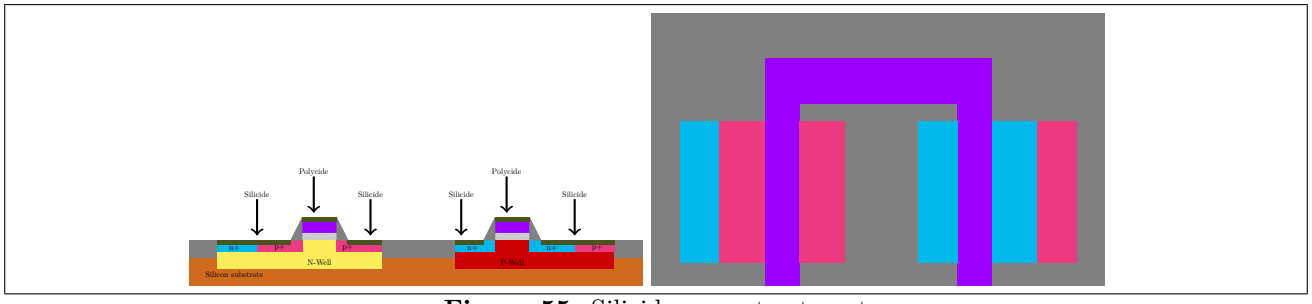

Figure 55: Silicide geometry target

In order to reduce the gate contact resistance as well as the source and drain resistance and in order to provide a more effective etch stop when plasma etching the contact windows to drain, source and gate, silicide/polycide is being added to the wafer as shown in Figure 55.

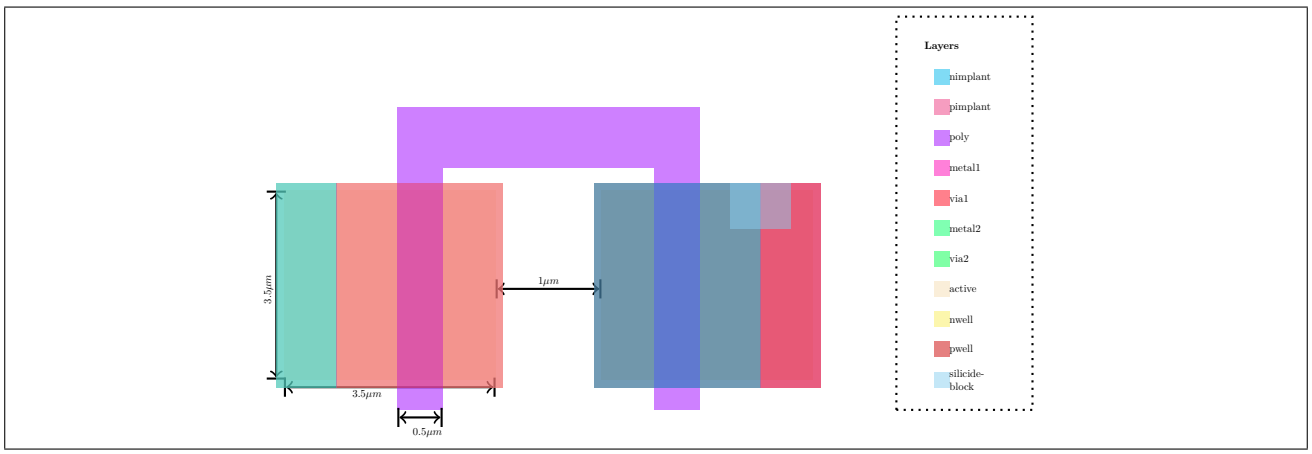

Figure 56: Silification layout

When titanium and silicon are brought into contact and heated at temperatures above 500 °C (in the presence of excess silicon) the higher-resistivity C49-$TiSi_2$ phase forms before the low-resistivity phase.
The C49-$TiSi_2$ phase has an orthorhombic base-centered structure with 12 atoms per unit cell and a resistivity of $60 - 90\mu\Omega - cm$.
The C54-$TiSi_2$ phase has an orthorhombic face-centered structure having 24 atoms per unit cell and a significantly lower resistivity ($12 - 20\mu\Omega - cm$) than the C49-$TiSi_2$.
The basic formation process of titanium SALICIDE is as follows:
A thin titanium film with 20-60 nm thickness is deposited on an entire wafer with MOSFETs structure. The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes by the first anneal at 600-700°C in N_2 ambient. In first anneal, C49-$TiSi_2$ phase is formed. Then, the unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution. The final step is second anneal at 800°C or above to transform high-resistivity C49-$TiSi_2$ phase to low-resistivity C54-$TiSi_2$ phase at the gate electrodes and source/drain areas.

[4] A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices, 07D53437, Ryuji Tomita

7.1 Oxide deposition

The thickness of this CVD deposited oxide layer will be the width of the spacer after having used highly anisotropic etching in the next few steps, for this reason the thickness of the oxide decides over the distance between the silicide and the gate oxide.
We make the oxide layer 50nm thick.

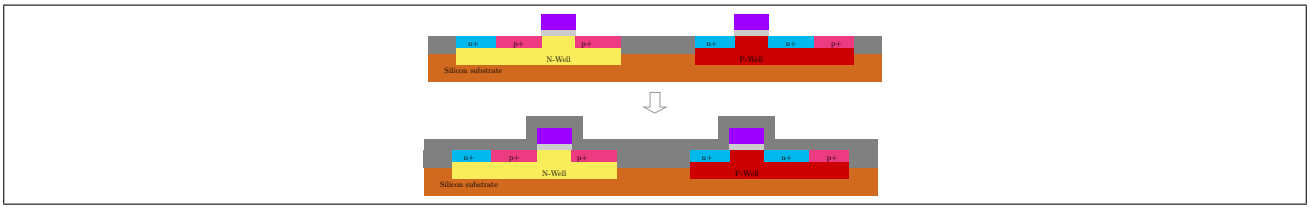

Figure 57: Oxide layer

We use the machine LPCVD machine from HKUST**??** and deposit around 50nm of silicon dioxide with the following recipe[5]:

- Temperature: 400 $°C$ ($SiH_4 + O_2 = SiO_2 + 2H_2$)
- Pressure = 250 mTorr
- Silane (SiH_4) flow = 40sccm
- Oxygen (O_2) flow = 48sccm

This will give a rate of 7nm ($\pm 1nm$) per minute, so we deposit for roughly seven minutes (7 min).

7.2 Silicide block patterning (optional)

We now have to pattern the mask for the silicide block layer which will produce oxide wherever no silicide is not desired within active areas.

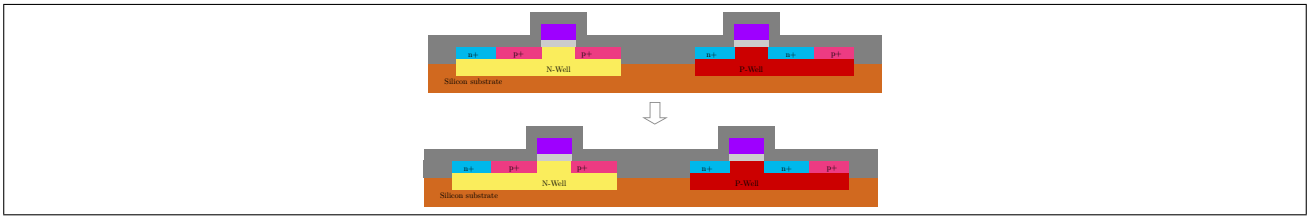

Figure 58: Patterning (silicide block)

7.3 Sputter etching(Spacers)

Now we have to etch our oxide as anisotropic as possible. This means that the etching mostly only comes "from above with a few to nearly none horizontal etching. That means the etching process only "sees" the sidewall as a "thicker layer" and starts etching downward. With an etching speed of 35 nm/min for thermal oxide and an oxide thickness of around 50nm and given that the polysilicon is much higher than 50nm we will have our desired spacer geometry forming as well as any potentially resist covered are (given silicide block is being used) with sharp etches.

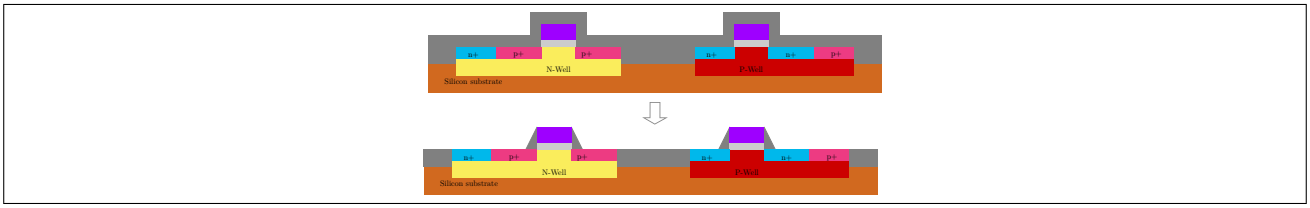

Figure 59: Anisotropic etching

The above mentioned machine is the "Trion RIE Etcher" at the NFF HKUST lab(**??**). The etching process runs on the oxide for 2 minutes.

[5] `https://people.rit.edu/lffeee/LPCVD_Recipes.pdf`

7.4 Titanium deposition

We deposit a layer of titanium with a thickness of around 20-60nm which will then be reacted into titanium-silicide and titanium-polycide respectively in the further steps.

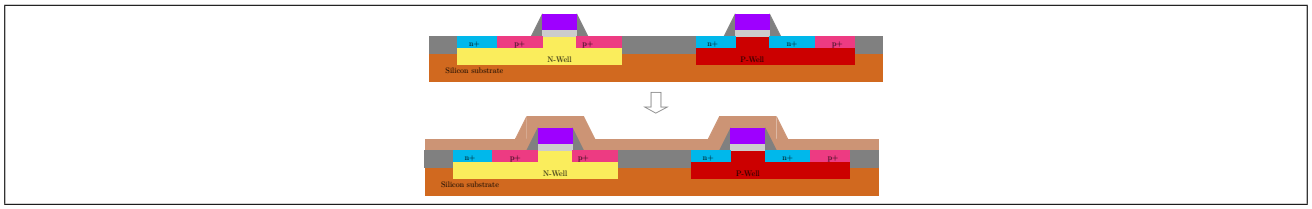

Figure 60: Titanium deposition

For this purpose we use the "Denton Sputter (SPT-Denton)" at HKUST NFF lab (**??**) which has a sputter rate of around 8.8 nm/min for titanium. This means we run the deposition process for around 5 minutes.

7.5 First reaction step

The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes by the first anneal at 600-700°C in N_2 ambient. In this first anneal, the C49-$TiSi_2$ phase is formed.

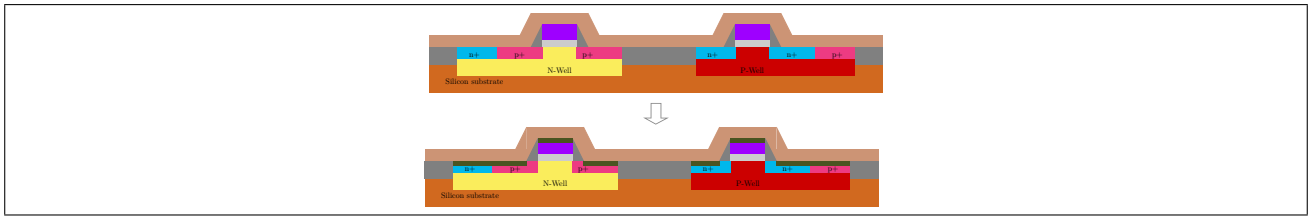

Figure 61: Reaction 1

We use the "AG610 RTP (DIF-R2)" from the HKUST**??** at 700°C for 240 seconds.

7.6 Etch

The unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution.

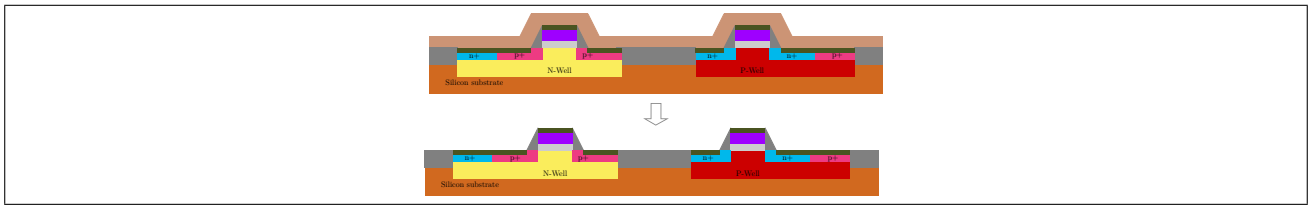

Figure 62: Titanium etch

7.7 Second reaction step

The final step is a second anneal at 800 °C or above to transform the high-resistivity C49-$TiSi_2$ phase to the low-resistivity C54-$TiSi_2$ phase at the gate electrodes and source/drain areas.

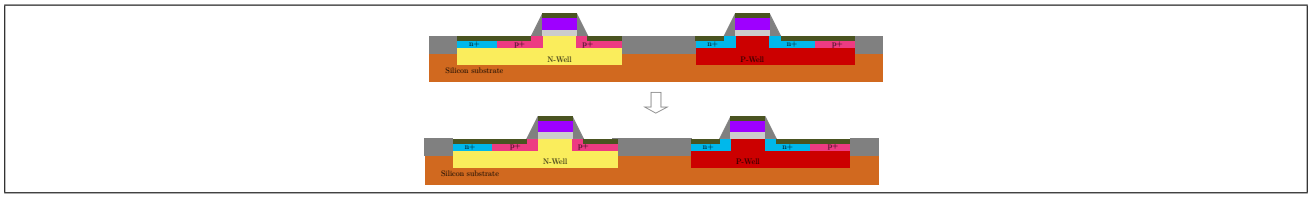

Figure 63: Reaction 2

We use the "AG610 RTP (DIF-R2)" again at 800°C for 240 seconds.

8 First vias

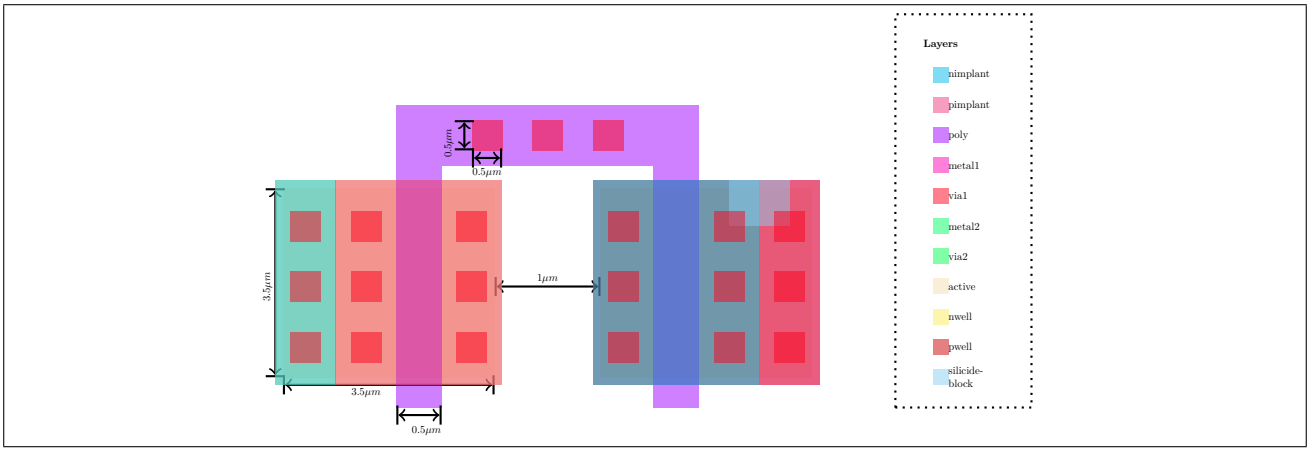

Figure 64: First via layout

9 First metal layer

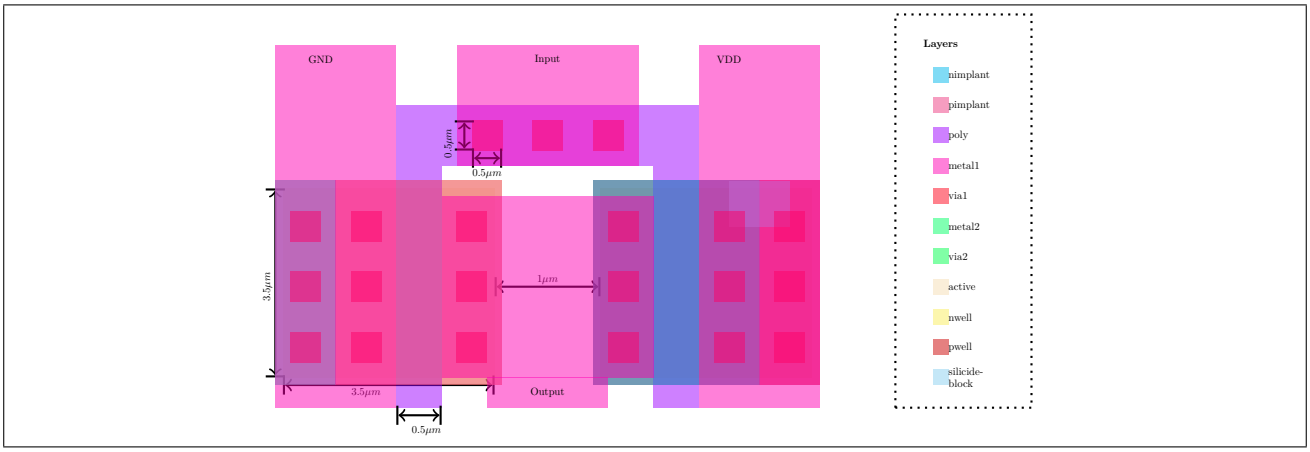

Figure 65: First metal layout

10 Additional vias

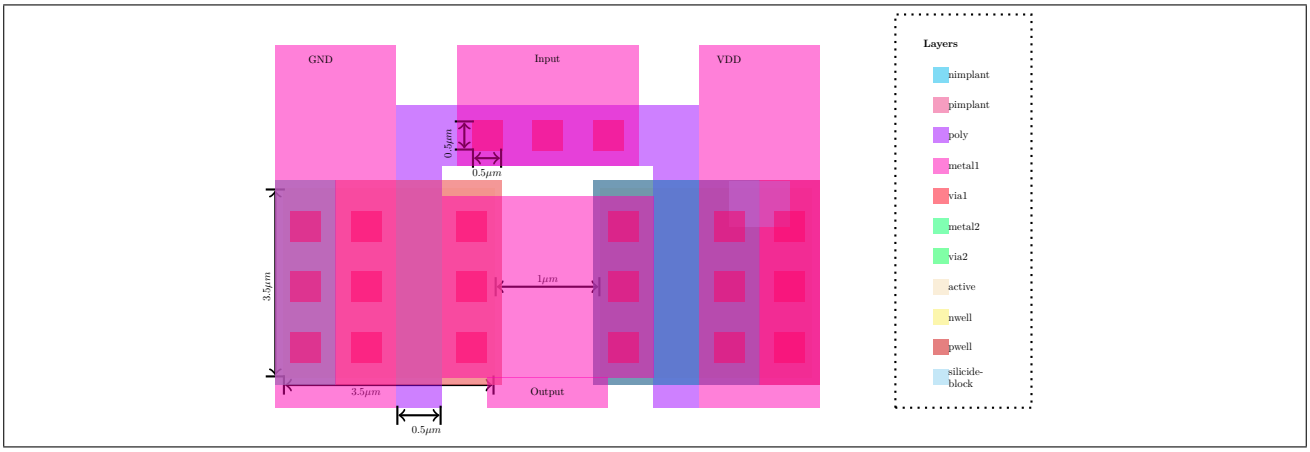

Figure 66: Additional via layout

11 Additional metal layer

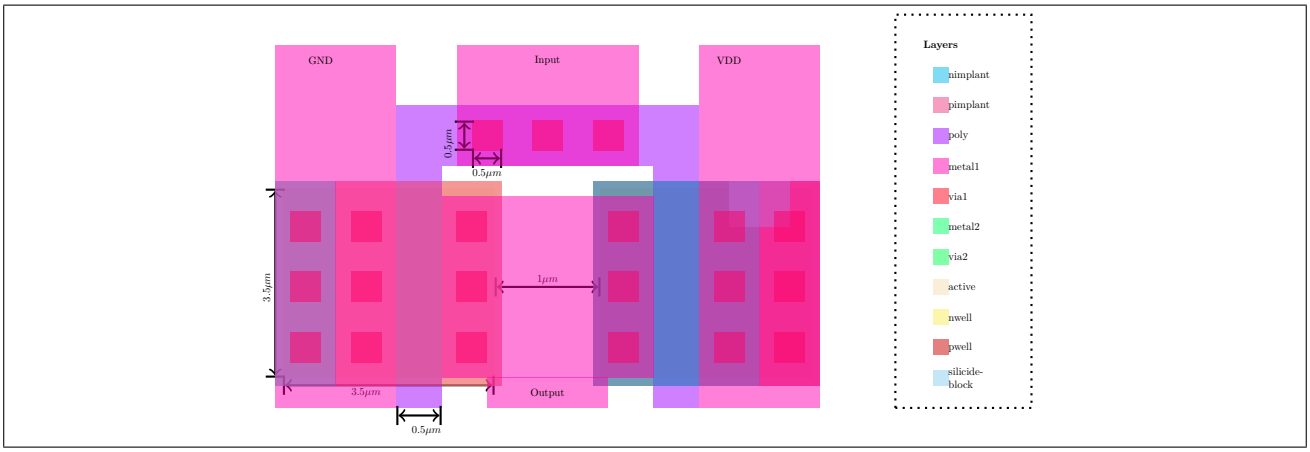

Figure 67: Additional metal layout