Libre Silicon process specification

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Abstract

This is the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1]and related free technology nodes from the LibreSilicon project.

[1]https://github.com/chipforge/StdCellLib

Contents

1 Discrete components

This basic initial process draft is CMOS only and for this reason only consists the two MOSFET typed n/p required to build CMOS technology. Resistors are not included within this initial process draft.

1.1 CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal–oxide–semiconductor field-effect transistors (MOSFET) are required.

Historicaly, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

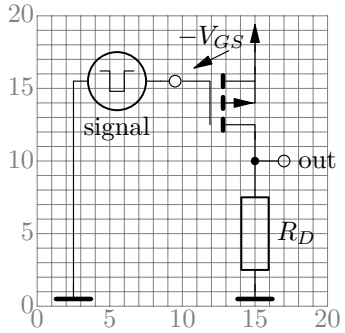


Figure 1: enhancement-mode PMOS transistor use-case

The sectional view of a PMOS transistor in silicon is being shown below

Historicaly later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

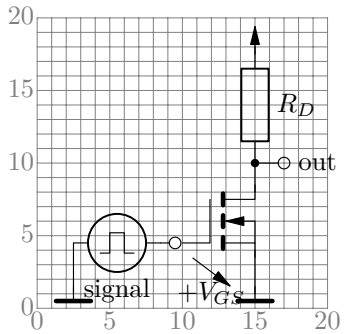


Figure 2: enhancement-mode NMOS transistor use-case

The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning also higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, now currents flows between Drain and Source anymore, the power consumption of the chip also goes low. Et violà, the US-Patent with Number 3356858[2]changed the world and combines both technologies to the new complementary metal-oxide-semiconductor (CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

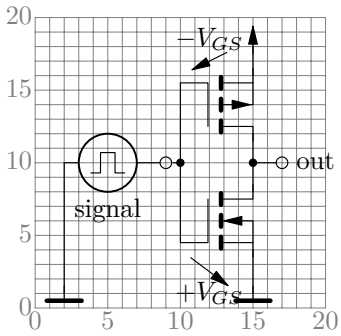
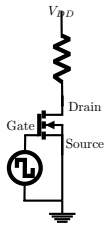


Figure 3: complementary PMOS and NMOS transistor couple use-case

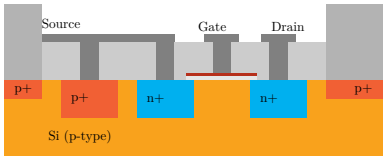
The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

1.2 NMOS

The following circuit symbol will be used throughout the document for symbolizing a NMOS transistor



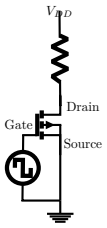
The geometry in silicon is being shown below



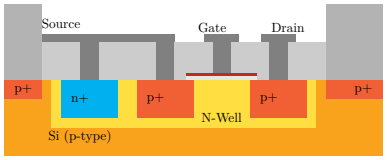
[1]https://www.google.com/patents/US3356858

1.3 PMOS

The following circuit symbol will be used throughout the document for symbolizing a PMOS transistor



The geometry in silicon is being shown below

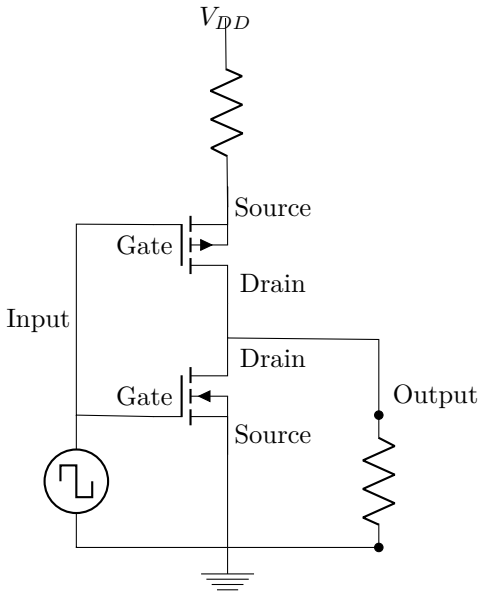


2 CMOS example

This section describes the example circuit on which based the process will be elaborated. It may variate slightly from the geometry of the actual transistors used in the LibreSilicon library because it is merely meant for explanatory purposes only.

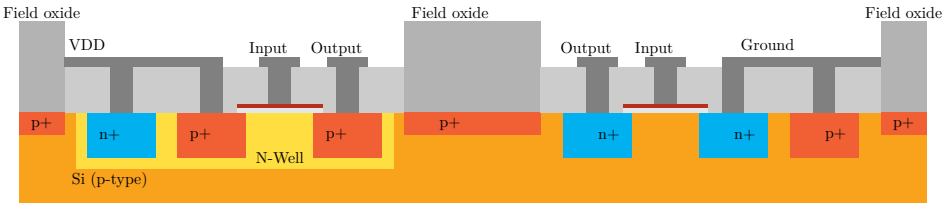
2.1 Schematic

The example which will be used for showing the process steps will be a simple CMOS inverter of which the schematics are drawn below



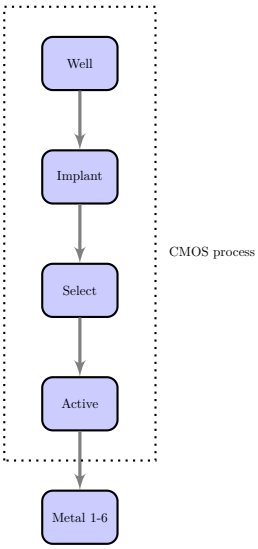
2.2 Geometry cross section

Below the cross section view of the inverter circuitry can be seen. For the run through of this process we will use this cross section diagram as reference.



3 Process

Below the general flow chart of the overall process flow can be seen. These process steps will be discussed within the following sections.



The four starting overall process steps are part of an overall active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world. For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The decision to use an n-well approach is based largely on the compatibility with the existing nMOS process. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

3.1 Initial cleaning

In order to remove the initial naturally grown silicon dioxide from the wafer, acid is being applied to the wafer which leads to a pure silicon substrate wafer as in the process illustration shown below.

This needs to be done because the naturally grown initially existing silicon oxide is not pure and may contain contamination which may render the final product unusable.

3.1.1 Sulfuric Cleaning

The sulfuric acid mixture, $H_2SO_4 + H_2O_2$ is being applied to the wafer for 10 minutes at a temperature of 120 °C.

3.1.2 HF dip

After the sulfuric cleaning a HF (HF:H_2O , 1:50) dip is being performed for one minute.
Hydrofluoric acid (HF) is used to remove native silicon dioxide from wafers. Since it acts quickly, one needs to only expose the wafer for a short time (”dip”). After that the wafer needs to be dried and quickly processed further before new uncontrolled natural oxide can build up on the wafer through the contact with air.

3.2 Well

In order to build CMOS (Complementary metal–oxide–semiconductor/P and N MOS) on the same substrate an n-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The n-well will serve us as an island of n-doped substrate within the p-doped basis substrate. The cross section as well as the top view of the targeted geometry are shown below.

3.2.1 Dioxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

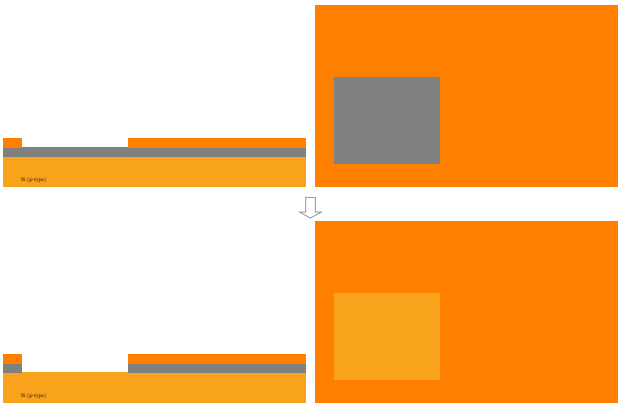
There is no clear general equation perfectly describing the dopant absorption behavior of silicon dioxide but the industrial best practice is a layer of around (500nm≈5000Å) thickness or more. For this purpose the wafer is being oxidized for at least 90 minutes at 1000°C using wet oxidation which results in a dioxide layer at least 500nm(≈5000Å) in thickness.

3.2.2 Patterning

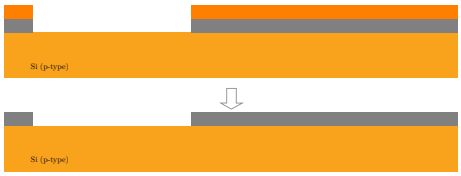
The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”nwell” layer within the GDS2 file.

The thickness of the resist layer and the backing duration will variate depending on the specific equipment for which this process will be implemented with.

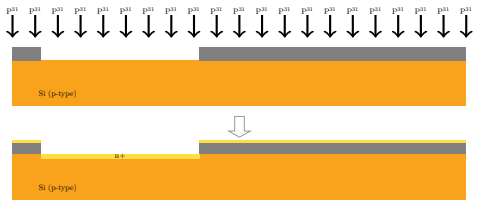
3.2.3 Etching



3.2.4 Cleaning



3.2.5 Predeposition



The n-well is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 KeV. The n-well is then annealed.

3.2.6 Sacrificial oxide

The wafer is being oxidized for 32 minutes at 1000°C in order to achieve a cover silicon layer of 250nm thickness (≈2500Å).

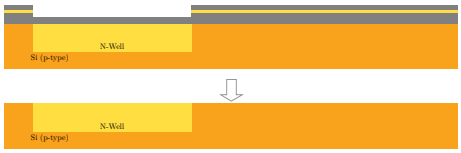
3.2.7 Infusion

In order to drive the carrier atoms deeper into the crystalline structure the wafer needs to be driven in after predeposition.

In this step the wafer is driven-in for 960 minutes at 1150°C in an inert ambient.

3.2.8 Oxide removal

We want an oxide free wafer with the n-well accessible for the further process steps.



We use hydrofluoric acid, because it doesn't etch silicon at all but is very aggressive towards SiO_2

For hydrofluoric acid in combination with SiO_2 the following reaction formula can be used

$$4HF_{(aq]} + SiO_{2(s]} \rightarrow SiF_{4(g]} \uparrow + 2H_2O_{(l]} \tag{1}$$

while with non oxidized silicon there is no reaction.

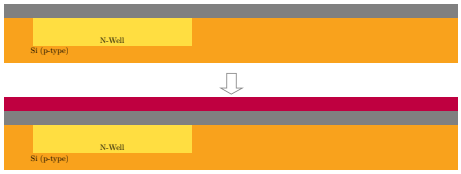
3.3 Channel stop

The channel-stop is material with the primary function to limit the spread of the channel area and to prevent the formation of parasitic channels. It is a highly doped p+ area. Its top view and cross section can be seen below.

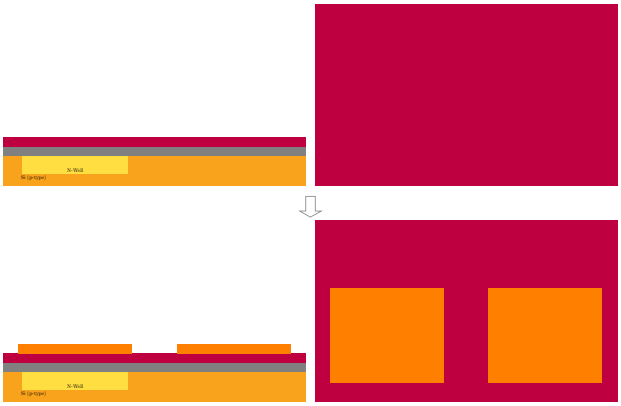
It surrounds all the active areas and covers all the non-active area. The channel-stop region is always accompanied by the field oxide layer and shares the same layout mask (just inverted) with it.

3.3.1 Dioxide layer

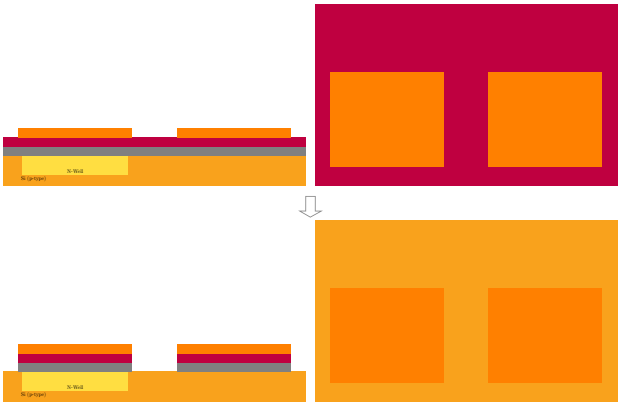
3.3.2 Nitride layer



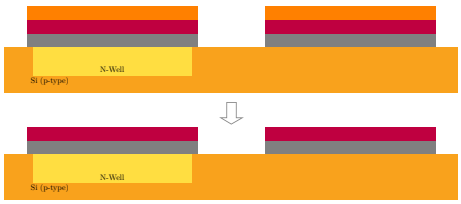
3.3.3 Patterning



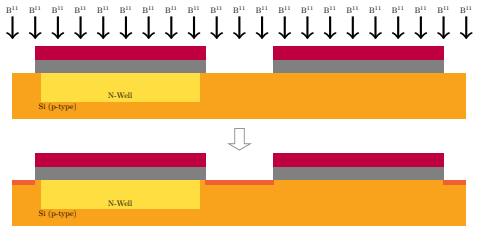
3.3.4 Etching



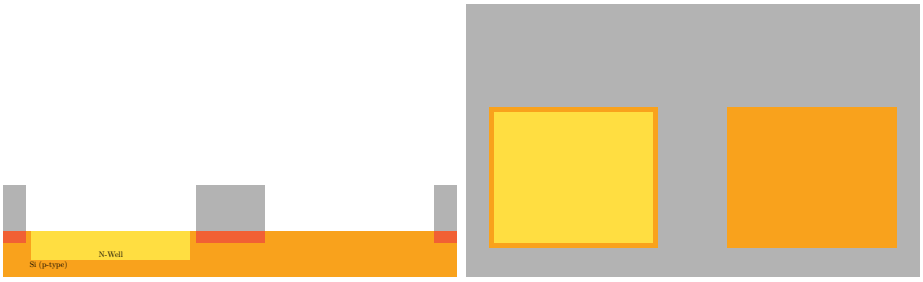
3.3.5 Cleaning



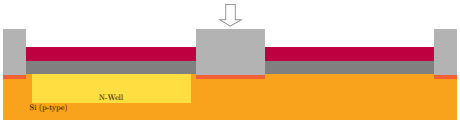
3.3.6 Predeposition



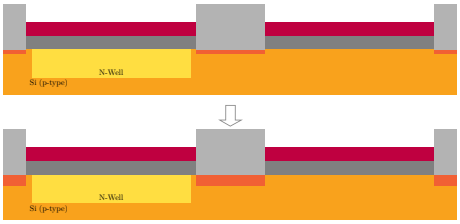
3.4 Field oxide



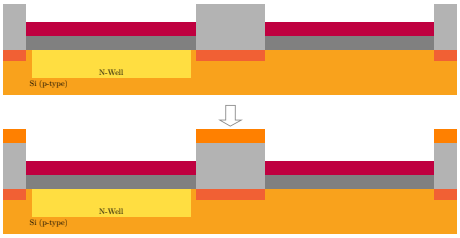
3.4.1 Thick oxide layer



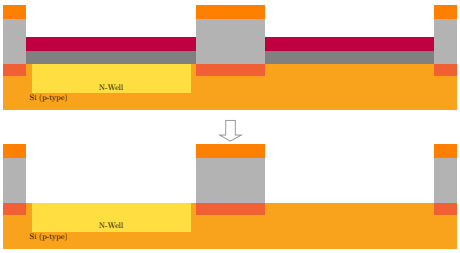
3.4.2 Infusion



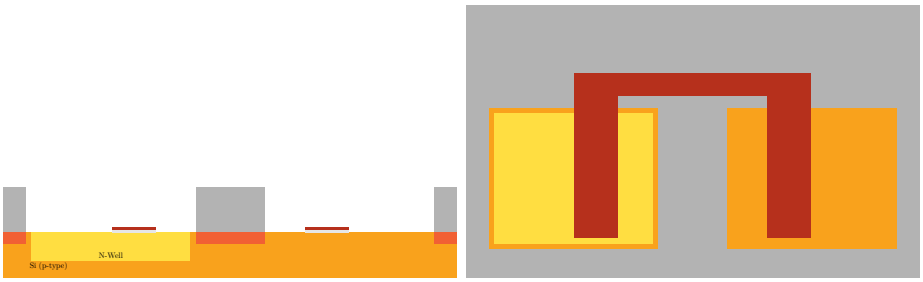
3.4.3 Patterning



3.4.4 Etching

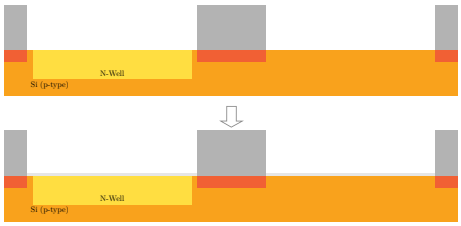


3.5 Active

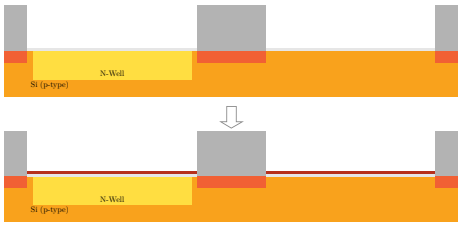


3.5.1 Gate oxide growth

The thickness of the gate oxide depends the capacity (slew rate) of the transistor. The thinner the layer is, the steeper the edges of the CMOS circuitry will be, however also the threshold voltage will be reduced the thinner the gate oxide gets.

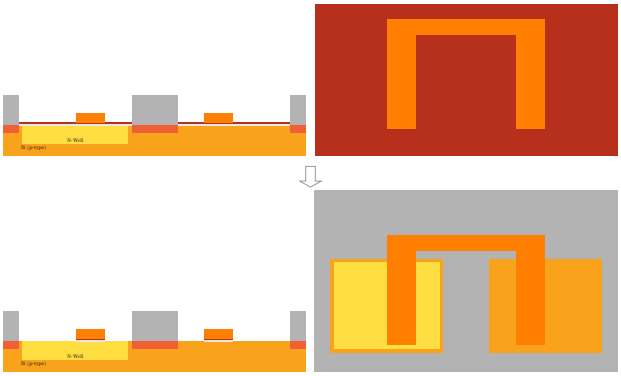


3.5.2 Polysilicon growth



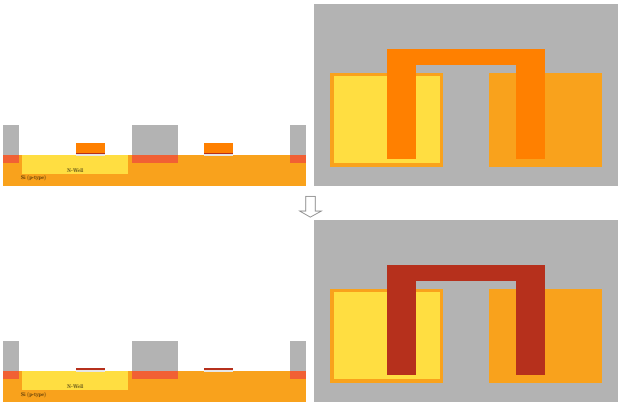
3.5.3 Patterning

3.5.4 Etching

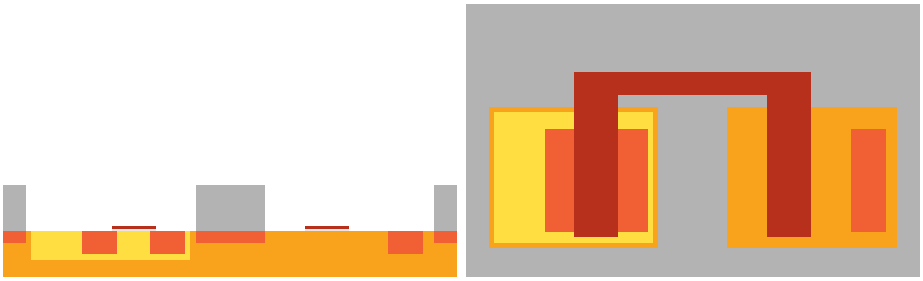


Because the exact shape of the gate contact is required for a reproducible property characterization of the transistor geometry, dry etching is being used for etching the poly-oxide layer stack.

3.5.5 Cleaning

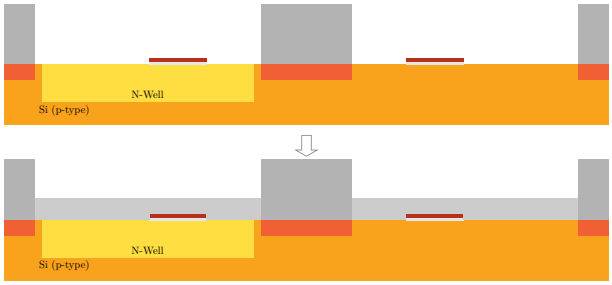


3.6 p+ Implant

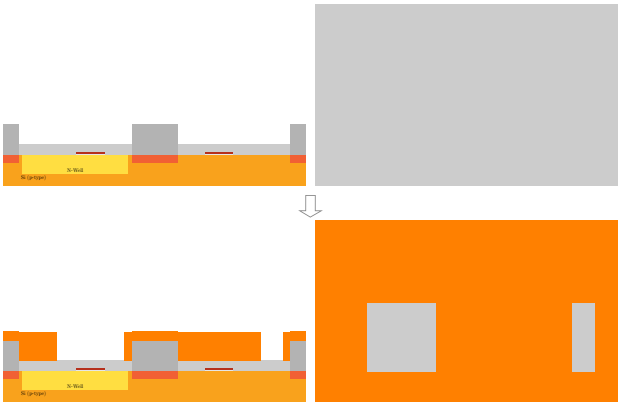


For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required. In this step we're going to build these.

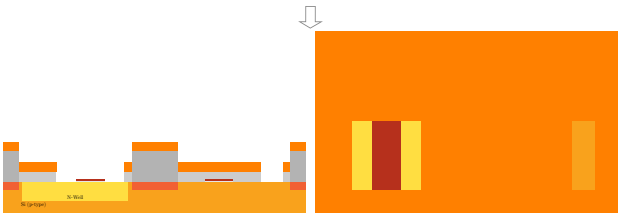
3.6.1 Dioxide layer



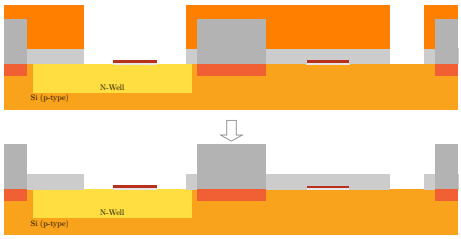
3.6.2 Pattering



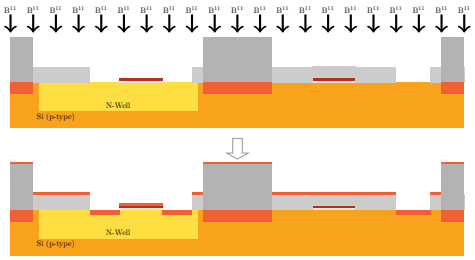
3.6.3 Etching



3.6.4 Cleaning

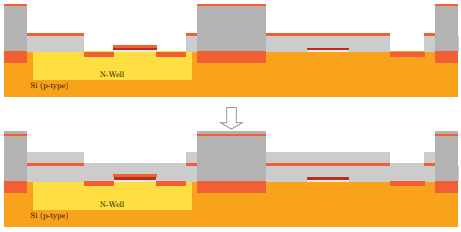


3.6.5 Predeposition

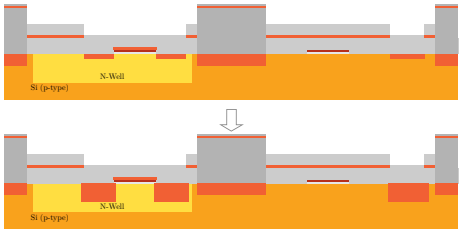


The p+ islands are implanted with a Boron (B^{11}) dose of $4 \times 10^{11} cm^{-2}$ at an energy of 35 KeV.

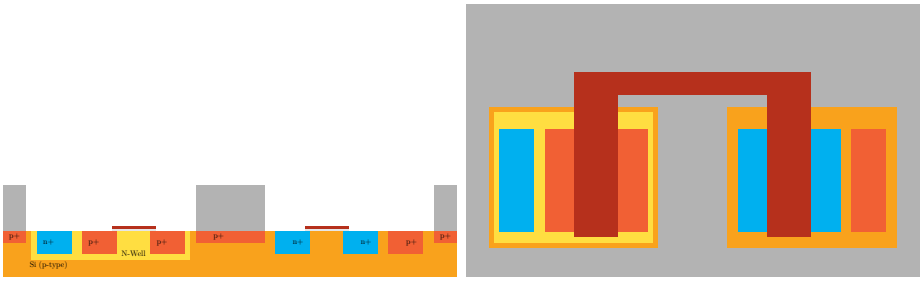
3.6.6 Sacrificial oxide



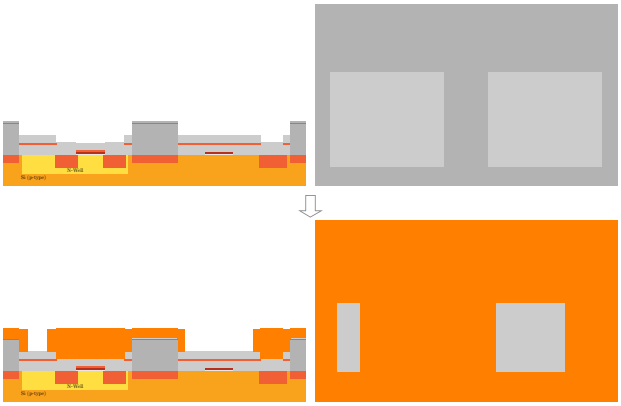
3.6.7 Infusion



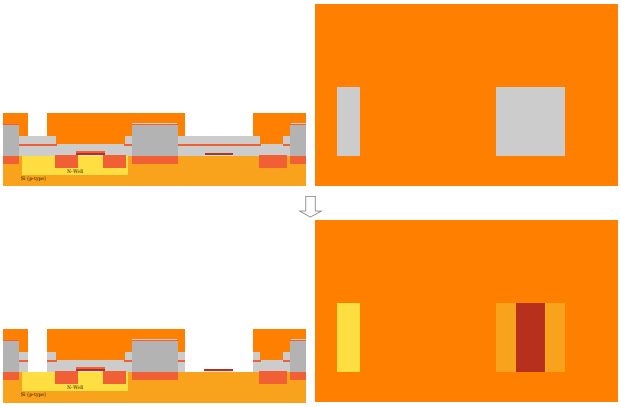
3.7 n+ Implant



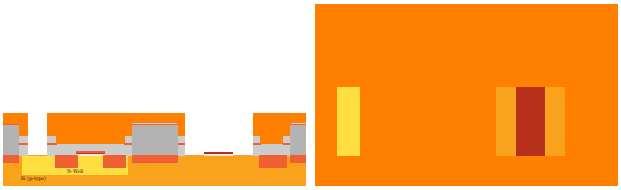
3.7.1 Pattering

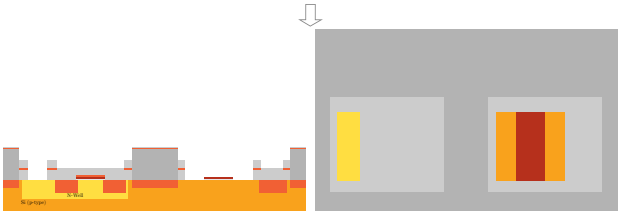


3.7.2 Etching

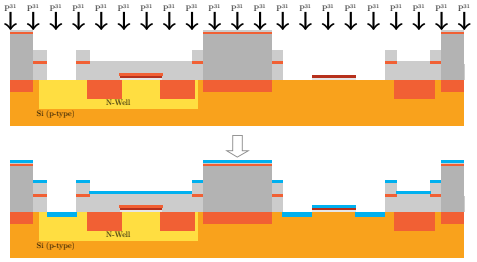


3.7.3 Cleaning

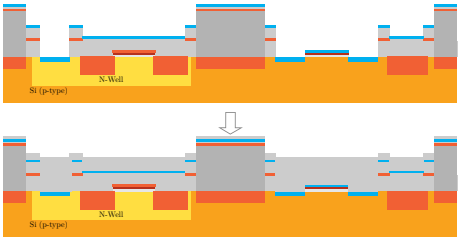




3.7.4 Predeposition



3.7.5 Sacrificial oxide



3.7.6 Infusion