## Abstract

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This is the specification of the free silicon manufacturing standard for manufacturing the ls018<sup>1</sup> standard logic cells and related free technology nodes from the LibreSilicon project.

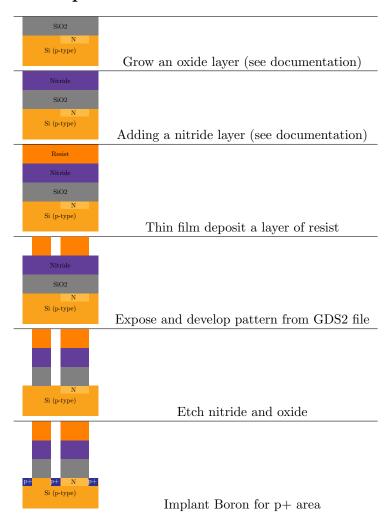
For further clarification consult the complete documentation of the process.

## 1 Well

Si (p-type)	Start with a p-type silicon wafer
SiO2	
Si (p-type)	Grow an oxide layer
Resist	
SiO2	
Si (p-type)	Thin film deposit a layer of resist
SiO2	
Si (p-type)	Expose and develop the pattern from the GDS2 layer information
Si (p-type)	Etch the oxide layer
Si (p-type)	Implant Phosphorus (P); Create N-well
N	
Si (p-type)	Remove resist
N Si (p-type)	Remove oxide
Si (p-type)  N Si (p-type)  N Si (p-type)	Etch the oxide layer  Implant Phosphorus (P); Create N-well  Remove resist

<sup>&</sup>lt;sup>1</sup>https://github.com/leviathanch/ls018

## 2 Implant



- 3 Select
- 4 Active
- 5 Metal