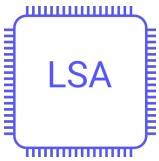
Libre Silicon 1.0μm process:

LS1UH

Hightech variant



DESCRIPTION

The LibreSilicons LS1UH process is a contemporary engineered 1.0 micron modular mixed signal CMOS technology for high reliability. Based upon the common single poly with up to 3 metal layers 1.0 micron drawn gate length and a twin-well process, enriched with newer features as non-volatile memory. The platform is ideal for mixed-signal applications in harsh environments, as well as emdedded systems reliable over large temperature and voltage supply ranges. Fitting for many applications in infrastructure, industrial and consumer market. Delivered NDA-free with industrial standard design rules, precise SPICE models, analog and digital libraries. IPs and development kits support the process for free and open source tools.

KEY FEATURES OVERVIEW

- 1.0-micron single poly, up to three-metal
- Twin-well CMOS process
- Lateral PNP/NPN BJT devices
- Integrated digital, analog and NVM in a single process
- Wide supply voltage range from 3.0V to 18V (max. 40V)
- Extended temperature range from -55$°C$ up to +125$°C$
- Shallow trench isolation for all MOS devices
- Insensitive towards cosmic radiation
- ESD protected
- Low-noise PMOS/NMOS transistors
- High-reliability NVM using SONOS technology
- 7 corner case models (typical/worst/best)
- Community based
- Under free license, no NDA

APPLICATIONS

- Analog and mixed-signal Circuits
- Avionics
- Infrastructure
- Automotive
- Robotics
- Safety

PRIMITIVE DEVICES

- PMOS/NMOS transistors
- SONOS flash cells
- Lateral PNP/NPN BJTs
- SRAM cells
- Poly, Metal, Diffusion Resistors
- Protection, Polysilicon diodes

LS1UH DEVICES CROSS SECTION

CMOS

Below you can see the cross section of the low power MOSFETs for the CMOS logic.

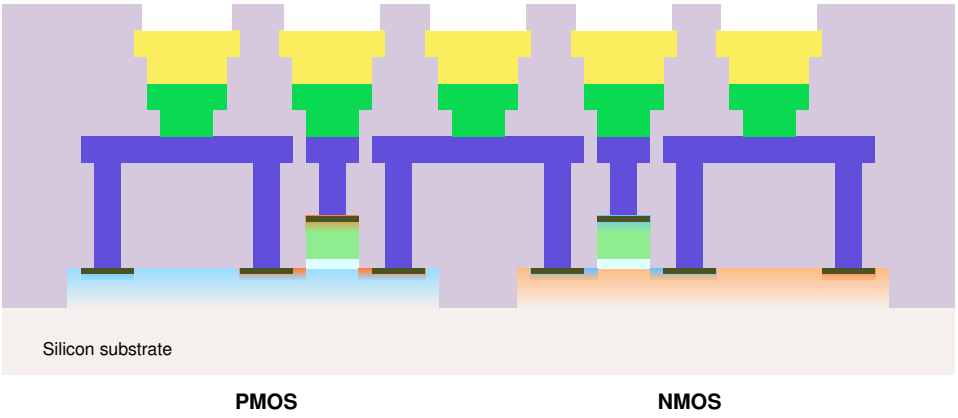


Figure 1: CMOS MOSFETs

The CMOS n-channel enhancement MOSFET and p-channel enhancement MOSFET transistors are being isolated from each other with shallow trench isolation (STI) which is being filled with a low permittivity, low temperature, low density oxide (LTO is 5 times less dense than thermal oxide). The gate dielectricum is a 40nm thermal silicon dioxide layer which results in a break through voltage of around 40V and above. The threshold voltage of the transistors have been dimensioned to be around +0.7V and -0.7V respectively.