Libre Silicon process specification

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Abstract

This is the specification of the free silicon manufacturing standard for manufacturing the ls180nm[1]standard logic cells and related free technology nodes from the LibreSilicon project.

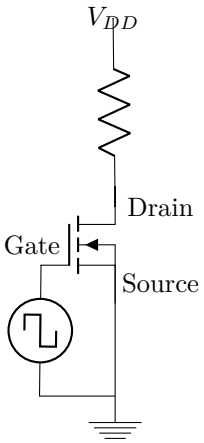
[1]https://github.com/leviathanch/ls180nm

1 Discrete components

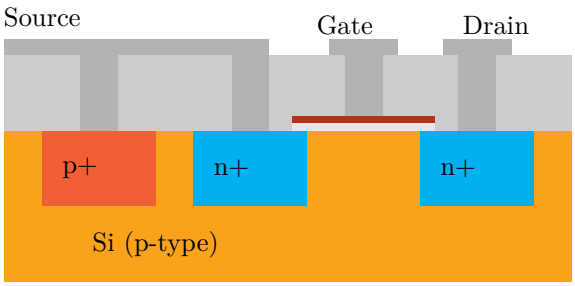
This basic initial process draft is CMOS only and for this reason only consists the two MOSFET typed n/p required to build CMOS technology. Resistors are not included within this initial process draft.

1.1 NMOS

The following circuit symbol will be used throughout the document for symbolizing a NMOS transistor

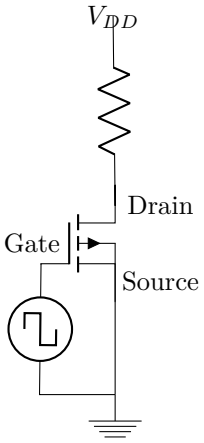


The geometry in silicon is being shown below

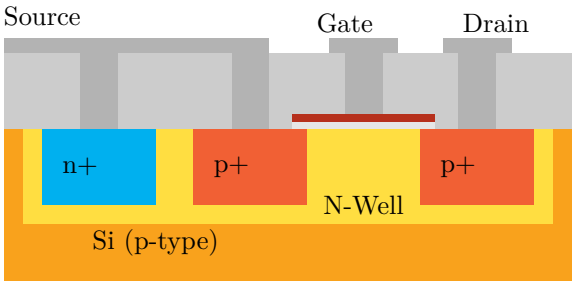


1.2 PMOS

The following circuit symbol will be used throughout the document for symbolizing a PMOS transistor

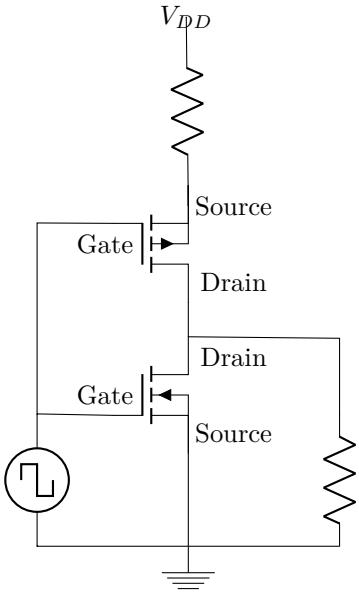


The geometry in silicon is being shown below

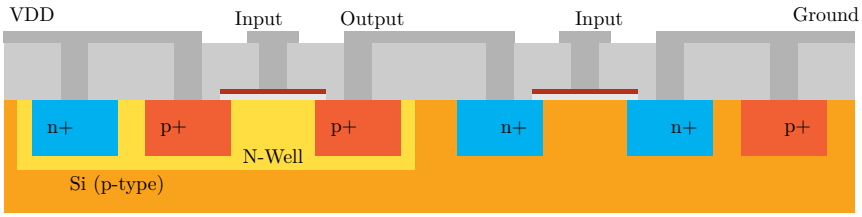


2 CMOS example

The example which will be used for showing the process steps will be a simple CMOS inverter of which the schematics are drawn below

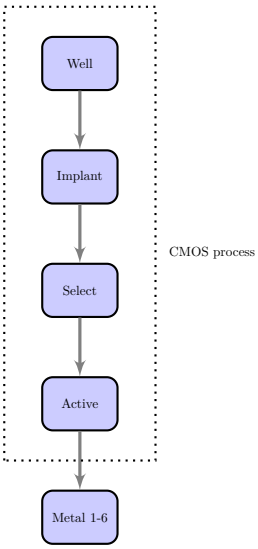


Below the cross section view of the inverter circuitry can be seen. For the run through of this process we will use this cross section diagram as reference.



3 Process

Below the general flow chart of the overall process flow can be seen. These process steps will be discussed within the following sections.



The four starting overall process steps are part of an overall active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world. For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The decision to use an n-well approach is based largely on the compatibility with the existing nMOS process. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

3.1 Well

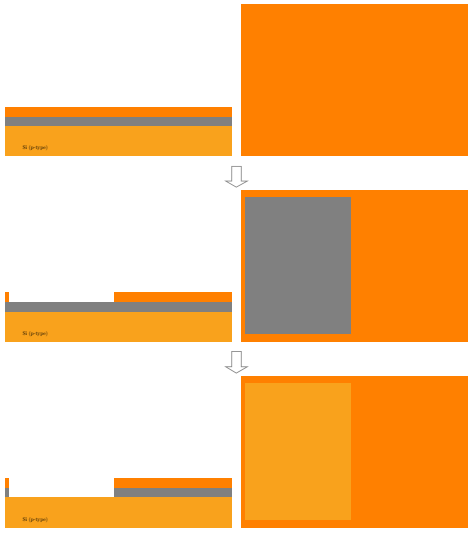
In order to build CMOS (Complementary metal–oxide–semiconductor/P and N MOS) on the same substrate an n-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The n-well will serve us as an island of n-doped substrate within the p-doped basis substrate. The cross section as well as the top view of the targeted geometry are shown below.

3.1.1 Dioxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

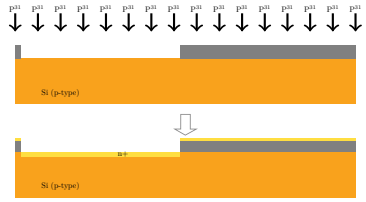
There is no clear general equation perfectly describing the absorption behavior of silicon dioxide but the industrial best practice is a layer of around (500nm≈5000Å) thickness or more. For this purpose the wafer is being oxidized for at least 90 minutes at 1000°C using wet oxidation which results in a dioxide layer at least 500nm(≈5000Å) in thickness.

3.1.2 Patterning and etching



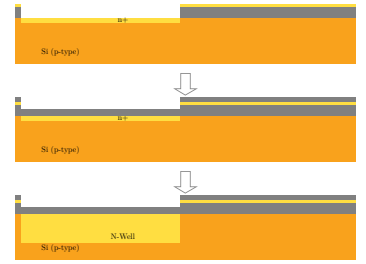
The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "nwell" layer within the GDS2 file. The thickness of the resist layer and the backing duration will variate depending on the specific equipment for which this process will be implemented with.

3.1.3 Predeposition



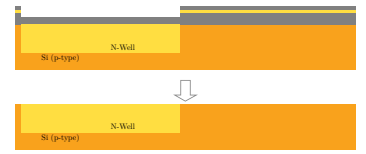
The n-well is implanted with a P^{31} dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 KeV.

3.1.4 Infusion



The n-well is then annealed, oxidized (250nm≈2500Å) for 32 minutes at 1000°C, and then driven-in for 960 minutes at 1150°C in an inert ambient.

3.1.5 Cleaning



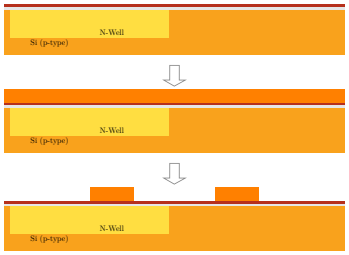
We use hydrofluoric acid, because it doesn't etch silicon at all but is very aggressive towards SiO_2

3.2 Active

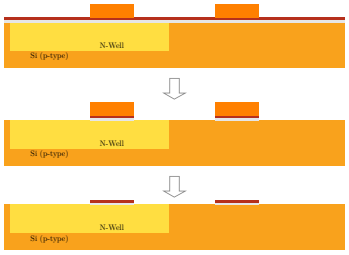
3.2.1 Gate oxide growth

3.2.2 Polysilicon growth

3.2.3 Patterning



3.2.4 Etching



Because the exact shape of the gate contact is required for a reproducible property characterization of the transistor geometry, dry etching is being used for etching the poly-oxide layer stack.

3.3 Implant

3.4 Select

3.5 Metal