# Libre Silicon process specification

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**Abstract**



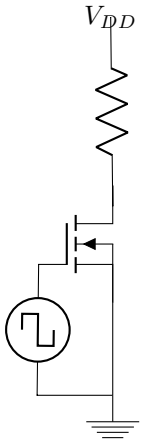
This is the specification of the free silicon manufacturing standard for manufacturing the ls018[1]standard logic cells and related free technology nodes from the LibreSilicon project.

[1]https://github.com/leviathanch/ls018

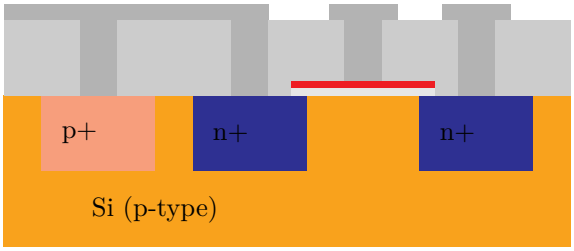
# 1 Components

## 1.1 NMOS

The following circuit symbol will be used throughout the document for symbolizing a NMOS transistor



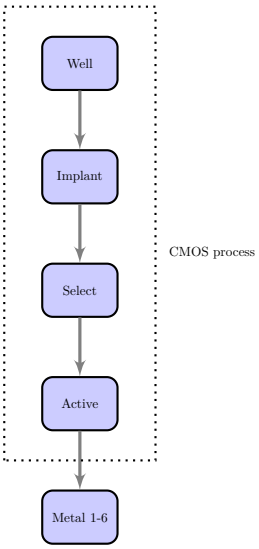

The geometry in silicon is being shown below




## 1.2 PMOS

# 2 Process

Below the general flow chart of the overall process flow can be seen. These process steps will be discussed within the following sections.



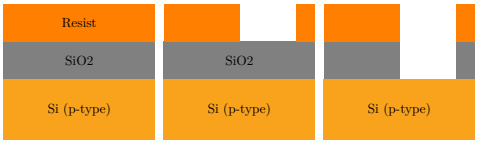

The four starting overall process steps are part of an overall active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world. For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL.

## 2.1 Well

### 2.1.1 Dioxide layer

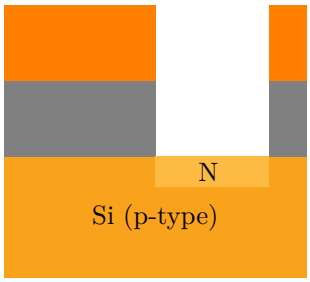

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide ($SiO_2$) layer needs to be grown on top of a p-type substrate. There is no clear general equation perfectly describing the absorption behavior of silicon dioxide but the industrial best practice is a layer of around $1\mu$m (1000nm) thickness.

### 2.1.2 Pattering and etching



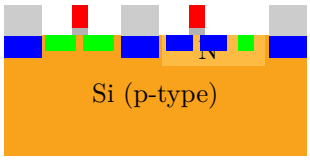

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”nwell” layer within the GDS2 file. The thickness of the resist layer and the backing duration will variate depending on the specific equipment for which this process will be implemented with.

### 2.1.3 Infusion

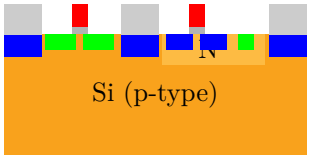



The decision to use an n-well approach is based largely on the compatibility with the existing nMOS process. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$. The n-well is implanted with a $P^{31}$ dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 KeV. The n-well is then annealed, oxidized for 32 minutes at 1000°C, and then driven-in for 960 minutes at 1150°C in an inert ambient.

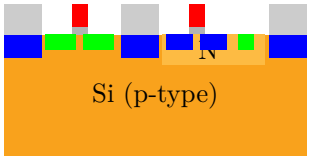
## 2.2 Implant




## 2.3 Select




## 2.4 Active




## 2.5 Metal