LibreSilicon process HKUST (NFF)

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July 26, 2018

Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

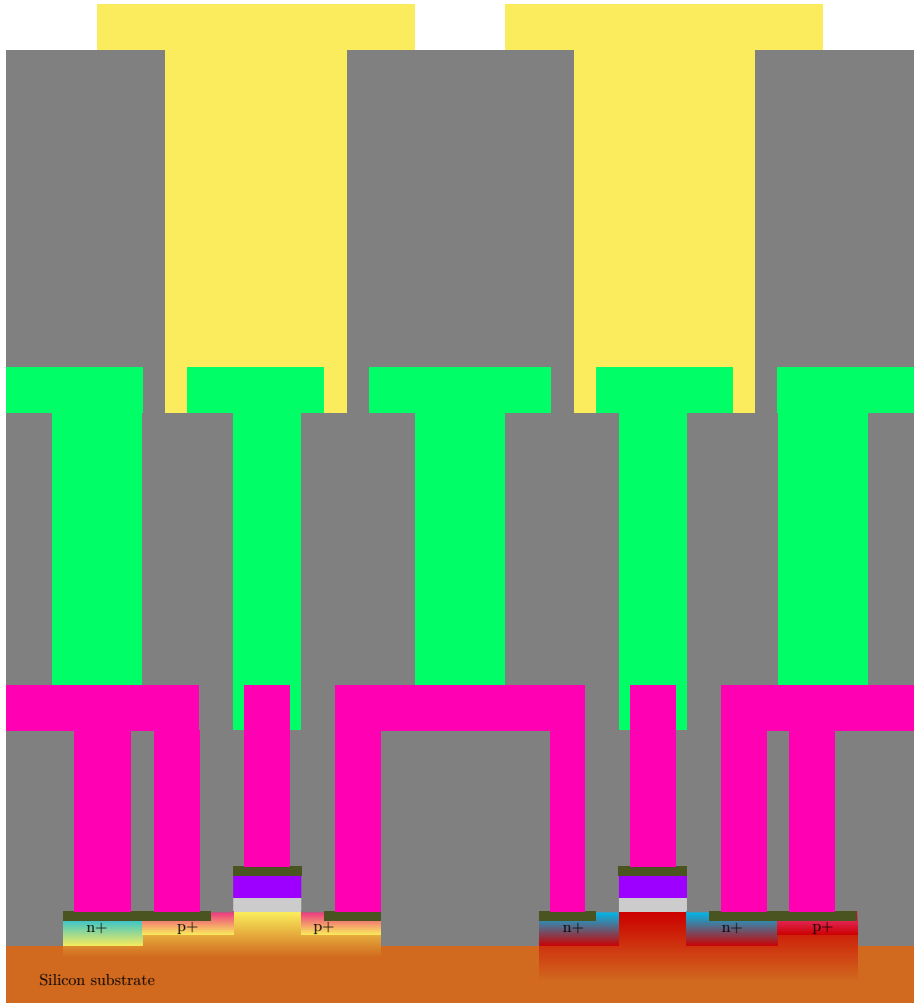
For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected. Please see the document with the generic steps[2] in order to get a detailed description of the different steps.

[1] https://github.com/chipforge/StdCellLib

[2] https://github.com/libresilicon/process/raw/master/process_steps/process_hightech/process_hightech_steps.pdf

Process Flow of Lanceville Technologies LibreSilicon $1\mu m$

- Project: LibreSilicon $1\mu m$
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer <100>
- Date: July 26, 2018



1 Initial alignment mask

Mask: basic

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean
Clean
Clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
1.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Initial Cleaning	H2SO4+H2O2, 10mins @ 120°C
1.2	A2:HF:H2O (1:50) (WET-A2)	P2-01000	Clean	HF dip	1 min
1.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
1.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
1.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
1.6	Lam 490 etcher (DRY-490)	P2-01000	Clean	Etching the alignment crosses from HKUST	1 minute ($2\mu m$)
1.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

2 Shallow trench isolation


Mask: active

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
2.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
2.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
2.3	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
2.4	DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	1 minute ($2\mu m$)
2.5	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

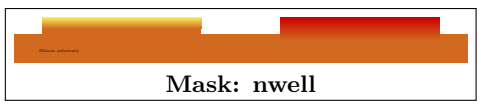
3 P-well


Mask: pwell

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
3.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
3.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
3.3	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
3.4	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$@100keV
3.5	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

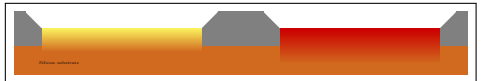
4 N-well


Mask: nwell

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
4.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
4.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
4.3	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
4.4	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$@100keV
4.5	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

5 Field oxide



Mask: active

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
5.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
5.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
5.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Thick oxide growth	1.23μm , 4 hours 30 minutes @ 1050°C in wet environment
5.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
5.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
5.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
5.7	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Field oxide etching	12 minutes 30 seconds
5.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
5.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

6 Gate

Mask: poly

Wafer Cleanliness
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean
Clean

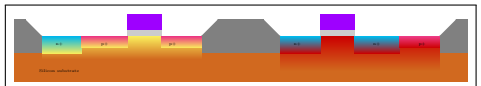
Step Number	Equipment	Location	Cleanliness	Process	Requirements
6.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.3	Diffusion Furnace-D2, dry oxidation (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
6.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.6	LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	600nm of poly silicon
6.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
6.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
6.9	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
6.10	Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	6 minute 10 seconds (600nm poly + 40nm oxide)
6.11	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
6.12	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

7 N+ implant

Mask: nimplant

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	7.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Clean	7.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	7.3	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Clean	7.4	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @ 90keV
Clean	7.5	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

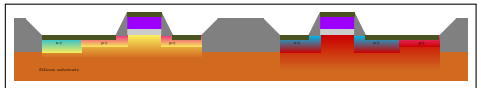
8 P+ implant



Mask: pimplant

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	8.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Clean	8.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	8.3	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Clean	8.4	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @ 35keV
Clean	8.5	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	

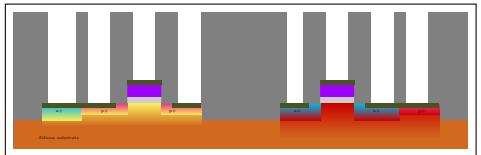
9 Silicification



Mask: silicideblock

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	9.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Spacer oxide	50 nm
Clean	9.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Clean	9.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	9.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Clean	9.7	AOE Etcher (DRY-AOE)	P2-01000	Clean	Anisotropic oxide etch	12 seconds
Clean	9.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	9.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	9.10	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Titanium	15 seconds (roughly 60nm)
Semi clean	9.11	AG610 RTP (DIF-R2)	P2-01000	Semi clean	First reaction phase	240 seconds @ 700°C
Semi clean	9.12	E2: General purpose (WET-E2)	P2-01000	Semi clean	Remove unreacted Titanium	APM solution (Ammonia and Hydrogen Peroxide mixture), 1 minute
Semi clean	9.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	9.14	AG610 RTP (DIF-R2)	P2-01000	Semi clean	Second reaction phase	240 seconds @ 800°C

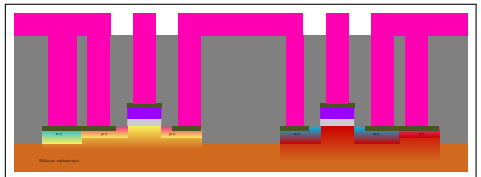
10 Contact



Mask: contact

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	10.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	10.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	10.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$4\mu m$
Semi clean	10.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Semi clean	10.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	10.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Semi clean	10.7	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	Oxide Etch	80 minutes ($4\mu m$)
Semi clean	10.8	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, $70^{\circ}C$
Semi clean	10.9	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

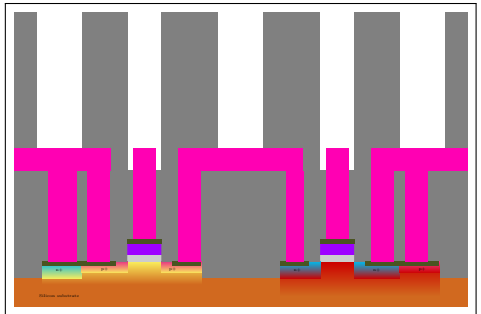
11 Metal 1



Mask: metal1

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	11.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	15 seconds (roughly 60nm)
Semi clean	11.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Semi clean	11.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	11.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Semi clean	11.5	Oxford Aluminum Etcher (DRY-Metal-2)	P2-01000	Semi clean	Wire formation	$4\mu m$
Semi clean	11.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, $70^{\circ}C$
Semi clean	11.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

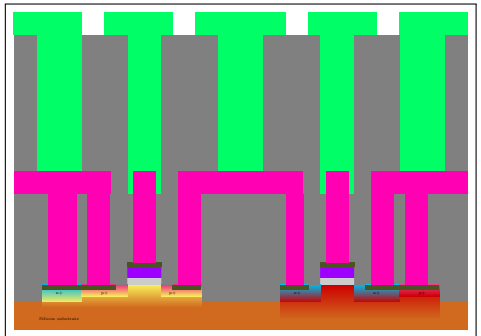
12 Via 1



Mask: via1

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	12.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	12.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	12.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$4\mu m$
Semi clean	12.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Semi clean	12.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	12.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Semi clean	12.7	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	Oxide Etch	80 minutes ($4\mu m$)
Semi clean	12.8	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, $70^{\circ}C$
Semi clean	12.9	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

13 Metal 2

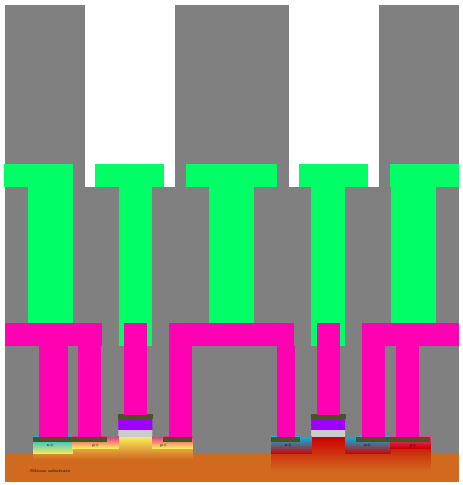


Mask: metal2

Wafer Cleanliness
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
13.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	15 seconds (roughly 60nm)
13.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
13.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
13.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
13.5	Oxford Aluminum Etcher (DRY-Metal-2)	P2-01000	Semi clean	Wire formation	$4\mu m$
13.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
13.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

14 Via 2



Mask: via2

Wafer Cleanliness
Semi clean
Semi clean
Semi clean
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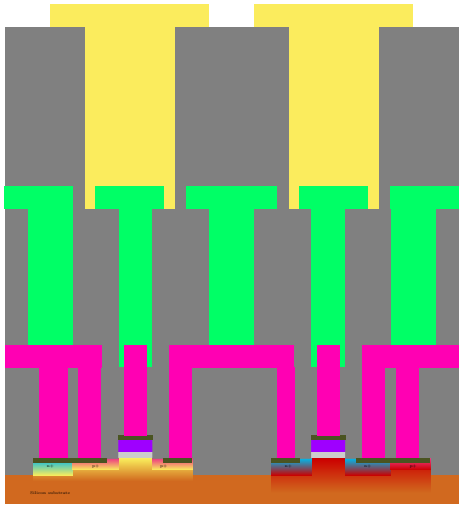
Semi clean
Semi clean
Semi clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
14.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
14.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
14.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$4\mu m$
14.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
14.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
14.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
14.7	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	Oxide Etch	80 minutes ($4\mu m$)
14.8	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
14.9	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

15 Metal 3



Mask: metal3

Wafer Cleanliness
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean
Semi clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
15.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	15 seconds (roughly 60nm)
15.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
15.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
15.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
15.5	Oxford Aluminum Etcher (DRY-Metal-2)	P2-01000	Semi clean	Wire formation	$4\mu m$
15.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
15.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	