LibreSilicon process HKUST (NFF)

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Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing** $1\mu m$ **only!** But further releases which will have been tested with smaller structure sizes can be expected. Please see the document with the generic steps[2] in order to get a detailed description of the different steps.

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[1] https://github.com/chipforge/StdCellLib
[2] https://github.com/leviathanch/libresiliconprocess/raw/master/process_steps/process_steps.pdf

Process Flow of Lanceville Technologies LibreSilicon 180nm

- Project: LibreSilicon $1\mu m$

- Name: Lanceville Technologies Group

- Substrate: P-Substrate silicon wafer <100>

- Date: May 20, 2018
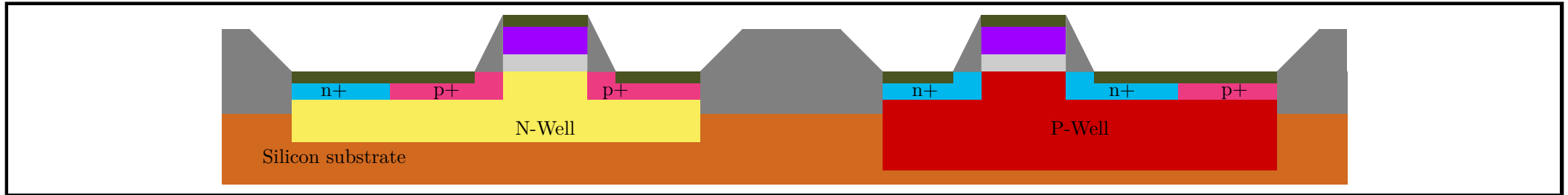
1 Shallow trench isolation

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
1.1	A3: Sulfuric Cleaning	P201000	Clean	Initial Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
1.2	A2: HF:H2O (1:50)	P201000	Clean	HF dip	1 min	Clean
1.3	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
1.4	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C	Clean
1.5	SVG Coater Track	P200100	Clean / Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2µm, soft bake: 110C 1min	Clean
1.6	ASML Stepper	P200100	Clean / Semi clean	Exposure of the "active" layer	??	Clean
1.7	SVG Developer Track	P200100	Clean / Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
1.8	C3: BOE	P201000	Clean	Oxide Etch	3 minutes 10 seconds	Clean
1.9	E4: Resist Strip	P201000	Clean / Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
1.10	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean
1.11	DRIE Etcher #1 (DRY-Si-1)	P201000	Clean / Semi clean	Etching the trenches	1 minute ($2\mu m$)	Clean
1.12	C3: BOE	P201000	Clean	Hard mask removal	1 minute 10 seconds	Clean
1.13	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean

2 P-well

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
2.1	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
2.2	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
2.3	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	500nm, 56 minutes @ 1050°C	Clean
2.4	SVG Coater Track	P200100	Clean Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2μm, soft bake: 110C 1min	Clean
2.5	ASML Stepper	P200100	Clean Semi clean	Exposure of the "pwell" layer	??	Clean
2.6	SVG Developer Track	P200100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
2.7	C3: BOE	P201000	Clean	Oxide Etch	5 minutes (500nm)	Clean
2.8	E4: Resist Strip	P201000	Clean Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
2.9	Spin Dryer-E	P201000	Clean Semi clean	Spin dry		Clean
2.10	IMP: CF−3000	P201000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$@100keV	Clean
2.11	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
2.12	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
2.13	Diff. Furnace-A1 Anneal/Oxidation	P201000	Clean	Annealing	Annealing 30 minutes @ 1050°C with N_2	Clean
2.14	C3: BOE	P201000	Clean	Hard mask removal	5 minutes (500nm)	Clean

Silicon substrate

3 N-well

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
3.1	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
3.2	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
3.3	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	300nm, 25 minutes @ 1050°C	Clean
3.4	SVG Coater Track	P200100	Clean / Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2μm, soft bake: 110C 1min	Clean
3.5	ASML Stepper	P200100	Clean / Semi clean	Exposure of the "nwell" layer	??	Clean
3.6	SVG Developer Track	P200100	Clean / Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
3.7	C3: BOE	P201000	Clean	Oxide Etch	3 minutes (300nm)	Clean
3.8	E4: Resist Strip	P201000	Clean / Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
3.9	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean
3.10	IMP: CF–3000	P201000	Clean / Semi clean	Phosphorus implant	$2.5 \times 10^{12} cm^{-2}$@100keV	Clean
3.11	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
3.12	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
3.13	Diff. Furnace-A1 Anneal/Oxidation	P201000	Clean	Annealing	Annealing 30 minutes @ 1050°C with N_2	Clean
3.14	C3: BOE	P201000	Clean	Hard mask removal	3 minutes (300nm)	Clean

4 Field oxide

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
4.1	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
4.2	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
4.3	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Thick oxide growth	$1\mu m$, 3 hours @ 1050°C in wet environment	Clean
4.4	SVG Coater Track	P200100	Clean / Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2µm, soft bake: 110C 1min	Clean
4.5	ASML Stepper	P200100	Clean / Semi clean	Exposure of the "active" layer	??	Clean
4.6	SVG Developer Track	P200100	Clean / Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
4.7	C3: BOE	P201000	Clean	Oxide Etch	10 minutes	Clean
4.8	E4: Resist Strip	P201000	Clean / Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
4.9	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean

5 Gate

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
5.1	A3: Sulfuric Cleaning	P201000	Clean	Default Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
5.2	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
5.3	Diff. Furnace-D1 Dry Oxidation	P201000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment	Clean
5.4	LPCVD-A3 Amor-Si/Poly	P201000	Clean	Gate electrode growth	600nm of poly silicon	Clean
5.5	SVG Coater Track	P200100	Clean / Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2µm, soft bake: 110C 1min	Clean
5.6	ASML Stepper	P200100	Clean / Semi clean	Exposure of the "gate" layer	??	Clean
5.7	SVG Developer Track	P200100	Clean / Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
5.8	DRY-Poly	P201000	Clean / Semi clean	Poly etcher	6 minute 10 seconds (600nm poly + 40nm oxide)	Clean
5.9	E4: Resist Strip	P201000	Clean / Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
5.10	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean