Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

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Libre Silicon process testing

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In order to get an idea on how strongly the actual product differs from the mathematical models being used before hand to define the initial parameters, one has to run a bunch of test wafers through the process over and over again, tweak parameters and measure out all kinds of aspects of the device.
This is also important for gathering the data which will finally end up within the data sheet.
In this chapter we will tackle the multiple different measurement and test objects we will need to put into the seal area during production in order to ensure the consistent quality of the chips we're going to sell in the end.

Testing parameters:

- Passive properties:
  - The capacity per m^2 from the n-well to the gate electrode
  - The capacity per m^2 from the p-well to the gate electrode
  - The actual resistance/m of the p-well
  - The actual resistance/m of the n-well
  - The actual resistance/m of the p-implant layer
  - The actual resistance/m of the n-implant layer
  - The actual resistance/m of the poly layer
  - The actual resistance/m of the silicide+p-implant layer
  - The actual resistance/m of the silicide+n-implant layer
  - The actual resistance/m of the silicide+poly layer
- Diodes:
  - ESD structure diodes (Voltage protection)
  - Lateral diodes
  - Vertical diodes
- Bipolar transistors:
  - Vertical bipolar transistor (to test latchup conditions)
  - Lateral bipolar transistors (to see what the beta is)
- NMOS as well as PMOS:
  - Frequency characteristics (Transient curve)
  - Drain-source resistance vs. gate-source voltage
  - Actual threshold voltage

Each of these values will variate based on the location on the wafer, because of diffraction towards the edge and also because of the uneven nature of the wafer.
Measuring the same test structure multiple times placed at multiple locations on the wafer will allow us to calculate an effective average value and tolerance ranges for taking into account for further dimensioning of circuits..

1 Diodes

There are multiple different diode types possible which could form, which can categorized into two categories: Lateral and vertical.
Lateral diodes can form between two wells or the well and the junction, the vertical diodes can form between the n-well and the p-substrate.

1.1 Lateral diodes

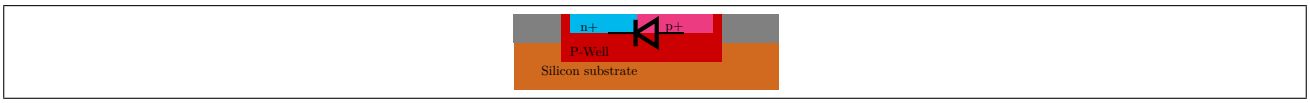

Figure 1: Lateral diode cross section

1.2 Vertical diodes

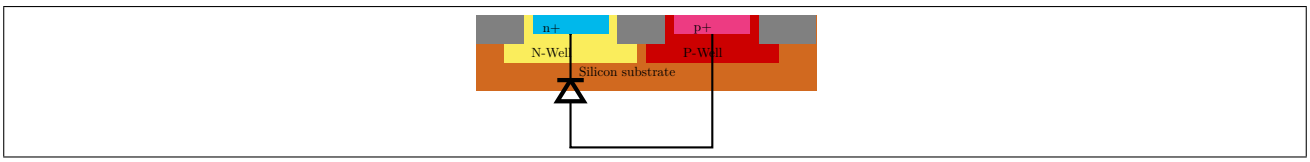

Figure 2: Vertical diode cross section

2 Bipolar transistors

A byproduct of the Bulk CMOS structure is a pair of parasitic bipolar transistors.[1] The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latchup can occur when both BJT's conduct, creating a low resistance path between VDD and GND and the product of the gains of the two transistors in the feedback loop $\beta_1 \times \beta_2$ is greater than one. The result of latchup is at the minimum a circuit malfunction, and in the worst case, the destruction of the device.

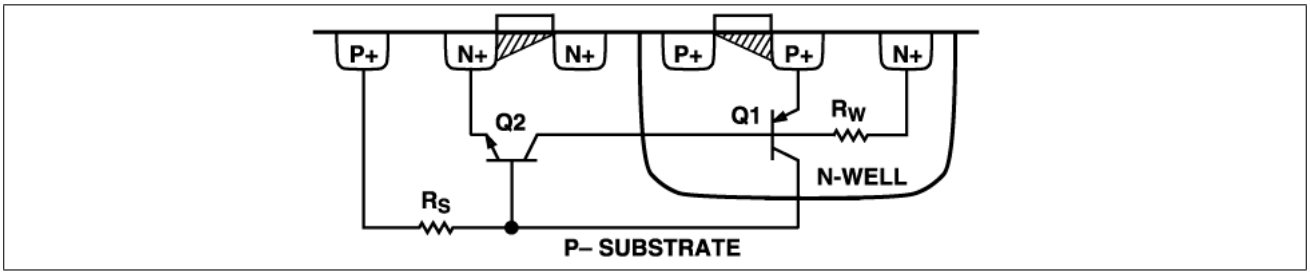

Figure 3: Lateral and vertical parasitic BJT

In Figure 3 we can see the two above mentioned transistors. In order to find out their average β we split it up into two separate test circuits, allowing us to measure their properties out with probes on our test wafer.

2.1 Lateral bipolar transistor

We split out the lateral bipolar junction transistor for testing.

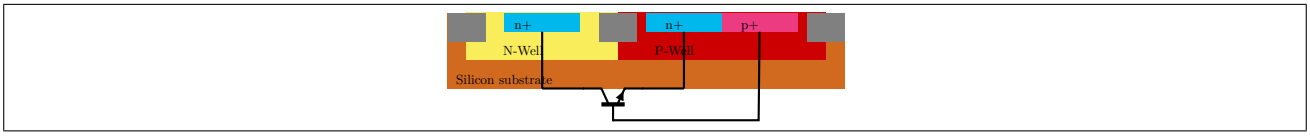

Figure 4: Lateral BJT cross section

In Figure 4 the cross section of our testing circuit can be seen. Now we can characterize the β value of the lateral bipolar transistor all over the wafer and get a good approximation of the worst case conditions.

2.2 Vertical bipolar transistor

We split out the vertical bipolar junction transistor for testing.

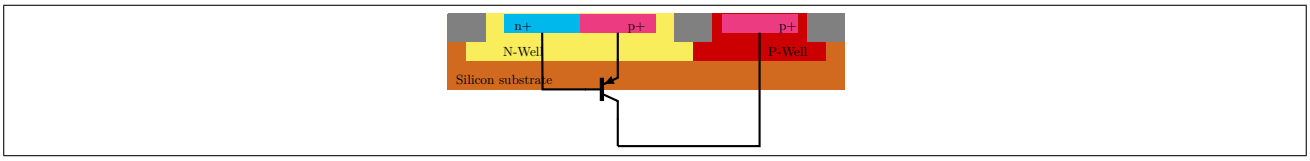

Figure 5: Vertical BJT cross section

In Figure 5 the cross section of our testing circuit can be seen. Now we can characterize the β value of the vertical bipolar transistor all over the wafer and get a good approximation of the worst case conditions.

[1] http://www.analog.com/en/analog-dialogue/articles/winning-the-battle-against-latchup.html

3 ESD circuit test

3.1 ESD diode on p-substrate

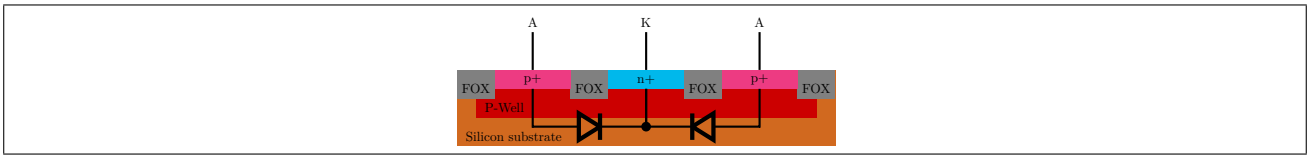

Figure 6: ESD diode on p-substrate cross section

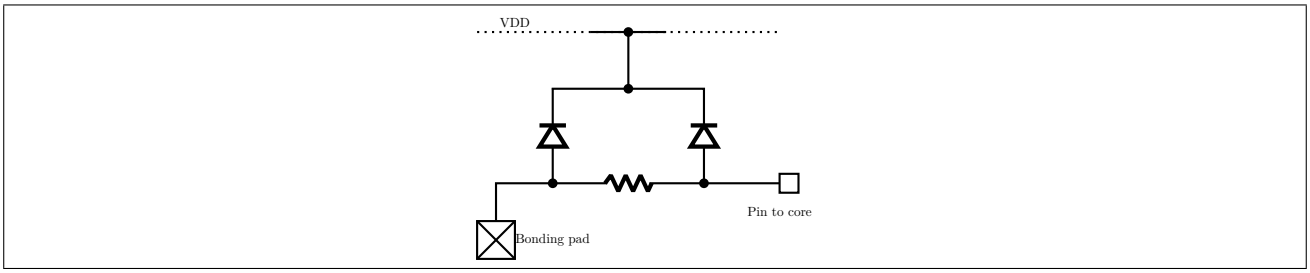

Figure 7: ESD diode on p-substrate schematics

3.2 ESD diode on n-substrate

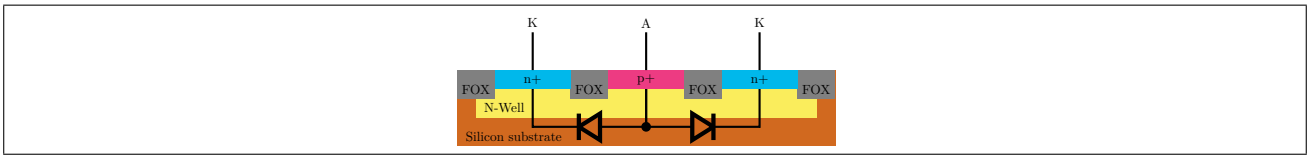

Figure 8: ESD diode on n-substrate cross section

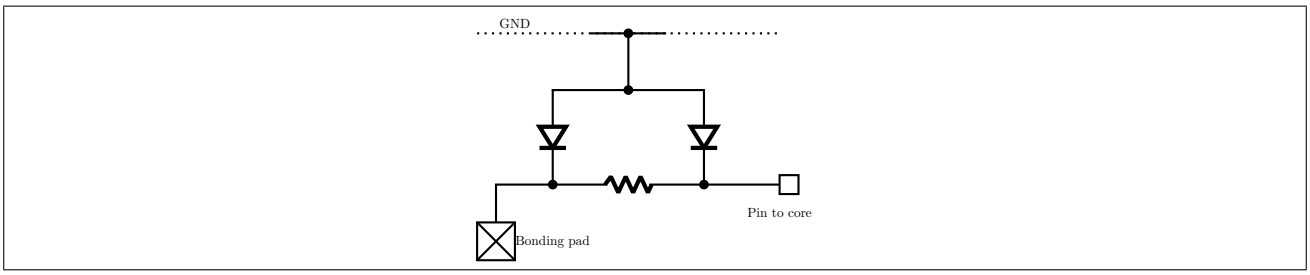

Figure 9: ESD diode on n-substrate schematics