LibreSilicon process HKUST (NFF)

David Lanzendörfer

June 16, 2018

Abstract

Copyright © 2017 LANCEVILLE TECHNOLOGY GROUP CO., LIMITED. All rights reserved.

This process is licensed under the Libre Silicon public license; you can redistribute it and/or modify it under the terms of the Libre Silicon public license as published by the Libre Silicon alliance, either version 1 of the License, or (at your option) any later version.

This design is distributed in the hope that it will be useful, but WITHOUT ANY WARRANTY; without even the implied warranty of MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. See the Libre Silicon Public License for more details.

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells¹ and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing** $1\mu m$ **only!** But further releases which will have been tested with smaller structure sizes can be expected. Please see the document with the generic steps² in order to get a detailed description of the different steps.

¹https://github.com/chipforge/StdCellLib

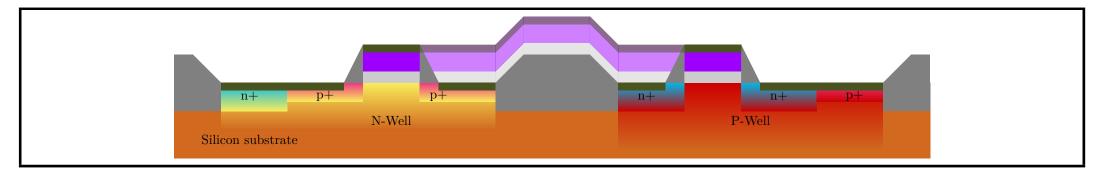
²https://github.com/leviathanch/libresiliconprocess/raw/master/process_steps/process_steps.pdf

Process Flow of Lanceville Technologies LibreSilicon 180nm

• Project: Libre Silicon $1\mu m$

• Name: Lanceville Technologies Group

• Date: June 16, 2018



1 Shallow trench isolation

Mask: active





Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
1.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Initial Cleaning	H2SO4+H2O2, 10mins @ 120°C
1.2	A2:HF:H2O (1:50) (WET- A2)	P2-01000	Clean	HF dip	1 min
1.3	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
1.4	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C, wet ambient
1.5	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
1.6	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
1.7	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
1.8	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Oxide Etch	1 minute
1.9	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
1.10	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4 + H2O2, 120°C , 10mins
1.11	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
1.12	DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	1 minute $(2\mu m)$
1.13	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Hard mask removal	1 minute
1.14	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

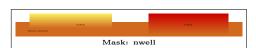
2 P-well





Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
2.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
2.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
2.3	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Hard mask dioxide growth	500nm, 56 minutes @ 1050°C , wet ambient
2.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
2.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
2.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
2.7	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Oxide Etch	5 minutes
2.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
2.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
2.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
2.11	CF-3000 Implanter (IMP- 3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
2.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
2.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
2.14	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
2.15	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Hard mask removal	5 minutes
2.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

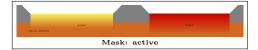
3 N-well

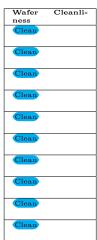




Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
3.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
3.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
3.3	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Hard mask dioxide growth	200nm, 14 minutes @ 1050 $^{\circ}$ C , wet ambient
3.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
3.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
3.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
3.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	2 minutes
3.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
3.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
3.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
3.11	CF-3000 Implanter (IMP- 3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
3.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
3.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
3.14	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
3.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	2 minutes
3.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

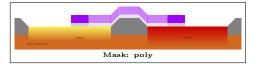
4 Field oxide

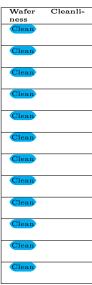




Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
4.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
4.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
4.3	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Thick oxide growth	$1\mu m$, 3 hours @ 1050 [◦] C in wet environment
4.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
4.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
4.6	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
4.7	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Hard mask removal	10 minutes
4.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
4.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
4.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

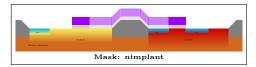
5 Gate

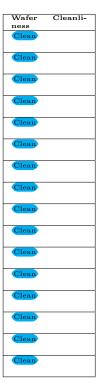




Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
5.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
5.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
5.3	Diffusion Furnace-D2, dry oxidation (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
5.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
5.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
5.6	LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	600nm of poly silicon
5.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
5.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
5.9	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
5.10	Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	6 minute 10 seconds (600nm poly + 40nm oxide)
5.11	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
5.12	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

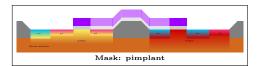
6 N+ implant

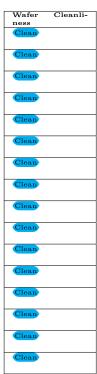




Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
6.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.3	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C, wet ambient
6.4	SVG Coater Track (PHT- T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
6.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
6.6	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
6.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	1 minutes
6.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
6.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
6.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
6.11	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
6.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.14	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
6.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	1 minutes
6.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

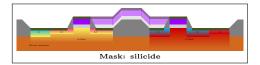
7 P+ implant





Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
7.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
7.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
7.3	Diffusion Furnace-D2, dry/wet oxidation (DIF- D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C, wet ambient
7.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
7.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
7.6	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
7.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	1 minutes
7.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
7.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
7.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
7.11	CF-3000 Implanter (IMP- 3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
7.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
7.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
7.14	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
7.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	1 minutes
7.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

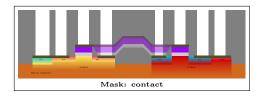
8 Silicification

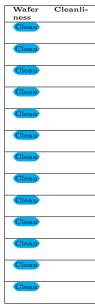




Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
8.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
8.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
8.3	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
8.4	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	2 minutes
8.5	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
8.6	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
8.7	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
8.8	CF-3000 Implanter (IMP- 3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
8.9	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
8.10	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
8.11	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
8.12	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	2 minutes
8.13	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

9 Contact





Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
9.1	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
9.2	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
9.3	SVG Developer Track (PHT- T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
9.4	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	2 minutes
9.5	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
9.6	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C, 10mins
9.7	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
9.8	CF-3000 Implanter (IMP- 3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @100keV
9.9	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
9.10	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
9.11	Diffusion Furnace-A1, an- neal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050° C with N_2
9.12	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	2 minutes
9.13	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	