LibreSilicon process HKUST (NFF)

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June 20, 2018

Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

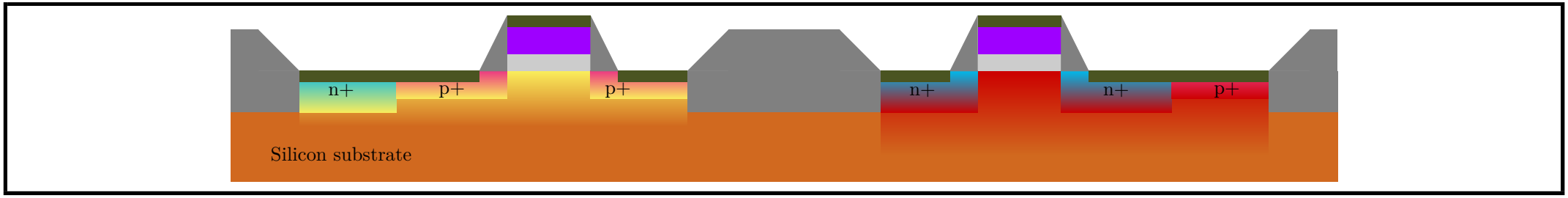
For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected. Please see the document with the generic steps[2] in order to get a detailed description of the different steps.

[1] `https://github.com/chipforge/StdCellLib`

[2] `https://github.com/leviathanch/libresiliconprocess/raw/master/process_steps/process_steps.pdf`

Process Flow of Lanceville Technologies LibreSilicon 180nm

- Project: LibreSilicon $1\mu m$
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer <100>
- Date: June 20, 2018



1 Shallow trench isolation

Mask: active

Wafer Cleanliness
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Step Number	Equipment	Location	Cleanliness	Process	Requirements
1.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Initial Cleaning	H2SO4+H2O2, 10mins @ 120°C
1.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
1.3	A2:HF:H2O (1:50) (WET-A2)	P2-01000	Clean	HF dip	1 min
1.4	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
1.5	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C , wet ambient
1.6	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
1.7	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
1.8	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
1.9	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Oxide Etch	1 minute
1.10	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
1.11	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4 + H2O2, 120°C , 10mins
1.12	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
1.13	DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	1 minute ($2\mu m$)
1.14	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Hard mask removal	1 minute
1.15	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

2 P-well

Mask: pwell

Wafer Cleanliness
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Step Number	Equipment	Location	Cleanliness	Process	Requirements
2.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
2.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
2.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Hard mask dioxide growth	500nm, 56 minutes @ 1050°C , wet ambient
2.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
2.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
2.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
2.7	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Oxide Etch	5 minutes
2.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
2.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
2.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
2.11	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$@100keV
2.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
2.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
2.14	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050°C with N_2
2.15	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Hard mask removal	5 minutes
2.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

3 N-well

Mask: nwell

Wafer Cleanliness
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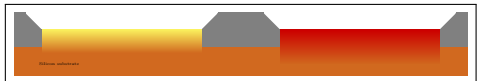
Step Number	Equipment	Location	Cleanliness	Process	Requirements
3.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
3.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
3.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Hard mask dioxide growth	200nm, 14 minutes @ 1050°C , wet ambient
3.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
3.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
3.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
3.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	2 minutes
3.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
3.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
3.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
3.11	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$@100keV
3.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
3.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
3.14	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050°C with N_2
3.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	2 minutes
3.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

4 Field oxide



Mask: active

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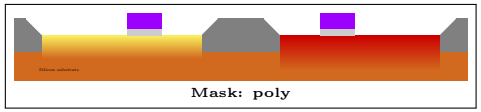
Step Number	Equipment	Location	Cleanliness	Process	Requirements
4.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
4.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
4.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Thick oxide growth	1.23μm , 4 hours 30 minutes @ 1050°C in wet environment
4.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
4.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
4.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
4.7	C3:BOE (WET-C3)	P2-01000	Clean	BOE: Field oxide etching	12 minutes 30 seconds
4.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
4.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
4.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

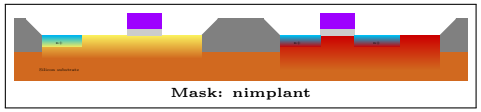
5 Gate



Mask: poly

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	5.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	5.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	5.3	Diffusion Furnace-D2, dry oxidation (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
Clean	5.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	5.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	5.6	LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	600nm of poly silicon
Clean	5.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Clean	5.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	5.9	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Clean	5.10	Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	6 minute 10 seconds (600nm poly + 40nm oxide)
Clean	5.11	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	5.12	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

6 N+ implant



Mask: nimplant

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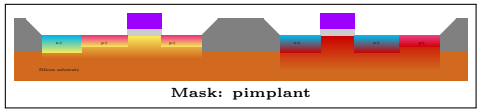
Step Number	Equipment	Location	Cleanliness	Process	Requirements
6.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C , wet ambient
6.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
6.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
6.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
6.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	1 minutes
6.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
6.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
6.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
6.11	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @ 35keV
6.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
6.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
6.14	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 10 minutes @ 1050°C with N_2
6.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	1 minutes
6.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

7 P+ implant



Mask: pimplant

Wafer Cleanliness
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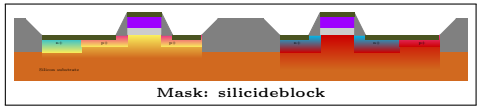
Step Number	Equipment	Location	Cleanliness	Process	Requirements
7.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
7.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
7.3	Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Hard mask dioxide growth	100nm, 5 minutes 30 seconds @ 1050°C , wet ambient
7.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
7.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
7.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
7.7	C3:BOE (WET-C3)	P2-01000	Clean	Oxide Etch	1 minutes
7.8	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	
7.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
7.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
7.11	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @ 13keV
7.12	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
7.13	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
7.14	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Annealing	Annealing 30 minutes @ 1050°C with N_2
7.15	C3:BOE (WET-C3)	P2-01000	Clean	Hard mask removal	1 minutes
7.16	Spin Dryer-C (SRD-C)	P2-01000	Clean	Dry the wafer automatically	

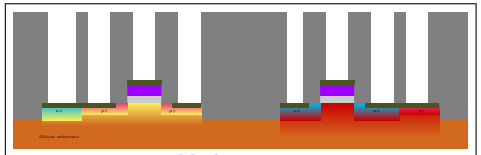
8 Silicification



Mask: silicideblock

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	8.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Spacer oxide	50 nm
Clean	8.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Clean	8.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	8.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Clean	8.7	AOE Etcher (DRY-AOE)	P2-01000	Clean	Anisotropic oxide etch	12 seconds
Clean	8.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	8.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	8.10	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Titanium	15 seconds (roughly 60nm)
Semi clean	8.11	AG610 RTP (DIF-R2)	P2-01000	Semi clean	First reaction phase	240 seconds @ 700°C
Semi clean	8.12	E2: General purpose (WET-E2)	P2-01000	Semi clean	Remove unreacted Titanium	APM solution (Ammonia and Hydrogen Peroxide mixture), 1 minute
Semi clean	8.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	8.14	AG610 RTP (DIF-R2)	P2-01000	Semi clean	Second reaction phase	240 seconds @ 800°C

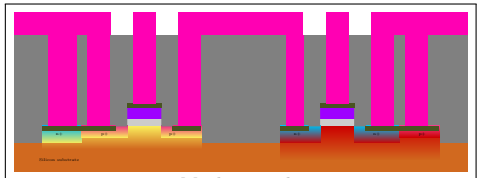
9 Contact



Mask: contact

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	9.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	9.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	9.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$4\mu m$
Semi clean	9.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
Semi clean	9.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	9.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
Semi clean	9.7	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	Oxide Etch	80 minutes ($4\mu m$)
Semi clean	9.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Semi clean	9.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

10 Metal 1



Mask: metal1

Wafer Cleanliness
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Semi clean

Step Number	Equipment	Location	Cleanliness	Process	Requirements
10.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	15 seconds (roughly 60nm)
10.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	
10.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
10.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	
10.5	Oxford Aluminum Etcher (DRY-Metal-2)	P2-01000	Semi clean	Wire formation	$4\mu m$
10.6	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
10.7	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	