# Libre Silicon process specification

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**Abstract**

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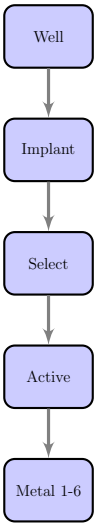
This is the specification of the free silicon manufacturing standard for manufacturing the ls018[1]standard logic cells and related free technology nodes from the LibreSilicon project.

[1]https://github.com/leviathanch/ls018

# 1 Overall process

Below the general flow chart of the overall process flow can be seen. These process steps will be discussed within the following sections.

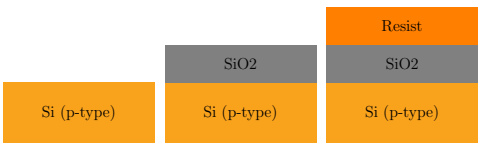



The four starting overall process steps are part of an overall active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world. For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL.

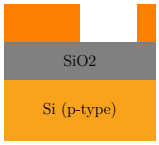
# 2 Well

## 2.1 Oxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective oxide layer needs to be grown on top of a p-type substrate.



## 2.2 Pattering and etching




## 2.3 Infusion

# 3 Implant

# 4 Select

# 5 Active

# 6 Metal