

# Libre Silicon process specification

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## Abstract

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This is the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells<sup>1</sup> and related free technology nodes from the LibreSilicon project.

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<sup>1</sup><https://github.com/chipforge/StdCellLib>

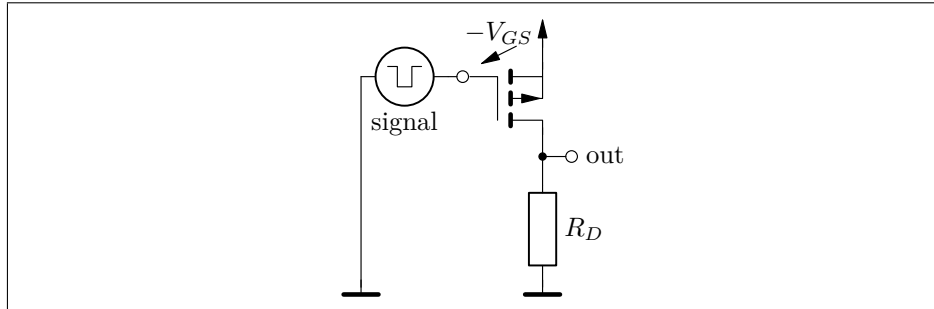
# Contents

<b>1</b>	<b>CMOS in a nutshell</b>	<b>3</b>
<b>2</b>	<b>Physics</b>	<b>5</b>
2.1	Infusion . . . . .	5
<b>3</b>	<b>Chemistry</b>	<b>6</b>
3.1	Etching silicon dioxide . . . . .	6
3.2	Etching silicon nitride . . . . .	7
<b>4</b>	<b>Process</b>	<b>8</b>
4.1	Shallow trench isolation . . . . .	9
4.1.1	Initial cleaning . . . . .	9
4.1.2	Sulfuric Cleaning . . . . .	10
4.1.3	HF dip . . . . .	10
4.1.4	Pad oxide . . . . .	10
4.1.5	Nitride layer . . . . .	10
4.1.6	Patterning . . . . .	10
4.1.7	Etching . . . . .	10
4.1.8	Deep oxidation . . . . .	10
4.2	Well . . . . .	11
4.2.1	Mask dioxide layer . . . . .	11
4.2.2	Patterning . . . . .	13
4.2.3	Etching . . . . .	13
4.2.4	Cleaning . . . . .	14
4.2.5	Injection . . . . .	14
4.2.6	Oxide for drive-in . . . . .	14
4.2.7	Drive-in . . . . .	14
4.2.8	Oxide mask removal . . . . .	15
4.3	n+ Implant . . . . .	16
4.3.1	Mask dioxide layer . . . . .	16
4.3.2	Patterning . . . . .	16
4.3.3	Etching . . . . .	17
4.3.4	Cleaning . . . . .	17
4.3.5	Injection . . . . .	17
4.3.6	Oxide removal . . . . .	17
4.4	p+ Implant . . . . .	18
4.4.1	Mask dioxide layer . . . . .	18
4.4.2	Patterning . . . . .	19
4.4.3	Etching . . . . .	19
4.4.4	Cleaning . . . . .	19
4.4.5	Injection . . . . .	20
4.4.6	Oxide removal . . . . .	20
4.5	Gate contact . . . . .	21
4.6	First vias . . . . .	22
4.7	First metal layer . . . . .	23

# 1 CMOS in a nutshell

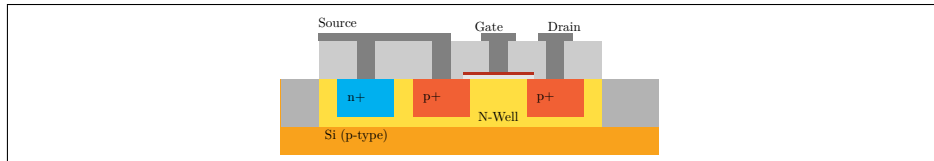
This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal-oxide-semiconductor field-effect transistors (MOSFET) are required.

Historically, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.



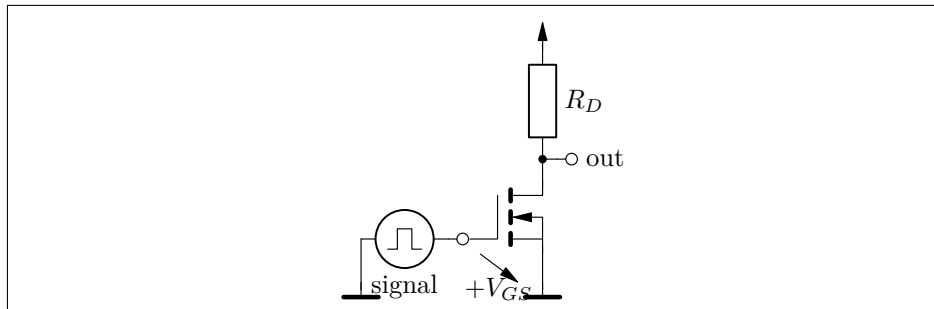
**Figure 1:** enhancement-mode PMOS transistor use-case

The sectional view of a PMOS transistor in silicon is being shown below



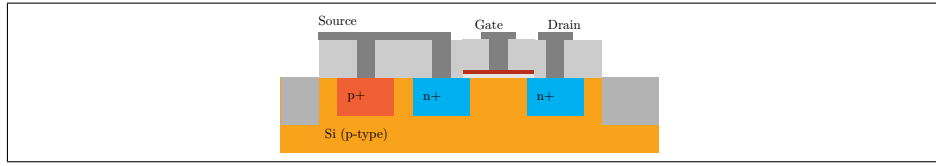
**Figure 2:** Sectional view of a PMOS transistor

Historically later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.



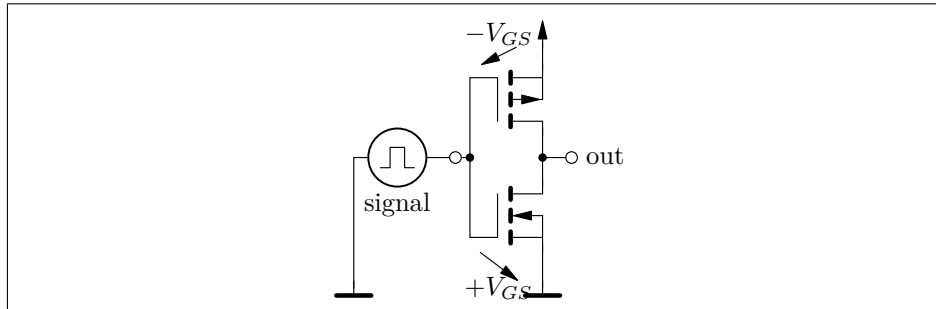
**Figure 3:** enhancement-mode NMOS transistor use-case

The sectional view of a NMOS transistor in silicon is being shown here also.



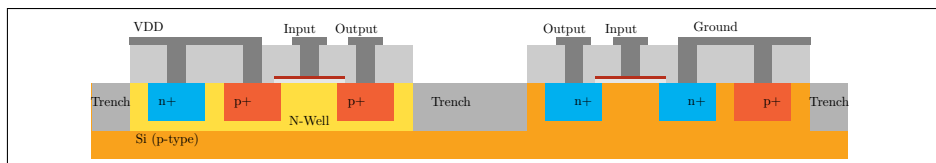
**Figure 4:** Sectional view of a NMOS transistor

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning also higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, now currents flows between Drain and Source anymore, the power consumption of the chip also goes low. Et voilà, the US-Patent with Number 3356858<sup>2</sup> changed the world and combines both technologies to the new complementary metal-oxide-semiconductor (CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.



**Figure 5:** complementary PMOS and NMOS transistor couple use-case

Below the sectional view of the inverter circuitry can be seen. For the run through of this process we will use this cross section diagram as reference.



**Figure 6:** Sectional view of a NMOS-PMOS transistor circuit

<sup>2</sup><https://www.google.com/patents/US3356858>

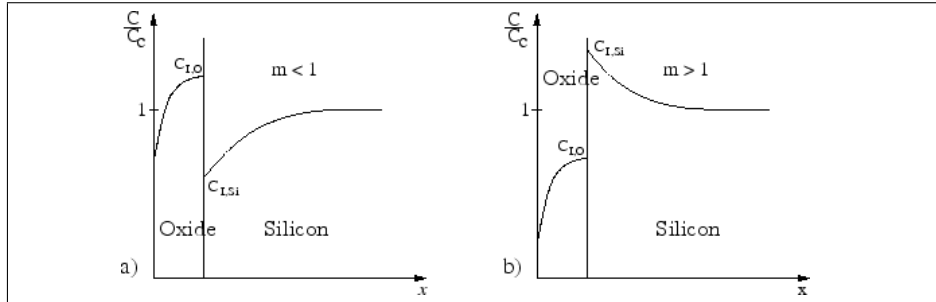
## 2 Physics

### 2.1 Infusion

The redistribution process depends on the ratio of the solubility of the doping material in silicon and  $\text{SiO}_2$ . At the Si/ $\text{SiO}_2$  interface the dopants are redistributed by segregation until the ratio of their concentration at the interface is the same as the ratio of their solubility in both materials. The ratio of dopant solubility is expressed by the segregation coefficient  $m$  which is

$$m = \frac{\text{solubility in silicon}}{\text{solubility in SiO}_2} \quad (1)$$

As listed in [Table 1](#) below there are dopant species which solubilize better in  $\text{SiO}_2$  than in silicon ( $m < 1$ ) and species which have a reversed behavior ( $m > 1$ ). In case of  $m < 1$ , as for Boron, the dopant concentration is enhanced at the  $\text{SiO}_2$  side, whereas beneath the interface, there is a dopant depletion at the silicon surface. For reversed solubility ratios ( $m > 1$ , like Phosphorus), only few dopant atoms penetrate the interface. In order to obtain the by  $m$  determined concentration ratio at the interface, dopant atoms from deeper silicon zones diffuse back to the surface zone. Therefore, the dopant concentration at the silicon surface is enhanced, as illustrated in [Figure 7b](#). In [Figure 7](#)  $C_c$  denotes the dopant concentration in the silicon surface zone before oxidation.  $x$  is the distance from the silicon surface.



**Figure 7:** Schematic illustration of dopant redistribution

Dopant species	Boron	Phosphor	Antimon	Arsen	Gallium
$m$	0.1-0.3	10	10	10	20

Table 1: Segregation coefficients  $m$  for important dopant species in silicon

## 3 Chemistry

### 3.1 Etching silicon dioxide

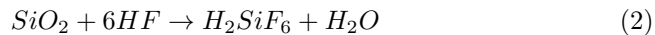
A very "selective" chemical for SiO<sub>2</sub> - i.e. does not etch silicon at all - is hydrofluoric acid (HF). If used directly such etchant has a too fast and aggressive action on the oxide, making very difficult the undercut and the linewidth control. For such reason, HF is universally used as a "buffered" solution, which can keep the etch rate low and constant, by moderating the PH level of the bath. This allows the etching time to be reliably correlated to the etching depth.

The industry standard buffered hydrofluoric acid solution (BHF) has the following formulation:

- 6 volumes of ammonium fluoride (NH<sub>4</sub>F, 40% solution)
- 1 volume of HF.

This can be prepared, for example, by mixing 113 g of NH<sub>4</sub>F in 170 ml of H<sub>2</sub>O, and adding 28 ml of HF.

The etch rate at room temperature can range from 1000 to 2500 Å/min (100-250nm/min). This depends on the actual density of the oxide which, as an amorphous layer, can have a more compact structure (if thermally grown in oxygen) or less compact (if grown by CVD). The following etching reaction holds:



where  $\text{H}_2\text{SiF}_6$  is water soluble.

A common buffered oxide etch solution comprises a 6:1 volume ratio of 40% NH<sub>4</sub>F in water to 49% HF in water. This solution will etch thermally grown oxide at approximately 2 nanometres per second at 25 degrees Celsius.<sup>3</sup>

Another popular etching formulation is the P-etch:

60 volumes of H<sub>2</sub>O + 3 vol. of HF + 2 vol. of HNO<sub>3</sub>, that is: 300 ml of H<sub>2</sub>O + 15 ml of HF + 10 ml of HNO<sub>3</sub>.

The P-etch action is strongly dependent on oxide density, as it results from the growth technique. An example is reported in the literature<sup>4</sup>, indicating 120 Å/min for thermal oxide and 250-700 Å/min for sputtered oxide.

A slow etching bath is preferred for opening mask windows for a silicon substrate. However, the etching process could be used just for removing the oxide film from the whole surface. In this case the etching speed is not critical, and a fast solution can be used, such as HF diluted 1:10 in water. The etching time can be easily evaluated by visually inspecting the surface. Once the oxide film is removed, the metal-grey color of the silicon surface appears.

Sometimes a very light etch is required, for removing just a few atomic layers. This is the case of surface cleaning and decontamination. HF diluted 1 : 50 in water can be used. The etching speed will be around 70 Å / min. For example, a typical 50 Å "native" oxide on silicon can be removed with a 45 - 50 sec light etch.

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<sup>3</sup>Wolf, S.; R.N. Tauber (1986). Silicon Processing for the VLSI Era: Volume 1 - Process Technology. pp. 532-533. ISBN 978-0-9616721-3-3

<sup>4</sup>A. Pliskin, J.Vac.Sci Technol., vol. 14, p.1064, 1977

### 3.2 Etching silicon nitride

Thin films made of amorphous silicon nitride ( $Si_3N_4$ ) are usually deposited by chemical vapour deposition from silane ( $SiH_4$ ) and ammonia ( $NH_3$ ). Since they act as a barrier for water and sodium, they have a major role as passivation layers in microchip fabrication. Patterned nitride layers are also used as a mask for spatially selective silicon oxide growth, and as an etch mask when  $SiO_2$  masks cannot be used.

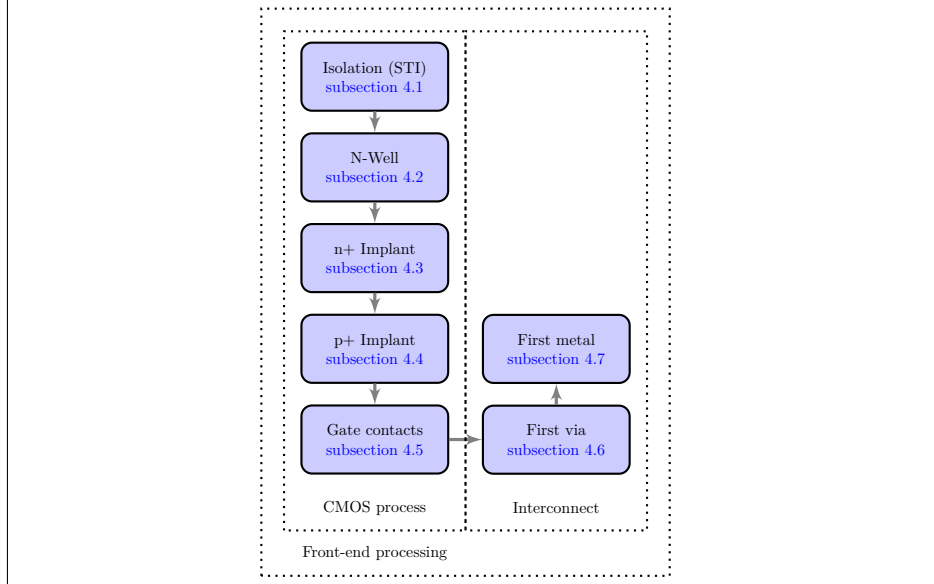
One example of the latter situation is given by the anisotropic etching of silicon in KOH. The etching rate of  $SiO_2$  in KOH is nearly 1000 times slower than the etching rate of silicon, and in most cases a  $SiO_2$  mask can be used successfully. However, a very deep selective etch may require a long etching time, and the 1000:1 etching rate ratio may result still too small to prevent the  $SiO_2$  mask from being etched off before the process is completed. In this circumstance  $Si_3N_4$ , thanks to its reduced etched rate, can successfully replace the oxide mask layer.

The wet etching of nitride films is often performed in concentrated hot orthophosphoric acid ( $H_3PO_4$ ). The bath temperature can range from 150°C to 180°C (boiling point) with a corresponding etch rate between 10 and 100 Å/min. It is good practice to bring the vapours into contact with a cold surface and to drive the condensed liquid back into the etching bath. This technique is referred to as "reflux".

The etching rates of silicon nitride, silicon oxide, and silicon in  $H_3PO_4$  are respectively in the 50 : 5 : 1 ratio.

## 4 Process

Below the general flow chart of the overall process flow can be seen in [Figure 8](#). These process steps will be discussed within the following sections.



**Figure 8:** Frontend and backend process flow

The five overall process steps are part of an active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world. For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The starting material is a p-type,  $\langle 100 \rangle$  oriented silicon with a doping concentration of  $\approx 9 \times 10^{14} \text{ cm}^{-3}$ .

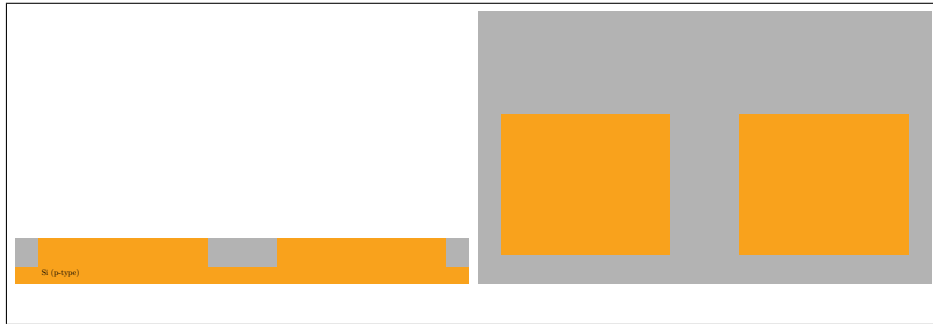
### Reasons for using p-substrate:

- We can't use two different substrates for our design because in the design both PMOS and NMOS is present. We have to choose which is more beneficial from fabrication point of view. In general or say it's true that NMOS devices are always more in the Semiconductor Industry in comparison to PMOS devices. For your reference-SRAM requires 6 transistors (4 NMOS, 2 PMOS).
- Another reason for more number of NMOS is because of difference of mobility of electron and holes. Electron mobility is almost twice of holes mobility and because of this ON-RESISTANCE of n-channel device is half of p-channel device with the same geometry and under the same operating conditions. That means to achieve same impedance size of n-channel transistors is almost half of p-channel devices. Same thing I can say in the different way that for same size of wafer, we can have more number of NMOS (means can perform more logical operation) in comparison to PMOS.



## 4.1 Shallow trench isolation

Shallow trench isolation (STI), also known as box isolation technique, is an integrated circuit feature which prevents electric current leakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 250 nanometers and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on LOCOS.<sup>5</sup> The geometry of a substrate with STI implemented can be seen in Figure 9.



**Figure 9:** Shallow trench isolation target geometry

We choose the STI approach because we wanna scale the technology node down in the future below 250nm and wanna ensure backwards compatibility of our process.

As can be seen in section 1, the n-well and the STI trench are supposed to have approximately the same depth. Because the n-well will be  $\approx 4\mu m$  in depth (subsection 4.2) we have to match this with our trench depth.

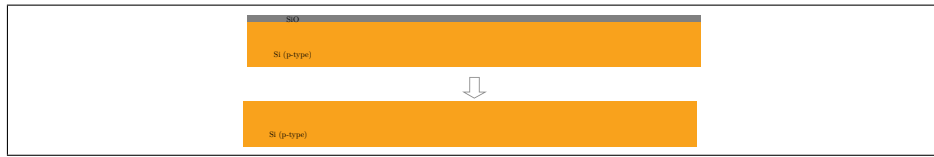


**Figure 10:** Shallow trench isolation layout

### 4.1.1 Initial cleaning

In order to remove the initial naturally grown silicon dioxide from the wafer, acid is being applied to the wafer which leads to a pure silicon substrate wafer as in the process illustration shown below.

<sup>5</sup>Quirk, Michael & Julian Serda (2001). Semiconductor Manufacturing Technology: Instructor's Manual Archived September 28, 2007, at the Wayback Machine., p. 25.



**Figure 11:** Initial cleaning

This needs to be done because the naturally grown initially existing silicon oxide is not pure and may contain contamination which may render the final product unusable.

#### 4.1.2 Sulfuric Cleaning

The sulfuric acid mixture,  $H_2SO_4 + H_2O_2$  is being applied to the wafer for 10 minutes at a temperature of 120 °C.

#### 4.1.3 HF dip

After the sulfuric cleaning a HF ( $HF:H_2O,1:50$ ) dip is being performed for one minute.

Hydrofluoric acid (HF) is used to remove native silicon dioxide from wafers. Since it acts quickly, one needs to only expose the wafer for a short time ("dip"). After that the wafer needs to be dried and quickly processed further before new uncontrolled natural oxide can build up on the wafer through the contact with air.

#### 4.1.4 Pad oxide

#### 4.1.5 Nitride layer

#### 4.1.6 Patterning

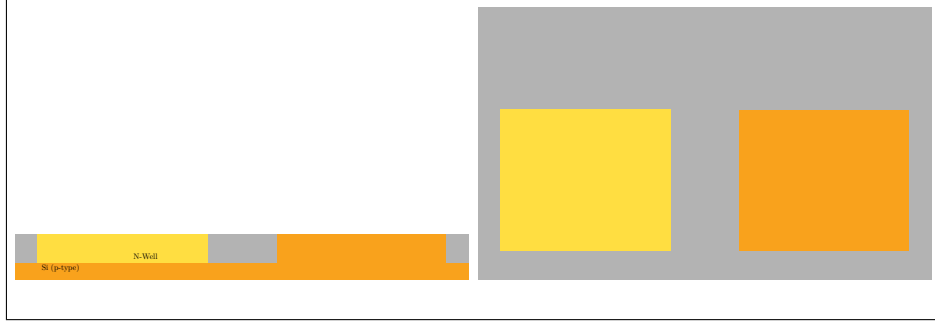
#### 4.1.7 Etching

Dry etching (RIE)

#### 4.1.8 Deep oxidation

## 4.2 Well

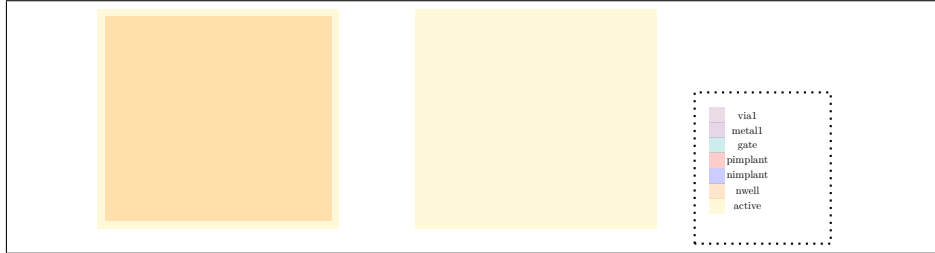
In order to build CMOS on the same substrate, an n-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The cross section as well as the top view of the targeted geometry are shown in [Figure 12](#)



**Figure 12:** N-well target geometry

The n-well will serve us as an island of n-doped substrate within the p-doped basis substrate. the n-well forms a natural p-n-junction to the later on implanted channel-stop which has a nice side effect of being an additional polarity protection. The dopant dose will be:  $2.5 \times 10^{12} cm^{-2}$

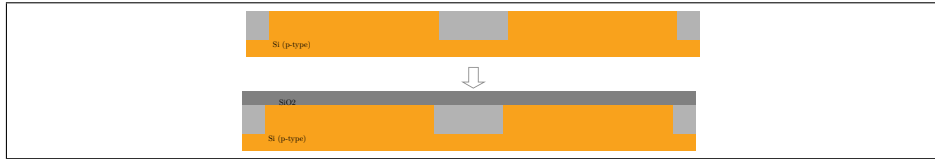
The surface concentration of the n-well ( $\approx 1 \times 10^{16} cm^{-3}$ ) is determined primarily by the need to maintain a sufficient high surface concentration to prevent field inversion of the n-well. The depth of the n-well ( $\approx 4\mu m$ ) is then determined by the need to prevent punch-through of the parasitic vertical pnp transistor under worst case bias conditions.



**Figure 13:** N-Well layout

### 4.2.1 Mask dioxide layer

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide ( $SiO_2$ ) layer needs to be grown on top of a p-type substrate.

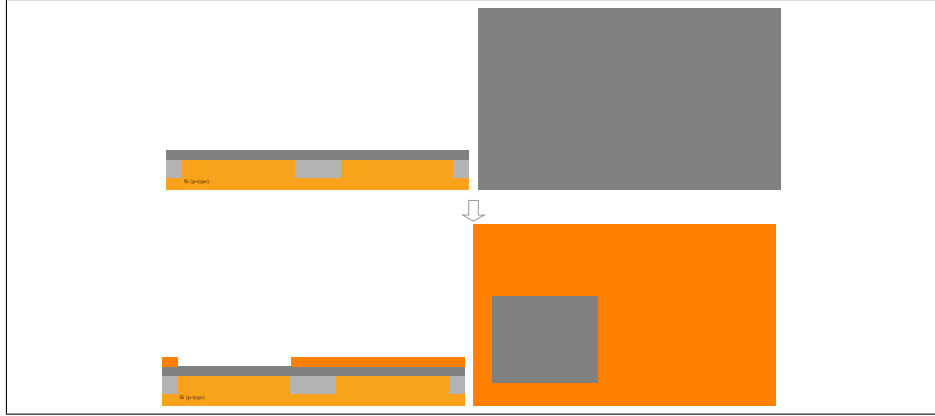


**Figure 14:** Dioxide layer growth

The industrial best practice is a layer of around ( $500\text{nm}\approx 5000\text{\AA}$ ) thickness or more. For this purpose the wafer is being oxidized for at least 90 minutes at  $1000^{\circ}\text{C}$  using wet oxidation which results in a dioxide layer at least  $500\text{nm}(\approx 5000\text{\AA})$  in thickness.

### 4.2.2 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "nwell" layer within the GDS2 file.

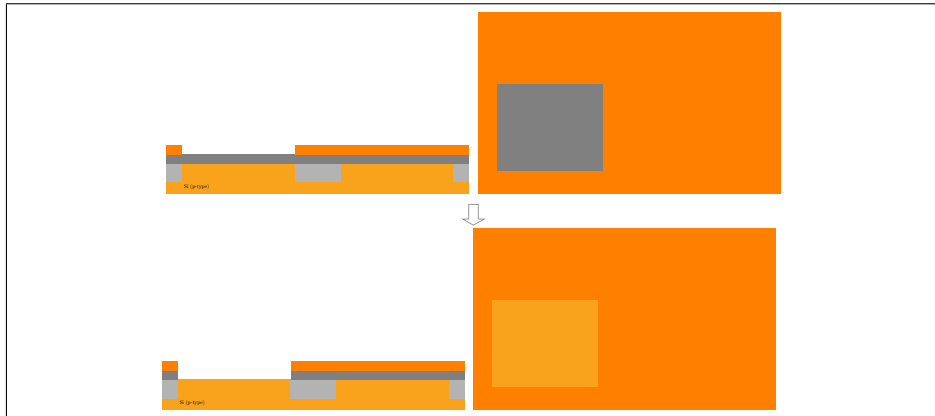


**Figure 15:** Cross/top view of n-well layout on resist

The thickness of the resist layer and the backing duration will variate depending on the specific equipment for which this process will be implemented with.

### 4.2.3 Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

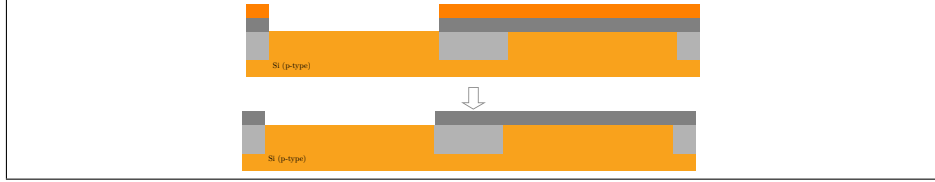


**Figure 16:** Cross/top view of n-well oxide window

Since the silicon dioxide layer is 500nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) ([Equation 3.1](#)) we can etch with a speed of approximately 2 nm/s at 25 °C, we can calculate the etching time to be  $\frac{500nm}{2nm/s}=250s=4 \text{ minutes } 10 \text{ seconds}$  (or make it rather 30 seconds instead of 10)

#### 4.2.4 Cleaning

In order to avoid contamination of the machines we need to make sure all the resist has been stripped off from the wafer.

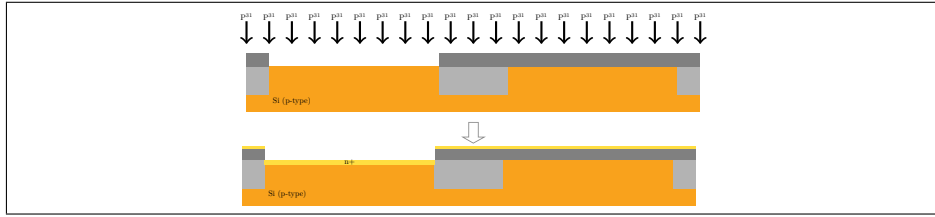


**Figure 17: Resist removal**

Please just use the solvent for the specific resist.

#### 4.2.5 Injection

We now need to inject the carriers into the upper level of the n-channel area so that we can later on drive them into the crystal during the drive-in step.

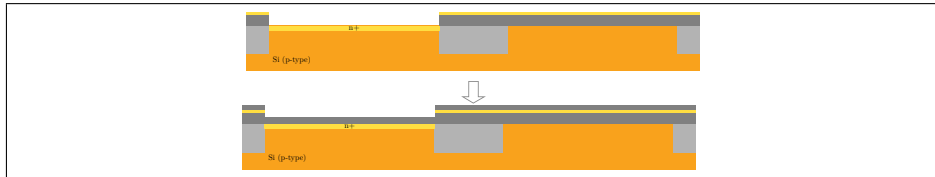


**Figure 18: Doping process**

The n-well is implanted with a Phosphorus ( $P^{31}$ ) dose of  $2.5 \times 10^{12} cm^{-2}$  at an energy of 100 KeV. The n-well is then annealed.

#### 4.2.6 Oxide for drive-in

Now we need to cover the now doped and annealed areas with an oxide layer for the drive-in phase.

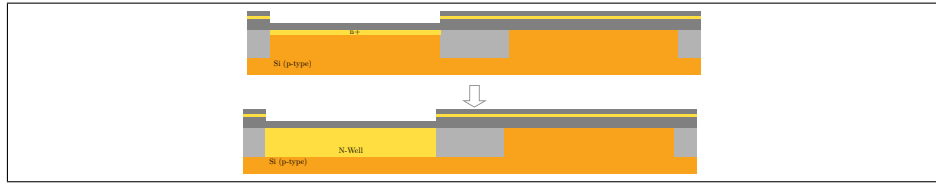


**Figure 19: Oxide growth**

The wafer is being oxidized for 32 minutes at 1000°C in order to achieve a cover silicon layer of 250nm thickness ( $\approx 2500\text{\AA}$ ).

#### 4.2.7 Drive-in

In order to drive the carrier atoms deeper into the crystalline structure the wafer needs to be driven in after predeposition.

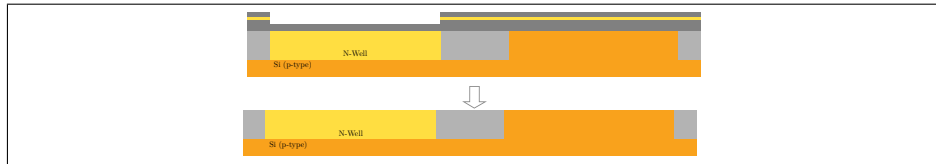


**Figure 20:** Drive-in process

In this step the wafer is driven-in for 960 minutes at 1150°C in an inert ambient.

#### 4.2.8 Oxide mask removal

We want to remove the silicon mask from the wafer so that the n-well becomes accessible for the further process steps but we don't want to etch "way too much" of the trench material.

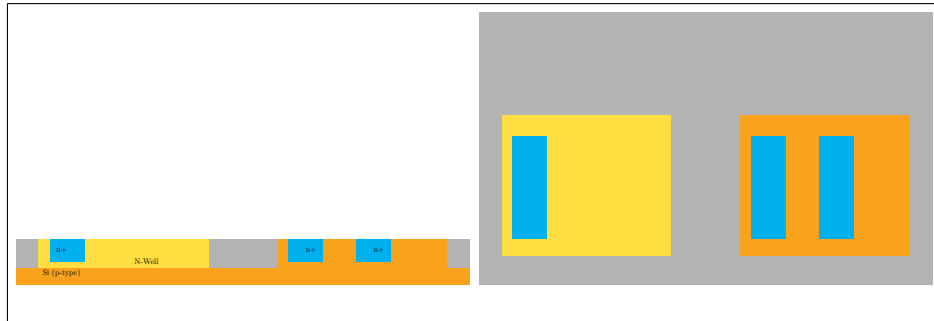


**Figure 21:** Oxide removal

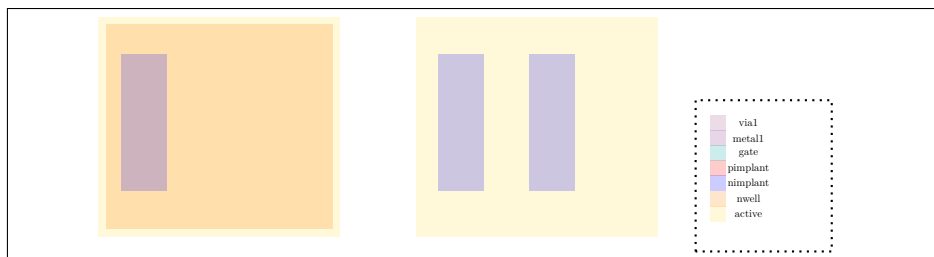
Since the silicon dioxide layer is 750nm (500nm+250nm) thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter. Using BHF (6:1) ([Equation 3.1](#)) we can etch with a speed of approximately 2 nm/s at 25 °C. We can calculate the etching time to be  $\frac{750nm}{2nm/s} = 375s = 6$  Minutes and 15 Seconds.

Etching away a "little bit too much" of the oxide isn't that bad, because the oxide within the trenches will be "filled up" again during the later steps.

### 4.3 n+ Implant

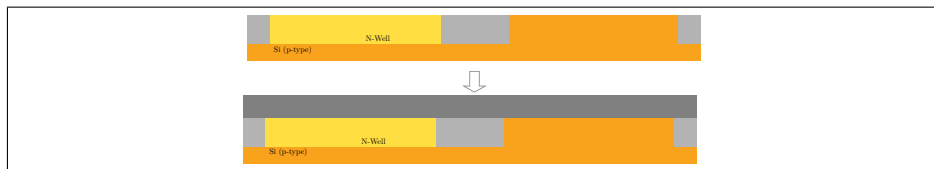


**Figure 22:** N+ implant geometry target



**Figure 23:** N+ layout

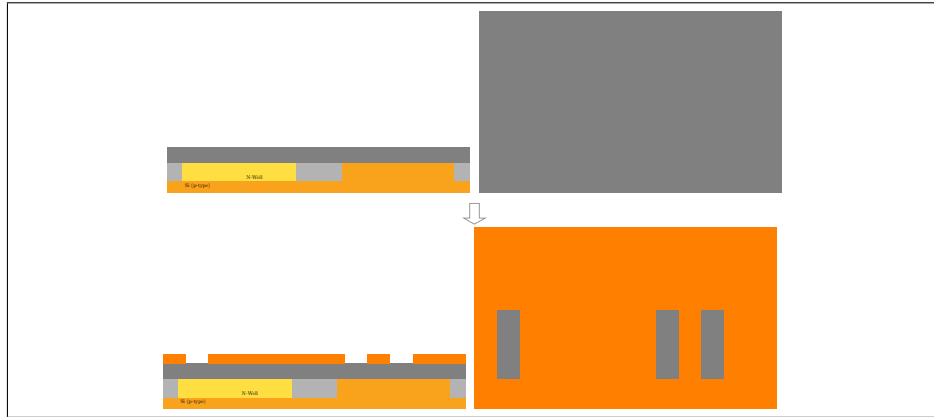
#### 4.3.1 Mask dioxide layer



**Figure 24:** Oxide layer

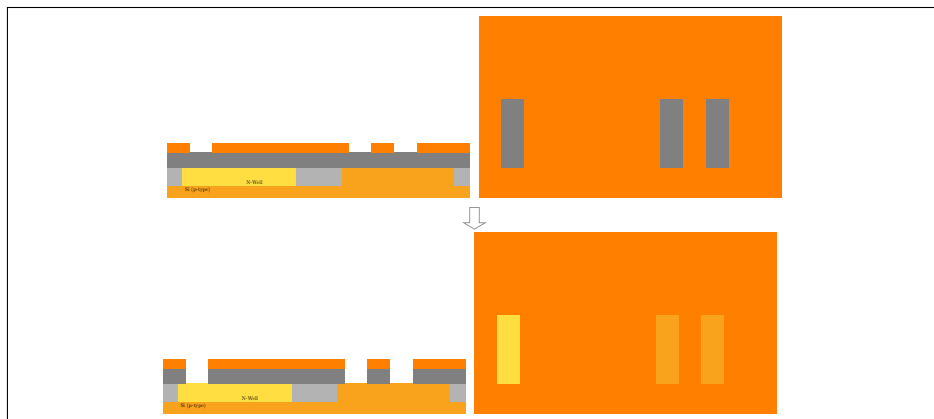


### 4.3.2 Patterning



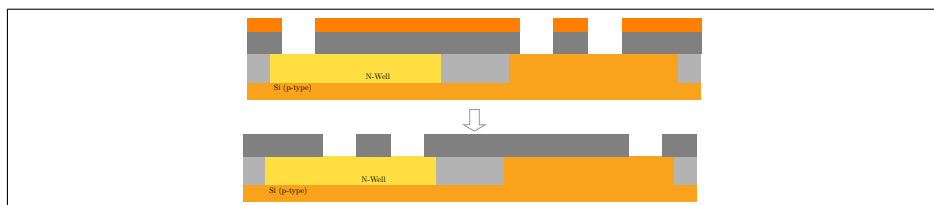
**Figure 25:** N+ region resist mask

### 4.3.3 Etching



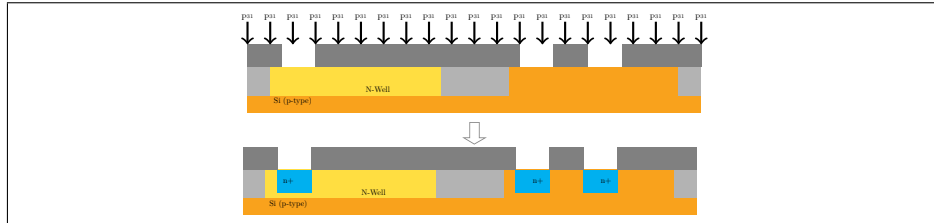
**Figure 26:** N+ region opened

### 4.3.4 Cleaning



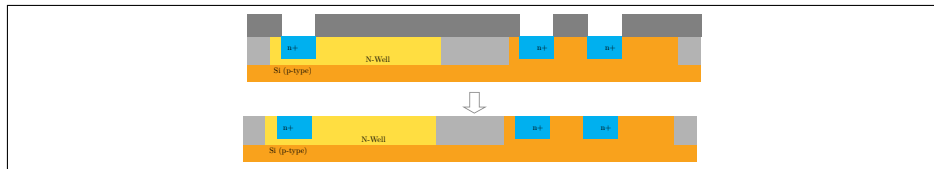
**Figure 27:** Resist removal

### 4.3.5 Injection



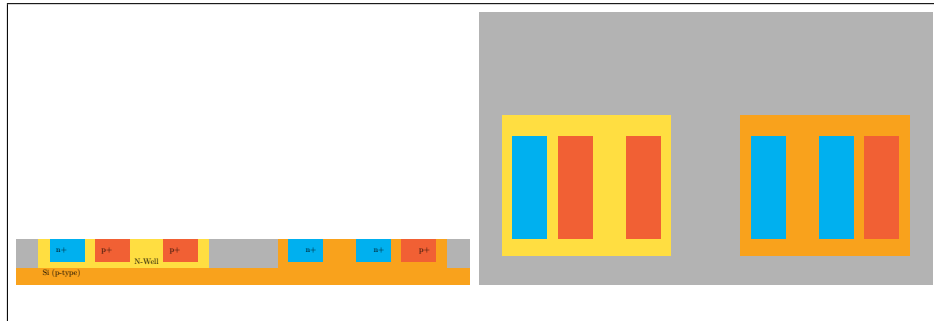
**Figure 28:** N+ injection process

### 4.3.6 Oxide removal



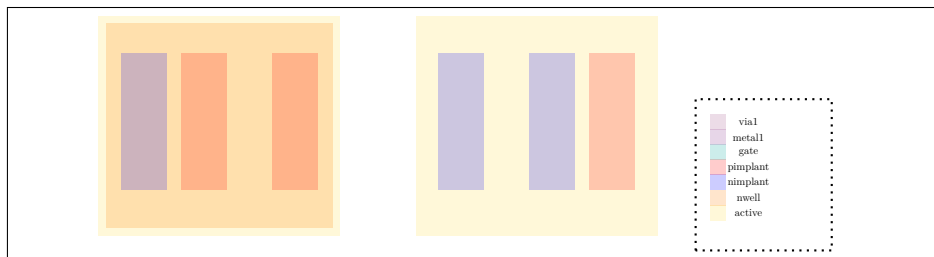
**Figure 29:** Oxide removal

## 4.4 p+ Implant



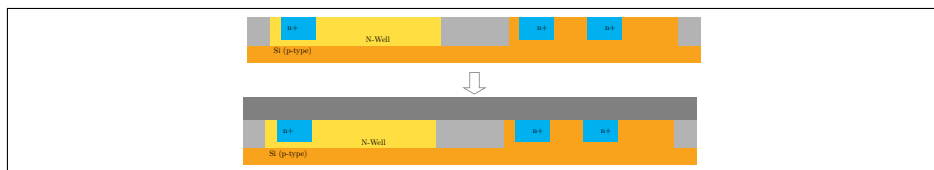
**Figure 30:** P+ implant geometry target

For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required. In this step we're going to build these.



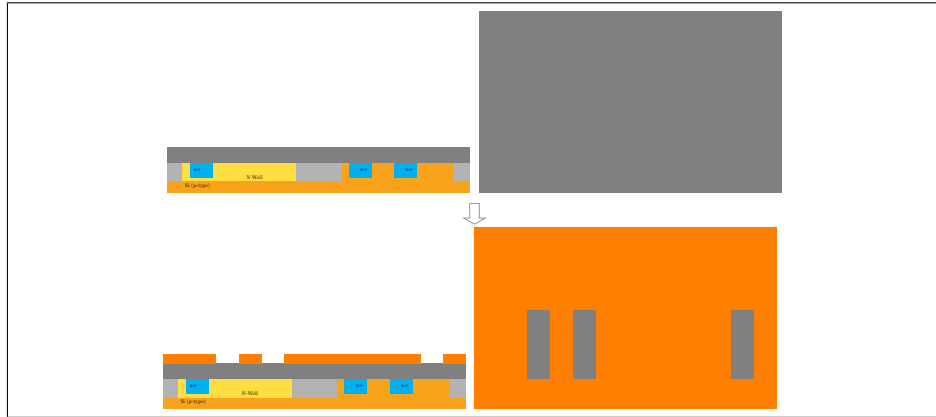
**Figure 31:** P+ layout

### 4.4.1 Mask dioxide layer



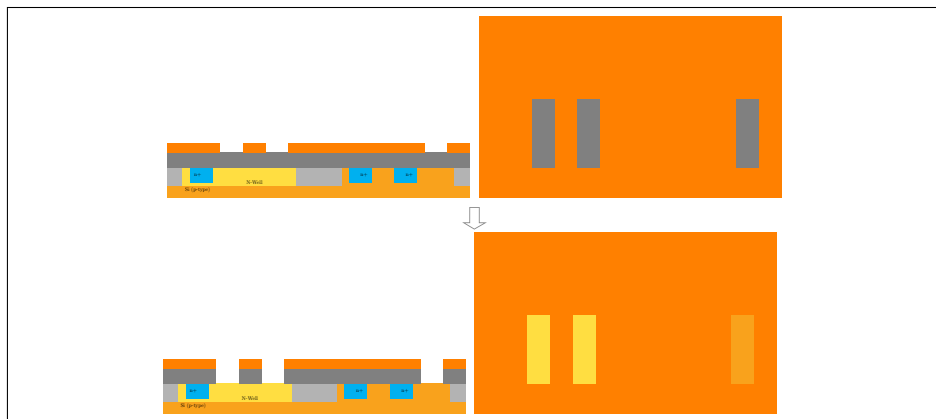
**Figure 32:** Oxide layer

#### 4.4.2 Patterning



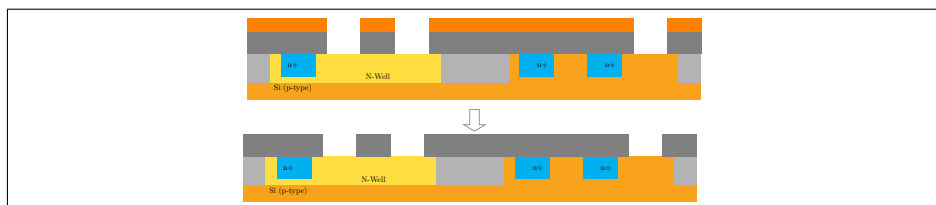
**Figure 33:** P+ region resist mask

#### 4.4.3 Etching



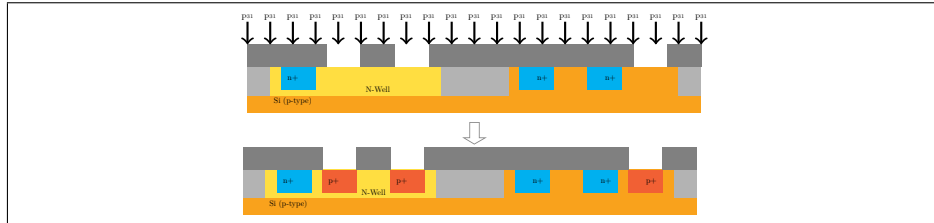
**Figure 34:** P+ region opened

#### 4.4.4 Cleaning



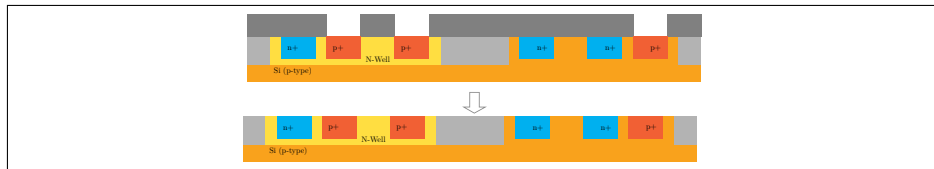
**Figure 35:** Resist removal

#### 4.4.5 Injection



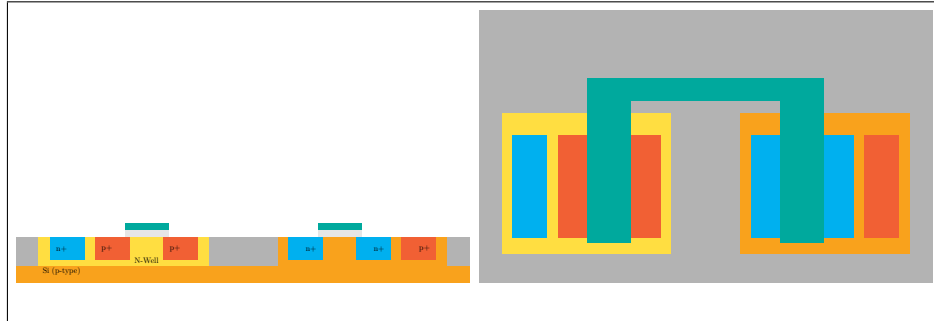
**Figure 36:** P+ injection process

#### 4.4.6 Oxide removal

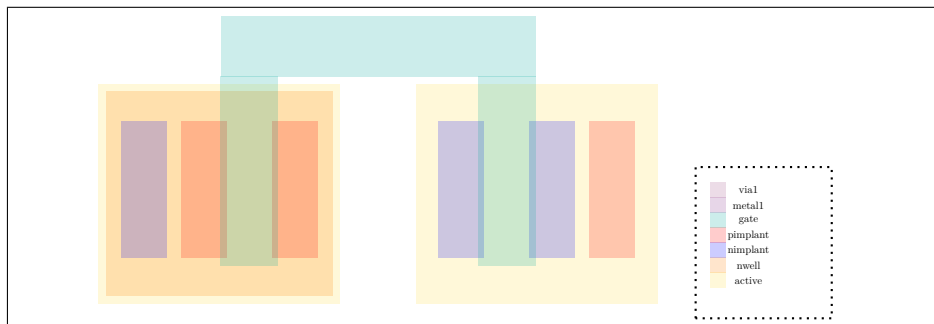


**Figure 37:** Oxide removal

## 4.5 Gate contact

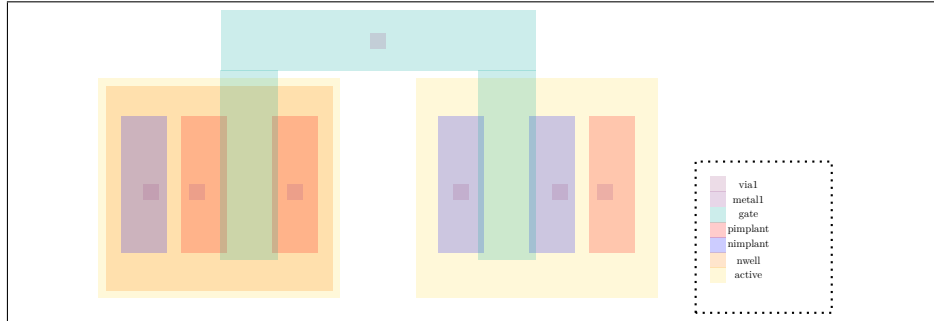


**Figure 38:** Aluminum gate contacts with gate oxide



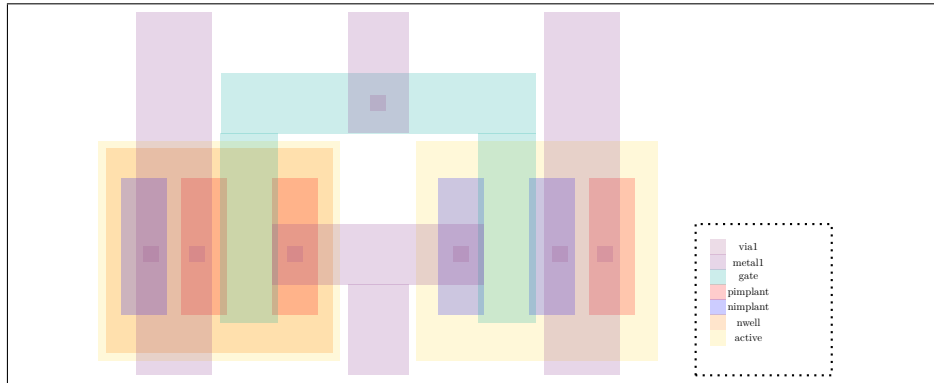
**Figure 39:** Gate layout

## 4.6 First vias



**Figure 40:** First via layout

## 4.7 First metal layer



**Figure 41:** First metal layout