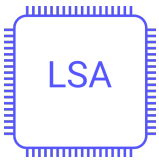
Libre Silicon 1.0μm process:

LS1UH

Hightech variant



DESCRIPTION

The LS1UH series is LibreSilicons 1.0 micron modular mixed signal CMOS technology with non-volatile memory. Based upon the industrial standard single poly with up to 3 metal layers 1.0 micron drawn gate length and a twin-well process, integrated with non-volatile memory and ultra-low noise modules, the platform is ideal for SoC applications in the automotive market, as well as emdedded high-voltage applications in the communications, consumer and industrial market. Comprehensive design rules, precise SPICE models, analog and digital libraries, IPs and development kits support the process for free and open source tools.

KEY FEATURES OVERVIEW

- 1.0-micron single poly, up to three-metal
- Twin-well CMOS process
- Typical supply voltage from 3.0 V to 18 V (maximum tollerance 40V)
- Extended temperature range from $-55°C$ up to $+125°C$
- Integrated digital, analog and NVM in a single process
- Isolation well for all MOS devices
- Lateral PNP/NPN BJT devices
- Insensitive towards cosmic radiation
- ESD protected
- Low-noise NMOS/PMOS
- High-reliability NVM using SONOS technology
- Typical and worst-case and best-case models - BSIM3v3 (MOS, BJT, RES, CAP)
- QFlow PDK

APPLICATIONS

- Automotive
- Robotics
- Safety

PRIMITIVE DEVICES

- MOS transistors
- SONOS flash cells
- Lateral PNP/NPN BJTs
- SRAM cells
- Poly, Metal, Diffusion Resistors
- Protection, Polysilicon diodes