Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Contents

Libre Silicon process steps

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June 19, 2018

The general flow chart of the overall process flow can be seen in Figure 1. These process steps will be discussed within the following sections.

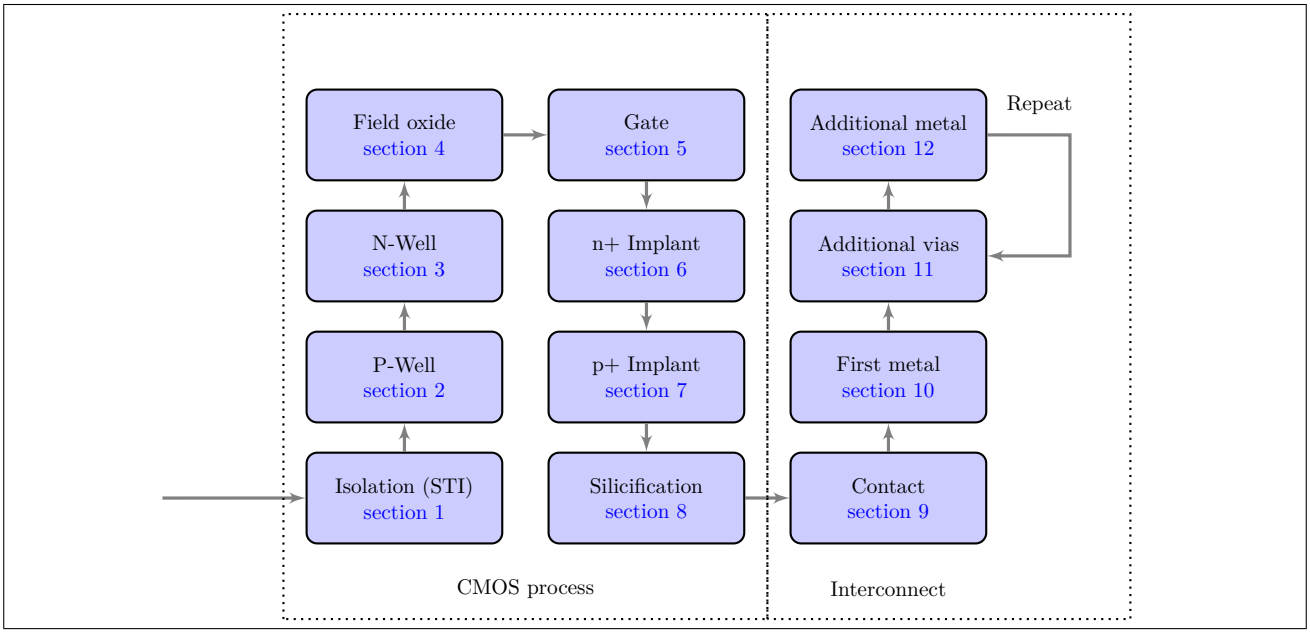

Figure 1: Frontend and backend process flow

The six overall process steps are part of an active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world.
For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

If you don't have a plasma etcher you will need <111> substrate!

You will **need** a sputterer for this process

1 Shallow trench isolation

The geometry of a substrate with STI implemented can be seen in Figure 2.

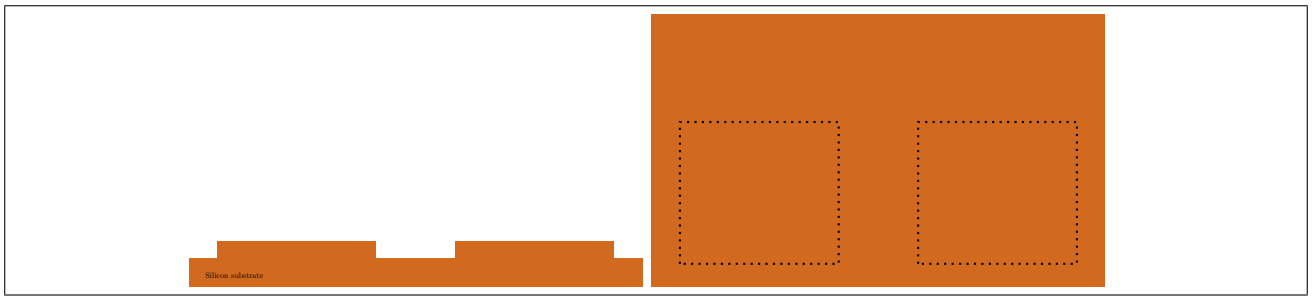

Figure 2: Shallow trench isolation target geometry

As can be seen in Figure 19, the n-well and the STI trench are supposed to have approximately the same depth but the n-well and p-well go down a little bit further. Because the n-well will be $\approx 4\mu m$ in depth we have to match this with our trench depth. I order to allow a sufficiently low resistance of the ESD diode but at the same time a sufficient isolation of between the standard cells a trade-ff has been done. The targeted depth of the box isolation is $\approx 2\mu m$.

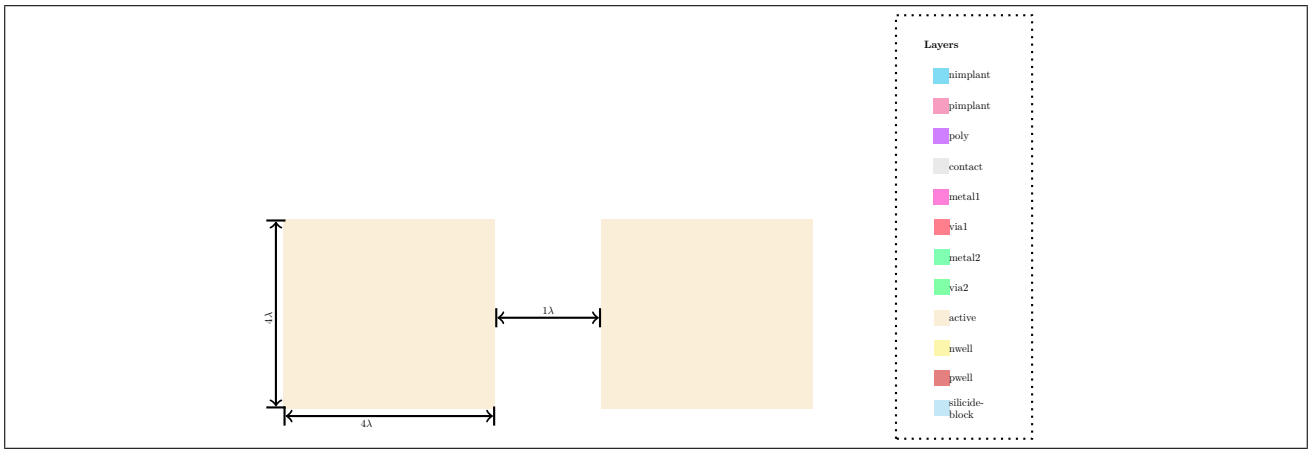

Figure 3: Shallow trench isolation layout

In Figure 3 we can see the layout for the STI area. The STI area will be everywhere, where no active areas are. The field oxide needs to be grown out of trenches which can't be etched out of the silicon by using resist as a mask. For that reason we will have to resort to a protective mask made from a silicon dioxide layer which has to be etched before hand. So the mask will be exposed onto positive resist on top of the hard mask oxide layer in order to form a protective mask covering the active areas from having etched trenches into them. After that we can either use a dry etching method or wet etching for cutting into the silicon substrate and making the active area become islands with trenches in between. After these steps we have to remove the hard mask. Our minimum width and height as well as the space between the active areas comes from the line space constrain of the silicon etcher and of course the optical limitations of the stepper which are as well $0.5\mu m$.

1.1 Initial cleaning

In order to remove the initial naturally grown silicon dioxide from the wafer, acid is being applied to the wafer which leads to a pure silicon substrate wafer as in the process illustration shown in Figure 4.

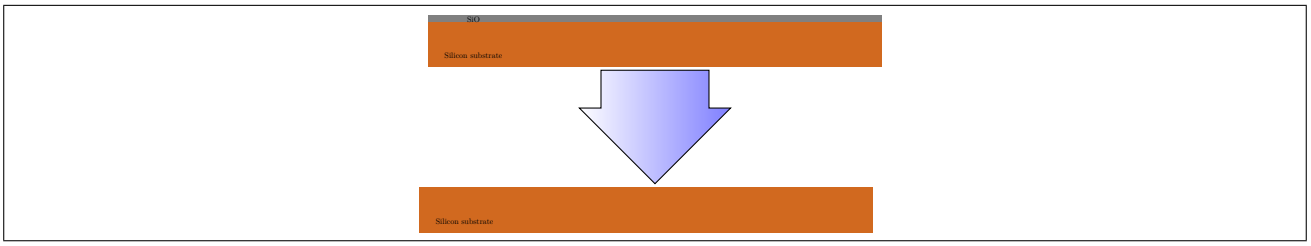

Figure 4: Initial cleaning

This needs to be done because the naturally grown initially existing silicon oxide is not pure and may contain contamination which may render the final product unusable.

1.1.1 Sulfuric Cleaning

The sulfuric acid mixture, $H_2SO_4 + H_2O_2$ is being applied to the wafer for 10 minutes at a temperature of 120 °C.

1.1.2 HF dip

After the sulfuric cleaning a HF (HF:H_2O,1:50) dip is being performed for one minute.
Hydrofluoric acid (HF) is used to remove native silicon dioxide from wafers. Since it acts quickly, one needs to only expose the wafer for a short time (”dip”).

1.1.3 Drying

After that the wafer needs to be dried and quickly processed further before new uncontrolled natural oxide can build up on the wafer through the contact with air.

1.2 Hard mask: Oxide growth

We need a thick layer of oxide as protective hard mask to etch the trenches into the silicon.

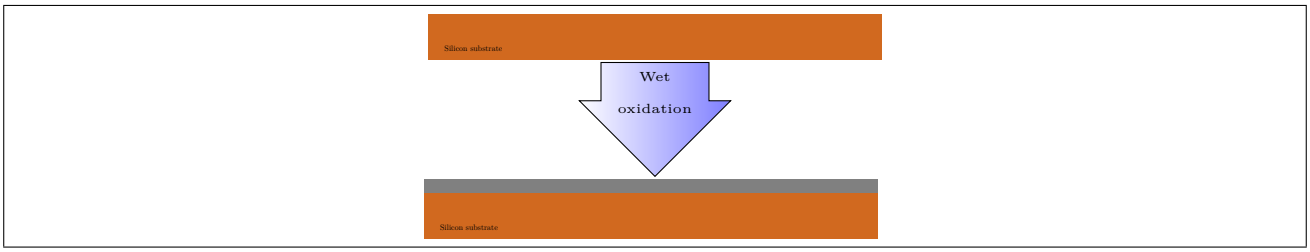

Figure 5: Hard mask growth

In subsection 1.6.we want to etch $2\mu m$ deep into the silicon which, depending on the approach, will take a different amount of oxide for an effective hard mask.

For now we only have the plasma etcher variant being verified because chemically etching the silicon wafer with KOH isn't allowed at the HKUST labs for contamination control reasons. In case you can verify this in your lab with a chemical etching method, please update this chapter and make a pull request!

Possible approaches:

- **"DRIE Etcher #1" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
  With this method it takes pretty much a minute to etch $2\mu m$ deep.
  In one minute the oxide will have been etched away by at most 25nm.
  This means we can grow a 100nm thick layer and are well off.
  Growing 100nm of dioxide takes around 5 minutes 30 seconds at $1050°C$ in wet ambient[1].

- **Chemical solution**
  When using KOH acid at $60°C$, it takes 4 minutes and 30 seconds in order to etch $2\mu m$ deep.
  This means the oxide layer needs to be at least 226 nm thick, so we choose a nice round number of 300nm.
  The layer of silicon dioxide of around 300nm thickness is grown in wet ambient for 25 minutes at $1050°C$ [2] in the diffusion furnace.

1.3 Hard mask: Patterning

The resist is being deposited using spin coating and then soft baked depending on the baking time for the specific resist. The requirement is a **positive** tone resist.

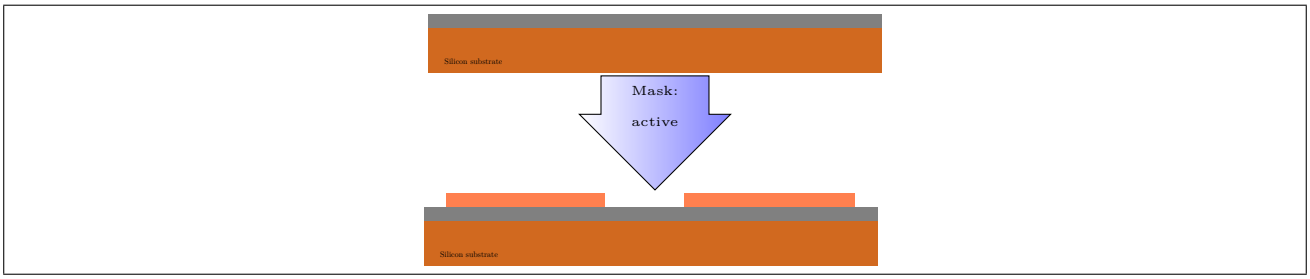

Figure 6: Patterning with positive resist

The layout for being exposed onto the resist is being extracted from the "active" layer within the GDS2 file onto a onto a **bright field** mask because we need to use the same mask again in section 4, so alignment needs to be possible.

[1] `http://cleanroom.byu.edu/OxideTimeCalc`
[2] `http://cleanroom.byu.edu/OxideTimeCalc`

1.4 Hard mask: Etching

We open the access to the silicon, outside of the active areas, in order to etch the trenches.

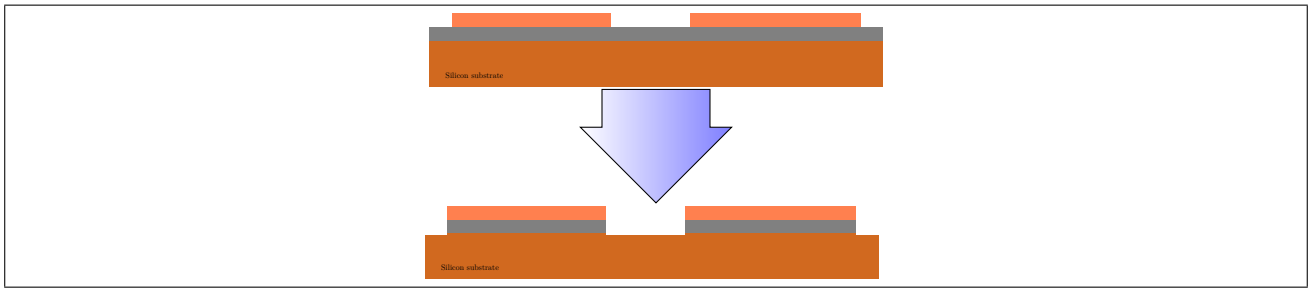

Figure 7: Nitride mask etching

There are dry etching and wet etching methods available for etching the oxide hard mask. The downside of wet etching is that it also etches horizontally, however the chemical BHF is readily available and allows for easy implementation of the process.

Possible approaches:

- **"DRIE Etcher #1" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for a little bit over 3 minutes in order to get through the 300nm of oxide or around 1 minute for 100nm.in case RIE is being used for silicon etching
  Etching too long might cause under-etch however!

1.5 Hard mask: Resist removal

Now we need to remove the contaminants for further processing.

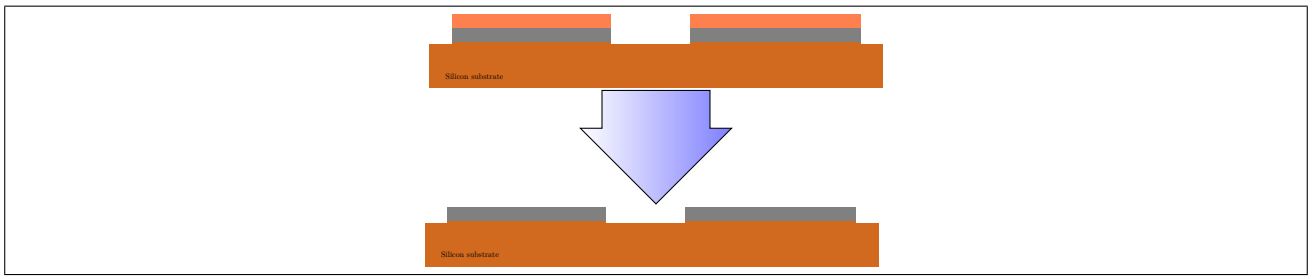

Figure 8: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

1.6 Silicon etching

Silicon can only be etched by a very aggressive chemical cocktail of KOH and TMAH (20%) or by plasma etching.

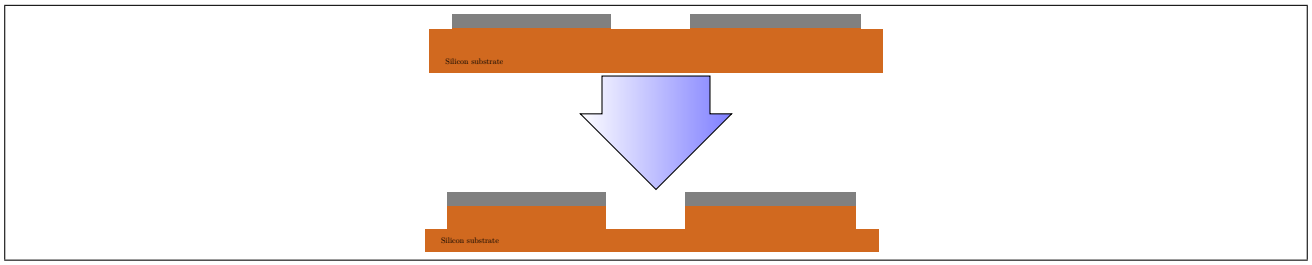

Figure 9: Trench etching

For now we only have the plasma etcher variant being verified because chemically etching the silicon wafer with KOH isn't allowed at the HKUST labs for contamination control reasons. In case you can verify this in your lab with a chemical etching method, please update this chapter and make a pull request!

Possible approaches:

- **"DRIE Etcher #1" from HKUST**
  This machine a normal etching rate of up to $2\frac{\mu m}{min}$ for etching silicon.
  This means we etch for 1 minute in order to reach the desired depth.
  The selectivity to oxide is >80:1 which means the etch speed for the hard mask will be at most $\frac{1}{80}2\frac{\mu m}{min} = \frac{1}{80}2000\frac{nm}{min} = 25\frac{nm}{min}$.
- **Chemical solution**
  Using a KOH solution of 20% at $60°C$ gives us an etch rate of roughly $26.57\mu m$ per hour[3].
  - The <100> etch rate is: 26.57 micron/hr = 0.44 micron/min
  - The <110> etch rate is: 40.5 micron/hr
  - The <111> etch rate is: 0.4932 micron/hr
  - The SiO2 etch rate is: 49.92 nanometers/hr

  With a desired depth of $2\mu m$ we will have to etch around 4 minutes and 30 seconds in order to reach the desired depth. The disadvantage of this approach is the imprecision and under-etch of the mask.

1.7 Hard mask: Removal

Now we have to remove the oxide hard mask for further processing in order to proceed with well formation without contamination during oxide growing.

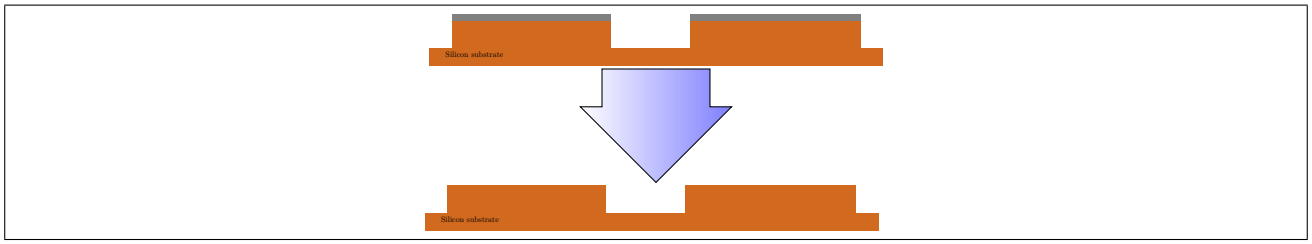

Figure 10: Trench etching

We use buffered hydrofluoric acid (BOE (1:6)) at room temperature for a little bit over 3 minutes in order to remove all of the 300nm thick oxide layer and roughly 1 minute for 100nm.

[3] `http://www.lelandstanfordjunior.com/KOH.html`

‘

2 P-well

In order to build CMOS on the same substrate, a P-well is required for building the complementary N-channel transistor for a n-p-channel logic circuitry. The cross section as well as the top view of the targeted geometry are shown in Figure 19

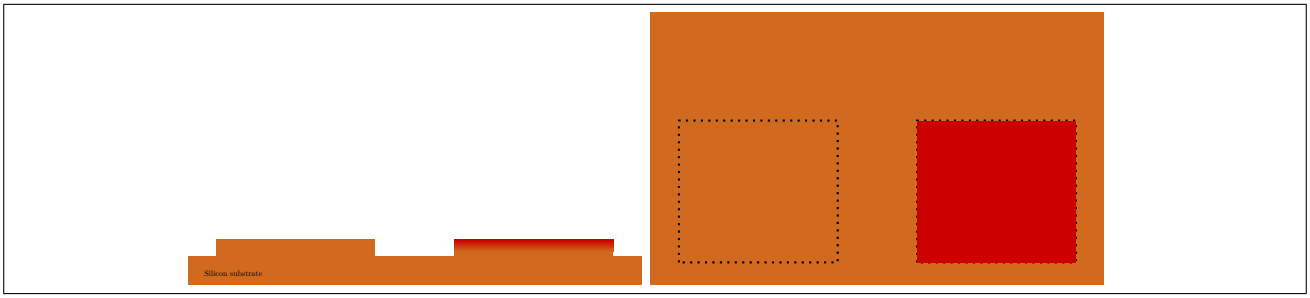

Figure 11: P-well target geometry

The P-well will serve us as an island of higher p-doped substrate within the slightly p-doped basis substrate. The dopant dose will be $2.5 \times 10^{12} cm^{-2}$ as calculated in the documentation of the process design leading to these steps[4].

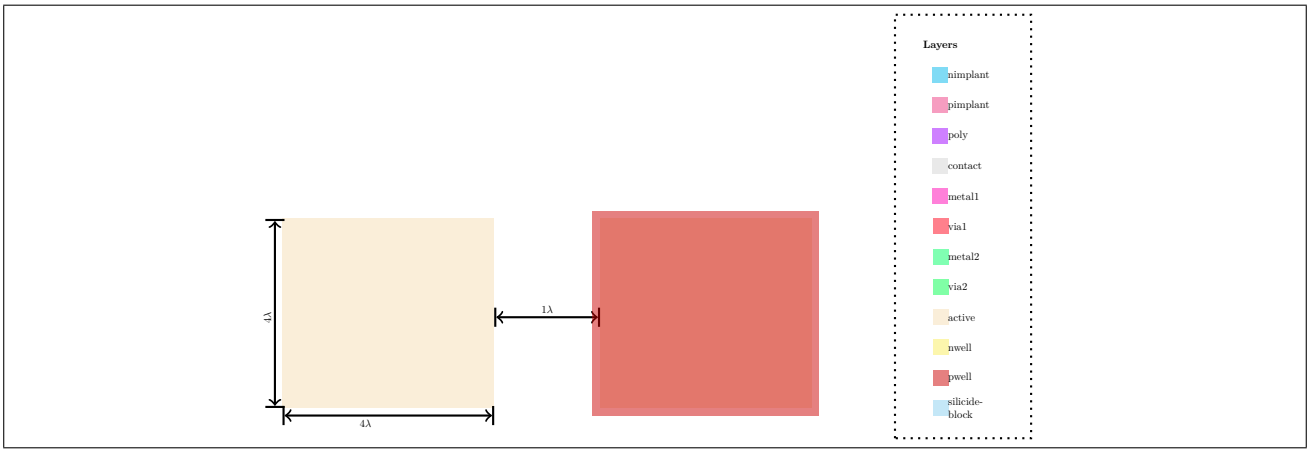

Figure 12: P-Well layout

In Figure 12 the layout of the P-well region on top of the active area region can be seen.
The p-well is being fit into the active area.
It should even be a little bit bigger than the active area, because of possible alignment offsets

[4] https://github.com/leviathanch/libresiliconprocess/raw/master/process_design/process_design.pdf

2.1 Hard mask: Dioxide growth

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

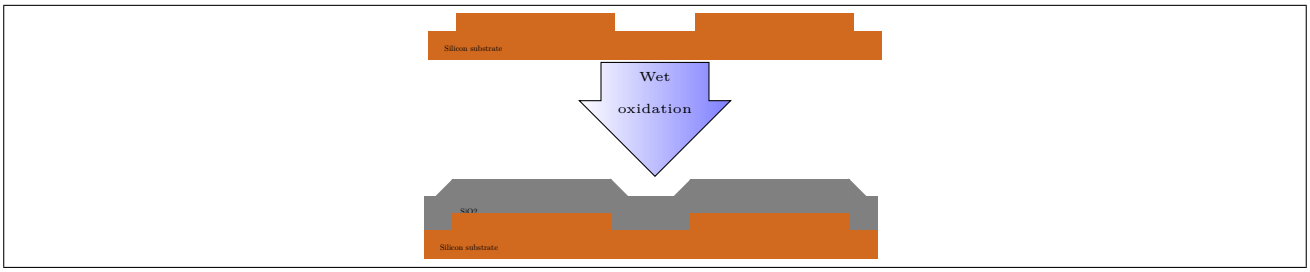

Figure 13: Dioxide layer growth

With an energy of 100keV for the implantation performed in subsection 2.5, the projected range of the dopants within the oxide will be 310nm (380nm tops) [5]. This means being on the safe side and having 500nm as the thickness is a good approach.
In order to grow the 500nm thick oxide layer, the wafer is being oxidized for around 56 minutes at 1050°C using wet oxidation which results in a dioxide layer of around 500nm in thickness[6].

2.2 Hard mask: Patterning

The resist is being deposited spray or spin coating (spray coating is better because of the uneven surface!) and then soft baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "pwell" layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

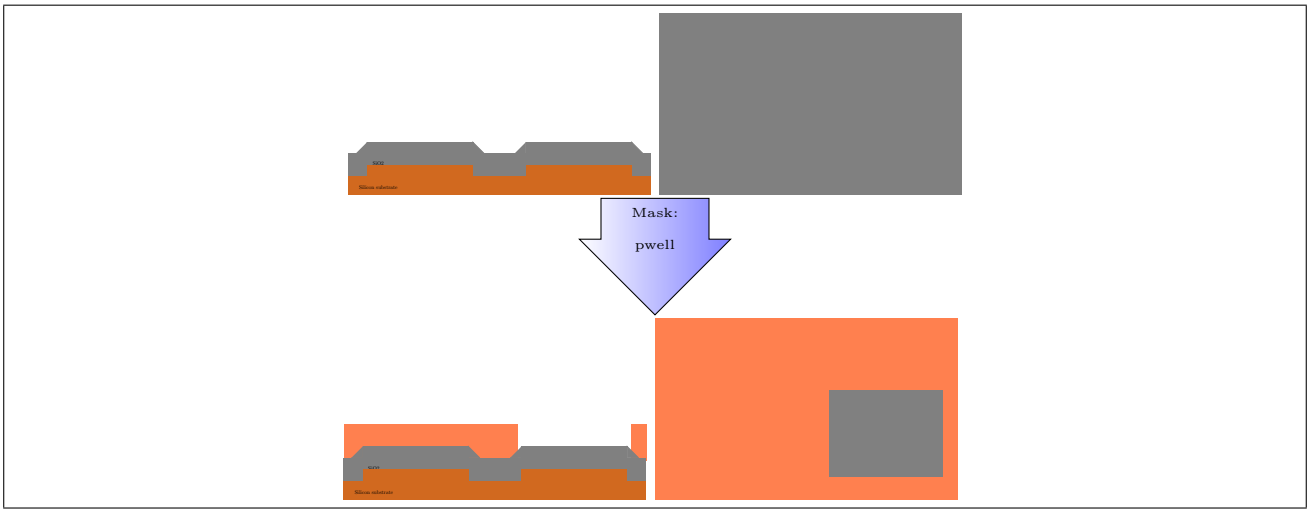

Figure 14: Cross/top view of P-well layout on resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

[5] http://cleanroom.byu.edu/rangestraggle
[6] http://cleanroom.byu.edu/OxideTimeCalc

2.3 Hard mask: Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

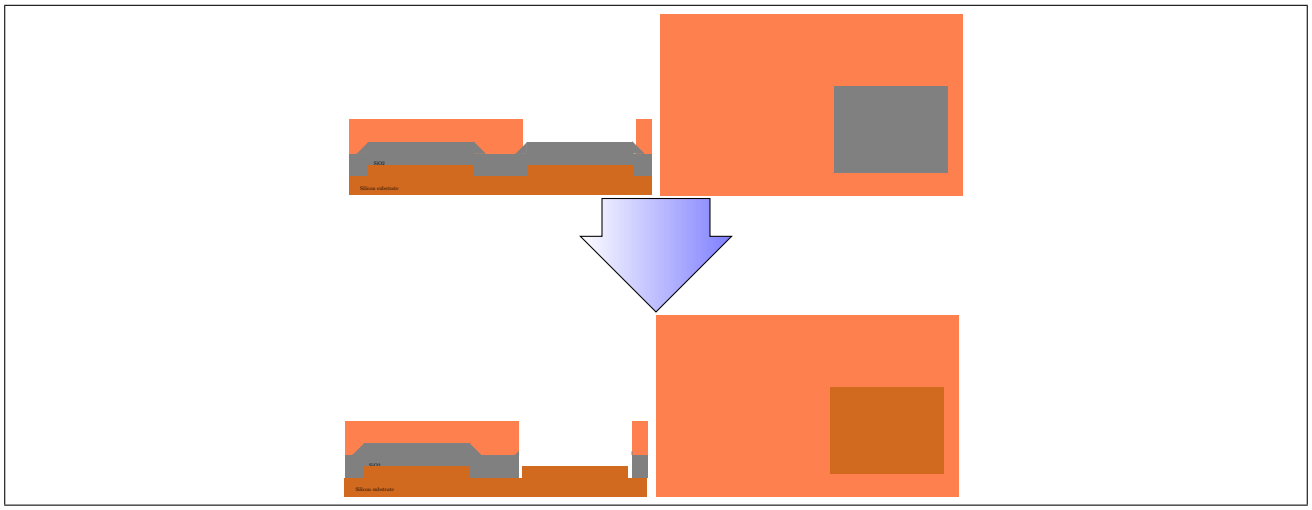

Figure 15: Cross/top view of P-well oxide window

There are multiple possible approaches to etch through these 500nm of oxide.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for 5 minutes in order to get through the 500nm of oxide.
  Too long over 4 minutes might cause under-etch however!

2.4 Hard mask: Resist strip

In order to avoid contamination of the machines we need to make sure all the resist has been stripped off from the wafer.

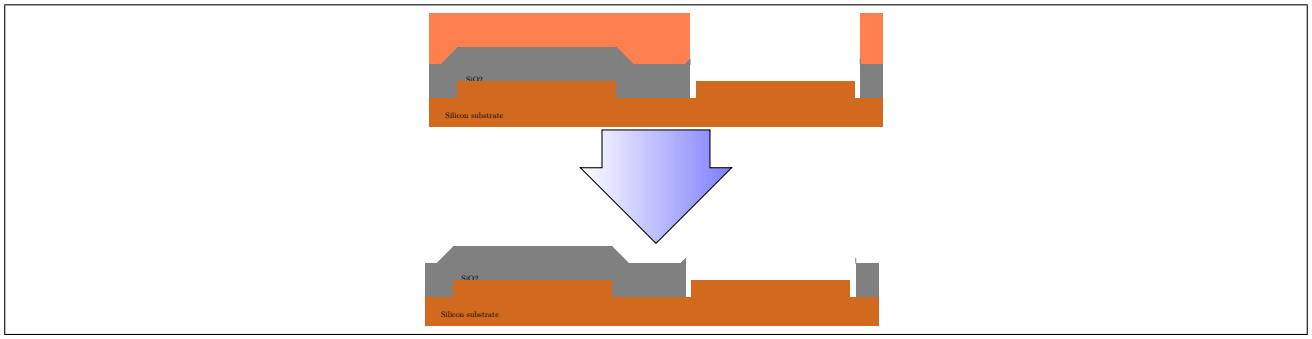

Figure 16: Resist removal

Please just use the solvent for the specific resist.

2.5 Implantation/Doping

We now need to inject the carriers into the upper level of the n-channel area so that we can later on drive them into the crystal during the drive-in step.

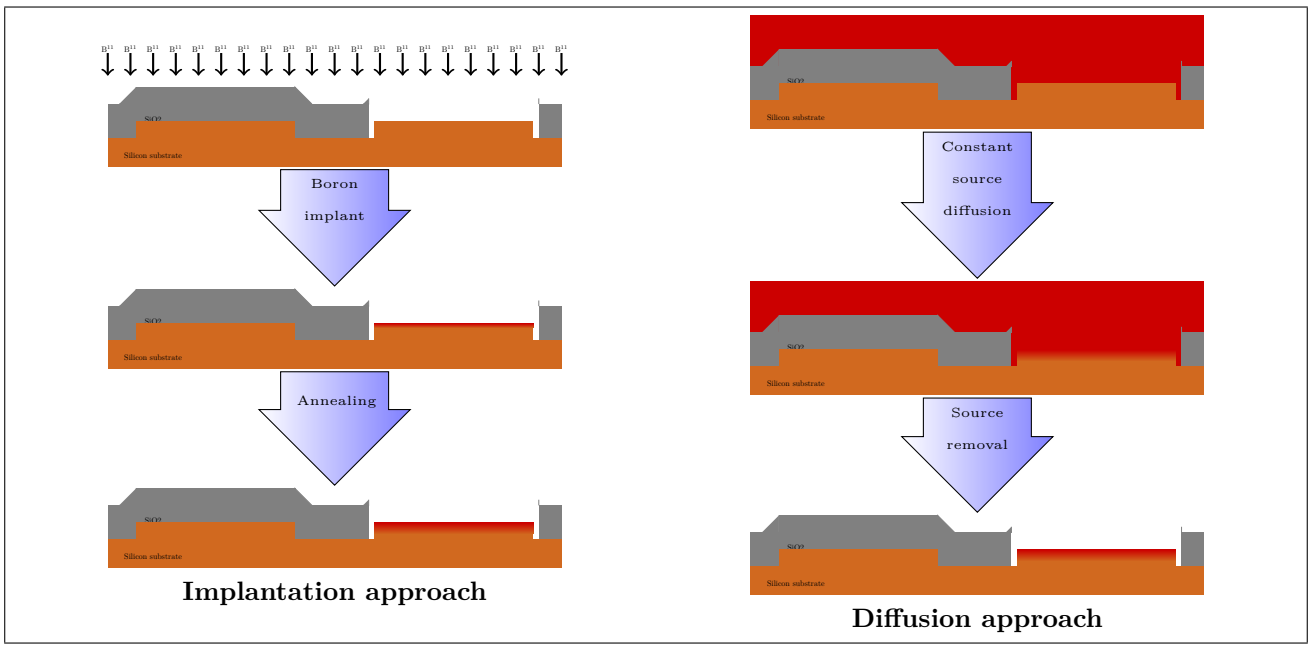

Figure 17: Doping process

Possible approaches:

- **"CF-3000 Implanter (IMP-3000)" from HKUST**
  At HKUST we have an implanter which gives us better control over the initial surface concentration. These steps are needed to arrive with the desired geometry:
  1. The P-well is implanted with a Boron (B^{11}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 keV
  2. The P-well is annealed for 30 minutes at $1050°C$ in N_2 environment (DIF-A1)
     After that the P-well will be around $1\mu m$ deep and will become deeper during subsection 3.5

- **Constant source diffusion**
  We can add a layer of Boron solution and diffusing in order to have an initial concentration in order to reach the desired concentration later by main diffusion.
  1. A constant source is added (gas or liquid)
  2. The source dopant is driven in for 10 minutes at $1050°C$
  3. The dopant source is removed by stopping the gas flow or cleaning the surface

2.6 Hard mask: Removal

Now we want to remove the silicon mask from the wafer and clean it for another clean oxide mask layer in order to perform the implantation of the N-well in the next step.

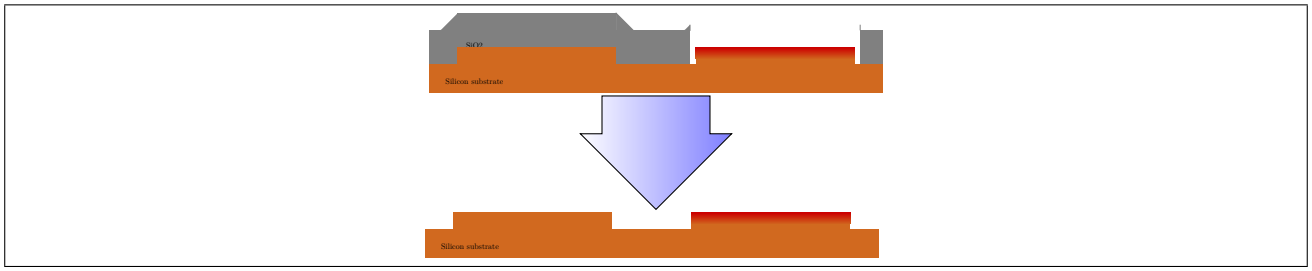

Figure 18: Oxide removal

We use buffered hydrofluoric acid (BOE (1:6)) at room temperature for 5 minutes in order to remove the 500nm of oxide layer.

3 N-well

In order to build CMOS on the same substrate, an N-well is required for building the complementary P-channel transistor for a n-p-channel logic circuitry as shown above in the example section. The cross section as well as the top view of the targeted geometry are shown in Figure 19

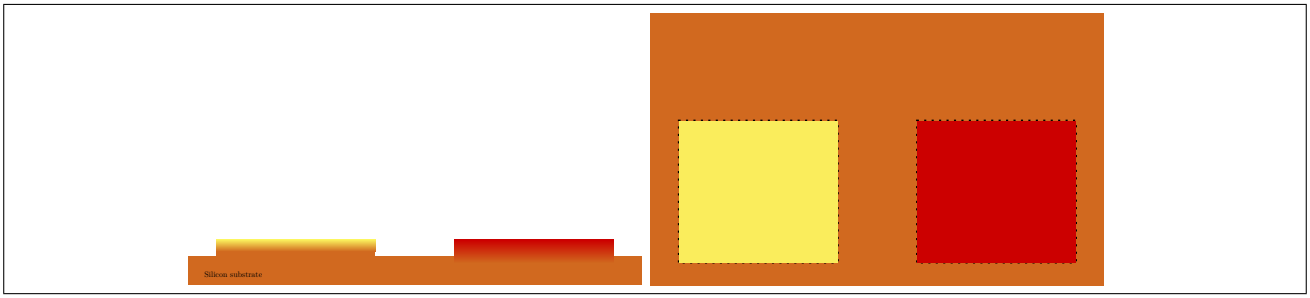

Figure 19: N-well target geometry

The N-well will serve us as an island of N-doped substrate within the P-doped basis substrate.
The dopant dose will be $2.5 \times 10^{12} cm^{-2}$ as calculated in the documentation of the process design leading to these steps[7].

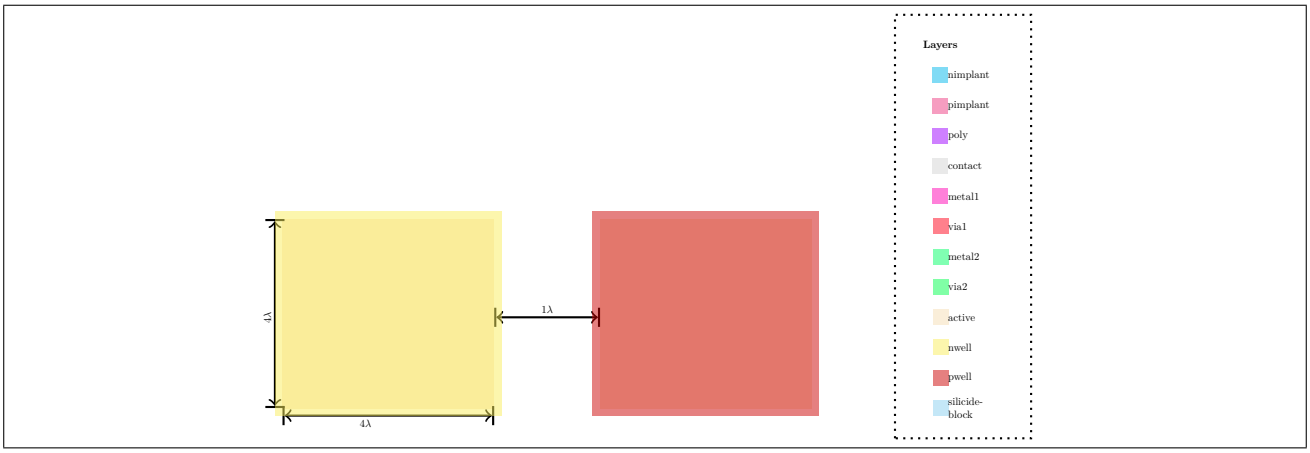

Figure 20: N-Well layout

In Figure 20 the layout of the n-well region on top of the active area region can be seen.
The n-well is being fit into the active area. It should even be a little bit bigger than the active area, because of possible alignment offsets

[7] https://github.com/leviathanch/libresiliconprocess/raw/master/process_design/process_design.pdf

3.1 Hard mask: Dioxide growth

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

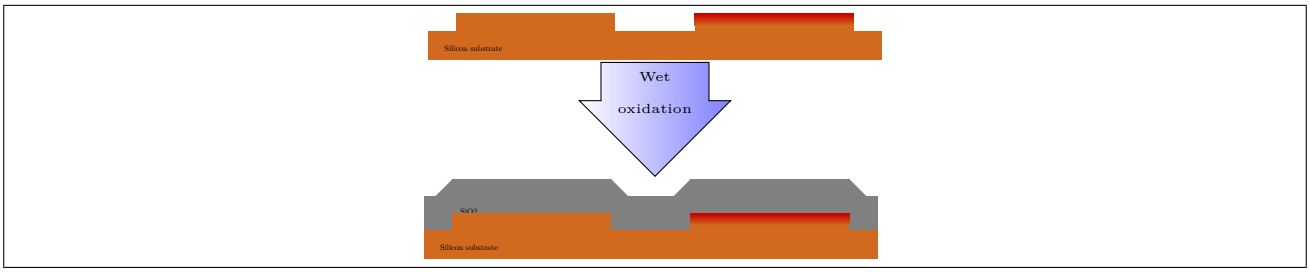

Figure 21: Dioxide layer growth

With an energy of 100keV for the implantation performed in subsection 3.5, the projected range of the dopants within the oxide will be 100nm (130nm tops) [8]. This means being on the safe side and having 200nm as the thickness is a good approach.
In order to grow the 200nm thick oxide layer, the wafer is being oxidized for around 14 minutes at 1050°C using wet oxidation which results in a dioxide layer of around 200nm in thickness[9].

3.2 Hard mask: Patterning

The resist is being deposited using spray coating because the uneven nature of the oxide layer. After that the wafer is being soft baked depending on the baking time and temperature for the specific resist. The layout for being exposed onto the resist is being extracted from the "nwell" layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

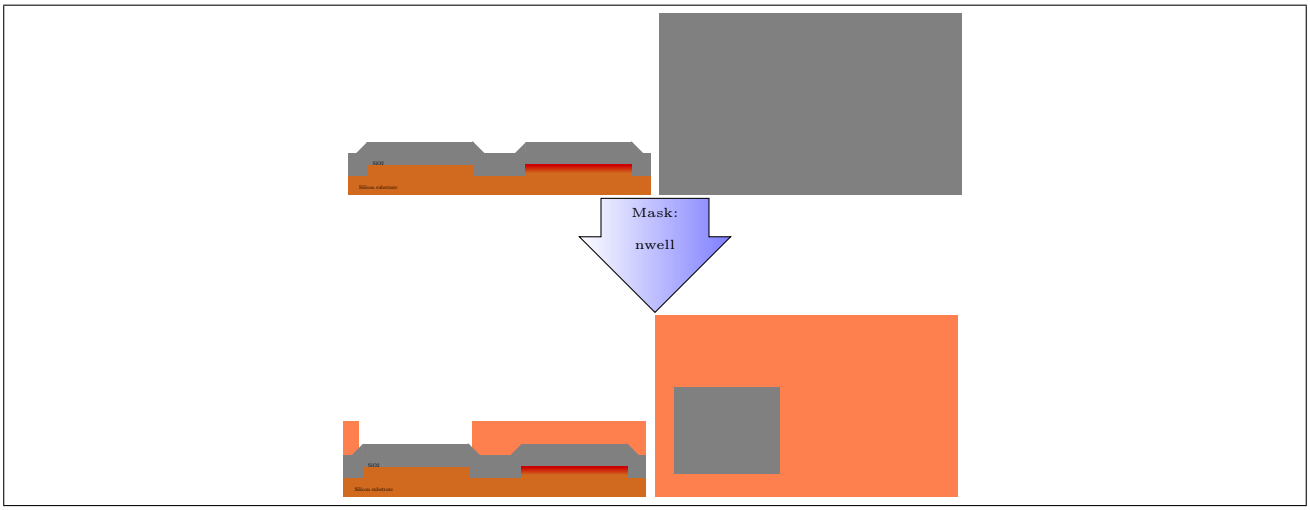

Figure 22: Cross/top view of n-well layout on resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

[8] http://cleanroom.byu.edu/rangestraggle
[9] http://cleanroom.byu.edu/OxideTimeCalc

3.3 Hard mask: Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

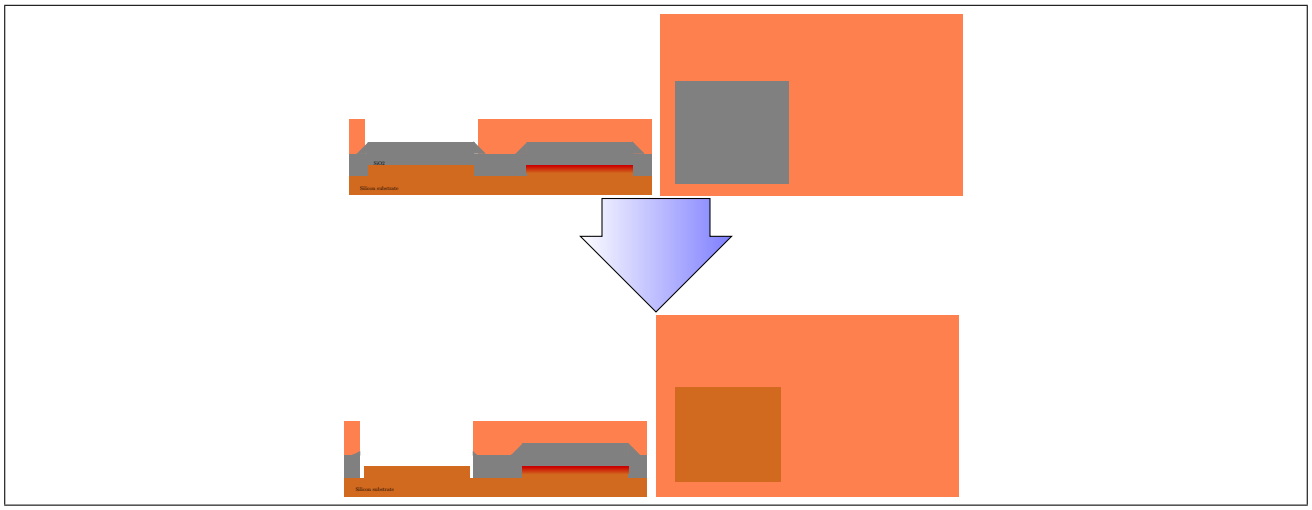

Figure 23: Cross/top view of n-well oxide window

Since the silicon dioxide layer is 300nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for a little bit over 3 minutes in order to get through the 300nm of oxide.
  Too long over 3 minutes might cause under-etch however!

3.4 Hard mask: Resist strip

In order to avoid contamination of the machines we need to make sure all the resist has been stripped off from the wafer.

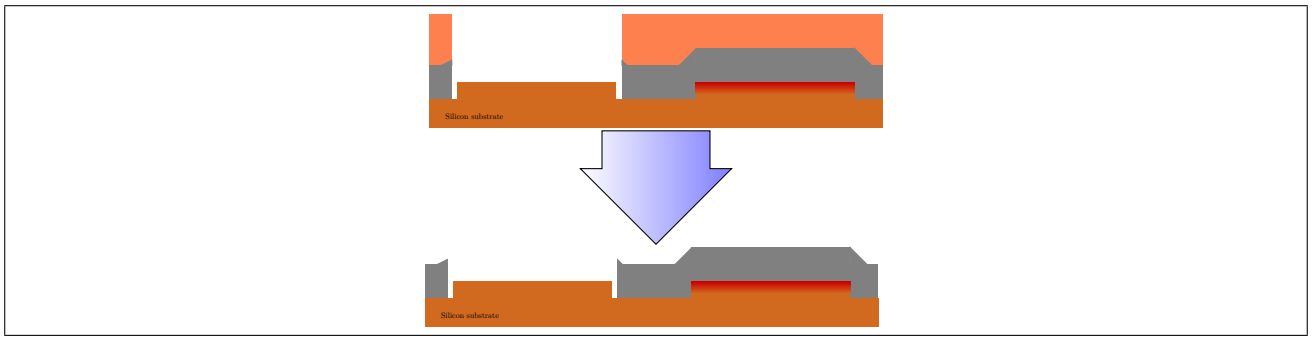

Figure 24: Resist removal

Please just use the solvent for the specific resist.

3.5 Implantation/Doping

We now need to inject the carriers into the upper level of the n-channel area so that we can later on drive them into the crystal during the drive-in step.

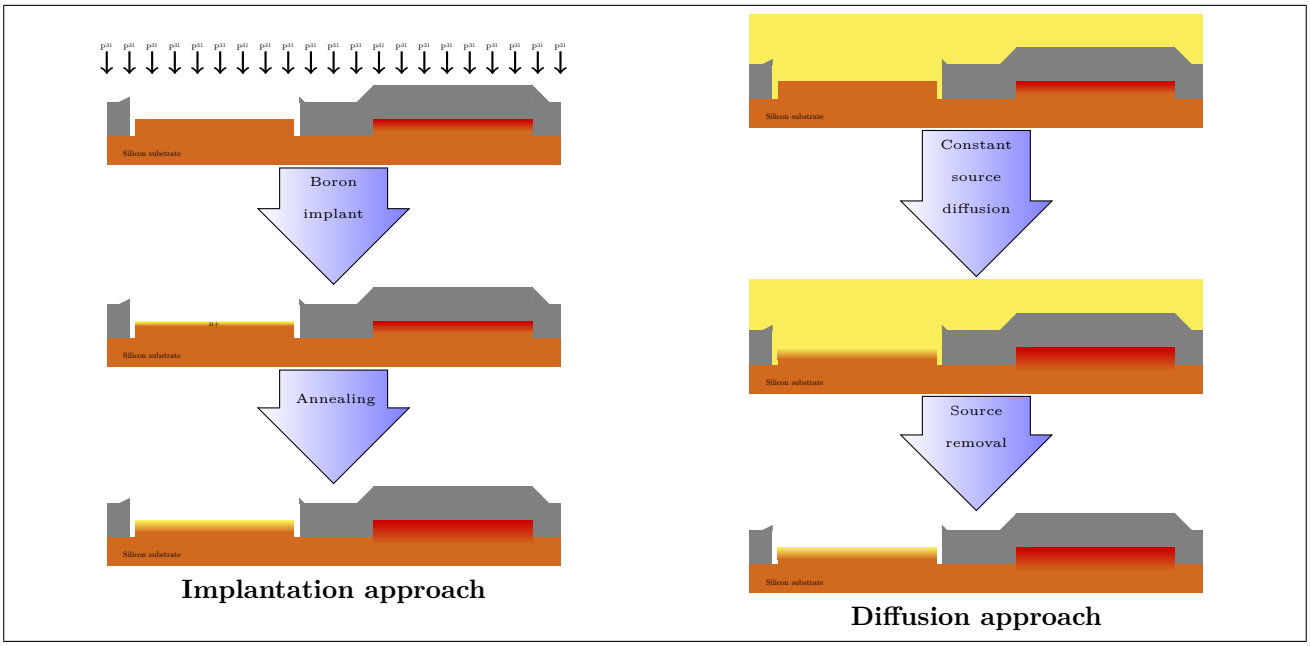

Figure 25: Doping process

Possible approaches:

- **"CF-3000 Implanter (IMP-3000)" from HKUST**
  At HKUST we have an implanter which gives us better control over the initial surface concentration. These steps are needed to arrive with the desired geometry:

  1. The N-well is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 100 keV.
  2. The N-well is annealed for 30 minutes at $1050°C$ in N_2 environment (DIF-A1)
     After that the P-well will be around $2\mu m$ deep and the N-Well around $1\mu m$ deep

- **Constant source diffusion**
  We can add a layer of Phosphorus solution and diffusing in order to have an initial concentration in order to reach the desired concentration later by main diffusion.

  1. A constant source is added (gas or liquid)
  2. The source dopant is driven in for 10 minutes at $1050°C$
  3. The dopant source is removed by stopping the gas flow or cleaning the surface

3.6 Hard mask: Oxide removal

Now we want to remove the silicon mask from the wafer and clean it for another clean oxide mask layer.

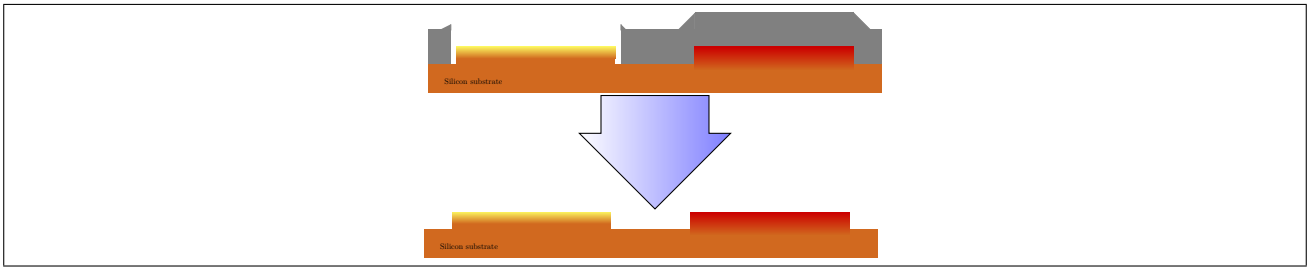

Figure 26: Oxide removal

We use buffered hydrofluoric acid (BOE (1:6)) at room temperature for 3 minutes in order to remove the 300nm of oxide layer.

4 Field oxide (+Drive-in)

The geometry of a substrate with the field oxide filling the shallow trenched from section 1 now needs to be made.

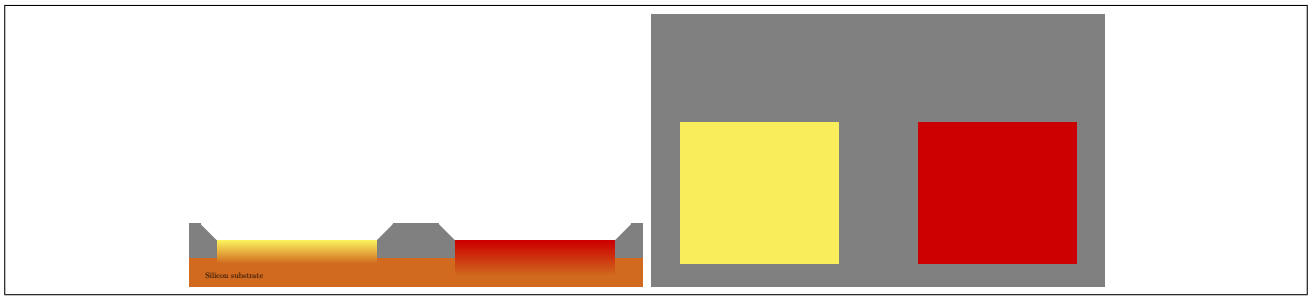

Figure 27: Shallow trench isolation target geometry

As can be seen in Figure 27, the STI trenches need to be filled with silicon oxide and windows need to be etched into them so that the gate can be constructed later on. The windows are needed so that the poly silicon is far enough away from the non-active areas so that the threshold voltage of the parasitic FETs is so high that they will never switch. Only within the active areas we want to allow the poly layer to touch down closer to the silicon.
During the oxidation the dopants will be further driven in which will lead to the final formation of the N-well with an approximate depth of $4\mu m$ and the P-well with an approximate depth of $5\mu m$.

4.1 Oxide growth/Drive-in

Now we need to fill the trenches with silicon dioxide which will provide a spacer between the non active area and the polysilicon gate layer. within the non-active areas.

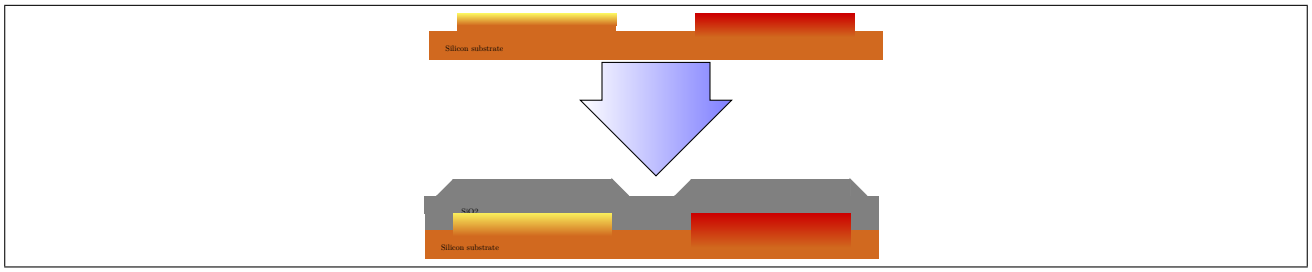

Figure 28: Hard mask growth

We grow a roughly $1.23\mu m$ thick layer of silicon dioxide by putting the wafer into the furnace at $1050°C$ for 4 hours and 30 minutes in a wet environment.
During the oxidation the dopants will be further driven in which will lead to the final formation of the N-well with an approximate depth of $4\mu m$ and the P-well with an approximate depth of $5\mu m$.

4.2 Patterning

We reuse the mask from section 1, because it's exactly the same layout, only inverted. The requirement is a **negative** tone resist.

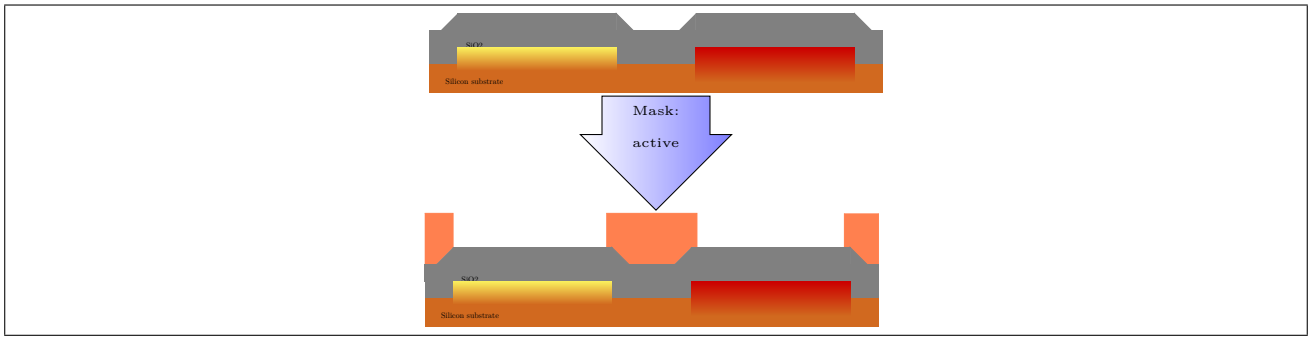

Figure 29: Patterning with positive resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

4.3 Etching

We open the access to the silicon inside of the active areas in order to touch down with the polysilicon further on.

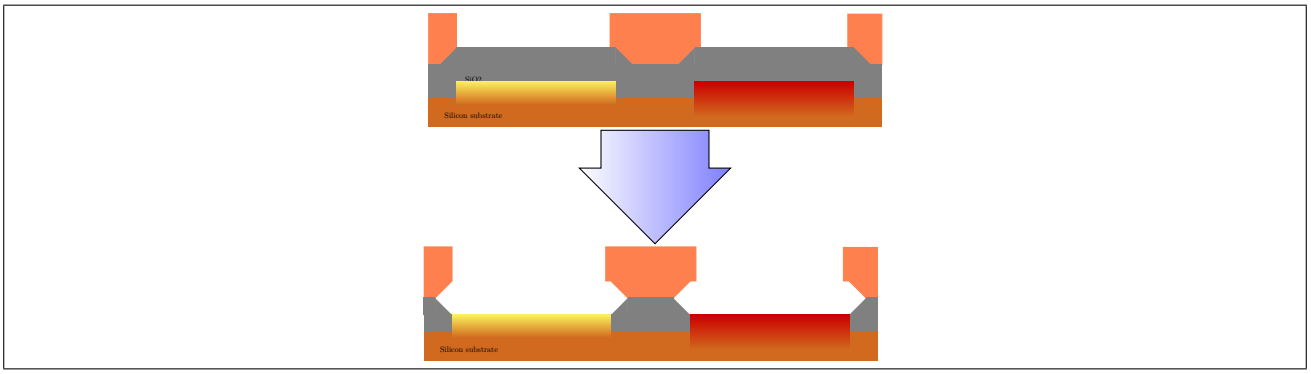

Figure 30: Nitride mask etching

There are dry etching and wet etching methods available for etching the thick field oxide. The downside of wet etching is that it also etches horizontally, however the chemical BHF is readily available and allows for easy implementation of the process.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for a little bit over 3 minutes in order to get through the 300nm of oxide.
  Too long over 3 minutes might cause under-etch however!

4.4 Resist strip

Now we need to remove the contaminants for further processing.

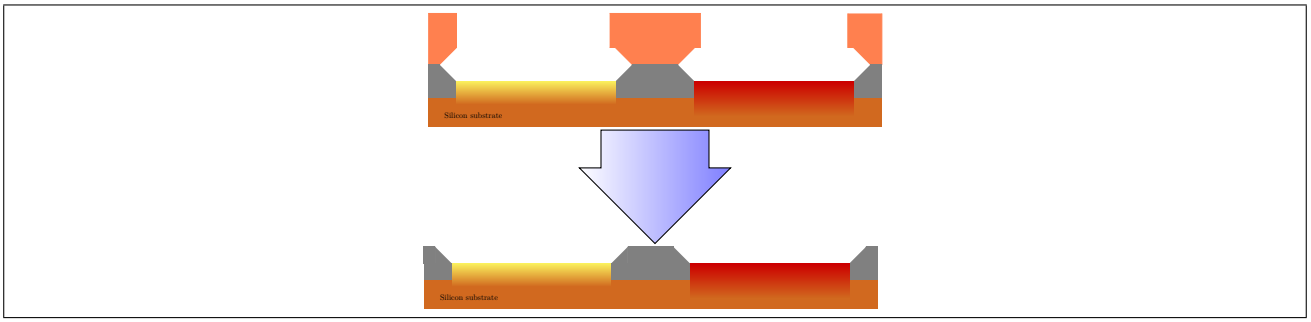

Figure 31: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

5 Gate

Now we have to build the initial gate structure which contains of the 40nm thick dielectric (in our case just silicon dioxide) and the polysilicon electrode.

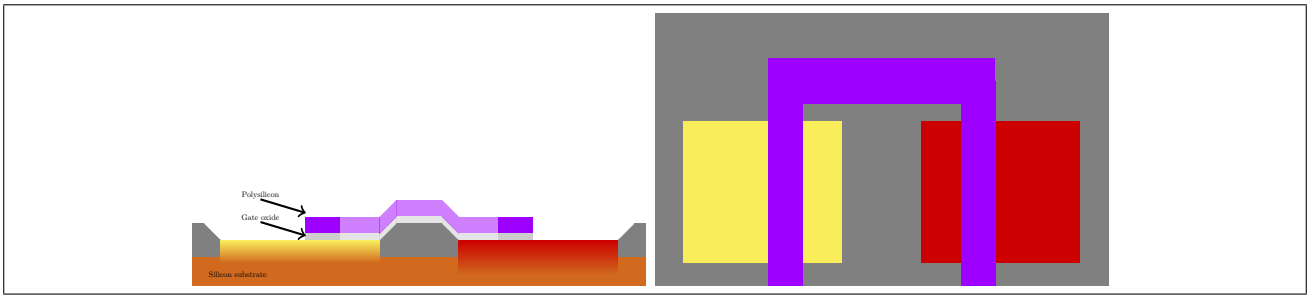

Figure 32: Poly silicon gate contacts with gate oxide

The line spacing of the polysilicon electrode shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.

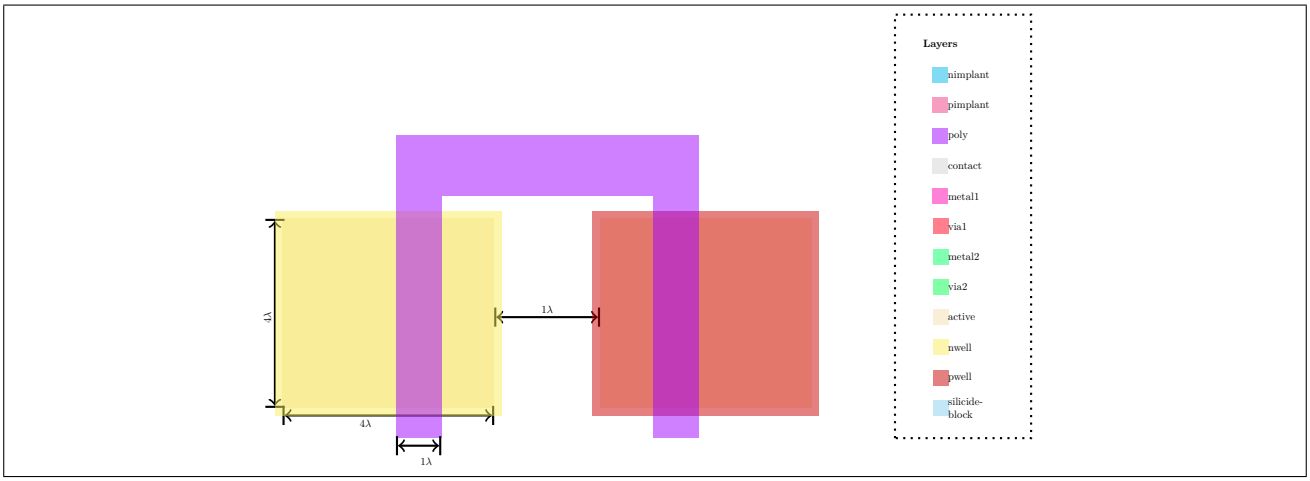

Figure 33: Gate layout

In Figure 33 we can see the layout honoring the $0.5\mu m$ spacing design rule for the gate structure shape and poly-layer interconnect between NMOS and PMOS.

5.1 Gate oxide deposition

Now we have to deposit the dielectric isolator between the gate electrode and the channel. As designed in the process design document, the layer will be 40nm thick.

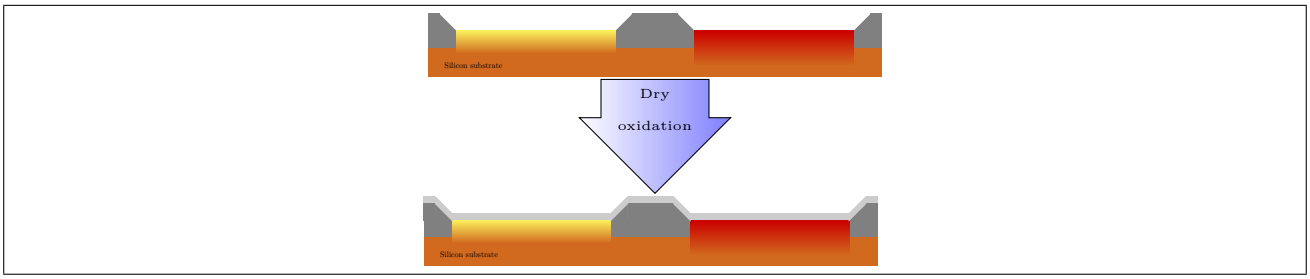

Figure 34: Thin oxide

The thickness of this layer decides over many critical key properties of the transistor, hence there should be little to no variation in the thickness of the gate oxide layer. For that reason we put the wafer into the diffusion furnace and perform dry oxidation at $1050°C$ for 33 minutes and 14 seconds.[10]

5.2 Polysilicon deposition

Now we need to add the polysilicon layer for forming the gate structure after etching.

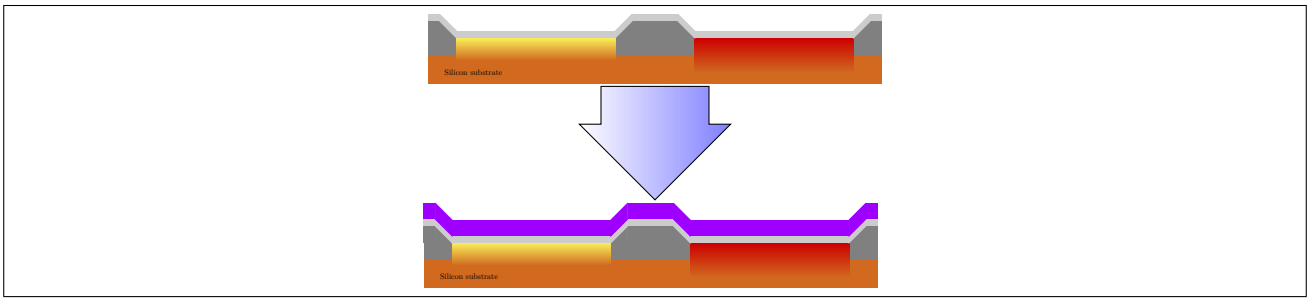

Figure 35: Polysilicon

We use the LPCVD machine and deposit a layer of around 600nm polysilicon[11].
We set the temperatue to $650°C$, the gas will be Silane (SiH_4 ($Si + 2H_2$)), the pressure will be set to 300 mTorr with a flow of 90sccm.
This will give us a growth rate of roughly 23.5 nm per minute, so for 600nm we let it grow half an hour.

[10] `http://cleanroom.byu.edu/OxideTimeCalc`
[11] `https://people.rit.edu/lffeee/LPCVD_Recipes.pdf`

5.3 Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”poly” layer within the GDS2 file onto a **bright field** mask. The requirement is a **positive** tone resist.

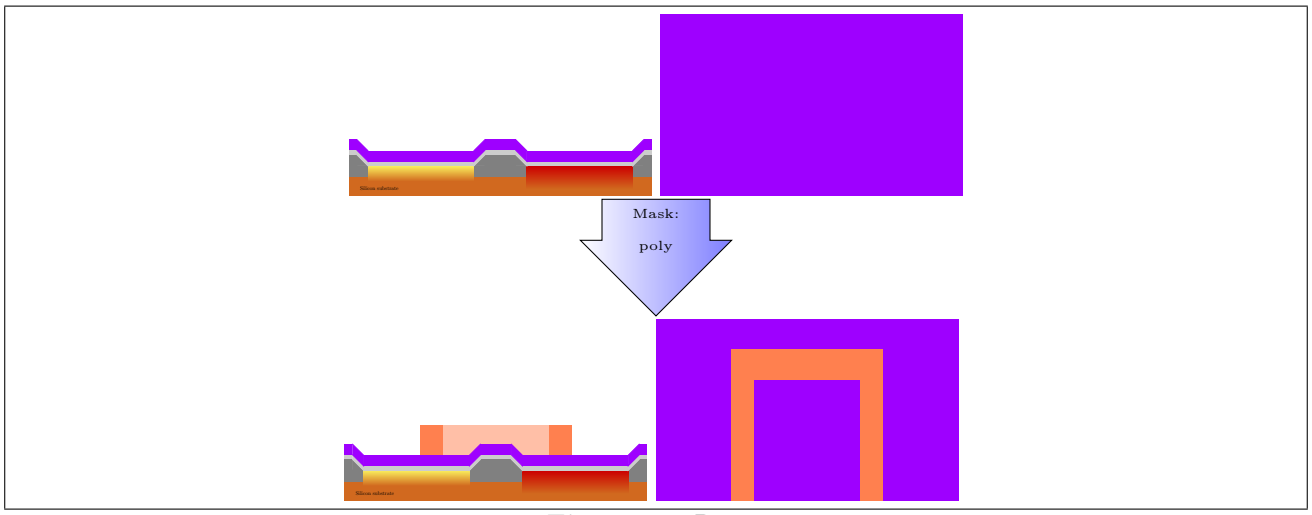

Figure 36: Resist

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn’t be forgotten!

5.4 Etching

Now we've got to etch the gate structures.

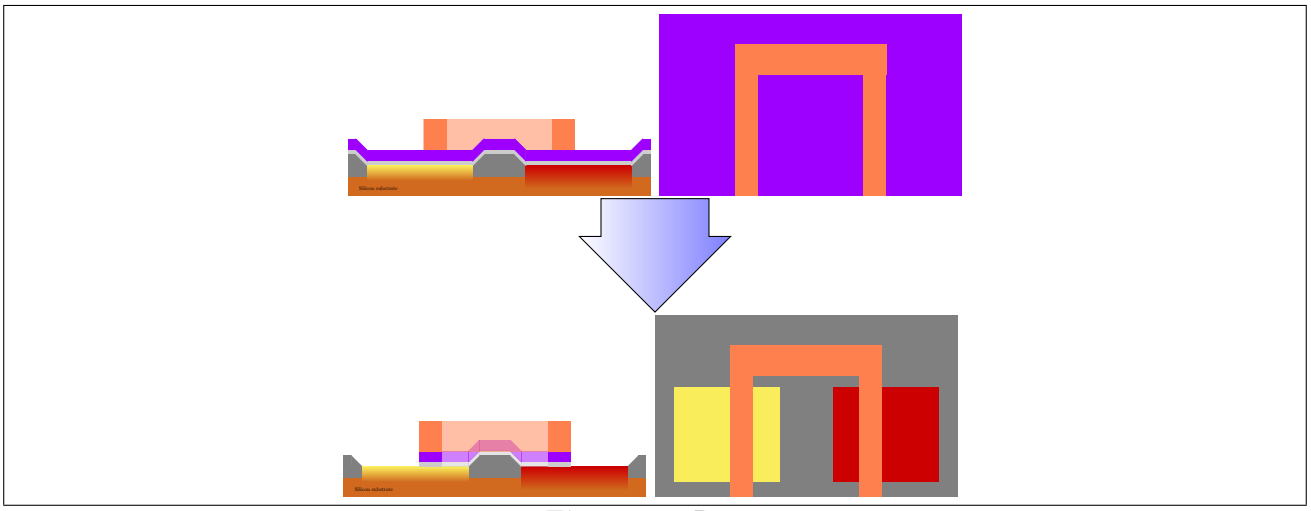

Figure 37: Resist

For now we only have the plasma etcher variant being verified because chemically etching polysilicon isn't allowed at the HKUST labs for contamination control reasons. In case you can verify this in your lab with a chemical etching method, please update this chapter and make a pull request!

Possible approaches:

- **"Poly Etcher (DRY-Poly)" from HKUST**
  An anisotropic plasma etcher, in order to etch the polysilicon and gate oxide layer. In subsection 5.2 we've grown 600nm of polysilicon which takes 200 seconds (= 3 minutes 20 seconds) (at 180nm/min) to etch. The selectivity to oxide is 13:1 which leads to an oxide etching speed of around 14nm/min, in subsection 5.1 we've grown a 40nm thick oxide layer which leads to the oxide adding another 2 minutes 51 seconds to the etching time. All together, we will have to etch for around **6 minutes and 10 seconds**.
- **Chemical method**
  Please add a verified method here!

5.5 Resist removal

Now we need to remove the contaminants for further processing.

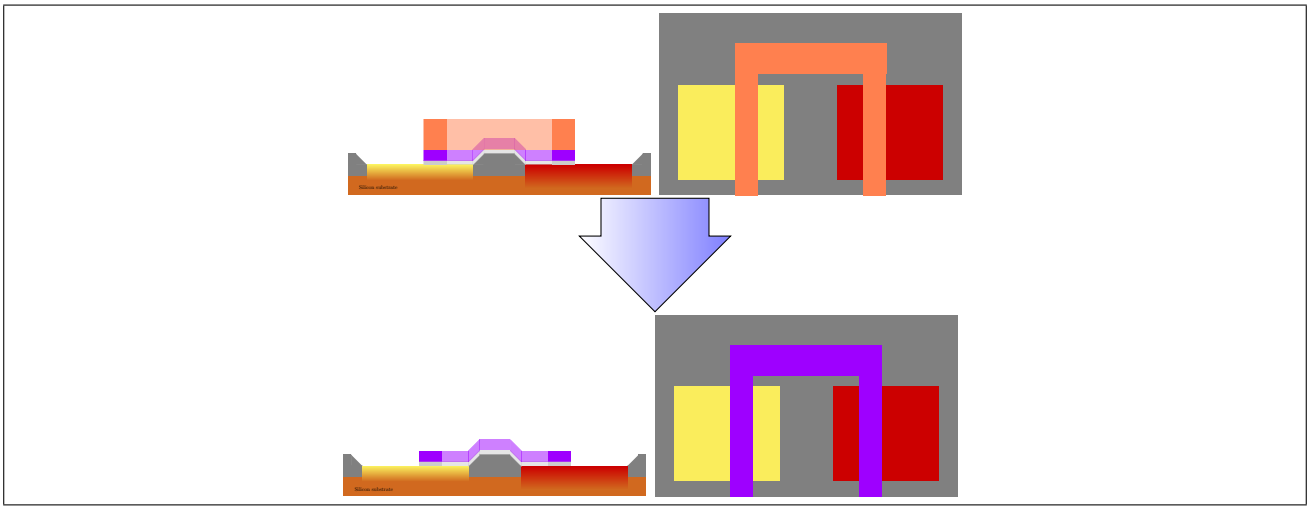

Figure 38: Resist

We strip the resist, rinse and perform sulfuric cleaning.

6 n+ Implant

For the bulk of the PMOS transistors and for the source and drain of the NMOS transistors highly doped n+ areas are required. In this step we're going to build these.

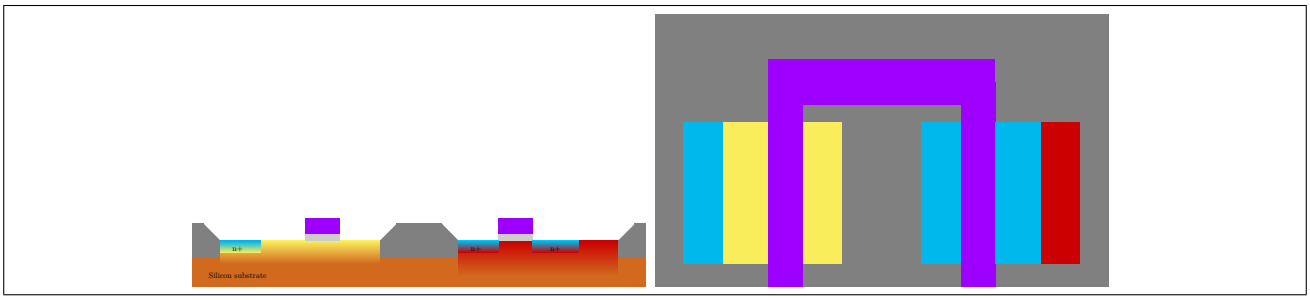

Figure 39: N+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.

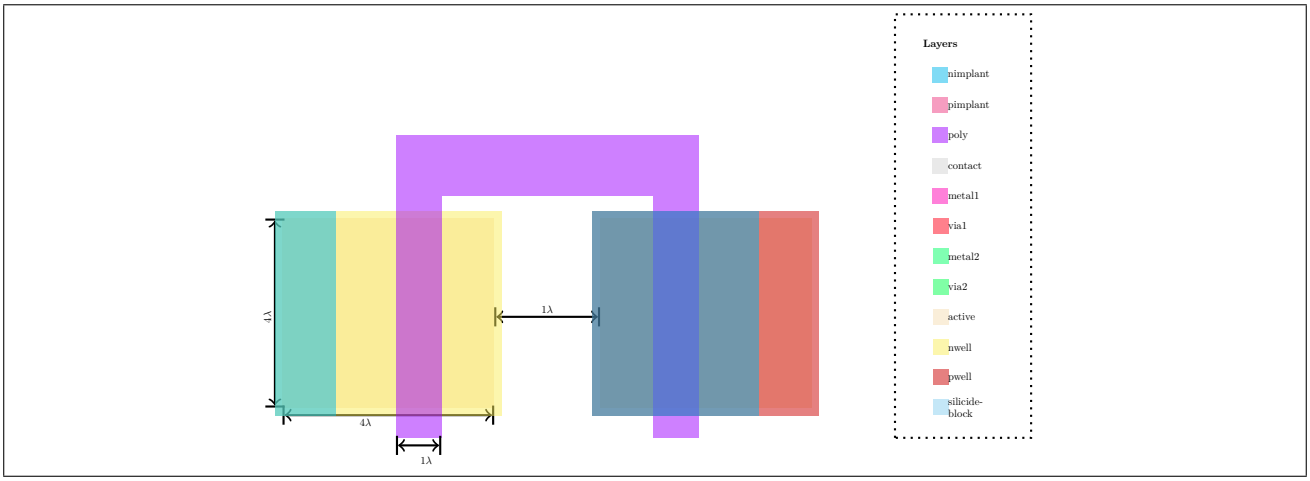

Figure 40: N+ layout

An example layout of p-implants can be seen in Figure 40, the mask is being extracted from the layer "n_plus_select".
Also important to notice is that this example layout is just for demonstration purposes only, please have a look at the standard cell documentation for the actual layouts.

6.1 Hard mask: Dioxide growth

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

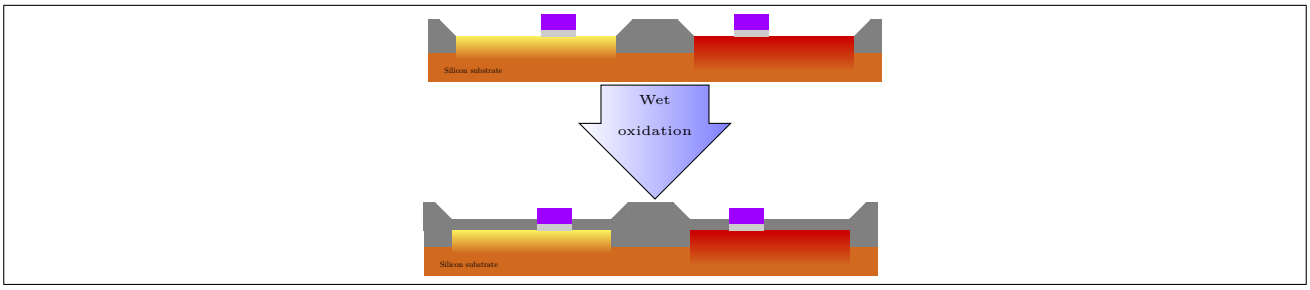

Figure 41: Oxide layer

With an energy of 35keV for the implantation performed in subsection 6.5, the projected range of the dopants within the oxide will be 34nm (47nm tops) [12]. This means being on the safe side and having 100nm as the thickness is a good approach. In order to grow the 100nm thick oxide layer, the wafer is being oxidized for around 5 minutes 30 seconds at 1050°C using wet oxidation which results in a dioxide layer of around 100nm in thickness[13].

6.2 Hard mask: Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "n_plus_select" layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

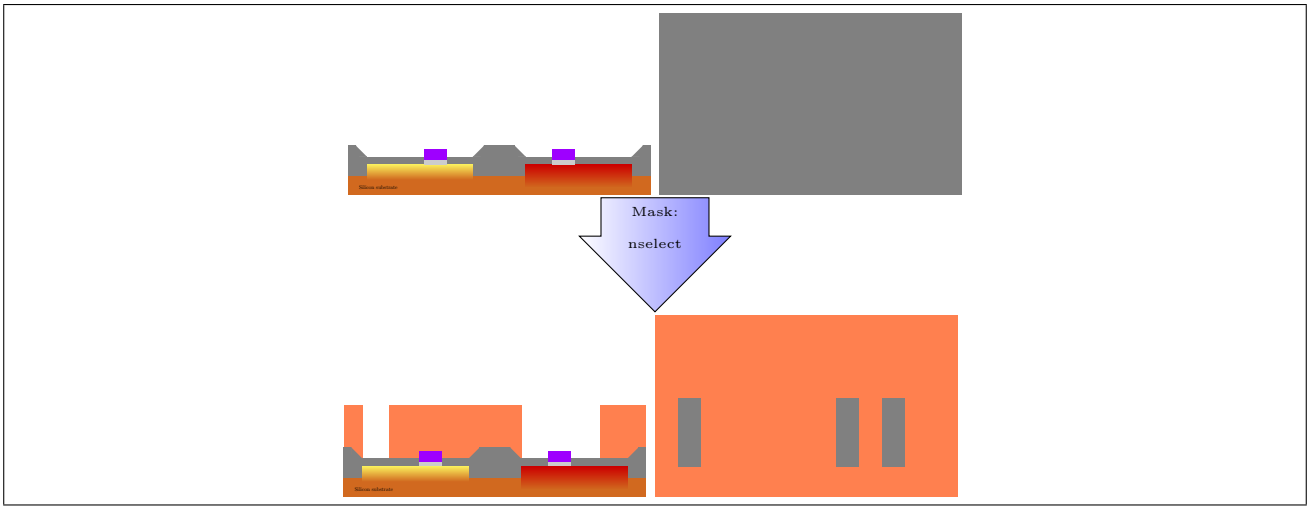

Figure 42: N+ region resist mask

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

[12] http://cleanroom.byu.edu/rangestraggle
[13] http://cleanroom.byu.edu/OxideTimeCalc

6.3 Hard mask: Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

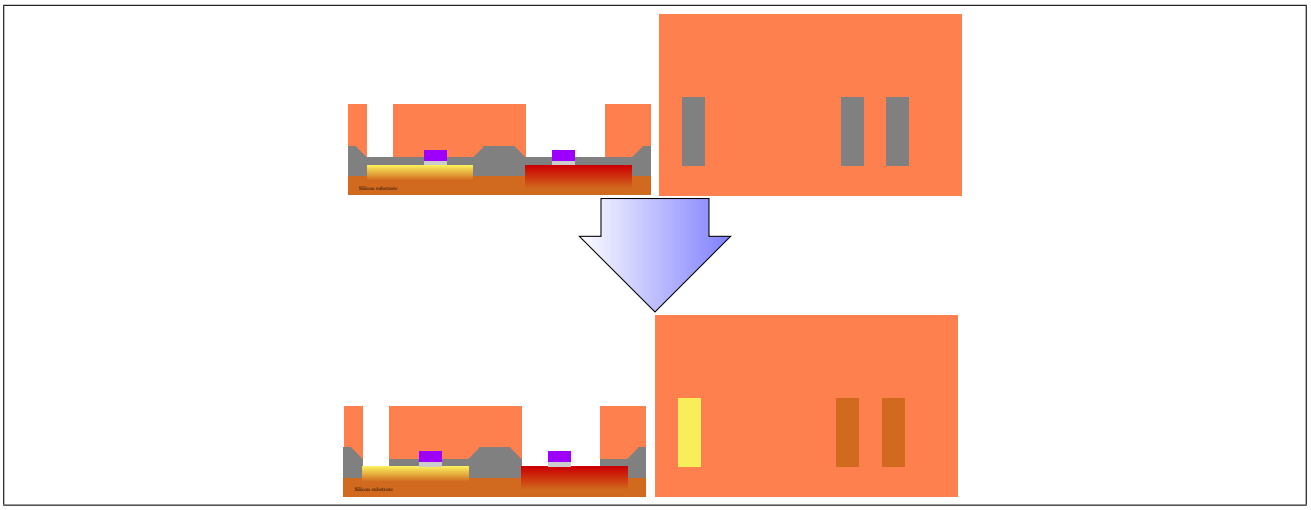

Figure 43: N+ region opened

Since the silicon dioxide layer is 100nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for one minute in order to get through the 100nm of oxide.
  (Too long over 1 minutes might cause under-etch!)

6.4 Hard mask: Resist strip

Now we need to remove the contaminants for further processing.

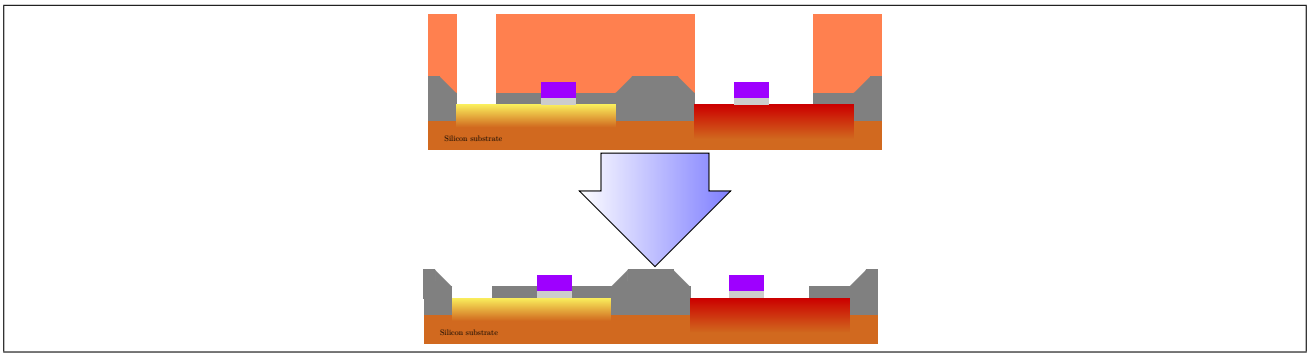

Figure 44: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

6.5 Implantation/Doping

We now need to bring in the carriers in order to build the n-junctions.

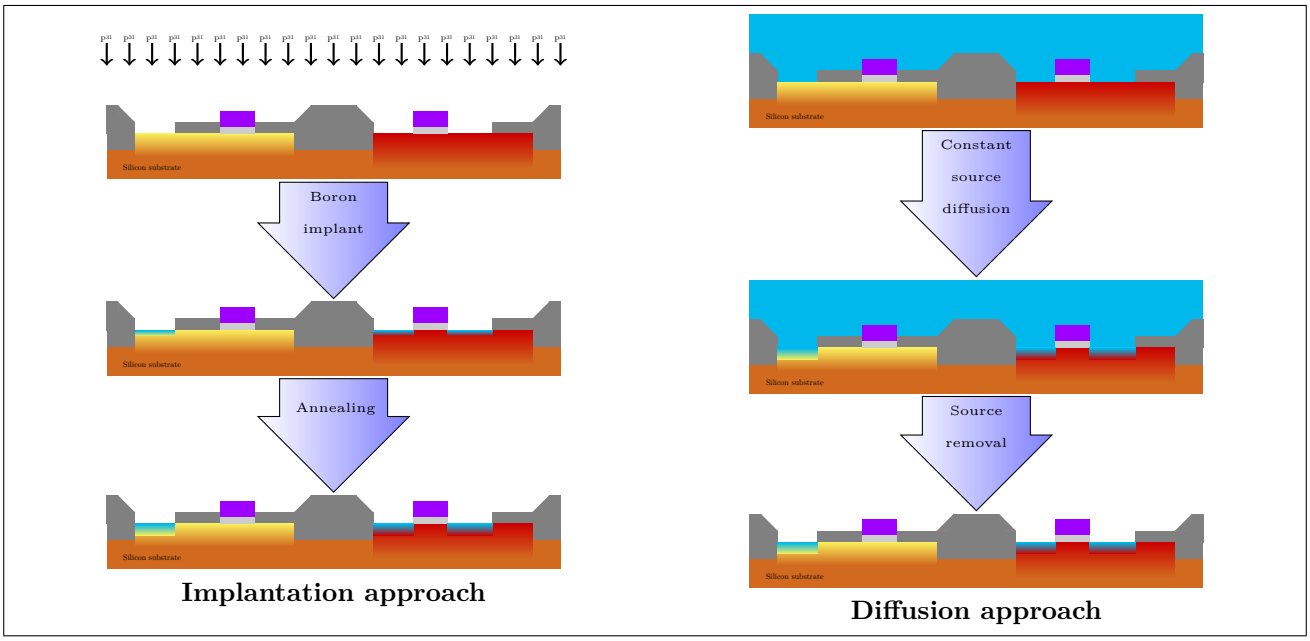

Figure 45: N+ doping process

Possible approaches:

- **"CF-3000 Implanter (IMP-3000)" from HKUST**
  At HKUST we have an implanter which gives us better control over the initial surface concentration. These steps are needed to arrive with the desired geometry:
  1. The nselect is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 35 keV (43nm±18nm deep)
  2. The nselect is annealed for 10 minutes at $1050°C$ in N_2 environment (DIF-A1)
- **Constant source diffusion**
  We can add a layer of Phosphorus solution and diffusing in order to have an initial concentration in order to reach the desired concentration later by main diffusion.
  1. A constant source is added (gas or liquid)
  2. The source dopant is driven in for 5 minutes at $1050°C$
  3. The dopant source is removed by stopping the gas flow or cleaning the surface

6.6 Hard mask: Removal

Now we want to remove the silicon mask from the wafer and clean it for another clean oxide mask layer.

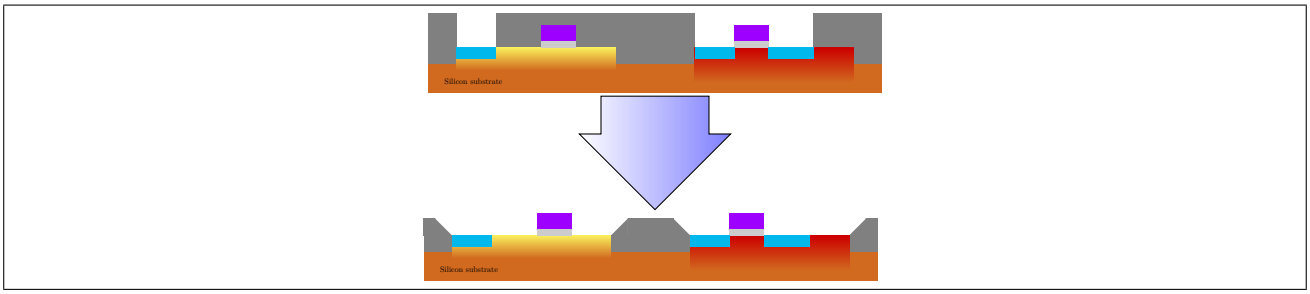

Figure 46: Oxide removal

We use buffered hydrofluoric acid (BOE (1:6)) at room temperature for 1 minute in order to remove the 100nm of oxide layer.

7 p+ Implant

For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required. In this step we're going to build these.

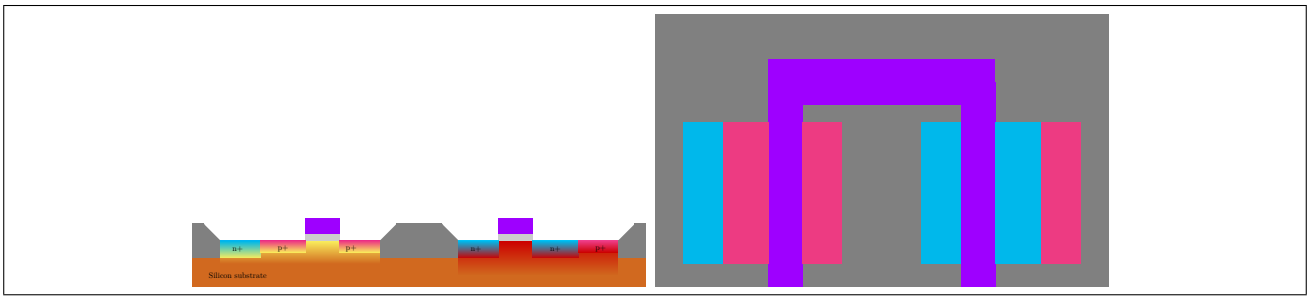

Figure 47: P+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.

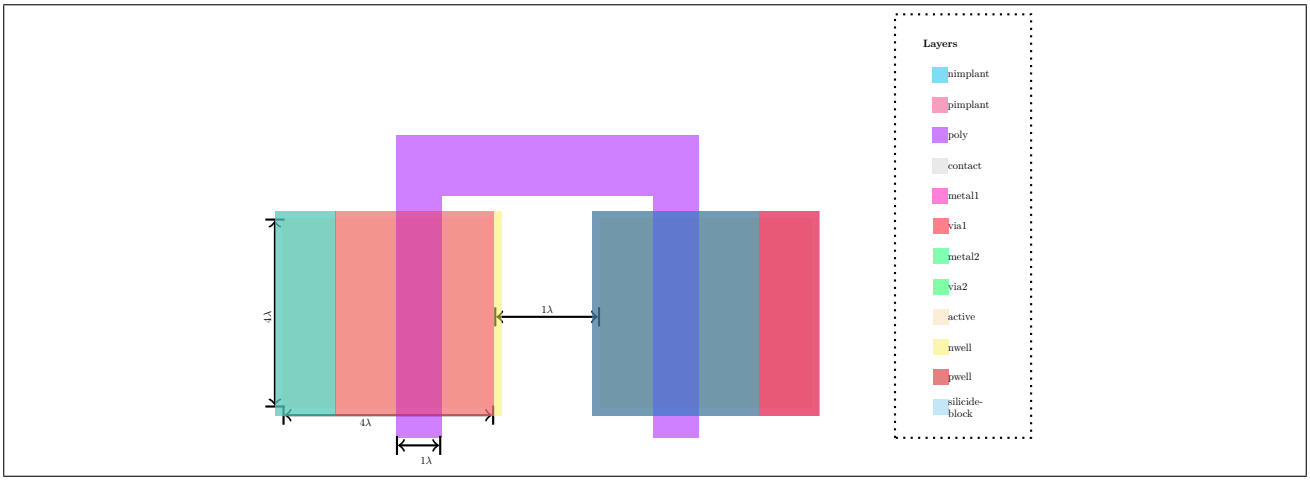

Figure 48: P+ layout

An example layout of p-implants can be seen in Figure 48, the mask is being extracted from the layer "p_plus_select"
Also important to notice is that this example layout is just for demonstration purposes only, please have a look at the standard cell documentation for the actual layouts.

7.1 Hard mask: Dioxide growth

In order to selectively inject charge carrying atoms into the crystalline structure a protective dioxide (SiO_2) layer needs to be grown on top of a p-type substrate.

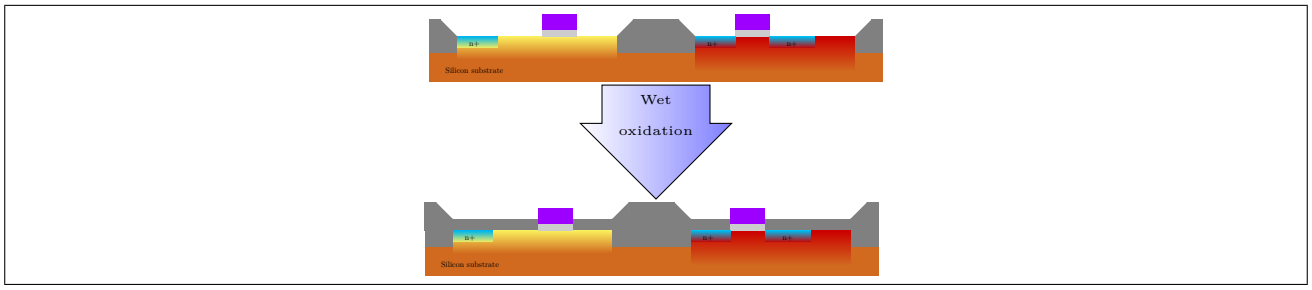

Figure 49: Oxide layer

With an energy of 13keV for the implantation performed in subsection 6.5, the projected range of the dopants within the oxide will be 40nm (58nm tops) [14]. This means being on the safe side and having 100nm as the thickness is a good approach. In order to grow the 100nm thick oxide layer, the wafer is being oxidized for around 5 minutes 30 seconds at 1050°C using wet oxidation which results in a dioxide layer of around 100nm in thickness[15].

7.2 Hard mask: Patterning

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "p_plus_select" layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

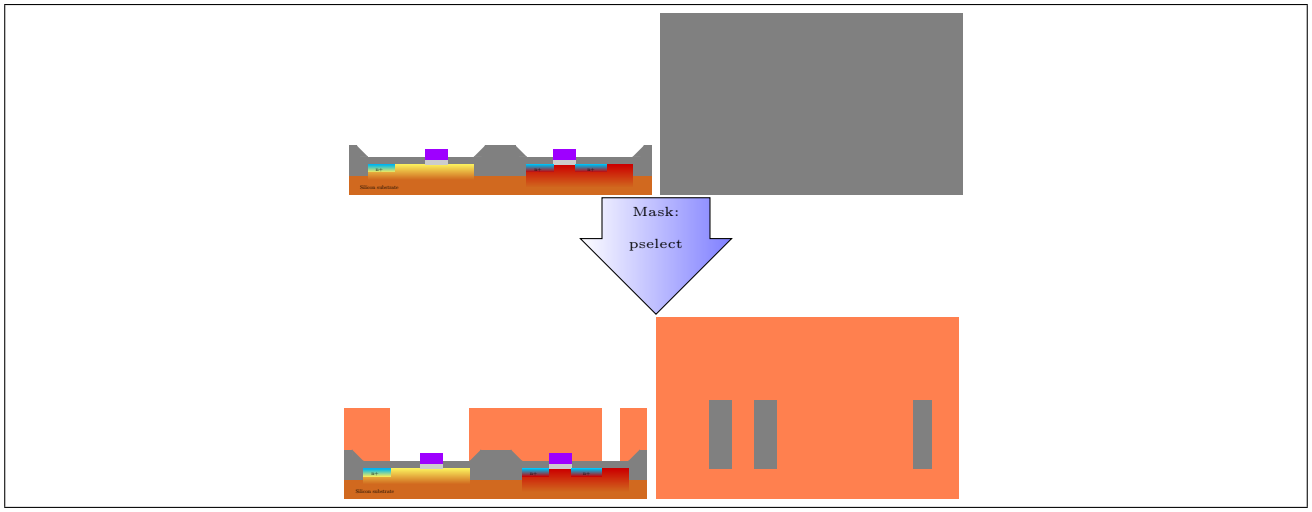

Figure 50: P+ region resist mask

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

[14] http://cleanroom.byu.edu/rangestraggle
[15] http://cleanroom.byu.edu/OxideTimeCalc

7.3 Hard mask: Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

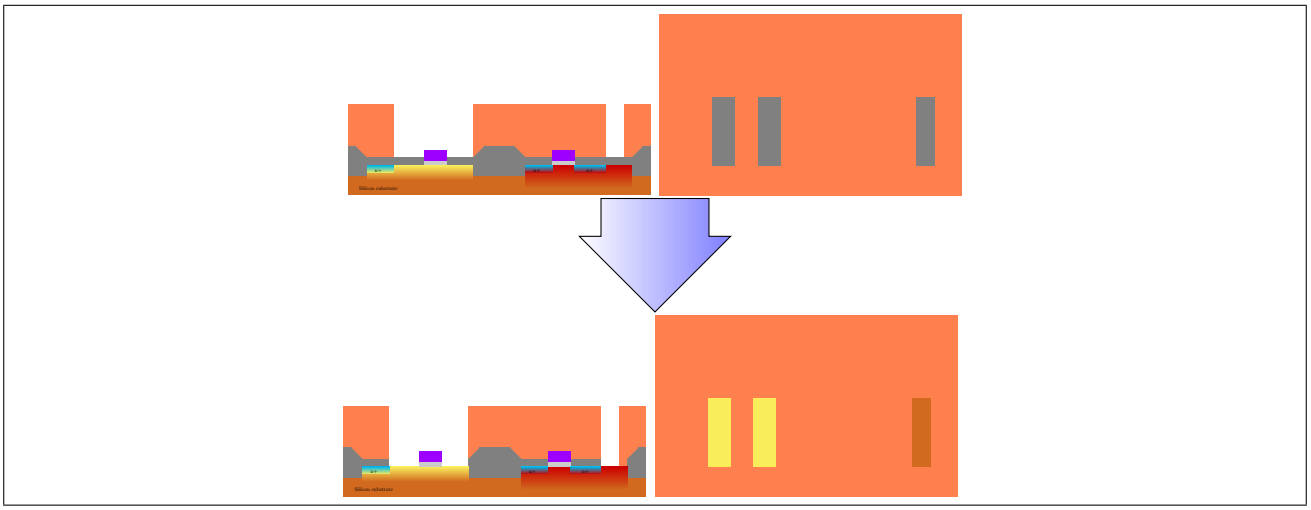

Figure 51: P+ region opened

Since the silicon dioxide layer is 100nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for one minutes in order to get through the 100nm of oxide.
  (Too long over 1 minutes might cause under-etch however!)

7.4 Hard mask: Resist strip

Now we need to remove the contaminants for further processing.

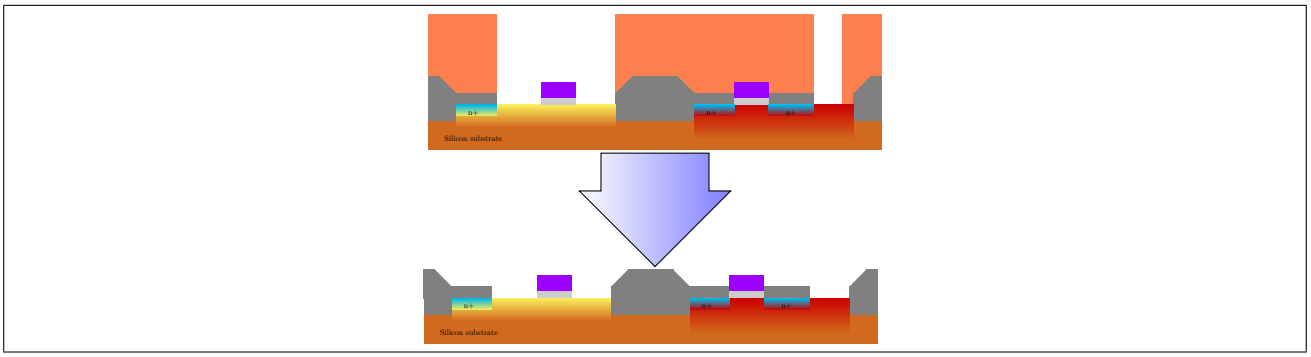

Figure 52: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

7.5 Implantation/Doping

We now need to bring in the carriers in order to build the p-junctions.

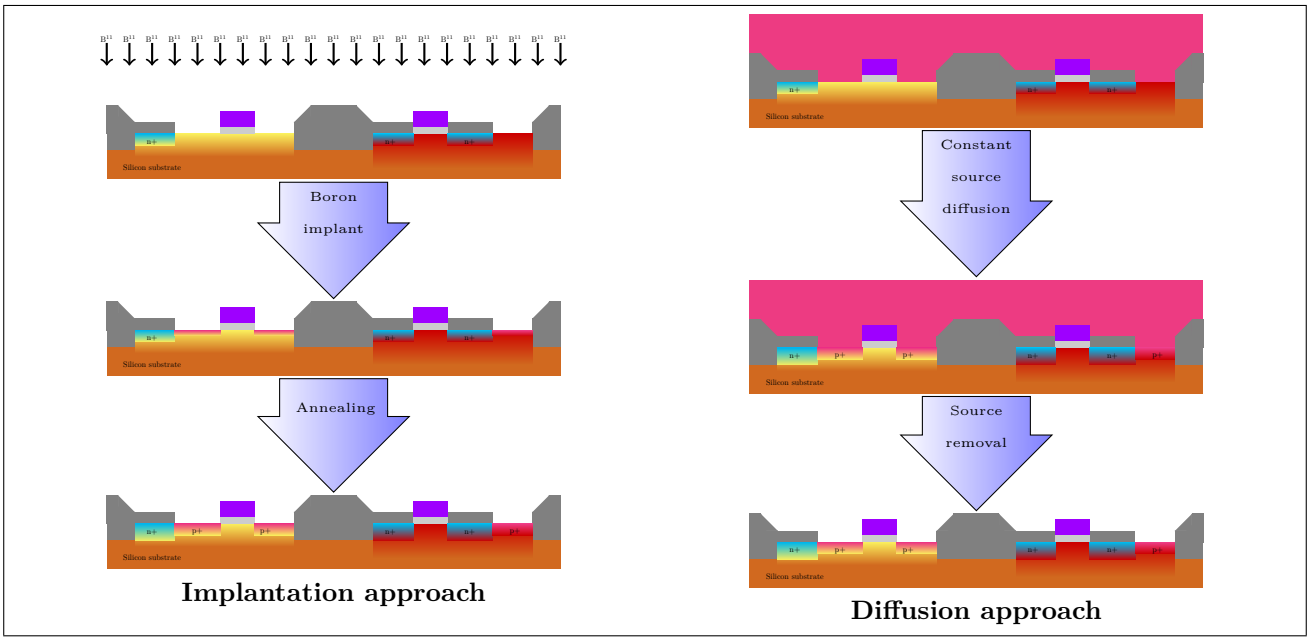

Figure 53: P+ doping process

Possible approaches:

- **"CF-3000 Implanter (IMP-3000)" from HKUST**
  At HKUST we have an implanter which gives us better control over the initial surface concentration. These steps are needed to arrive with the desired geometry:

  1. The pselect is implanted with a Boron (B^{11}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 13 keV (43nm±18nm deep)
  2. The pselect is annealed for 10 minutes at $1050°C$ in N_2 environment (DIF-A1)

- **Constant source diffusion**
  We can add a layer of Phosphorus solution and diffusing in order to have an initial concentration in order to reach the desired concentration later by main diffusion.

  1. A constant source is added (gas or liquid)
  2. The source dopant is driven in for 5 minutes at $1050°C$
  3. The dopant source is removed by stopping the gas flow or cleaning the surface

7.6 Hard mask: Removal

Now we want to remove the silicon mask from the wafer and clean it for another clean oxide mask layer.

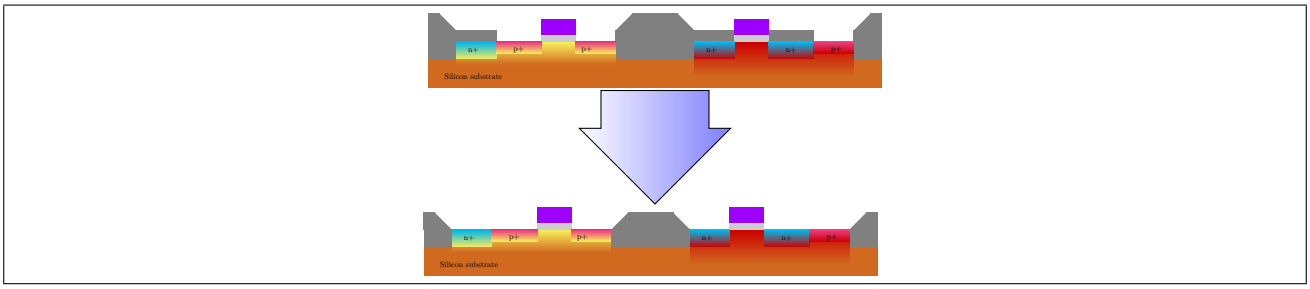

Figure 54: Oxide removal

We use buffered hydrofluoric acid (BOE (1:6)) at room temperature for 1 minute in order to remove the 100nm of oxide layer.

8 Silicification

Titanium silicide is one of the first SALICIDE material introduced in ULSI devices owing to its low resistivity, high thermal stability, ease in deposition and compatibility with silicon processes. Titanium has been one of the familiar materials in ULSI productions, which is also an important advantage in practical use of titanium SALICIDE.[16]

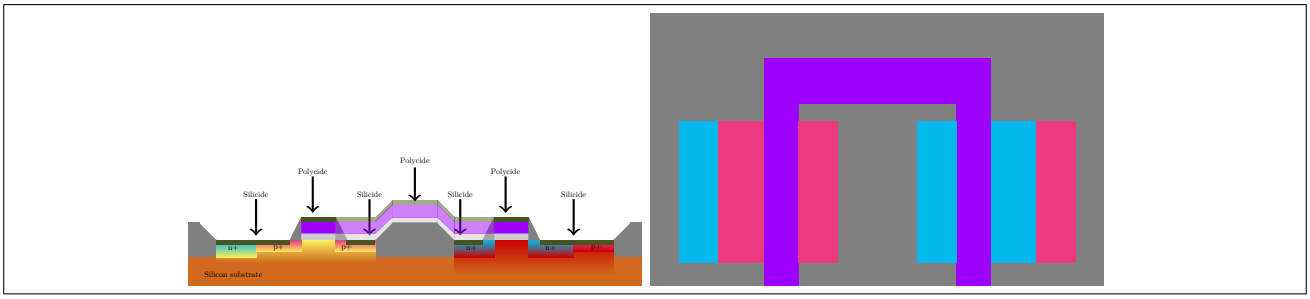

Figure 55: Silicide geometry target

In order to reduce the gate contact resistance as well as the source and drain resistance and in order to provide a more effective etch stop when plasma etching the contact windows to drain, source and gate, silicide/polycide is being added to the wafer as shown in Figure 55.

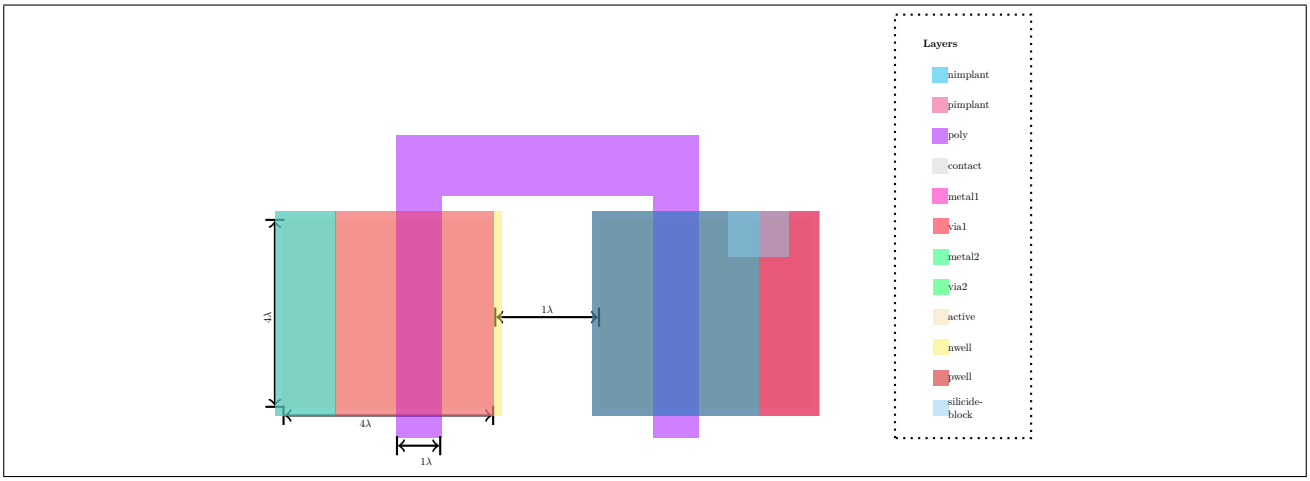

Figure 56: Silification layout

When titanium and silicon are brought into contact and heated at temperatures above 500 °C (in the presence of excess silicon) the higher-resistivity C49-$TiSi_2$ phase forms before the low-resistivity phase.
The C49-$TiSi_2$ phase has an orthorhombic base-centered structure with 12 atoms per unit cell and a resistivity of $60 - 90\mu\Omega - cm$.
The C54-$TiSi_2$ phase has an orthorhombic face-centered structure having 24 atoms per unit cell and a significantly lower resistivity ($12 - 20\mu\Omega - cm$) than the C49-$TiSi_2$.
The basic formation process of titanium SALICIDE is as follows:
A thin titanium film with 20-60 nm thickness is deposited on an entire wafer with MOSFETs structure. The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes by the first anneal at 600-700°C in N_2 ambient. In first anneal, C49-$TiSi_2$ phase is formed. Then, the unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution. The final step is second anneal at 800°C or above to transform high-resistivity C49-$TiSi_2$ phase to low-resistivity C54-$TiSi_2$ phase at the gate electrodes and source/drain areas.

[16] A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices, 07D53437, Ryuji Tomita

8.1 Oxide deposition

The thickness of this CVD deposited oxide layer will be the width of the spacer after having used highly anisotropic etching in the next few steps, for this reason the thickness of the oxide decides over the distance between the silicide and the gate oxide.
We make the oxide layer 50nm thick.

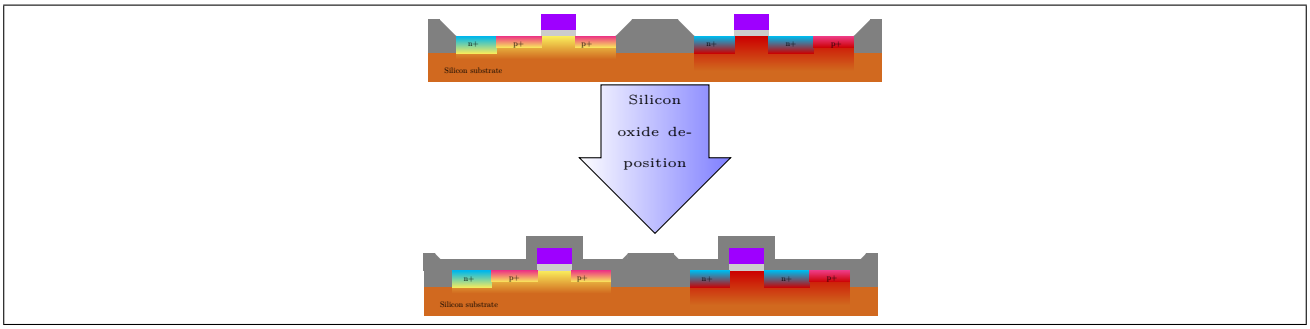

Figure 57: Oxide layer

We use the machine LPCVD machine from HKUST and deposit around 50nm of silicon dioxide with the following recipe[17]:

- Temperature: 400 $°C$ ($SiH_4 + O_2 = SiO_2 + 2H_2$)
- Pressure = 250 mTorr
- Silane (SiH_4) flow = 40sccm
- Oxygen (O_2) flow = 48sccm

This will give a rate of 7nm ($\pm 1nm$) per minute, so we deposit for roughly seven minutes (7 min).

8.2 Silicide block patterning (optional)

We now have to pattern the mask for the silicide block layer which will produce oxide wherever no silicide is not desired within active areas.

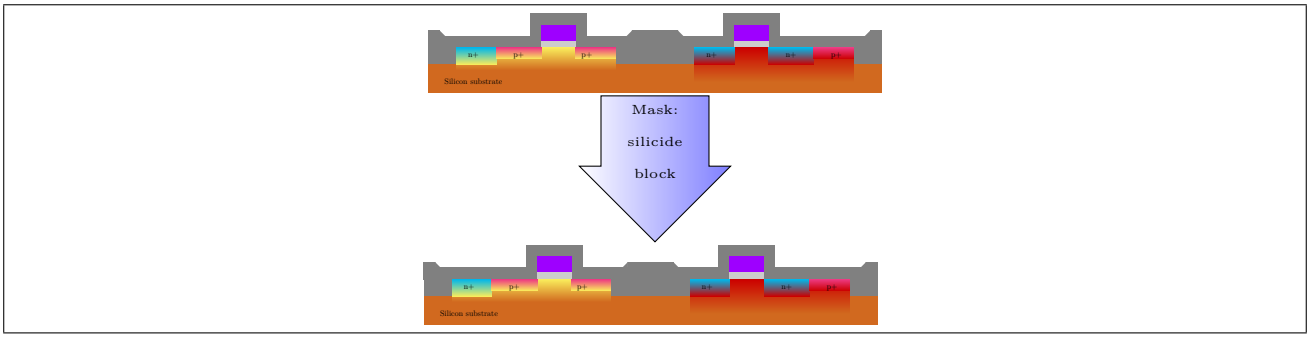

Figure 58: Patterning (silicide block)

It is not yet clear whether we will be needing this feature in the future, which means we have not yet finally decided whether wanna keep this step and layer within our process and technology.

[17] https://people.rit.edu/lffeee/LPCVD_Recipes.pdf

8.3 Sputter etching(Spacers)

Now we have to etch our oxide as anisotropic as possible. This means that the etching mostly only comes "from above" with a few to nearly none horizontal etching. Thit means the etching process only "sees" the sidewall as a "thicker layer" and starts etching downward.

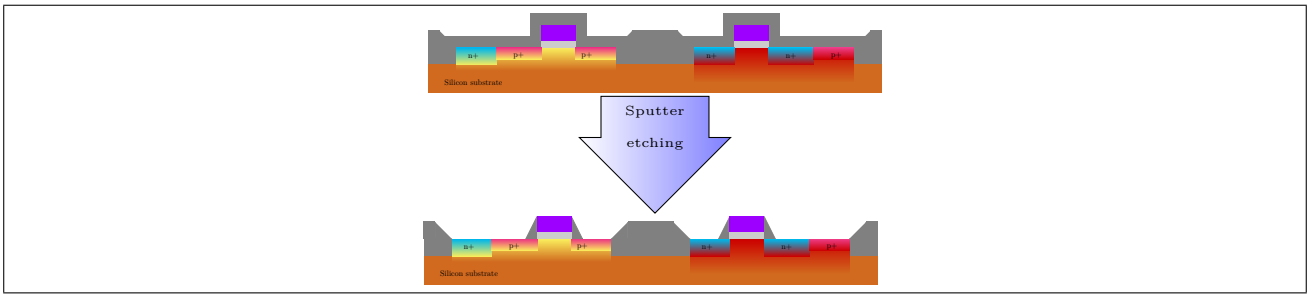

Figure 59: Anisotropic etching

Possible approaches:

- **"AOE Etcher" at the NFF HKUST lab**
  With an etching speed of 250 nm/min for thermal oxide and an oxide thickness of around 50nm etching will take around 12 seconds.

After that we will have our desired spacer geometry forming as well as any potentially resist covered area (if silicide block is being used) with sharp etches.

8.4 Titanium deposition

We deposit a layer of titanium with a thickness of around 20-60nm which will then be reacted into titanium-silicide and titanium-polycide respectively in the further steps.

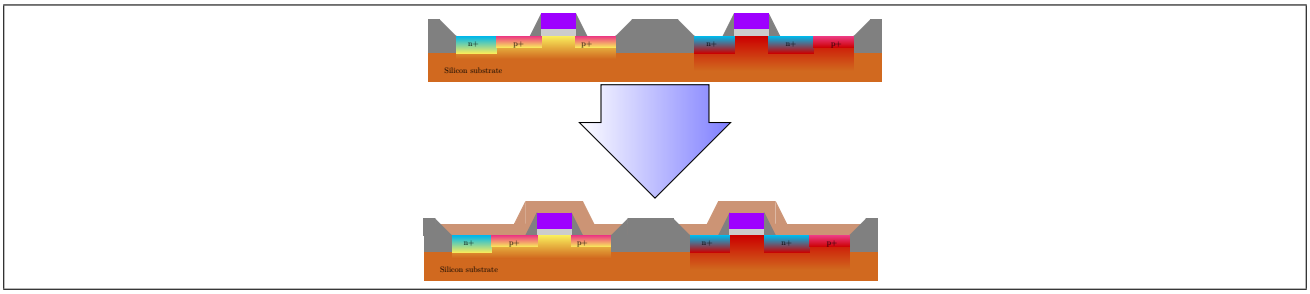

Figure 60: Titanium deposition

Possible approaches:

- **"Varian 3180 Sputter (SPT-3180)" at HKUST NFF lab**:
  Has has a sputter rate of around 4 nm/s for titanium.
  This means we run the deposition process for around 15 seconds.

8.5 First reaction step

The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes by the first anneal at 600-700°C in N_2 ambient. In this first anneal, the C49-$TiSi_2$ phase is formed.

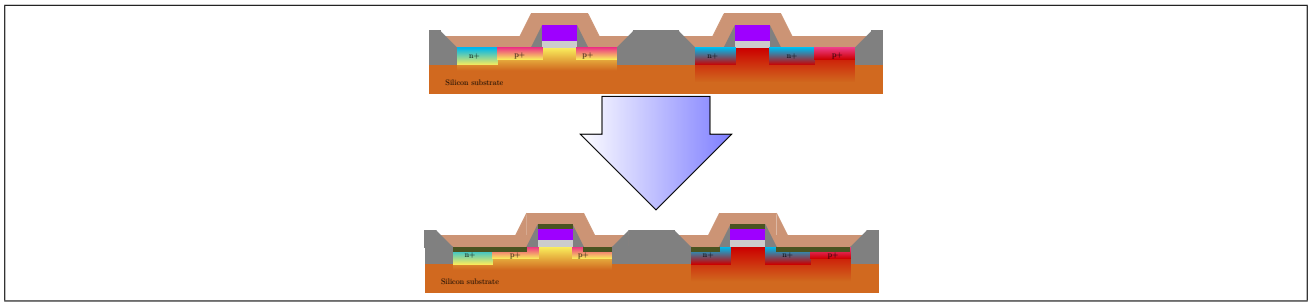

Figure 61: Reaction 1

We use the "AG610 RTP (DIF-R2)" from the HKUST at 700°C for 240 seconds.

8.6 Metal removal

The unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution.

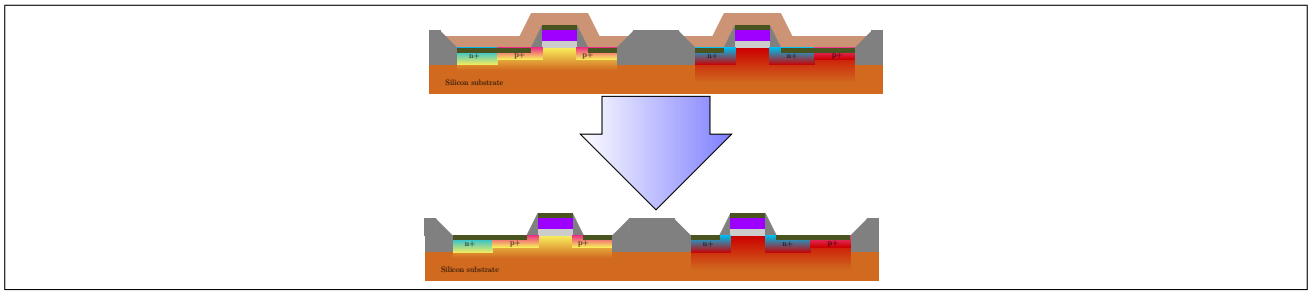

Figure 62: Titanium etch

8.7 Second reaction step

The final step is a second anneal at 800 °C or above to transform the high-resistivity C49-$TiSi_2$ phase to the low-resistivity C54-$TiSi_2$ phase at the gate electrodes and source/drain areas.

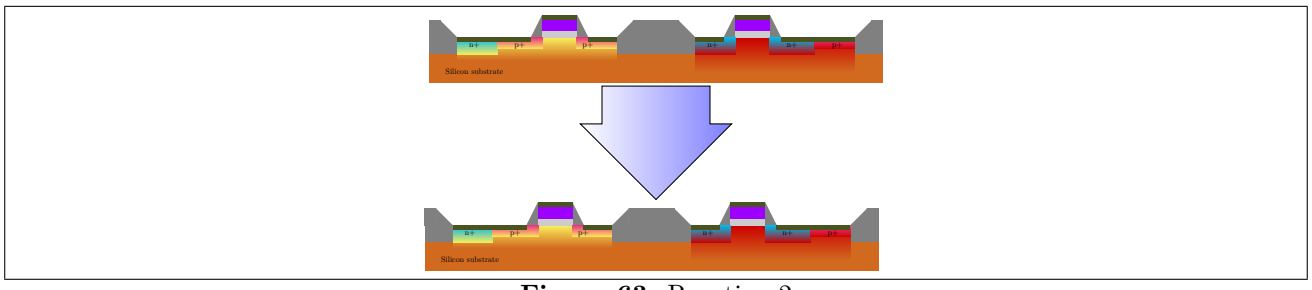

Figure 63: Reaction 2

We use the "AG610 RTP (DIF-R2)" again at 800°C for 240 seconds.

9 Contacts to active area

Now we have to build the first set of vias connecting the first metal layer to the active area. These vias are in the fringe between front-end and back-end process.

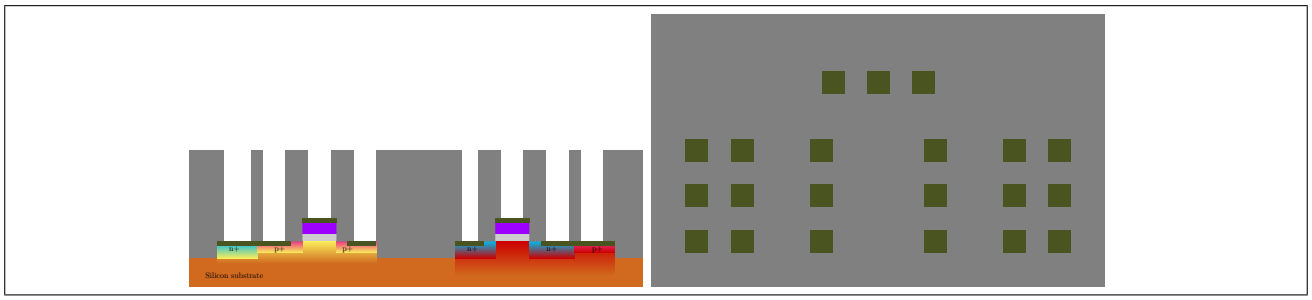

Figure 64: Contact geometry target

As can be seen in Figure 64, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the silicide and polyside in order to form wires later on. We do not wanna etch down anywhere else than the silicide/polycide areas because these function as etch stoppers, while everywhere else we might etch further than desired with small variations in etching time which might result in a drastic variation in sheet resistance of the junctions and gate.

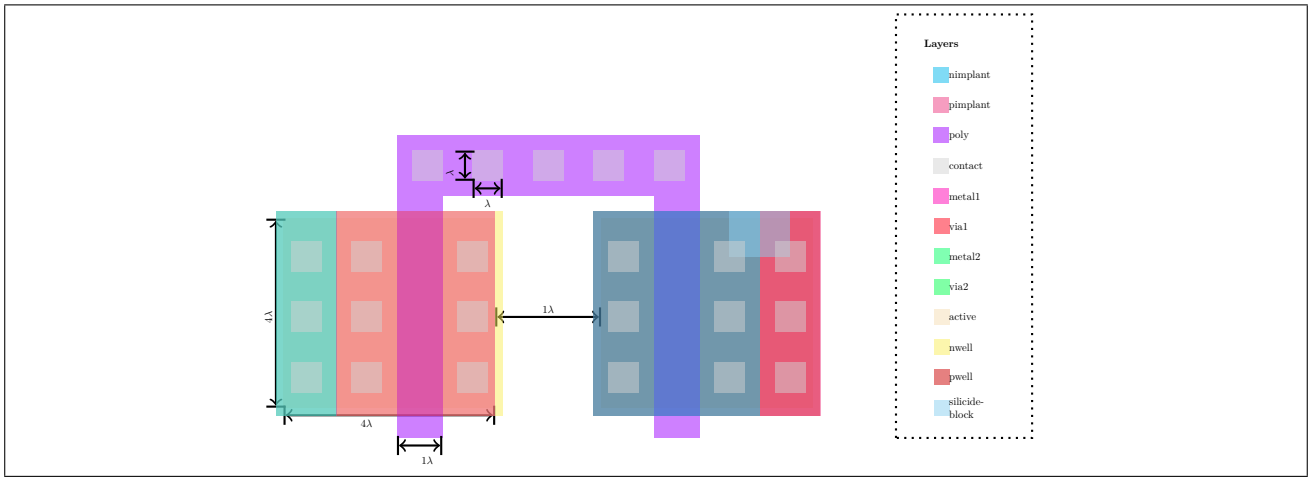

Figure 65: First via layout

It should be noted again that the via placement and dimensions in Figure 65 are solely for demonstration purposes for the process and are in no way the actual standard cell design for the final standard cell lib.

In later iterations of this process we might be switching to Tungsten as the metal material for this step.

9.1 Isolation dioxide layer

We now need to grow a layer of thick oxide in order to isolate the Aluminum interconnect layer from the active area. We can't use oxide grown in from the silicon itself inside a furnace, because of the polysilicon and silicide covering the wafer. For that reason we resort to deposited LTO (low temperature oxide), which has a lower density which is even better, because of the spacing between the isolation between the metal layers is even better.

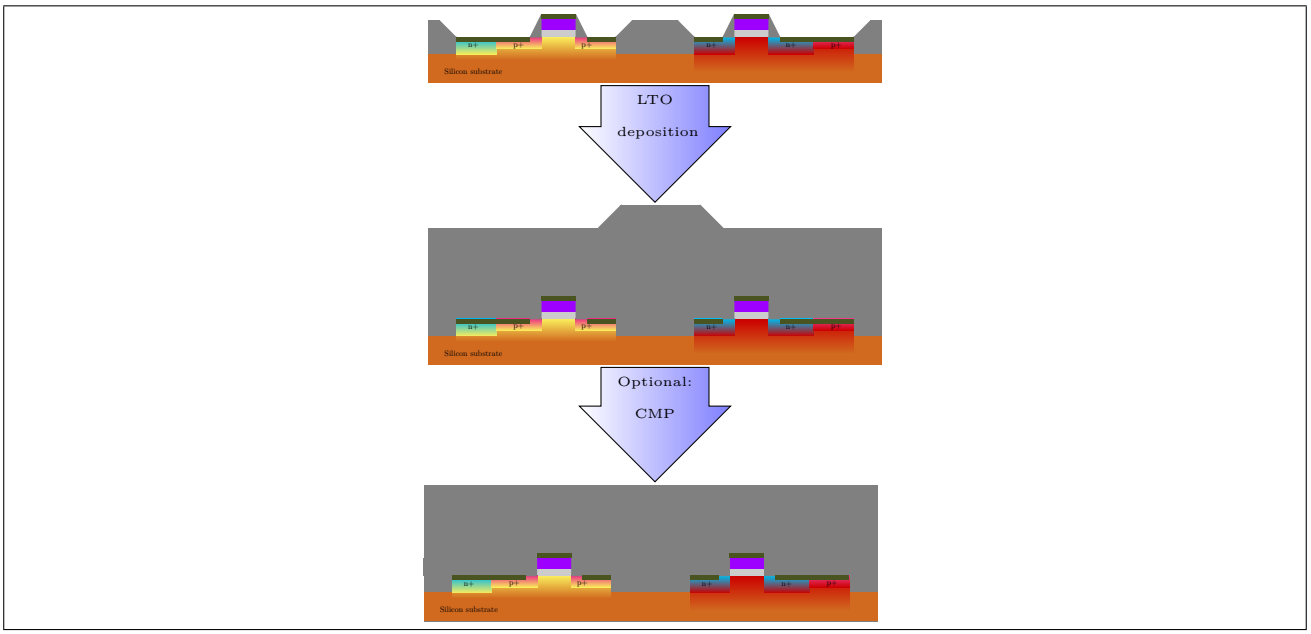

Figure 66: Oxide layer

We target a isolation layer thickness to $2\mu m$ in order to be sure that we have covered the polysilicon gate everywhere.
Possible approaches:

- **"LPCVD-B3 LTO (CVD-B3)" from HKUST**
  At HKUST we have a chemical vapor deposition unit which gives us better control over the layer thicknes. These steps are needed to arrive with the desired geometry[18]

  1. Set the growth rate to 14 nm/min
  2. Run for 140 minutes

- **In a furnace ("a hack around")**
  In case of a lack of LPCVD equipment one might also resort to "hack together" a solution for LTO deposition using a furnace[19]

  1. Deposit tetraethyl orthosilicate ($SiC_8H_{20}O_4$)
  2. React for 20 minutes at $1050°C$ in N_2 environment in a furnace

After depositing the oxide, one might wanna perform a CMP step in order to planarize the oxide surface for a more uniform deposition of metal in subsection 10.1

[18] http://memslab.blogspot.com/2013/01/lto-lpcvd.html
[19] https://www.sciencedirect.com/science/article/pii/0167577X89900062

9.2 Pattering

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "contact" layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

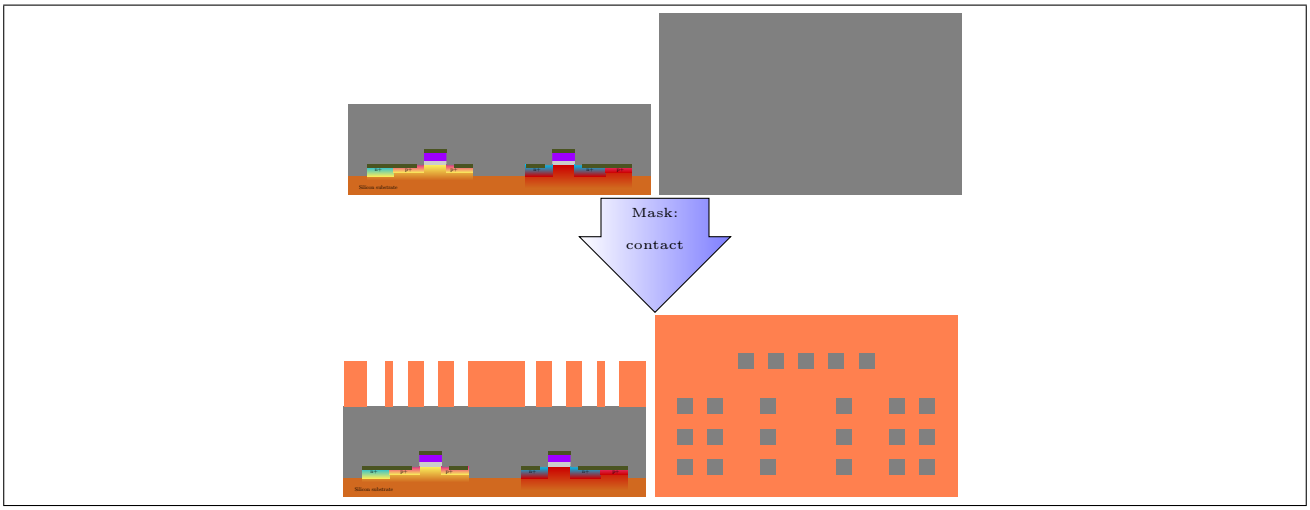

Figure 67: Patterning contact vias

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

9.3 Etching

We now need to open a window in the dioxide layer, through which the later on deposited Aluminum will touch down onto the silicide/polycide contacts of the active area.

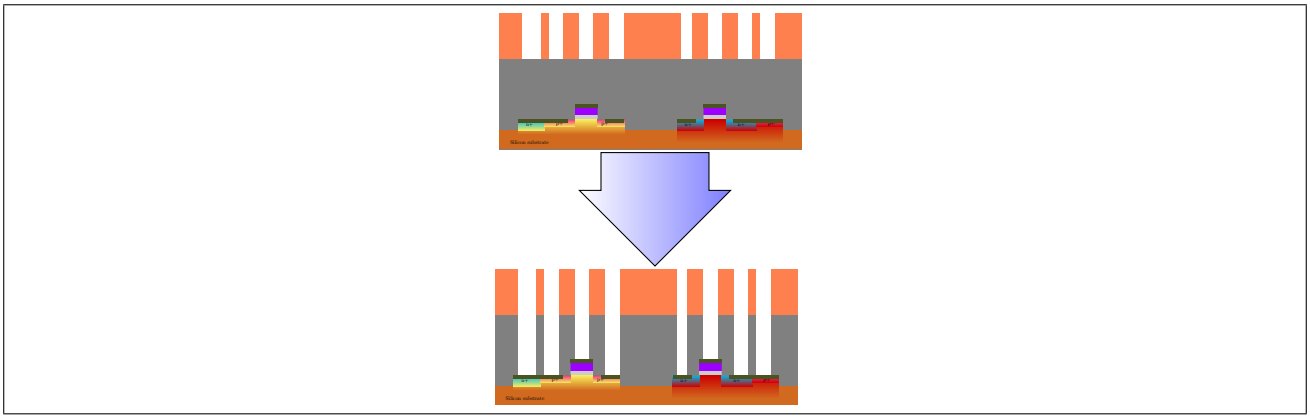

Figure 68: Etching contact holes

Since the silicon dioxide layer is $2\mu m$ thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature (≈508 nm/min) for around 4 minutes in order to get through the $2\mu m$ of oxide.
  Too long over 4 minutes might cause under-etch however!

9.4 Resist strip

Now we need to remove the contaminants for further processing.

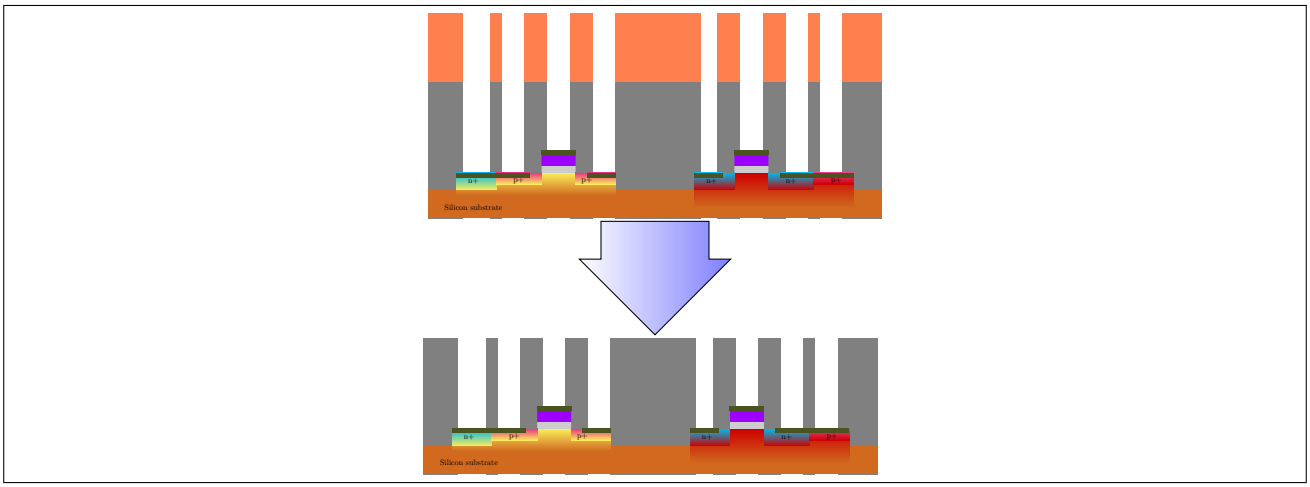

Figure 69: Resist removal

We strip the resist, rinse and perform sulfuric cleaning.

10 First metal layer

Now we've got to build the first interconnect wires, connecting the contact vias to the "metal1" wires, which will provide a way to contact to them with the via1 contact layout.

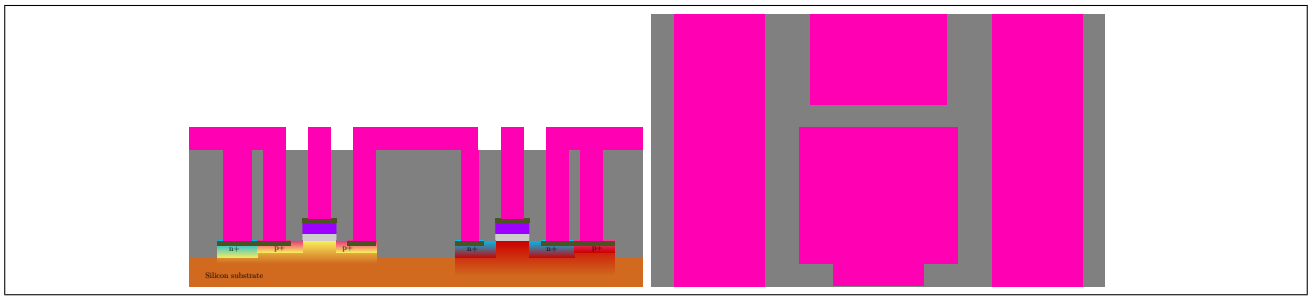

Figure 70: Metal geometry target

As can be seen in Figure 70, the goal of this step is purely to etch the wire structure for the first metal layer into the in subsection 10.1 deposited metal layer, and form wires by doing so.

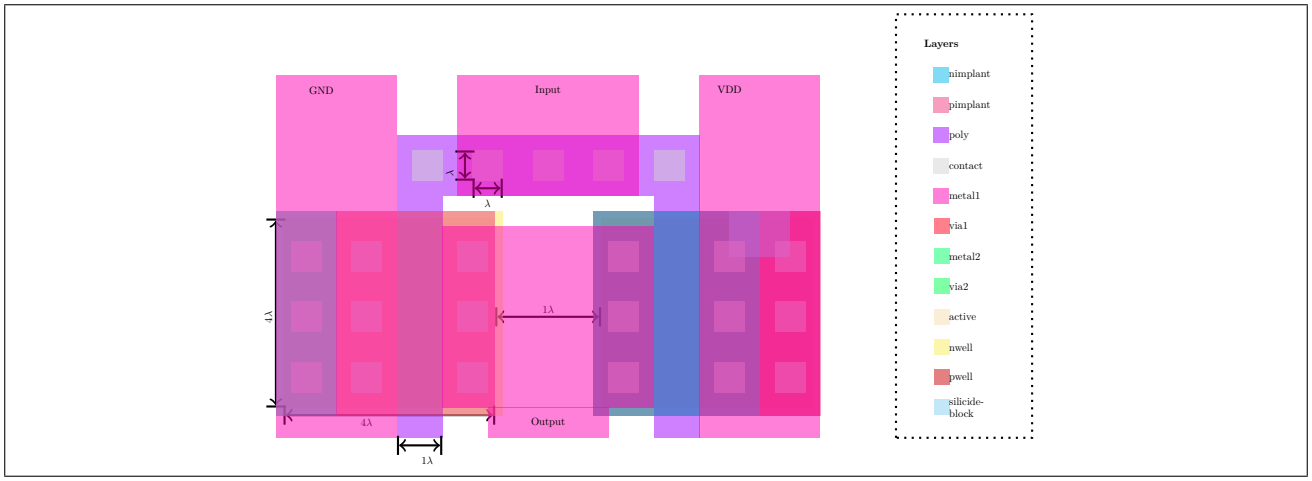

Figure 71: First metal layout

It should be noted again that the via placement and dimensions in Figure 71 are solely for demonstration purposes for the process and are in no way the actual standard cell design for the final standard cell lib.

In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.

10.1 Metal deposition

Now we somehow have got to get the metal onto our silicon oxide in a fashion so that it fills the holes we've etched in subsection 9.3 and touches down onto the silicide/polycide, thus making a contact to the active area.

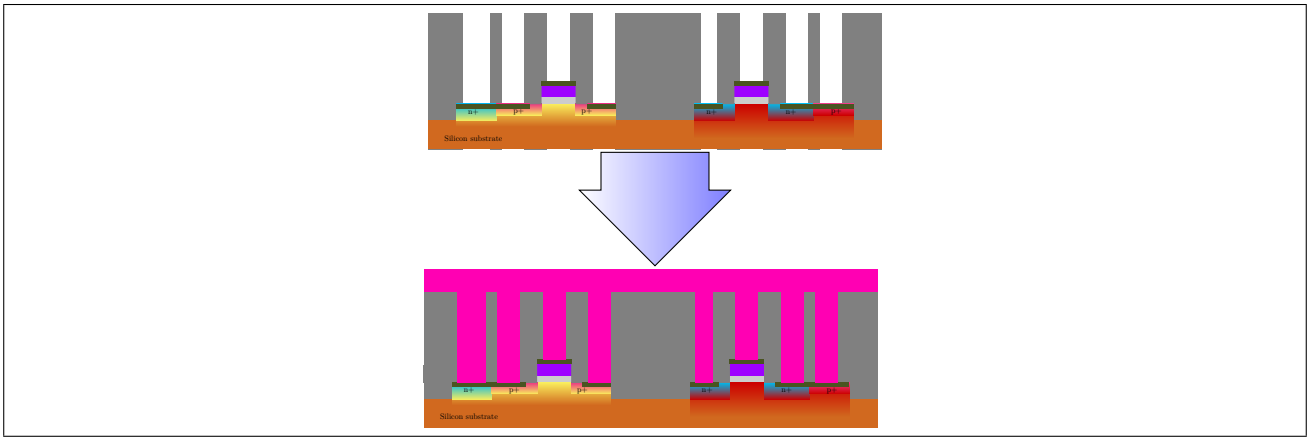

Figure 72: Metal deposition

In order to reach the target of filling the holes in the oxide and having at least another depth worth of space in order to have an enough low resistance of the wire interconnect. We end up with a target thickness of $4\mu m$.
Possible approaches:

- **"Varian 3180 Sputter (SPT-3180)" from HKUST**
  The deposition speed is 16nm/s which gives us a required deposition time of 250 seconds for $4\mu m$.
- **Add your solution here!**

10.2 Pattering

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the "metal1" layer within the GDS2 file onto a **bright field** mask. The requirement is a **positive** tone resist.

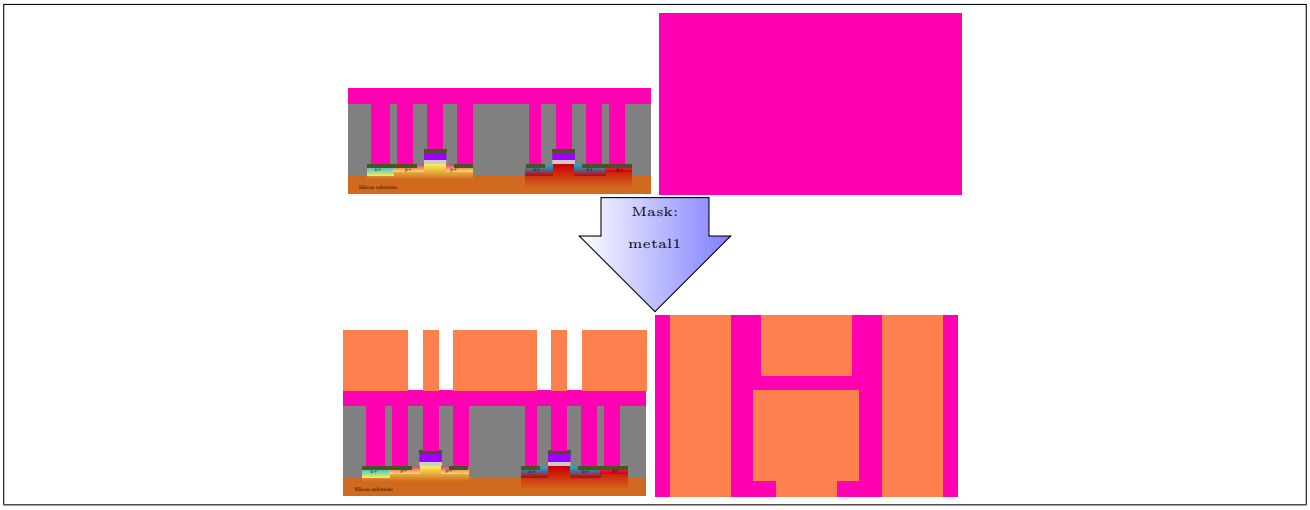

Figure 73: Patterning first wires

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn't be forgotten!

10.3 Etching

Now we've got to etch the Aluminum which hasn't been covered yet by the resist in order to get the desired wire structures.

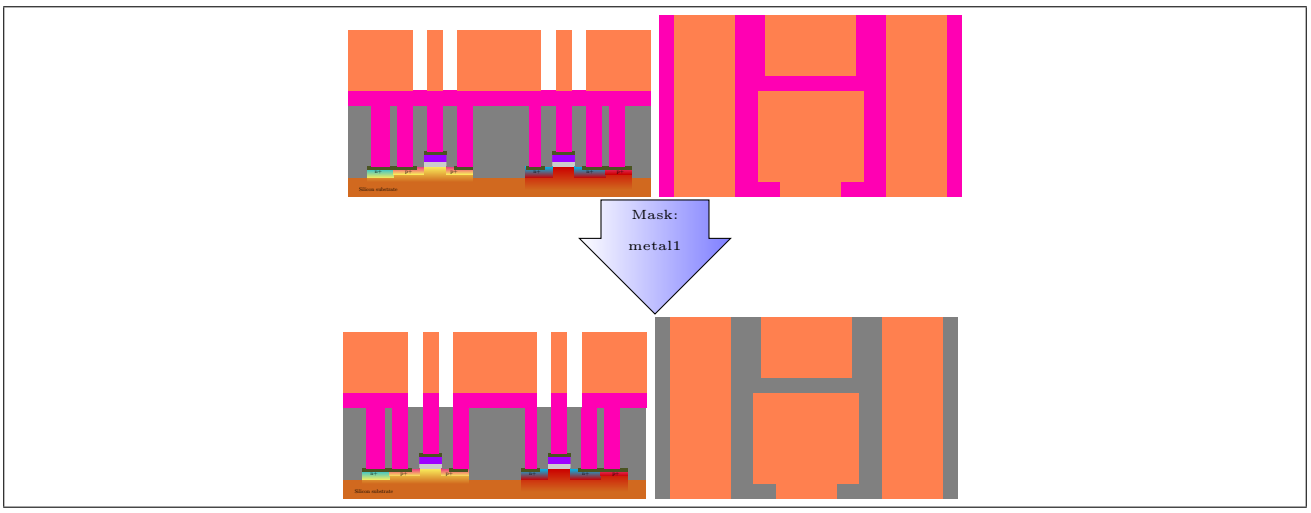

Figure 74: Etching first wires

Possible approaches:

- **"Oxford Aluminum Etcher (DRY-Metal-2)" from HKUST**
  The normal etch rate for Aluminum is 180 nm/min with this machines
  We've deposited $4\mu m$ Aluminum in subsection 10.1 which means we've got to etch for around 22 minutes and 13 seconds
- **Chemical solution**
  Please specify here!

10.4 Resist strip

Now we need to remove the photo resist for further processing because it would contaminate the equipment.

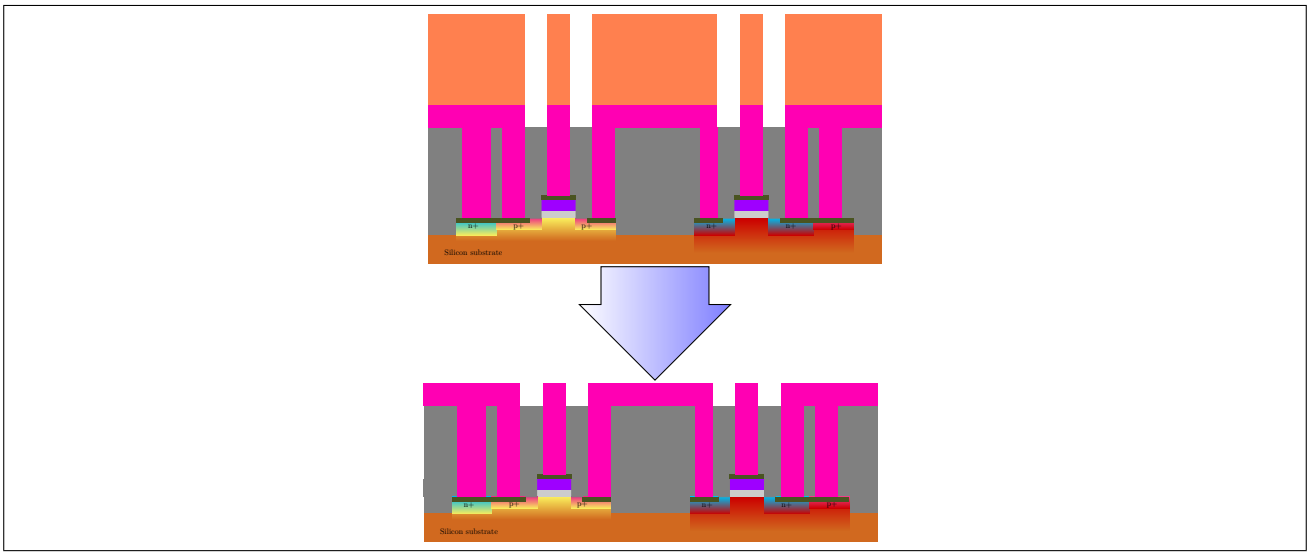

Figure 75: Resist removal

Because we now have a metal layer we can't use sulfuric acids because this would dissolve/attack the Aluminum as well as the photo resist. Instead we have got to use an organic solvent which does not react with Aluminum.
Possible approaches:

- **"MS2001 resist stripper" from HKUST**
  It can be found at the wet stations: Wetstation W, X, Y and Z (WET-W1 to WET-W2, WET-X1 to WET-X2, WET-Y1to WET-Y2, WET-Z1 to WET-Z2)
- **Another chemical solution**
  Please specify here!

11 Via

Now we have to build an additional set of vias connecting the first metal layer to the next metal layer. These vias are already part of the front-end process.

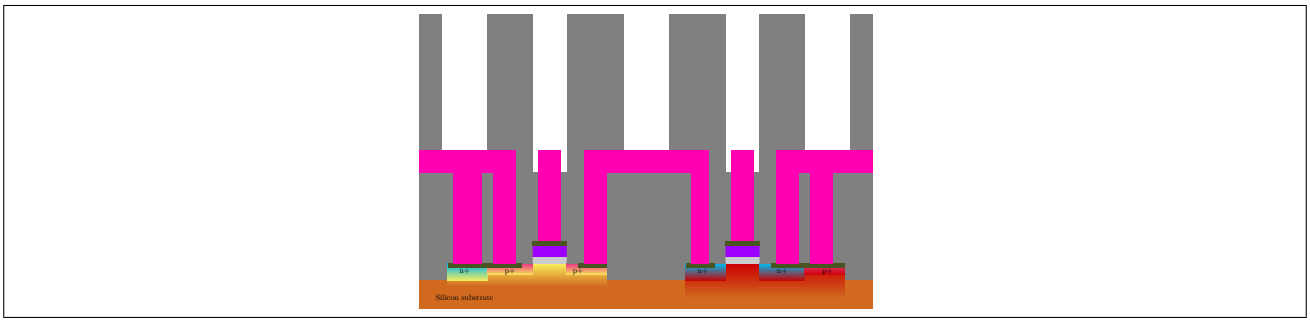

Figure 76: Contact geometry target

As can be seen in Figure 76, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.

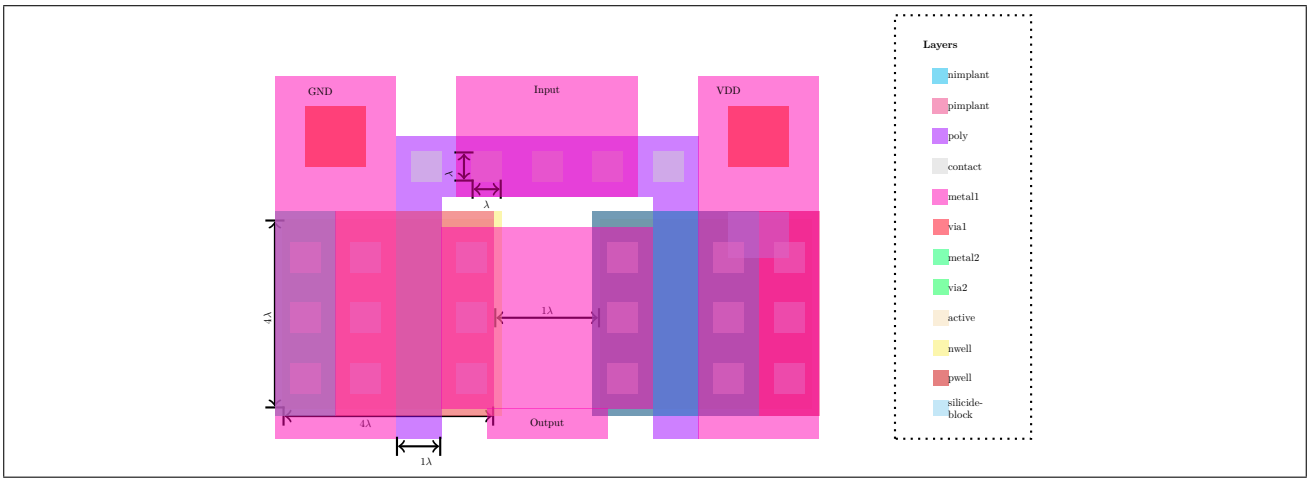

Figure 77: First via layout

It should be noted again that the via placement and dimensions in Figure 77 are solely for demonstration purposes for the process and are in no way the actual standard cell design for the final standard cell lib.

In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.

11.1 Isolation dioxide layer

We now need to grow a layer of thick oxide in order to isolate the Aluminum interconnect layer from the active area.

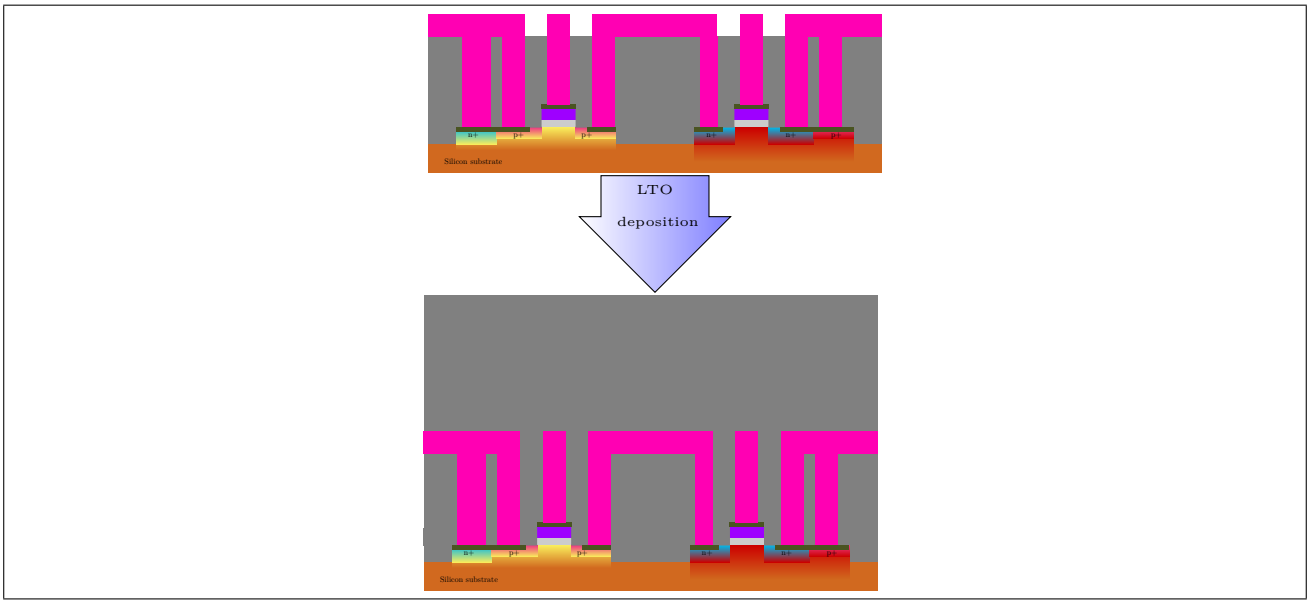

Figure 78: Oxide layer

Possible approaches:

- **"LPCVD-B3 LTO (CVD-B3)" from HKUST**
  At HKUST we have a chemical vapor deposition unit which gives us better control over the layer thicknes. These steps are needed to arrive with the desired geometry[20]

  1. Set the growth rate to 14 nm/min
  2. Run for 140 minutes

- **In a furnace ("a hack around")**
  In case of a lack of LPCVD equipment one might also resort to "hack together" a solution for LTO deposition using a furnace[21]

  1. Deposit tetraethyl orthosilicate ($SiC_8H_{20}O_4$)
  2. React for 20 minutes at $1050°C$ in N_2 environment in a furnace

[20] `http://memslab.blogspot.com/2013/01/lto-lpcvd.html`
[21] `https://www.sciencedirect.com/science/article/pii/0167577X89900062`

11.2 Pattering

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”contact” layer within the GDS2 file onto a **bright field** mask. The requirement is a **negative** tone resist.

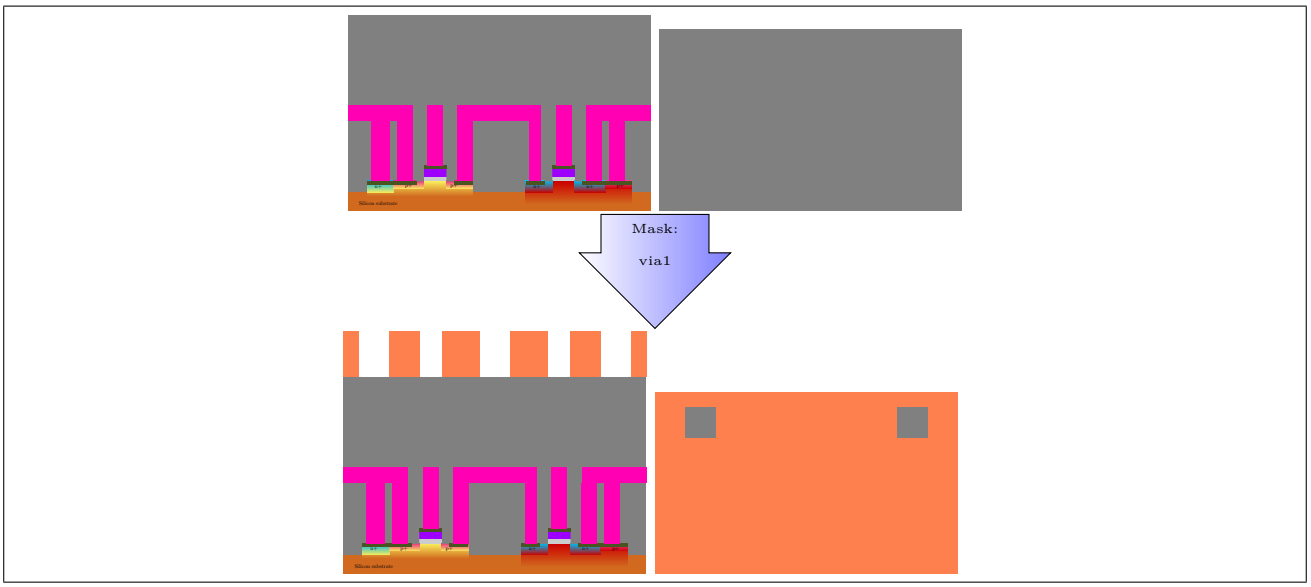

Figure 79: N+ region resist mask

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn’t be forgotten!

11.3 Etching

We now need to open a window in the dioxide layer, through which we will inject carrier atoms into the silicon crystal structure.

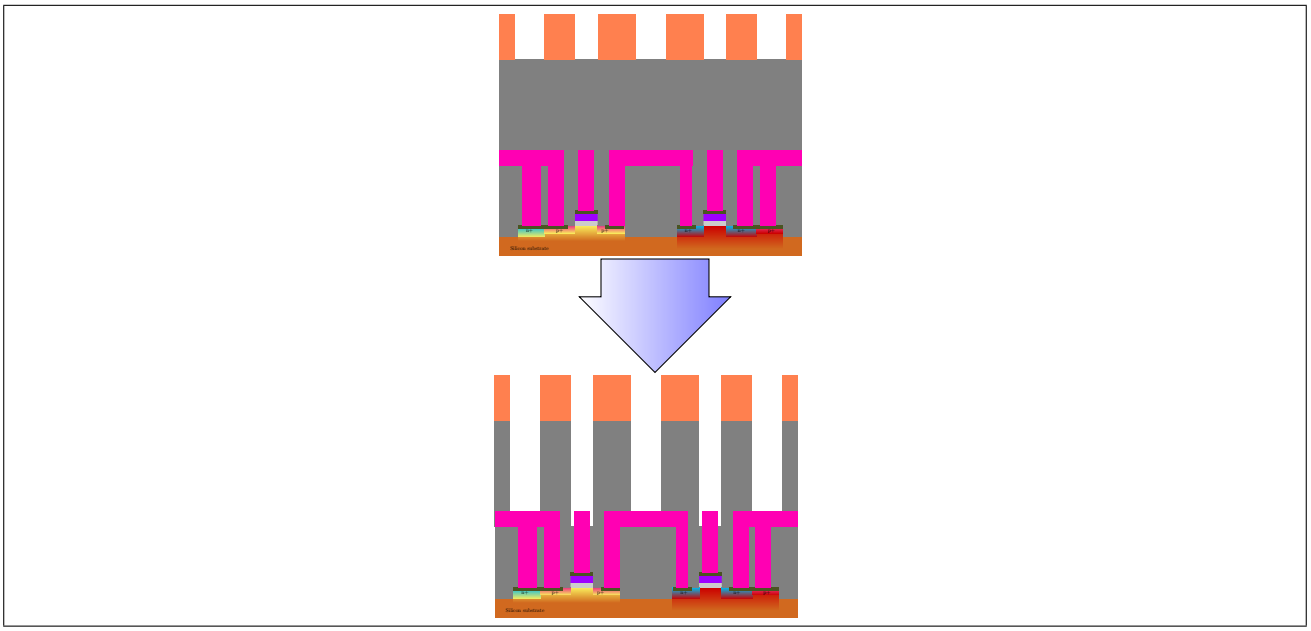

Figure 80: N+ region opened

Since the silicon dioxide layer is 100nm thick and we wanna reach the silicon below we can use wet etching as described in the chemistry chapter.

Possible approaches:

- **"AOE Etcher (DRY-AOE)" from HKUST**
  We can use anisotropic plasma etching for sharper borders.
- **Chemical solution**
  We can use buffered hydrofluoric acid (BOE (1:6)) at room temperature for a little bit over 3 minutes in order to get through the 100nm of oxide.
  Too long over 1 minutes might cause under-etch however!

11.4 Cleaning

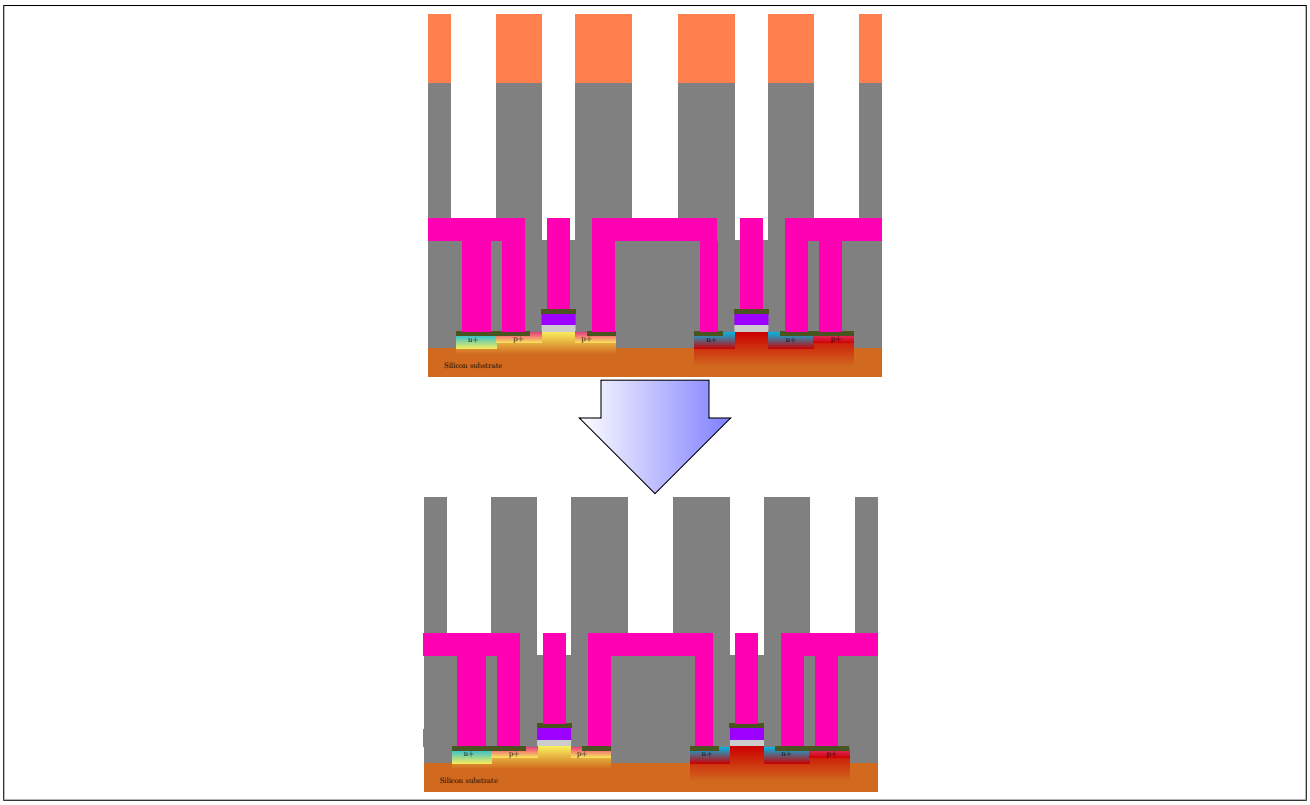

Figure 81: Resist removal

12 Additional metal layer

Now we've got to build the more interconnect wires, connecting the contact vias to the "metal2" wires, which will provide a way to contact to them with the via2 contact layout.

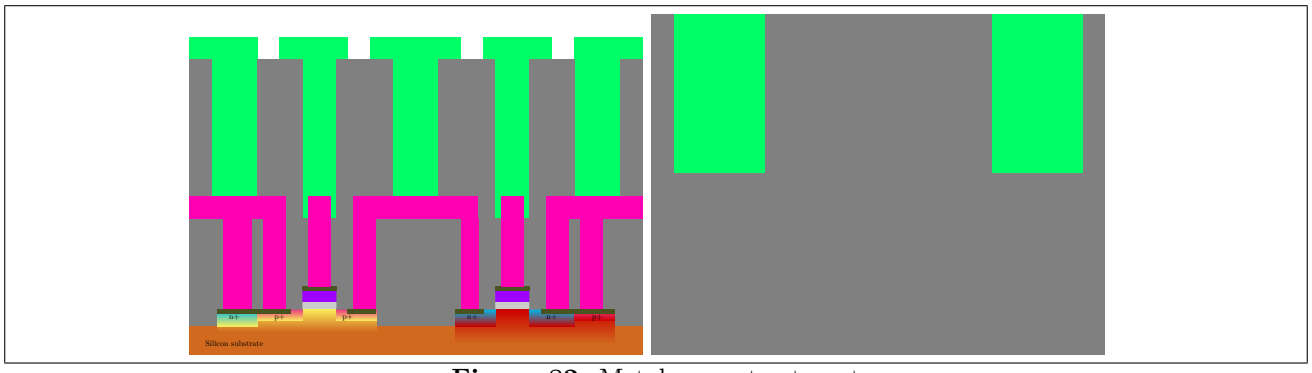

Figure 82: Metal geometry target

As can be seen in Figure 82, the goal of this step is purely to etch the wire structure for the additional metal layer into the in subsection 12.1 deposited metal layer, and form wires by doing so.

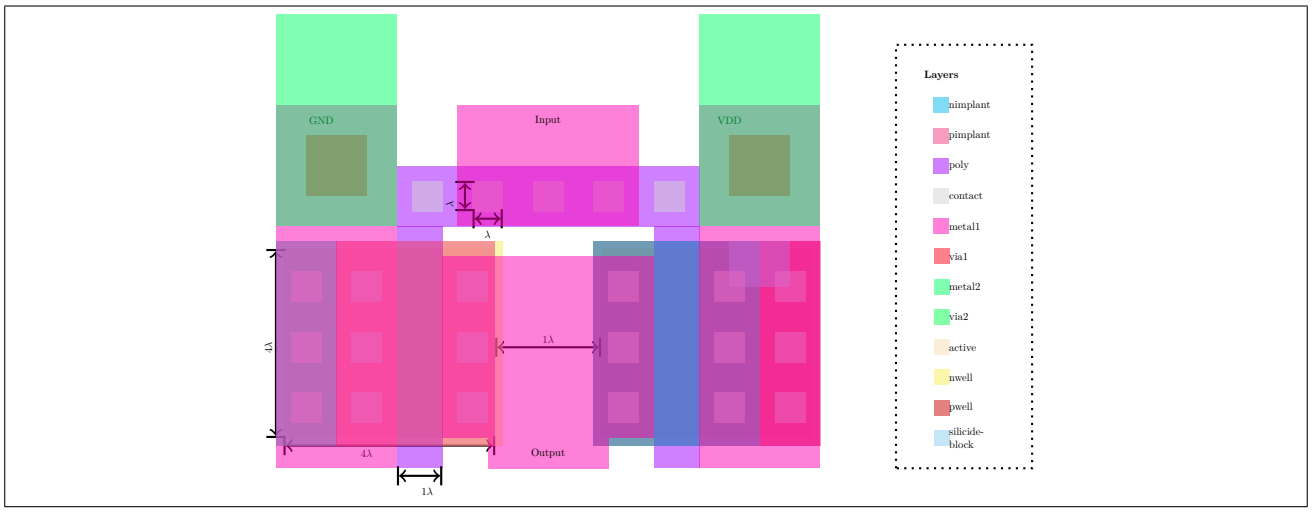

Figure 83: Second metal layout

It should be noted again that the via placement and dimensions in Figure 83 are solely for demonstration purposes for the process and are in no way the actual standard cell design for the final standard cell lib.

In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.

12.1 Metal deposition

Now we somehow have got to get the metal onto our silicon oxide in a fashion so that it fills the holes we've etched in subsection 11.3 and touches down onto the last metal layer, thus making a contact to the plane below.

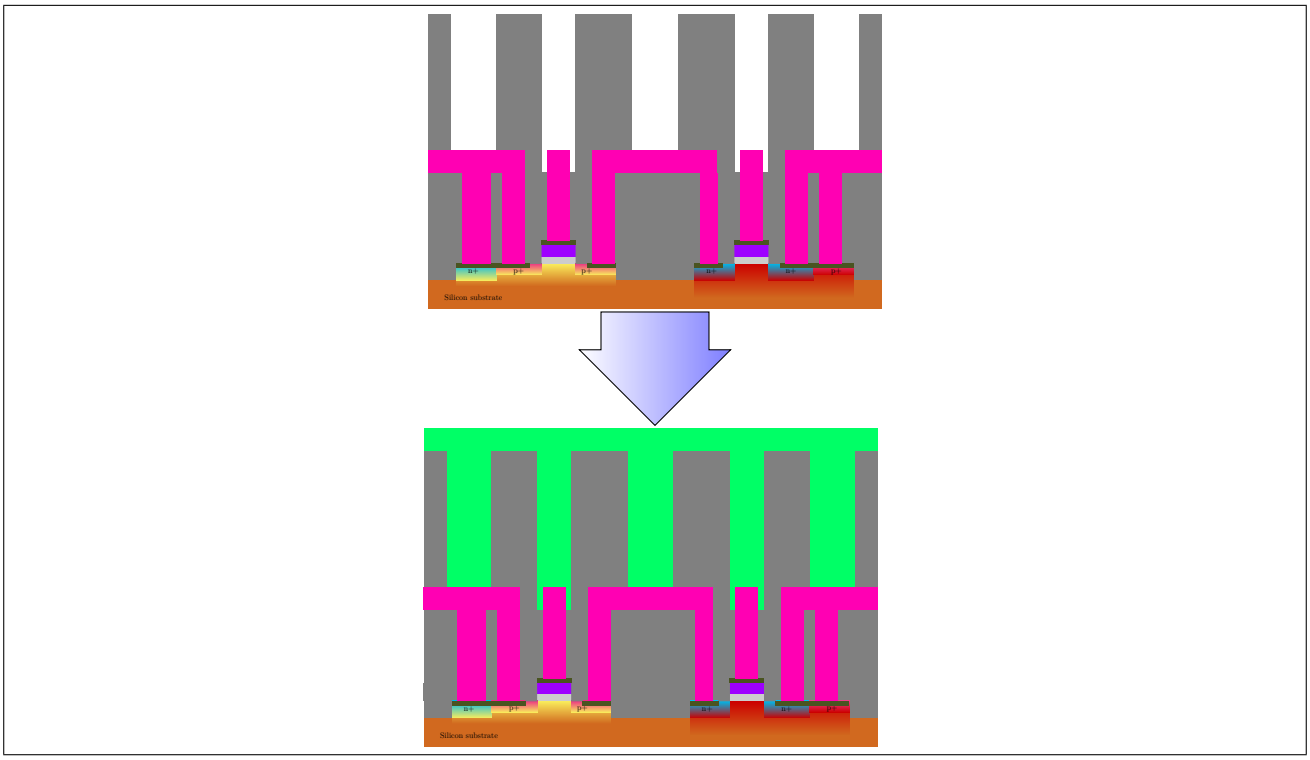

Figure 84: Metal deposition

In order to reach the target of filling the holes in the oxide and having at least another depth worth of space in order to have an enough low resistance of the wire interconnect. We end up with a target thickness of $4\mu m$.
Possible approaches:

- **"Varian 3180 Sputter (SPT-3180)" from HKUST**
  The deposition speed is 16nm/s which gives us a required deposition time of 250 seconds for $4\mu m$.
- **Add your solution here!**

12.2 Pattering

The resist is being deposited using spin coating and then baked depending on the baking time for the specific resist. The layout for being exposed onto the resist is being extracted from the ”more1” layer within the GDS2 file onto a **bright field** mask. The requirement is a **positive** tone resist.

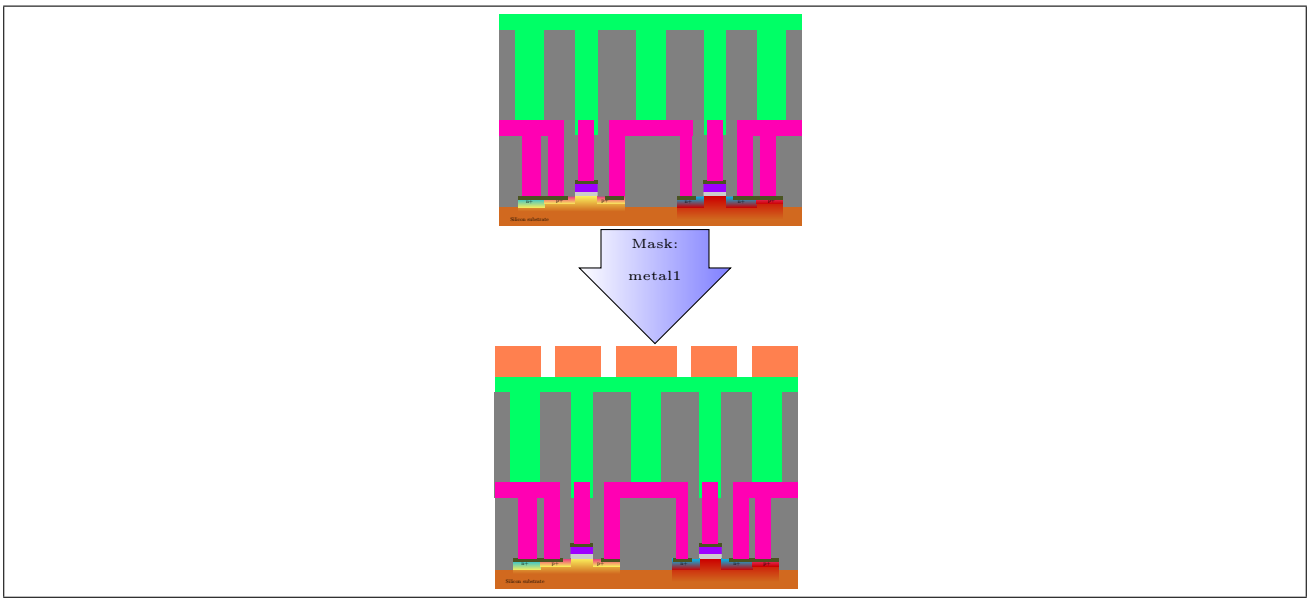

Figure 85: Patterning first wires

The thickness of the resist layer and the baking duration will variate depending on the specific equipment for which this process will be implemented with. Also after the exposure and development, the hard baking shouldn’t be forgotten!

12.3 Etching

Now we've got to etch the Aluminum which hasn't been covered yet by the resist in order to get the desired wire structures.

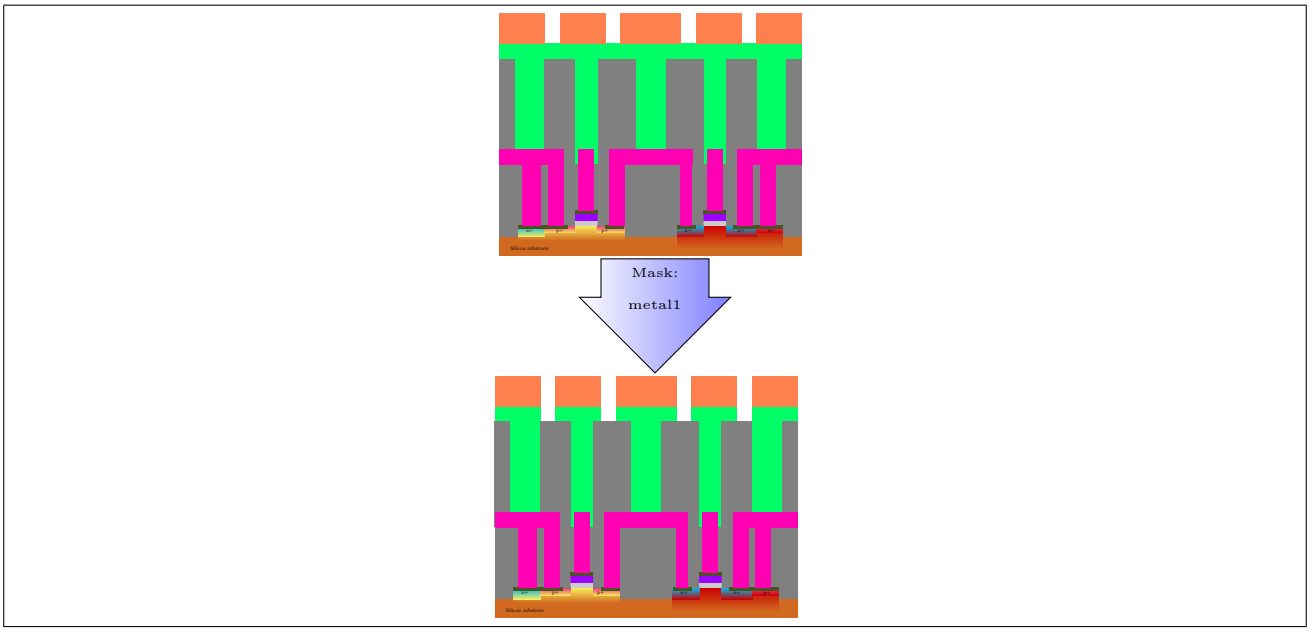

Figure 86: Etching first wires

Possible approaches:

- **"Oxford Aluminum Etcher (DRY-Metal-2)" from HKUST**
  The normal etch rate for Aluminum is 180 nm/min with this machines
  We've deposited $4\mu m$ Aluminum in subsection 12.1 which means we've got to etch for around 22 minutes and 13 seconds
- **Chemical solution**
  Please specify here!

12.4 Resist strip

Now we need to remove the photo resist for further processing because it would contaminate the equipment.

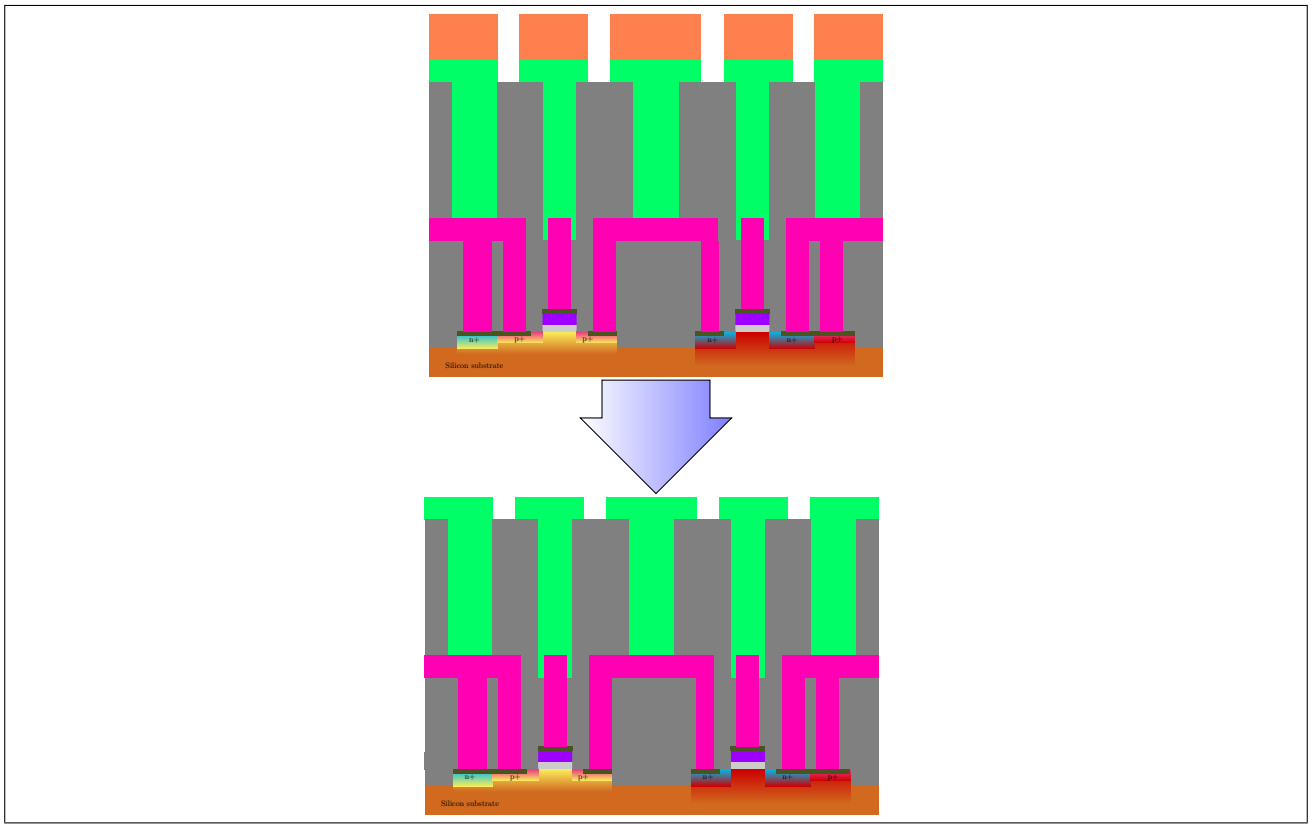

Figure 87: Resist removal

Because we now have a metal layer we can't use sulfuric acids because this would dissolve/attack the Aluminum as well as the photo resist. Instead we have got to use an organic solvent which does not react with Aluminum.
Possible approaches:

- **"MS2001 resist stripper" from HKUST**
  It can be found at the wet stations: Wetstation W, X, Y and Z (WET-W1 to WET-W2, WET-X1 to WET-X2, WET-Y1to WET-Y2, WET-Z1 to WET-Z2)
- **Another chemical solution**
  Please specify here!