

## Abstract

Copyright © 2017 LANCEVILLE TECHNOLOGY GROUP CO., LIMITED. All rights reserved.

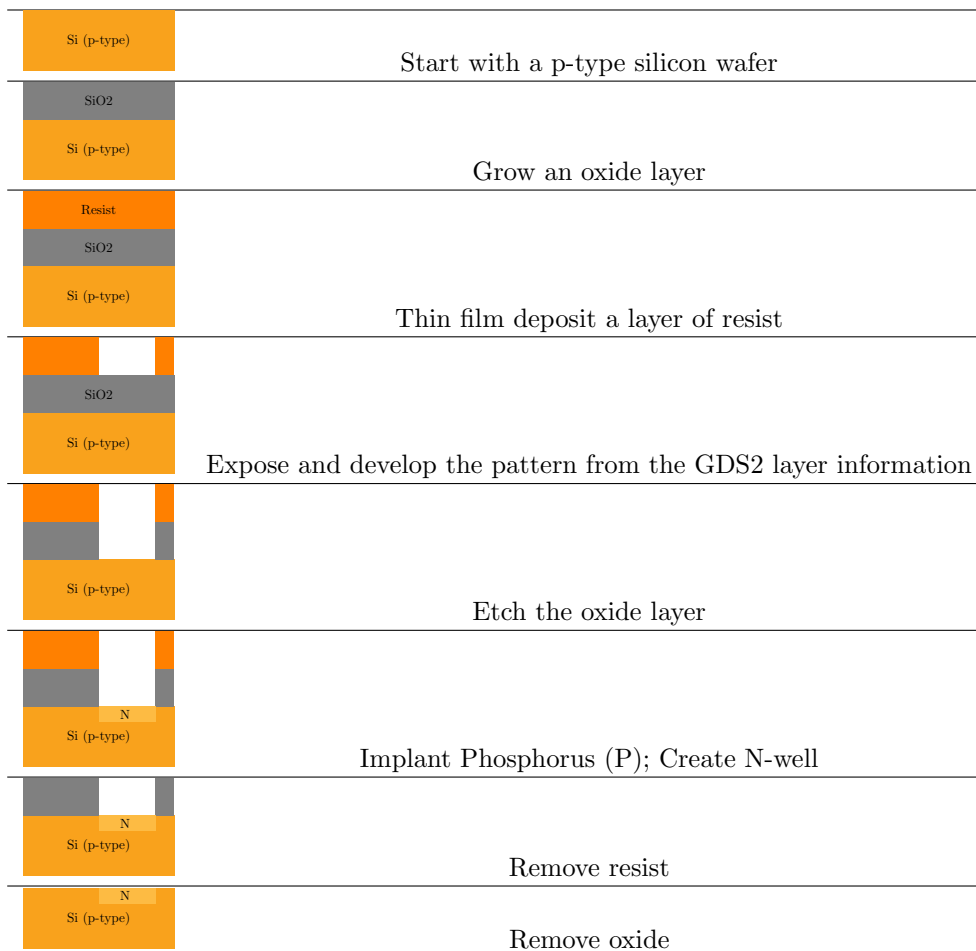
This process is licensed under the Libre Silicon public license; you can redistribute it and/or modify it under the terms of the Libre Silicon public license as published by the Libre Silicon alliance, either version 2 of the License, or (at your option) any later version.

This design is distributed in the hope that it will be useful, but WITHOUT ANY WARRANTY; without even the implied warranty of MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. See the Libre Silicon Public License for more details.

This is the specification of the free silicon manufacturing standard for manufacturing the ls018<sup>1</sup> standard logic cells and related free technology nodes from the LibreSilicon project.

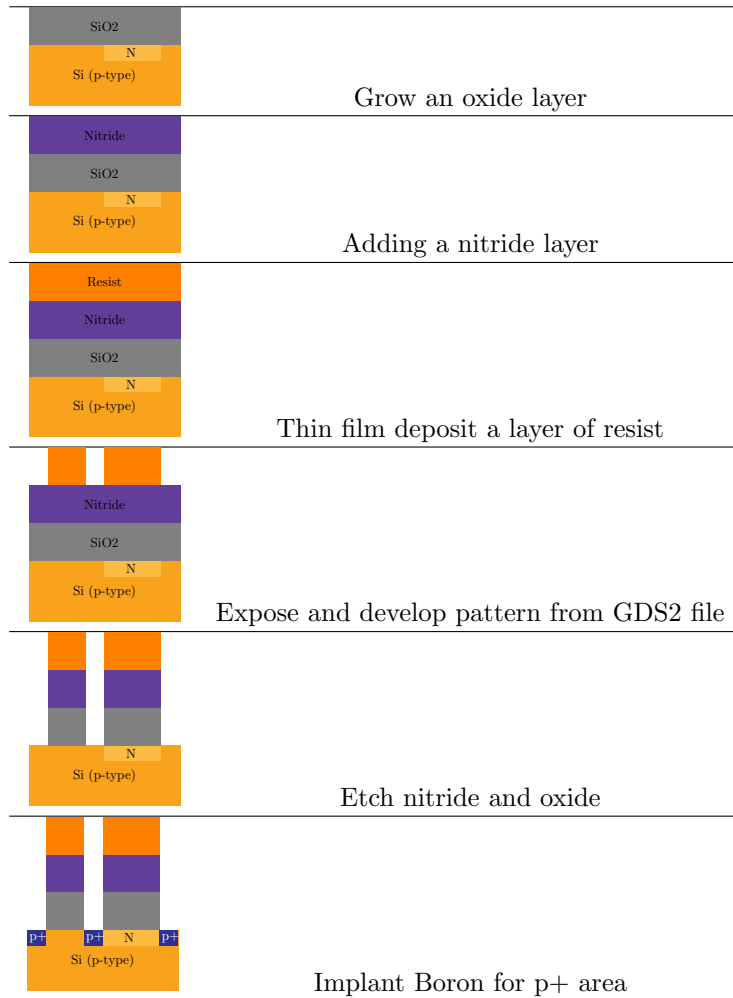
For further clarification consult the complete documentation of the process.

## 1 Well



<sup>1</sup><https://github.com/leviathanch/ls018>

## 2 Implant



## 3 Select

## 4 Active

## 5 Metal