# Generic LibreSilicon process overview

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#### Abstract

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This is the specification of the free silicon manufacturing standard for manufacturing the ls018<sup>1</sup> standard logic cells and related free technology nodes from the LibreSilicon project.

For further clarification consult the complete documentation of the process.

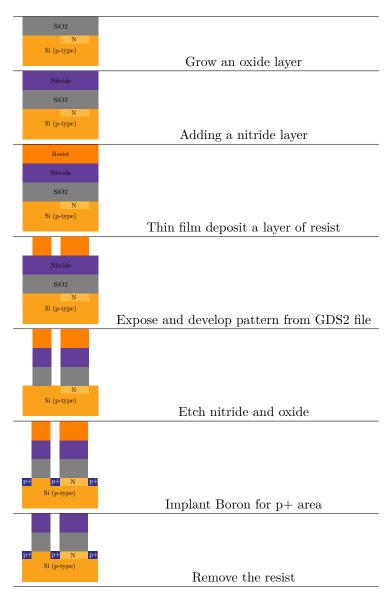
<sup>&</sup>lt;sup>1</sup>https://github.com/leviathanch/ls018

## 1 N-Well

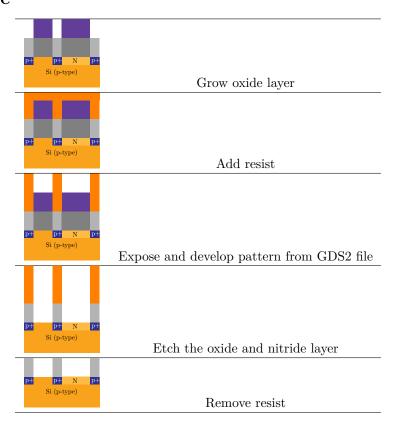
The n-well is required for CMOS technology built on a p-substrate. For this process p-substrate is required.

Si (p-type)	
	Start with a p-type silicon wafer
SiO2	
Si (p-type)	0 11
	Grow an oxide layer
Resist	
SiO2	
Si (p-type)	
	Thin film deposit a layer of resist
SiO2	
Si (p-type)	
Si (p-type)	Expose and develop the pattern from the GDS2 layer information
	Empose and develop the pattern from the GEO- layer information
Si (p-type)	Tt-1- 41 1- 1
	Etch the oxide layer
N	
Si (p-type)	
	Implant Phosphorus (P); Create N-well
N	
Si (p-type)	
	Remove resist
N	
Si (p-type)	Damana anida
	Remove oxide

# 2 P+ Implant



## 3 Field oxide



# 4 Poly

