LibreSilicon process HKUST (NFF)

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Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Process Flow of Lanceville Technologies LibreSilicon 180nm

- Project: LibreSilicon $1\mu m$
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer <100>
- Date: May 15, 2018

1 Shallow trench isolation

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
1.1	A3: Sulfuric Cleaning	P201000	Clean	Initial Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
1.2	A2: HF:H2O (1:50)	P201000	Clean	HF dip	1 min	Clean
1.3	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
1.4	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	300nm, 25 minutes @ 1050°C	Clean
1.5	B1: Sulfuric Cleaning	P201000	Clean	Standard Cleaning	H2SO4 + H2O2, 10mins @ 120°C	Clean
1.6	Spin Dryer-B	P201000	Clean	Dry the wafer automatically		Clean
1.7	SVG Coater Track	P200100	Clean / Semi clean	HMDS, PR coating, soft bake	AZ 504, 1.2µm, soft bake: 110C 1min	Clean
1.8	ASML Stepper	P200100	Clean / Semi clean	Exposure of the active layer	??	Clean
1.9	SVG Developer Track	P200100	Clean / Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120C, 1min	Clean
1.10	C3: BOE	P201000	Clean	Oxide Etch	3 minutes 10 seconds	Clean
1.11	E4: Resist Strip	P201000	Clean / Semi clean	Sulfuric resist strip	H2SO4 + H2O2,120C, 10mins	Clean
1.12	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean
1.13	DRIE Etcher #1 (DRY-Si-1)(We can't use KOH because of contamination control rules)	P201000	Clean / Semi clean	Etching the trenches	$2\mu m$	Clean
1.14	C3: BOE	P201000	Clean	Oxide Etch	3 minutes 10 seconds	Clean
1.15	Spin Dryer-E	P201000	Clean / Semi clean	Spin dry		Clean

2 P-well

Step Number	Equipment	Location	Cleanliness	Process	Requirements	Wafer Cleanliness
2.1	A3: Sulfuric Cleaning	P201000	Clean	Initial Clean	H2SO4 + H2O2, 10mins @ 120°C	Clean
2.2	A2: HF:H2O (1:50)	P201000	Clean	HF dip	1 min	Clean
2.3	Spin Dryer-A	P201000	Clean	Dry the wafer automatically		Clean
2.4	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	300nm, 25 minutes @ 1050°C	Clean
2.5	B1: Sulfuric Cleaning	P201000	Clean	Initial Clean	H2SO4 + H2O2, 10mins @ 120°C	Clean
2.6	Spin Dryer-B	P201000	Clean	Dry the wafer automatically		Clean
2.7	Diff. Furnace-D2 Dry/Wet Oxidation	P201000	Clean	Hard mask dioxide growth	300nm, 25 minutes @ 1050°C	Clean