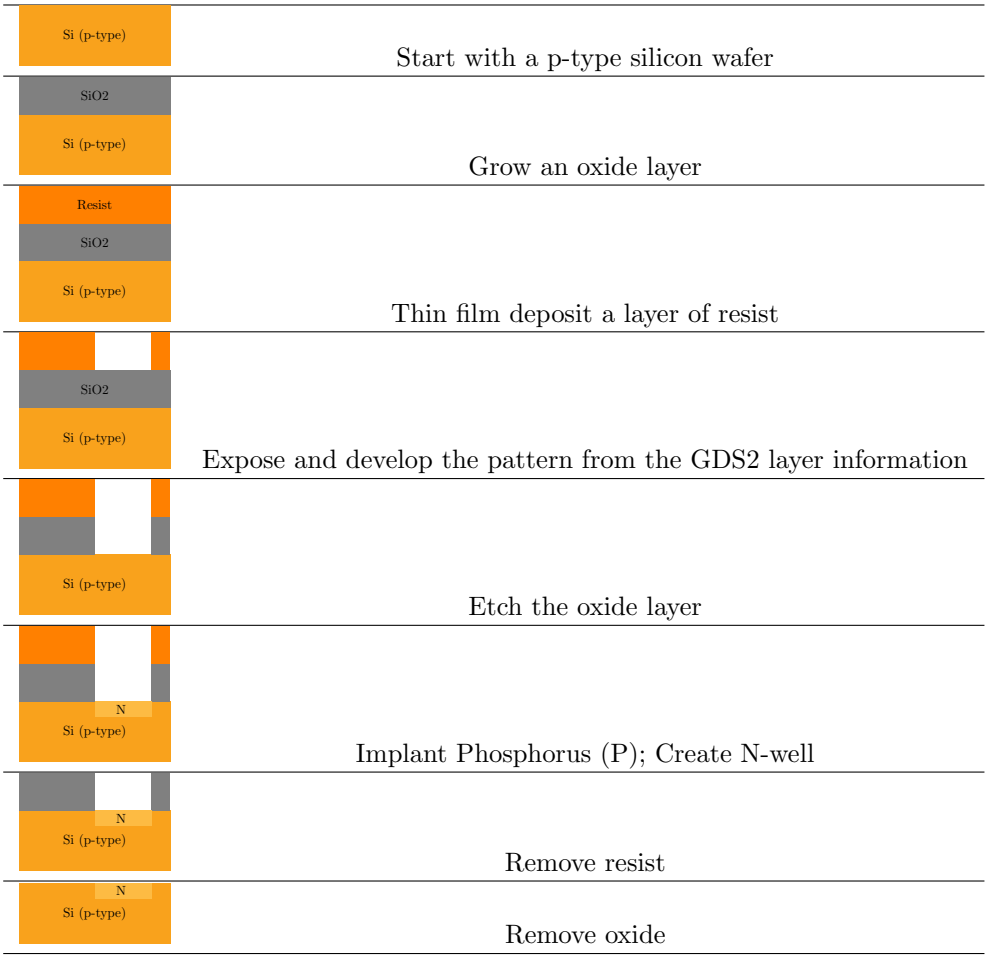
Abstract

This is the specification of the free silicon manufacturing standard for manufacturing the ls018[1]standard logic cells and related free technology nodes from the LibreSilicon project.

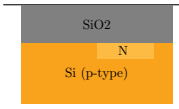
For further clarification consult the complete documentation of the process.

1 Well

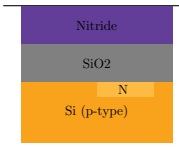


[1]https://github.com/leviathanch/ls018

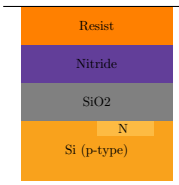
2 Implant



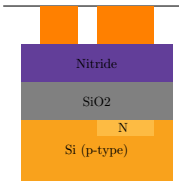
Grow an oxide layer (see documentation)



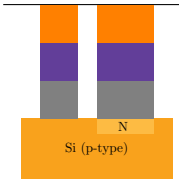
Adding a nitride layer (see documentation)



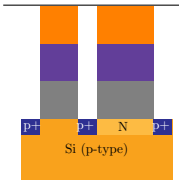
Thin film deposit a layer of resist



Expose and develop pattern from GDS2 file



Etch nitride and oxide



Implant Boron for p+ area

3 Select

4 Active

5 Metal