

# LibreSilicon process HKUST (NFF)

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September 23, 2018

## Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells<sup>1</sup> and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent  $1\mu m$  to smaller structure sizes. **This process is for manufacturing  $1\mu m$  only!** But further releases which will have been tested with smaller structure sizes can be expected. Please see the document with the generic steps<sup>2</sup> in order to get a detailed description of the different steps.

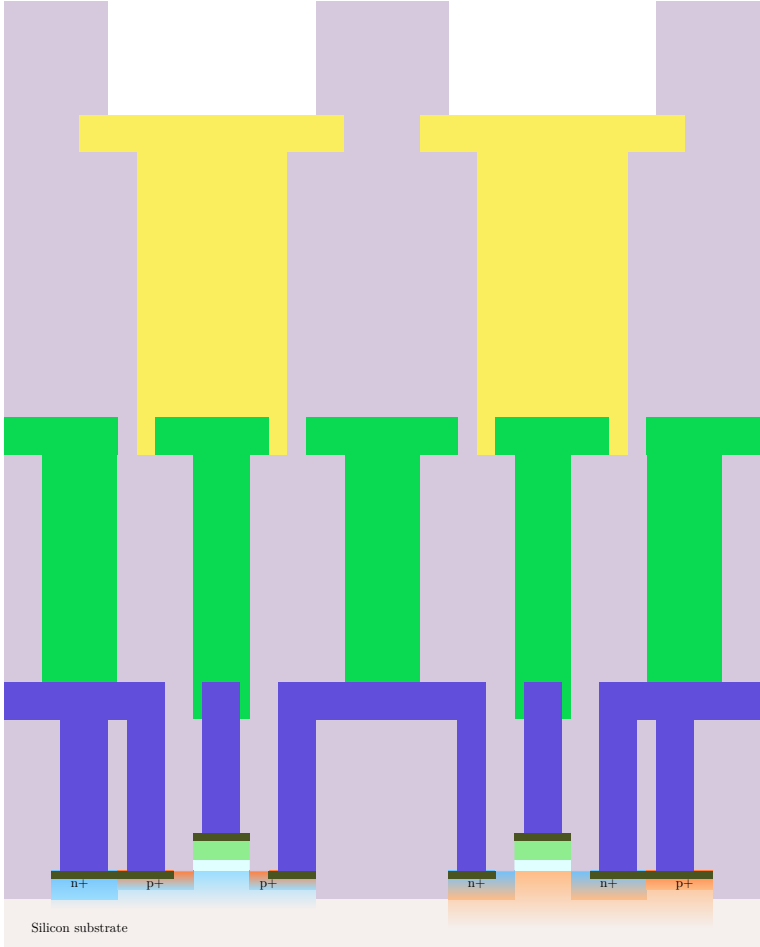
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<sup>1</sup><https://github.com/chipforge/StdCellLib>

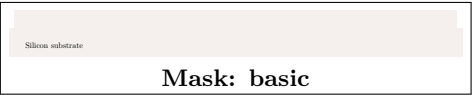
<sup>2</sup>[https://github.com/libresilicon/process/raw/master/process\\_steps/process\\_hightech/process\\_hightech\\_steps.pdf](https://github.com/libresilicon/process/raw/master/process_steps/process_hightech/process_hightech_steps.pdf)

## Process Flow of Lanceville Technologies LibreSilicon 1 $\mu m$

- Project: LibreSilicon  $1\mu m$
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer  $\langle 100 \rangle$
- Date: September 23, 2018

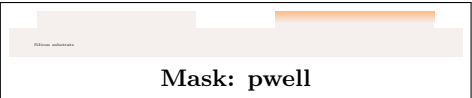


1 Initial alignment mask



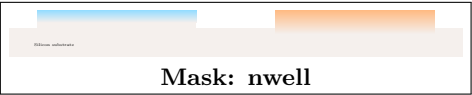
Wafer ness	Cleanli-	Step ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		1.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		1.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		1.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Clean		1.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		1.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean		1.6	Lam 490 etcher (DRY-490)	P2-01000	Clean	Etching the alignment crosses from HKUST	2 minutes (120nm)
Clean		1.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		1.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		1.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

2 P-well



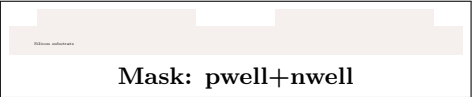
Wafer ness	Cleanli-	Step ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		2.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		2.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		2.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Clean		2.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		2.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean		2.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @60keV
Clean		2.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		2.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		2.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

### 3 N-well



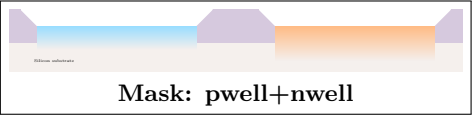
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		3.1		B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		3.2		Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		3.3		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( $\approx 1.5\mu m$ ), soft bake: $110^{\circ}C$ 1min
Clean		3.4		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		3.5		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: $120^{\circ}C$ , 1min
Clean		3.6		CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phosphorus implant	$2.5 \times 10^{12} cm^{-2}$ @130keV
Clean		3.7		PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		3.8		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		3.9		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

### 4 Shallow trench isolation



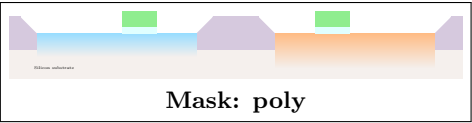
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		4.1		B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		4.2		Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		4.3		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: $110^{\circ}C$ 1min
Clean		4.4		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		4.5		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: $120^{\circ}C$ , 1min
Clean		4.6		DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	1 minute ( $2\mu m$ )
Clean		4.7		PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		4.8		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		4.9		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

5 Field oxide



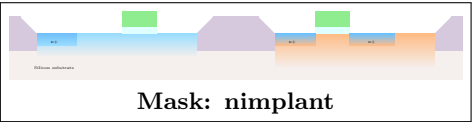
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
	Clean	5.1		A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
	Clean	5.2		Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
	Clean	5.3		Diffusion Furnace-D2, dry/wet oxidation (DIF-D2)	P2-01000	Clean	Drive in	4 hours 30 minutes @ 1050°C in dry environment
	Clean	5.4		A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
	Clean	5.5		Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
	Clean	5.6		LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	3μm (filling the trenches)
	Clean	5.7		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ≈1.5μm ), soft bake: 110°C 1min
	Clean	5.8		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
	Clean	5.9		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
	Clean	5.10		C3:BOE (WET-C3)	P2-01000	Clean	BOE: Field oxide etching	6 minutes (3000 nm, 500nm/min)
	Clean	5.11		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
	Clean	5.12		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

6 Gate



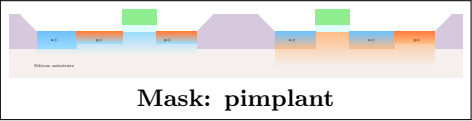
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
	Clean	6.1		A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
	Clean	6.2		Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
	Clean	6.3		Diffusion Furnace-D2, dry oxidation (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
	Clean	6.4		A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
	Clean	6.5		Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
	Clean	6.6		LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	600nm of poly silicon
	Clean	6.7		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ≈1.5μm ), soft bake: 110°C 1min
	Clean	6.8		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
	Clean	6.9		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
	Clean	6.10		Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	6 minute 10 seconds (600nm poly + 40nm oxide)
	Clean	6.11		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
	Clean	6.12		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

7 N+ implant



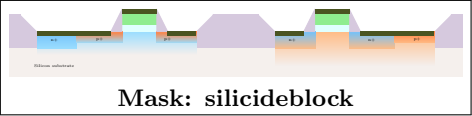
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		7.1		B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		7.2		Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		7.3		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Clean		7.4		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		7.5		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean		7.6		CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phosphorus implant	$2.5 \times 10^{12} cm^{-2}$ @ 90keV
Clean		7.7		PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		7.8		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		7.9		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

8 P+ implant



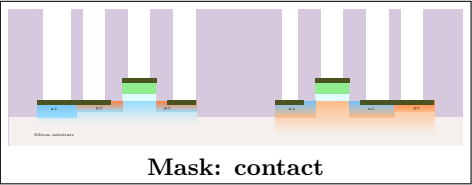
Wafer ness	Cleanli- ness	Step ber	Num- ber	Equipment	Location	Cleanliness	Process	Requirements
Clean		8.1		B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean		8.2		Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean		8.3		SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Clean		8.4		ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean		8.5		SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean		8.6		CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @ 35keV
Clean		8.7		PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean		8.8		E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean		8.9		Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

9 Silicification



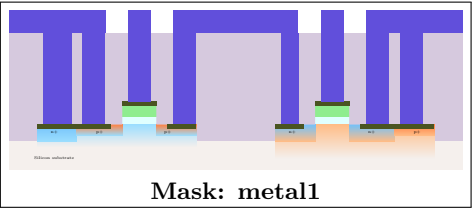
Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Clean	9.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Spacer oxide	50 nm
Clean	9.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Clean	9.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Clean	9.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	9.7	AOE Etcher (DRY-AOE)	P2-01000	Clean	Anisotropic oxide etch	12 seconds
Clean	9.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	9.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	9.10	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Titanium	15 seconds (roughly 60nm)
Semi clean	9.11	AG610 RTP (DIF-R2)	P2-01000	Semi clean	First reaction phase	240 seconds @ 700°C
Semi clean	9.12	E2: General purpose (WET-E2)	P2-01000	Semi clean	Remove unreacted Titanium	APM solution (Ammonia and Hydrogen Peroxide mixture), 1 minute
Semi clean	9.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	9.14	AG610 RTP (DIF-R2)	P2-01000	Semi clean	Second reaction phase	240 seconds @ 800°C

10 Contact



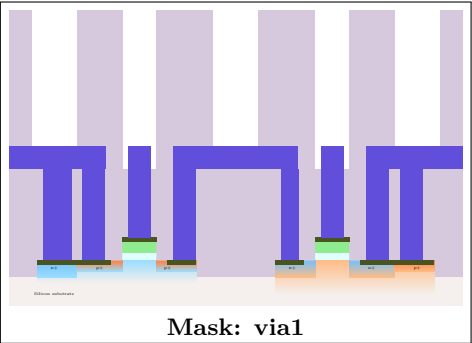
Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	10.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	10.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	10.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	500 nm
Semi clean	10.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	10.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	10.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	10.7	E2: General purpose (WET-E2)	P2-01000	Semi clean	BOE (1:6), LTO Etch	1 minute (500 nm, 500nm/min)
Semi clean	10.8	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	10.9	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	10.10	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

11 Metal 1



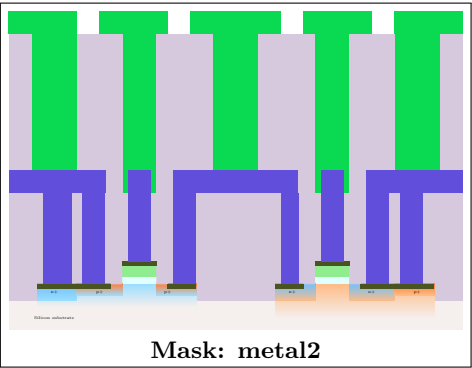
Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	11.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	37.5 seconds (roughly 600nm)
Semi clean	11.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	11.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	11.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	11.5	D1: Aluminum etch (WET-D1)	P2-01000	Semi clean	Wire formation	2 minutes (600 nm, 282.3 nm/min)
Semi clean	11.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	11.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

12 Via 1



Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	12.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	12.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	12.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	500 nm
Semi clean	12.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	12.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	12.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	12.7	E2: General purpose (WET-E2)	P2-01000	Semi clean	BOE (1:6), LTO Etch	1 minute (500 nm, 500nm/min)
Semi clean	12.8	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	12.9	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	12.10	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

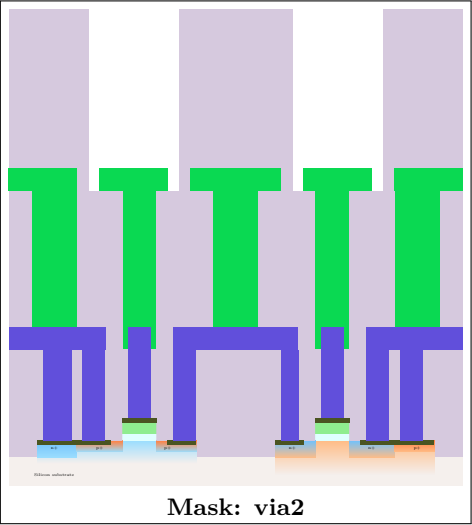
13 Metal 2



Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	13.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum	37.5 seconds (roughly 600nm)
Semi clean	13.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	13.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	13.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	13.5	D1: Aluminum etch (WET-D1)	P2-01000	Semi clean	Wire formation	2 minutes (600 nm, 282.3 nm/min)
Semi clean	13.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	13.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

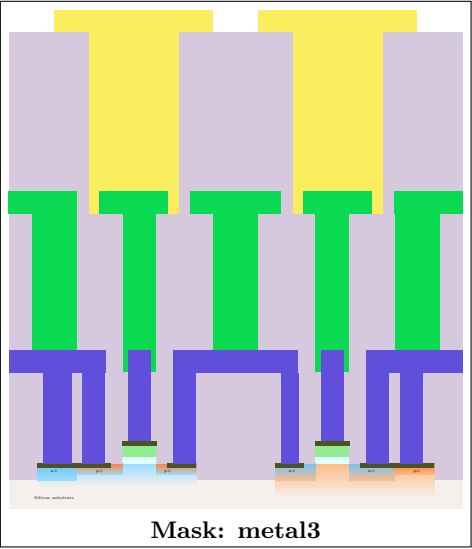


14 Via 2



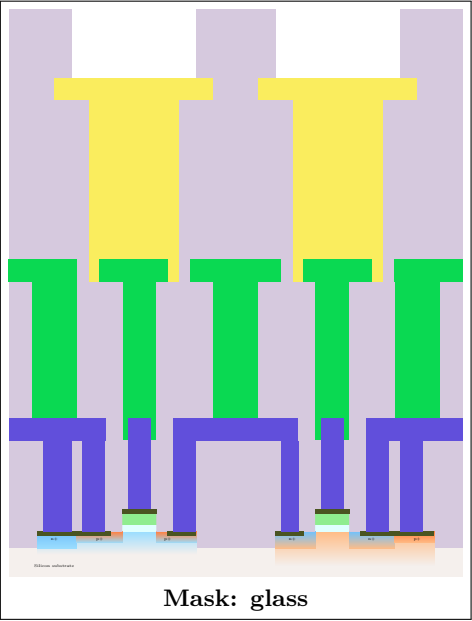
Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	14.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	14.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	14.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	500 nm
Semi clean	14.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	14.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	14.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	14.7	E2: General purpose (WET-E2)	P2-01000	Semi clean	BOE (1:6), LTO Etch	1 minute (500 nm, 500nm/min)
Semi clean	14.8	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	14.9	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	14.10	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

15 Metal 3



Wafer Cleanli-ness	Step Num-ber	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	15.1	NSC3000 Sputter (SPT-NSC3000)	P2-01000	Semi clean	Deposit Titanium-Tungsten alloy (TiW -> 5nm/min)	120 minutes = 2 hours (roughly 600nm)
Semi clean	15.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	15.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
Semi clean	15.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	15.5	E2: General purpose (WET-E2)	P2-01000	Semi clean	Wire formation	APM solution (Ammonia and Hydrogen Peroxide mixture), 10 minutes
Semi clean	15.6	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	15.7	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
Semi clean	15.8	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

16 Glass



Wafer	Cleanli- ness
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean
	Semi clean

Step Num- ber	Equipment	Location	Cleanliness	Process	Requirements
16.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
16.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
16.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	500 nm
16.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( $\approx 1.5\mu m$ ), soft bake: 110°C 1min
16.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	
16.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
16.7	E2: General purpose (WET-E2)	P2-01000	Semi clean	BOE (1:6), LTO Etch	1 minute (500 nm, 500nm/min)
16.8	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
16.9	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist Stripping	5mins, 70°C
16.10	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	