

logic level source acceptable voltages for our CMOS "ON" state range from 2V to V_{DD} (which typically is around $\pm 0.25V$

$$(1) V_{on} \geq 2V$$

$$(2) V_{on} > 4 \cdot V_{Tn}$$

$$(3) V_{on} = 2V$$

$$(4) 4 \cdot V_{Tn} < 2V \Rightarrow V_{Tn} < 500mV$$

dimensioning and as surface concentration for our P-well of $22 \frac{1}{m^3}$

$$\approx 0.28V$$

$$N_p =$$

$$10^{16} \frac{1}{cm^3} =$$

$$10^{22} \frac{1}{m^3}$$

$$W_{drain} \approx$$

$$2.73 \mu m$$

$$10^{-7} m =$$

$$273nm$$

range and struggle or use the web tool linked in the implant chapter.

$$N_B \approx$$

$$7 \cdot$$

$$10^{14} \frac{1}{cm^3} =$$

$$7 \cdot$$

$$10^{20} \frac{1}{m^3}$$

$$(5) N_p - N_B = 10^{22} \frac{1}{m^3} - 7 \cdot 10^{20} \frac{1}{m^3} = 9.3 \cdot 10^{21} \frac{1}{m^3}$$

$$\approx 2 \mu m$$

$$drive_{in}$$

$$(6) x_e = 2 \cdot \sqrt{D_e \cdot t_e} \gg 2 \cdot \sqrt{D_v \cdot t_v} = x_v$$