Generic LibreSilicon process overview

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Abstract

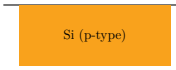
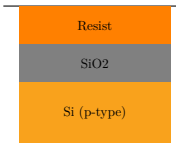
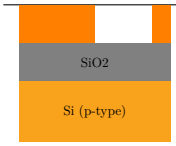
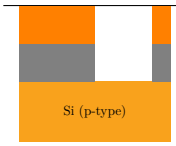
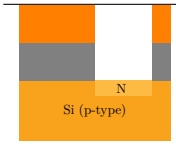
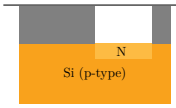
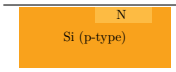
This is the specification of the free silicon manufacturing standard for manufacturing the ls018[1]standard logic cells and related free technology nodes from the LibreSilicon project.

For further clarification consult the complete documentation of the process.

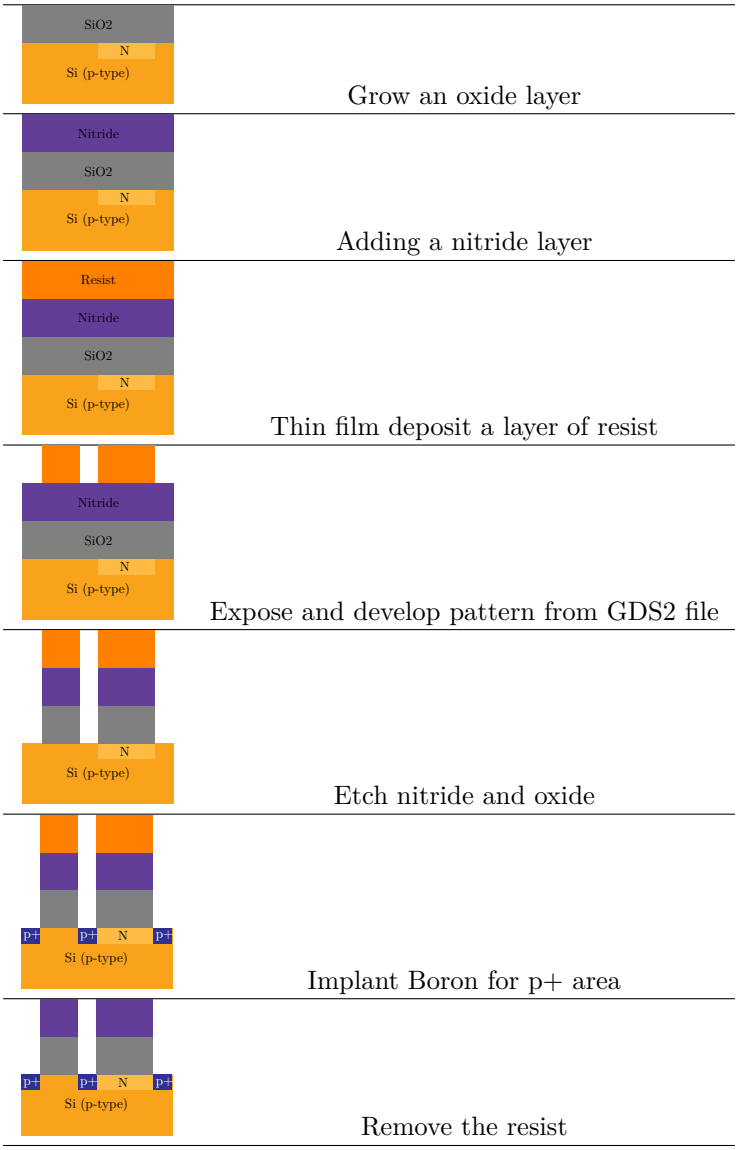
[1]https://github.com/leviathanch/ls018

1 N-Well

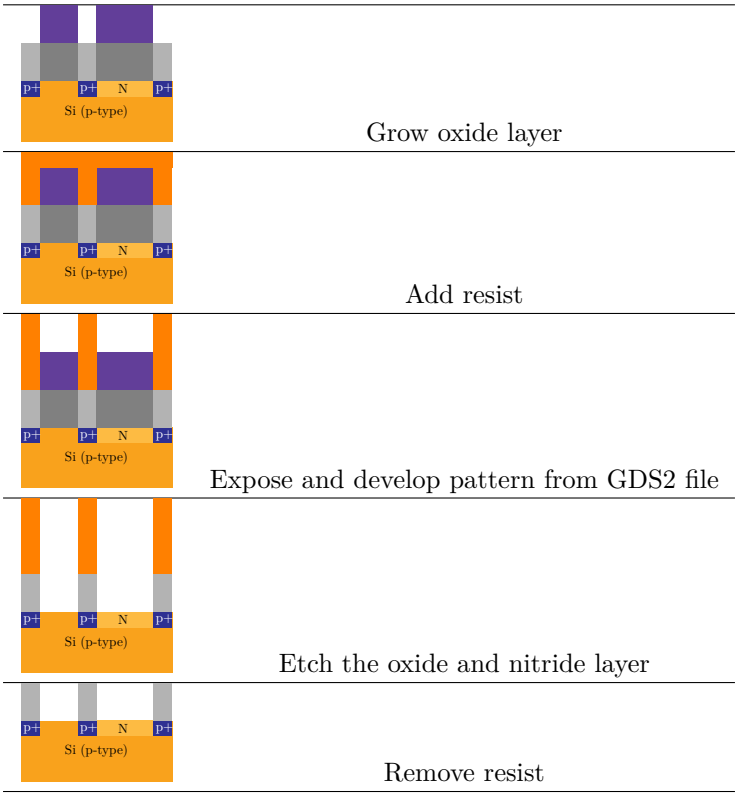
The n-well is required for CMOS technology built on a p-substrate. For this process p-substrate is required.

	Start with a p-type silicon wafer
	Grow an oxide layer
	Thin film deposit a layer of resist
	Expose and develop the pattern from the GDS2 layer information
	Etch the oxide layer
	Implant Phosphorus (P); Create N-well
	Remove resist
	Remove oxide

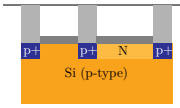
2 P+ Implant


SiO2
N
Si (p-type)
Grow an oxide layer
Nitride
SiO2
N
Si (p-type)
Adding a nitride layer
Resist
Nitride
SiO2
N
Si (p-type)
Thin film deposit a layer of resist
Nitride
SiO2
N
Si (p-type)
Expose and develop pattern from GDS2 file
N
Si (p-type)
Etch nitride and oxide
p+
p+
N
p+
Si (p-type)
Implant Boron for p+ area
p+
p+
N
p+
Si (p-type)
Remove the resist

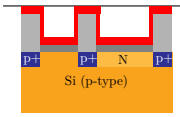
3 Field oxide



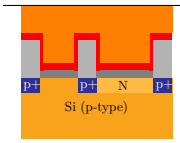
4 Poly



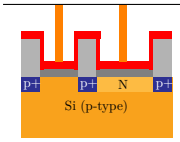
Grow thin gate oxide



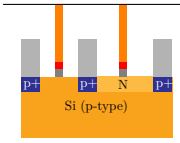
Grow poly silicon



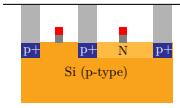
Add resist



Expose and develop pattern from GDS2 file



Precision etching (suggestion: Dry etching)



Remove resist