Abstract

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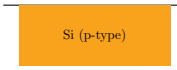
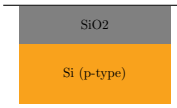
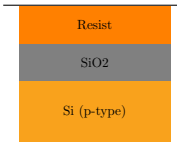
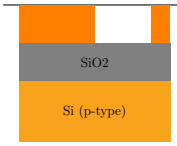
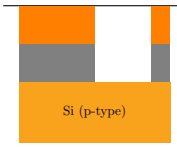
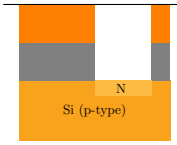
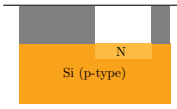
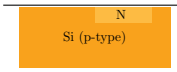
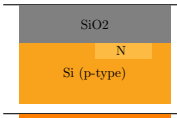
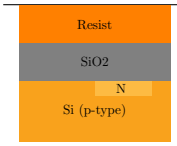
This is the specification of the free silicon manufacturing standard for manufacturing the ls018[1]standard logic cells and related free technology nodes from the LibreSilicon project.

1 Well

	We start with a p-type silicon wafer
	We grow an oxide layer of approximately 1000 angstrom thickness (see documentation)
	We thin film deposit a layer of resist
	We expose and develop the pattern from the GDS2 layer information
	We etch the 1000 angstrom oxide layer
	Ion implantation: Implant Phosphorus (P); n-type impurity to create N-well (see documentation)
	Remove resist
	Remove oxide

2 Implant

	We grow an oxide layer of approximately 1000 angstrom thickness (see documentation)
	We thin film deposit a layer of resist

[1]https://github.com/leviathanch/ls018

3 Select

4 Active

5 Metal